

EE 508

Lecture 40

What filter architectures are really being used today?

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A CMOS/Thin-Film Fluorescence Contact Imaging Microsystem for DNA Analysis

Ritu Raj Singh, *Student Member, IEEE*, Derek Ho, *Student Member, IEEE*, Alireza Nilchi, *Student Member, IEEE*, Glenn Gulak, *Member, IEEE*, Patrick Yau, and Roman Genov, *Member, IEEE*

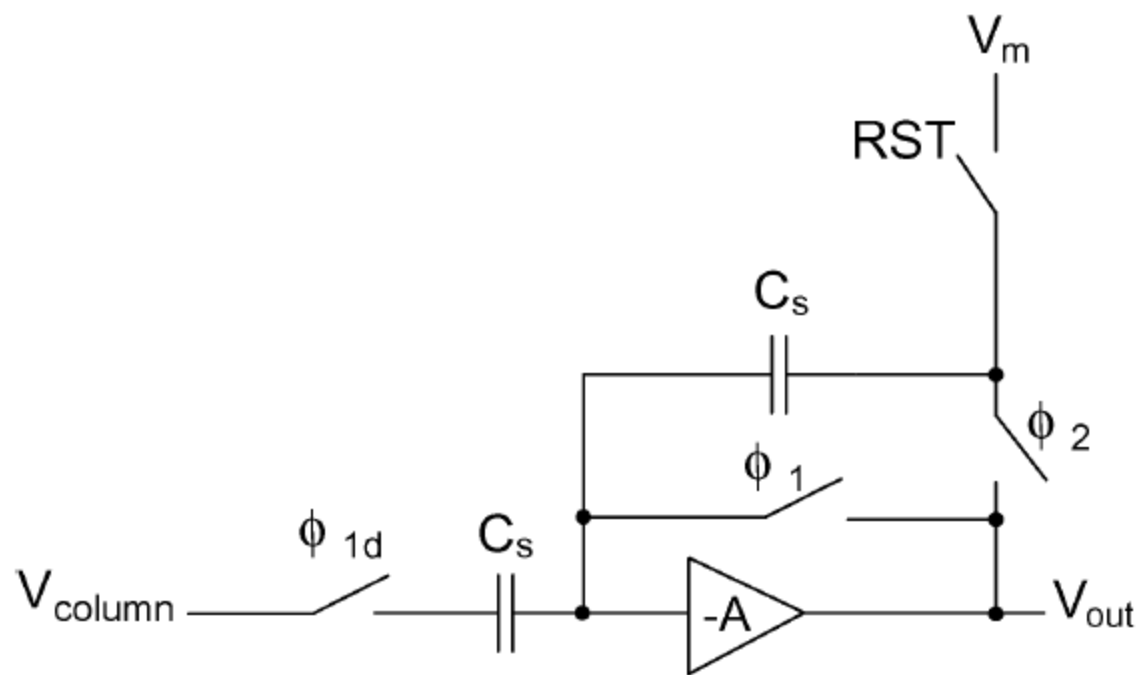


Fig. 5. Column-parallel switched-capacitor difference circuit.

An Ultra-Low Voltage, Low-Noise, High Linearity 900-MHz Receiver With Digitally Calibrated In-Band Feed-Forward Interferer Cancellation in 65-nm CMOS

Ajay Balankutty, *Student Member, IEEE*, and Peter R. Kinget, *Fellow, IEEE*

2272

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 10, OCTOBER 2011

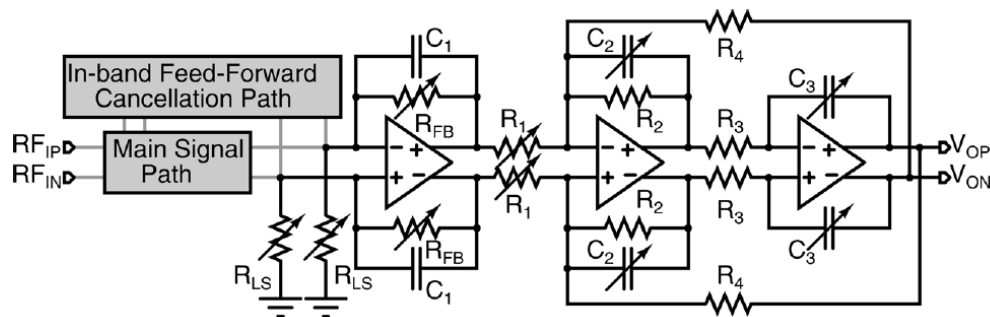


Fig. 5. TIA and channel select filter; the variable resistors and capacitors are implemented as discretely switched banks of resistors and capacitors.

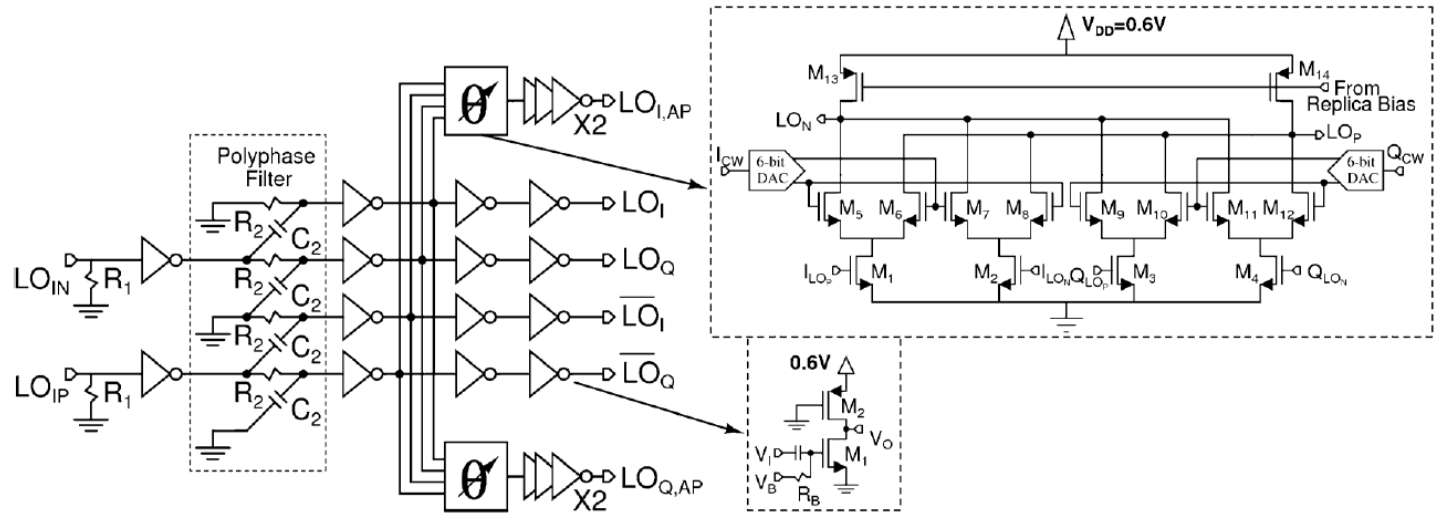


Fig. 6. Schematics of the passive polyphase filter, LO phase shifter, and LO buffers.

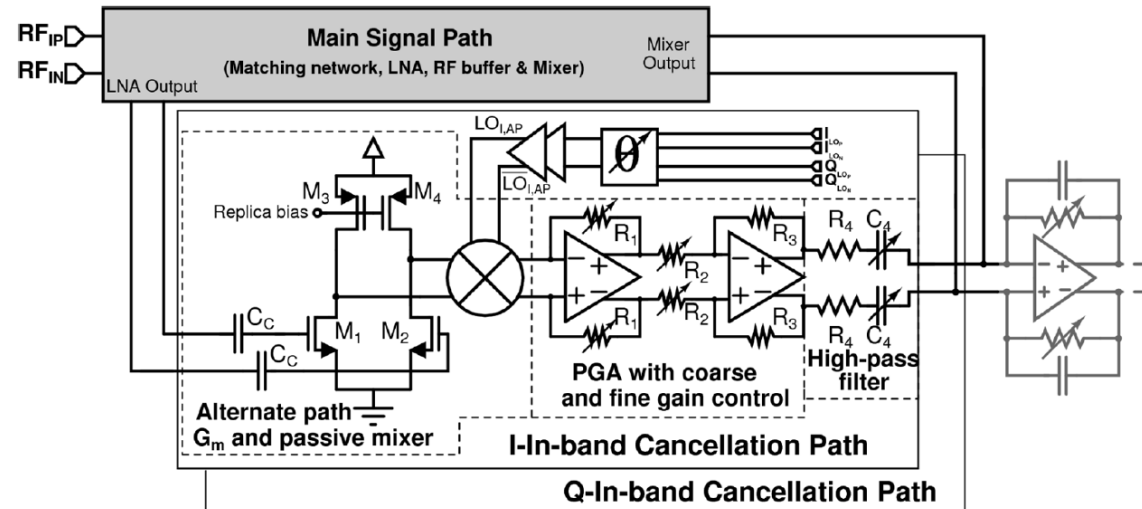
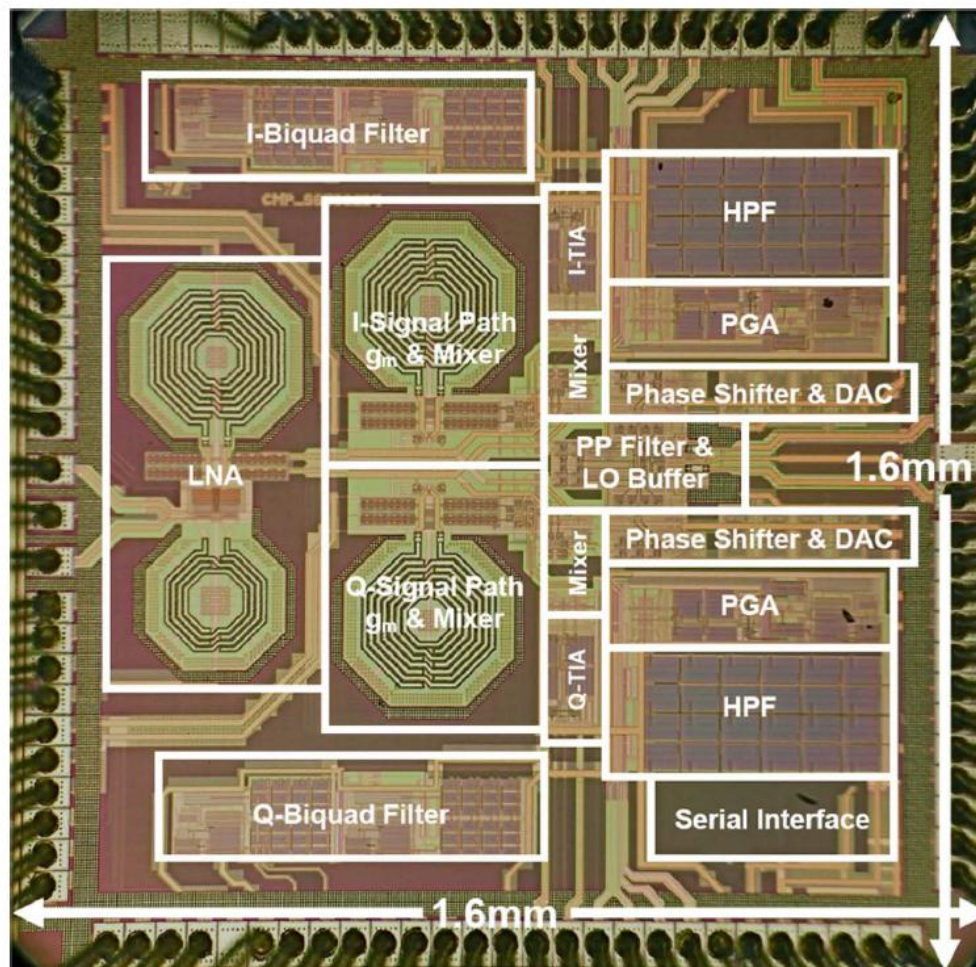


Fig. 7. Alternate path transconductor, downconversion mixer, PGA, and high-pass filter implementation.



A Low Area, Switched-Resistor Based Fractional-N Synthesizer Applied to a MEMS-Based Programmable Oscillator

Michael H. Perrott, *Senior Member, IEEE*, Sudhakar Pamarti, *Member, IEEE*, Eric G. Hoffman, *Member, IEEE*, Fred S. Lee, *Member, IEEE*, Shouvik Mukherjee, Cathy Lee, Vadim Tsinker, Sathi Perumal, Benjamin T. Soto, Niveditha Arumugam, and Bruno W. Garlepp, *Member, IEEE*

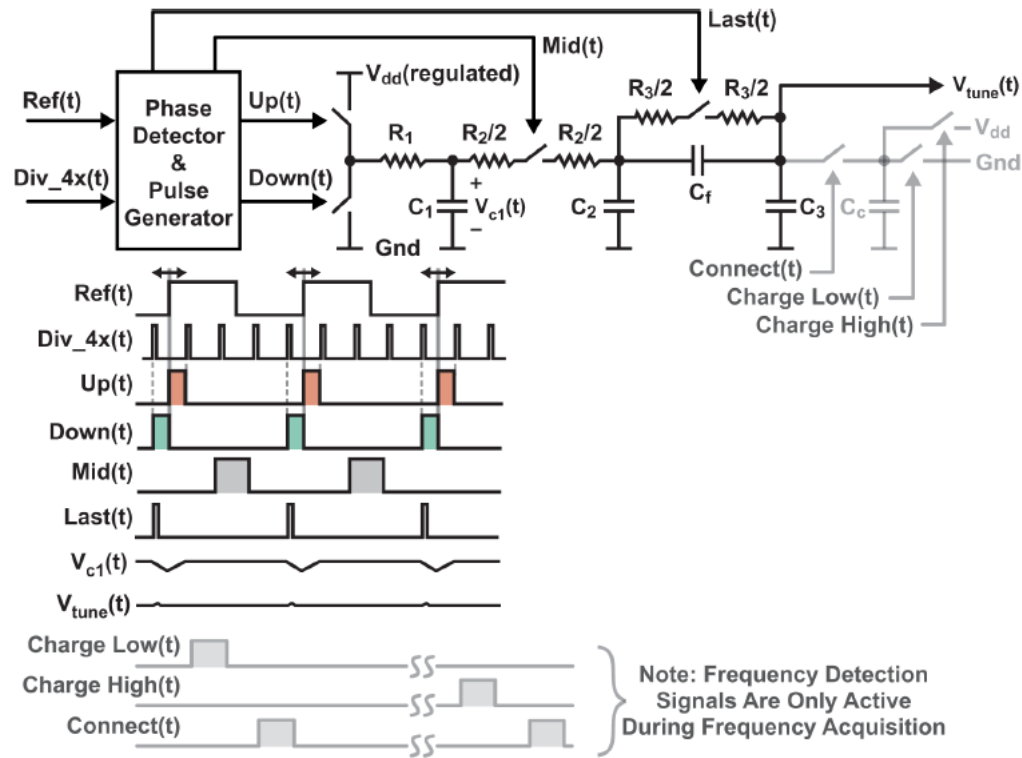


Fig. 3. Proposed switched resistor loop filter. Note that the R_3 pulsing frequency can also be set lower than the reference frequency, and is implemented at $1/4$ the reference frequency in the prototype.

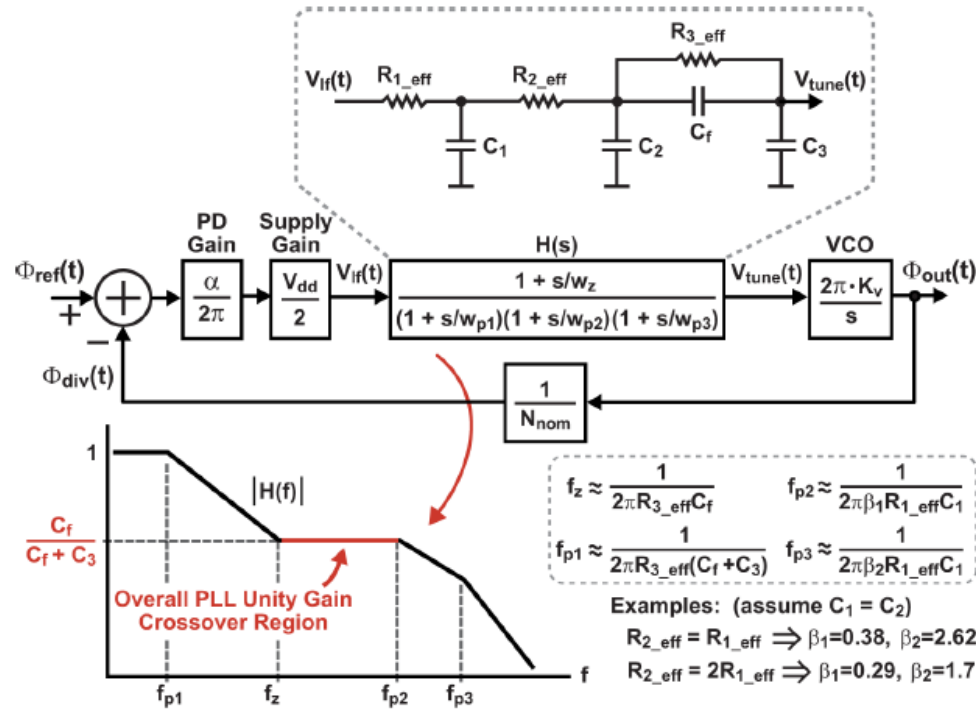


Fig. 5. Transfer function analysis of a switched resistor PLL in which the Bode plot of the loop filter, $H(f)$, is considered within the context of the overall PLL block diagram. Note that the values of β_1 and β_2 are calculated using the Quadratic formula by ignoring the influence of R_{3_eff} , C_f , and C_3 on poles f_{p2} and f_{p3} .

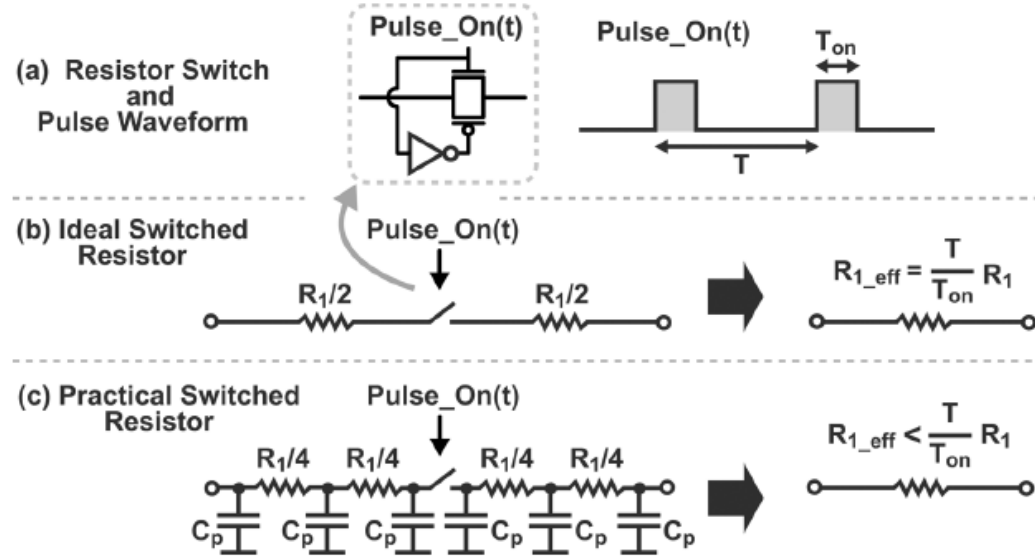


Fig. 4. Implementation of switched resistor using CMOS devices and poly resistors, along with impact of pulsed switching and parasitic capacitance on the effective resistance.

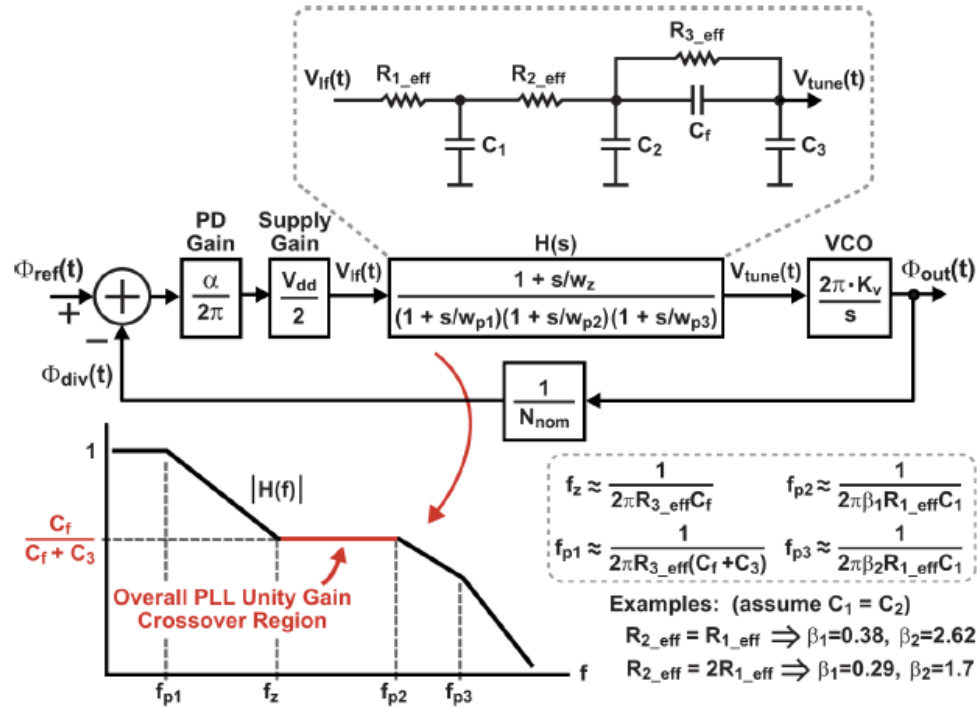


Fig. 5. Transfer function analysis of a switched resistor PLL in which the Bode plot of the loop filter, $H(f)$, is considered within the context of the overall PLL block diagram. Note that the values of β_1 and β_2 are calculated using the Quadratic formula by ignoring the influence of R_{3_eff} , C_f , and C_3 on poles f_{p2} and f_{p3} .

A Wideband Receiver for Multi-Gbit/s Communications in 65 nm CMOS

Federico Vecchi, *Member, IEEE*, Stefano Bozzola, Enrico Temporiti, Davide Guermandi, Massimo Pozzoni, Matteo Repossi, Marco Cusmai, Ugo Decanis, *Student Member, IEEE*, Andrea Mazzanti, *Member, IEEE*, and Francesco Svelto, *Member, IEEE*

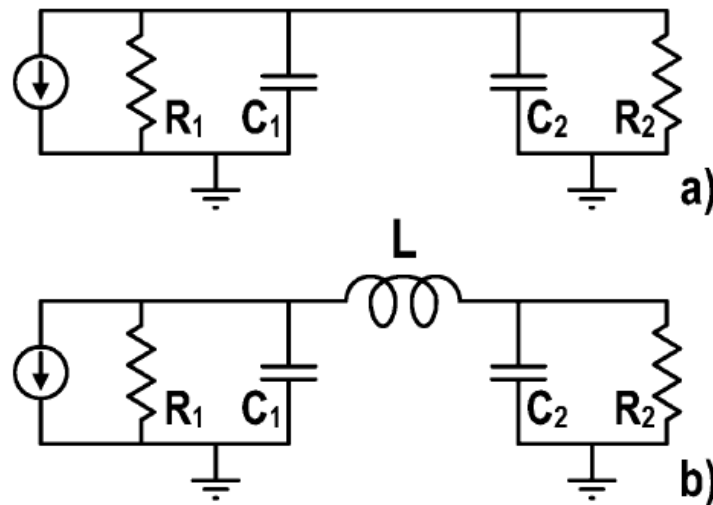


Fig. 4. (a) Equivalent circuit of a baseband amplifier with low-pass transfer function: a transconductor drives two separate RC groups (R_1 , C_1 and R_2 , C_2). (b) The two capacitors are separated by means of a series inductor improving gain-bandwidth.

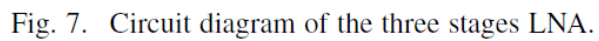


Fig. 7. Circuit diagram of the three stages LNA.

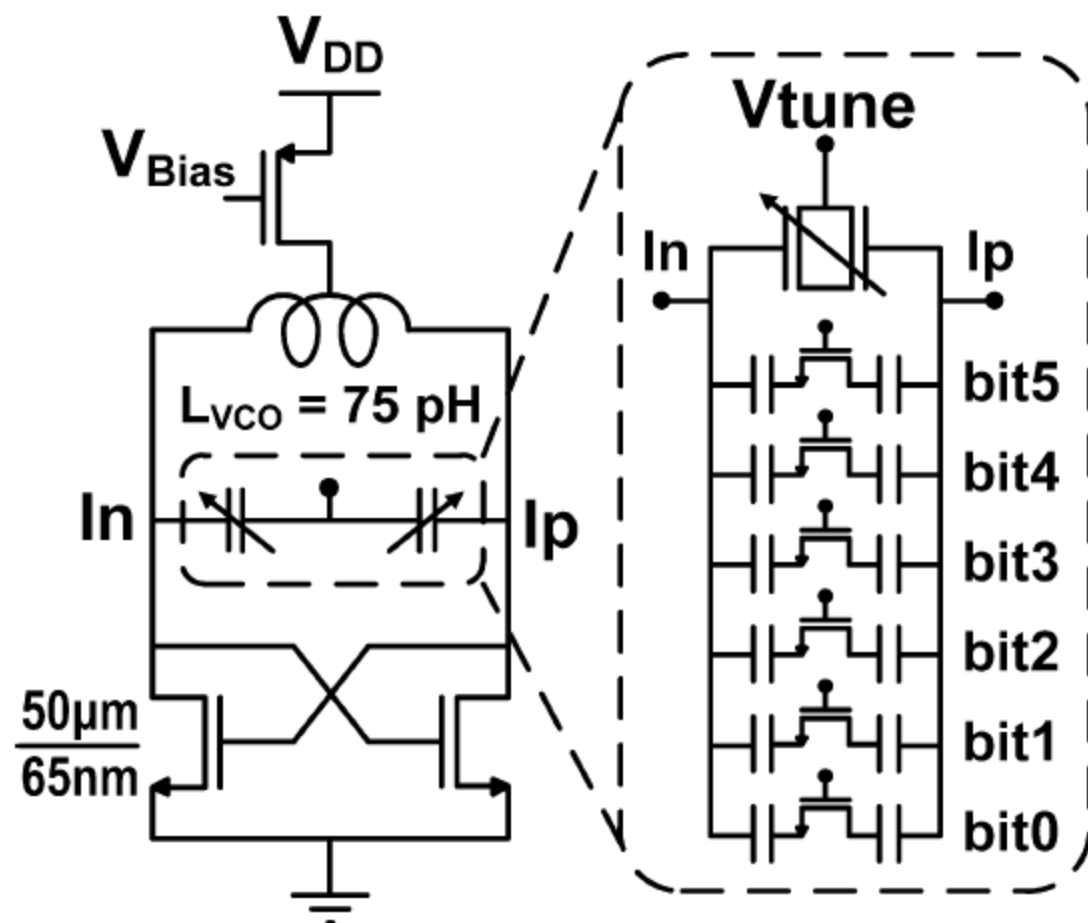


Fig. 11. LC VCO. A 5 bits capacitor tank is adopted for coarse tuning with an nMOS varactor for fine tuning.

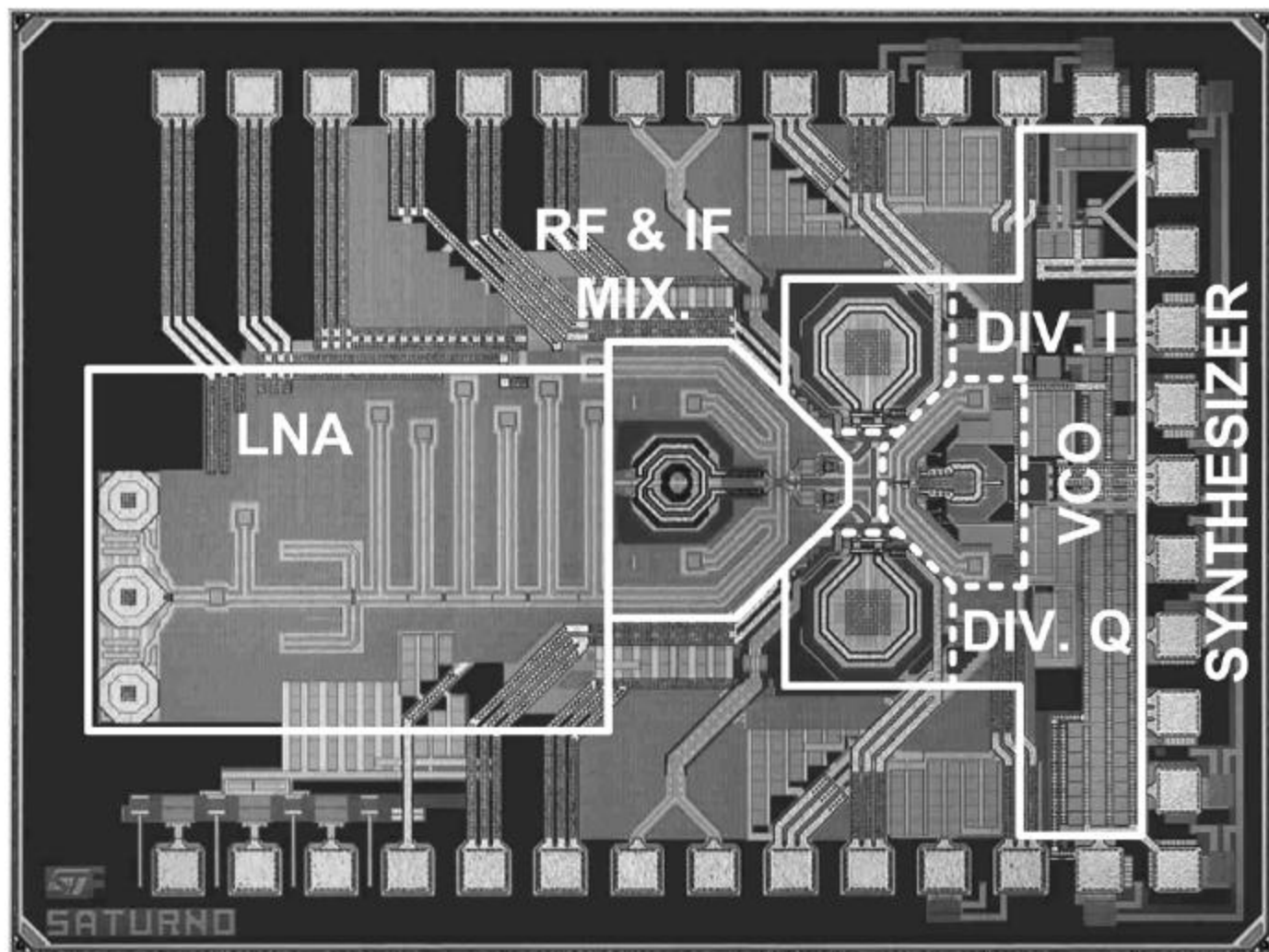


Fig. 13. Chip microphotograph.

A Broadband CMOS RF Front-End for Universal Tuners Supporting Multi-Standard Terrestrial and Cable Broadcasts

Donggu Im, *Student Member, IEEE*, Hongteuk Kim, *Member, IEEE*, and Kwyro Lee, *Senior Member, IEEE*

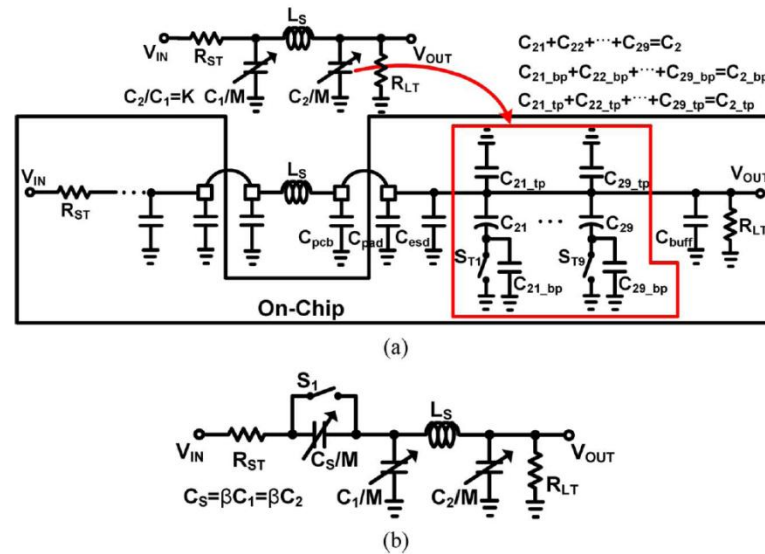


Fig. 7. (a) Third-order pi-section LC filter and its detailed schematic for calculating parasitic capacitance. (b) Modified 3rd-order pi-section LC filter with the variable capacitor C_S to increase the tuning range.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{M^2 w_{cL}^3}{s^3 + [2M] w_{cL} s^2 + \left[\left(\frac{1+K}{2} \right) M \right] w_{cL}^2 s + M^2 w_{cL}^3} \quad (8)$$

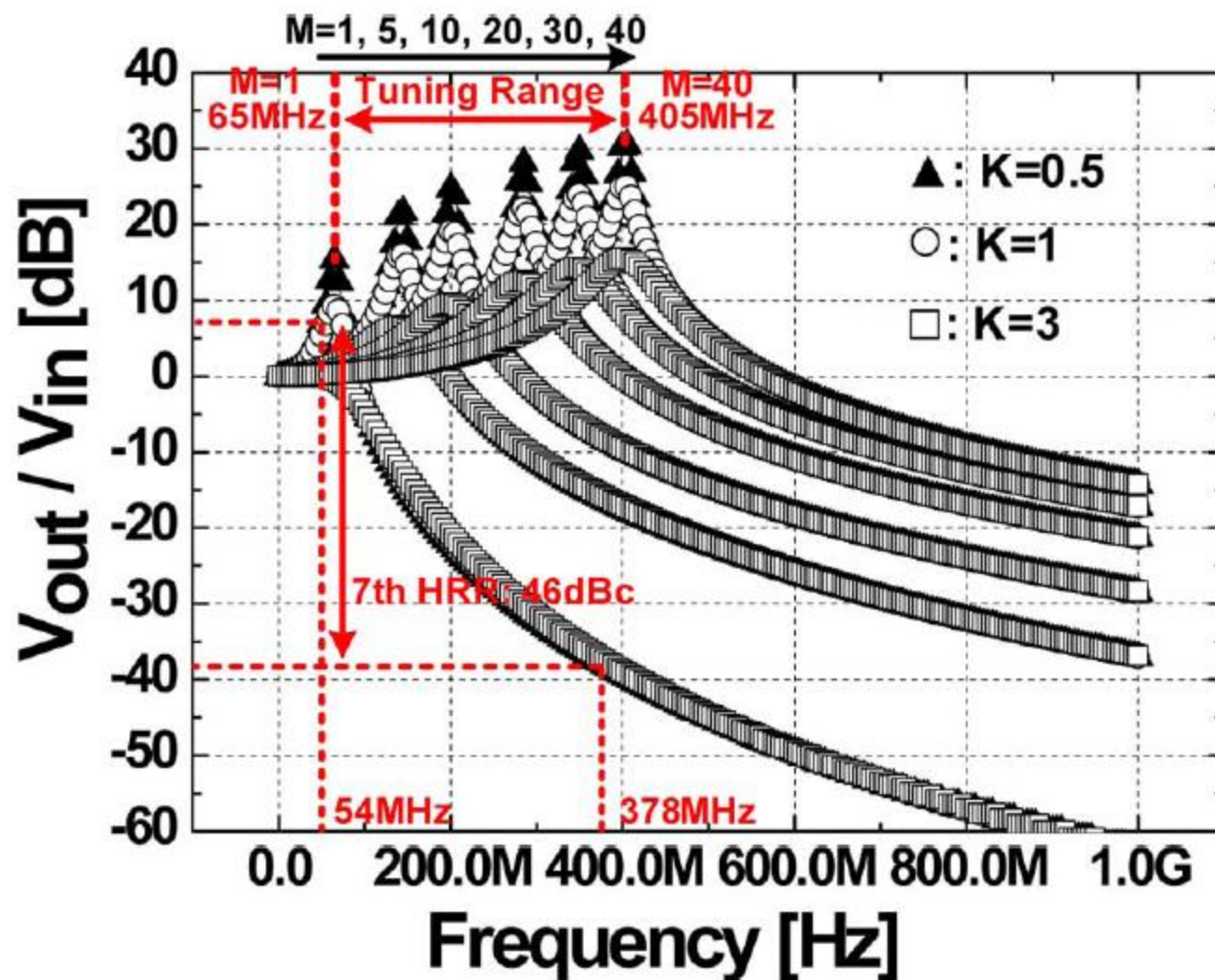


Fig. 8. Frequency response of (8) according to the variation of the M for $K = 0.5, 1$, and 3 .

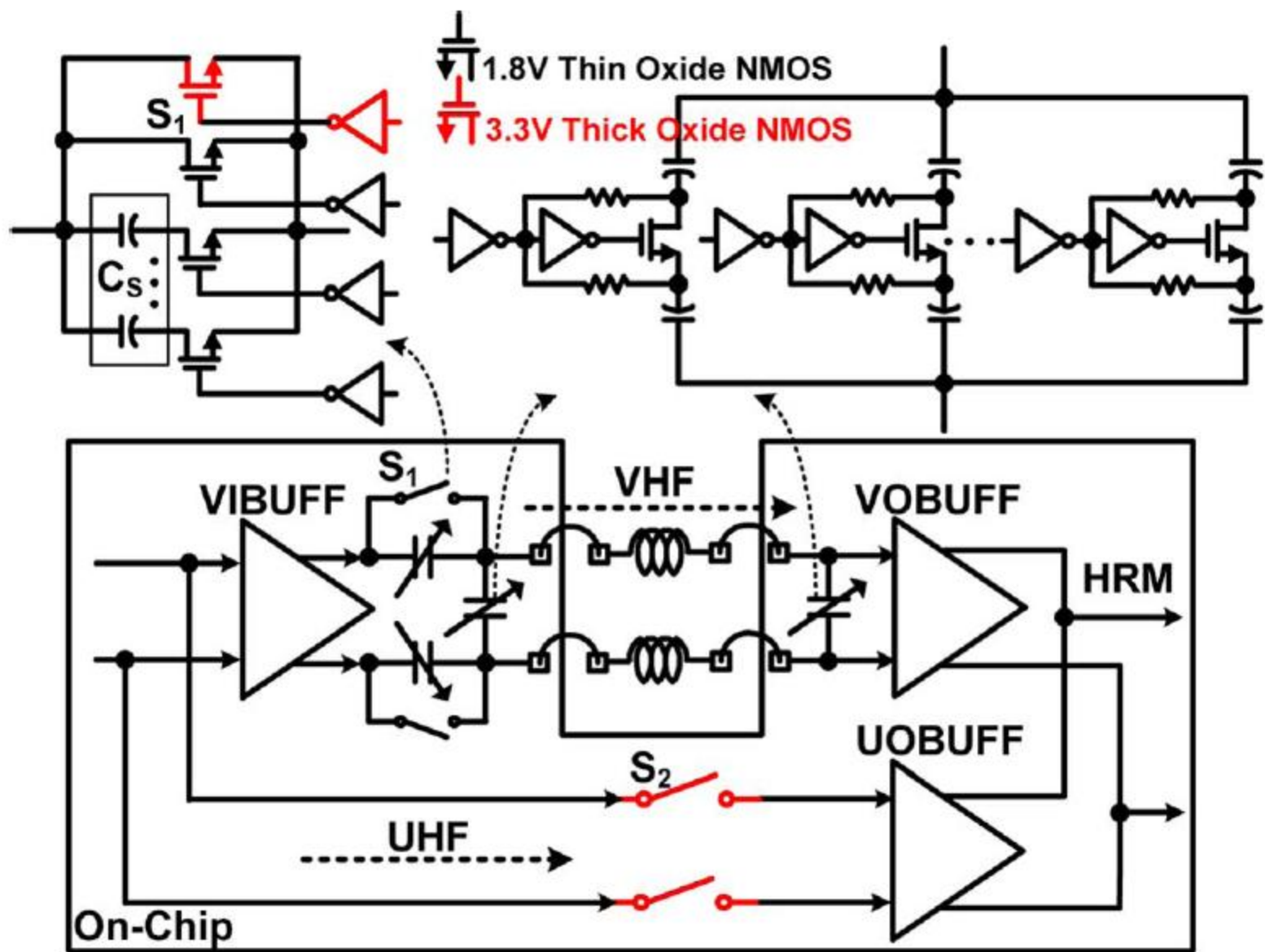


Fig. 11. Complete passive tunable filter.

Motion Image Sensor with On-chip Adaptation and Programmable Filtering

Peng Xu*, Pamela Abshire*, and J. Sean Humbert[†]

*Dept. of Electrical and Computer Engineering, *Institute for Systems Research, [†]Dept. of Aerospace Engineering
University of Maryland, College Park, MD 20742

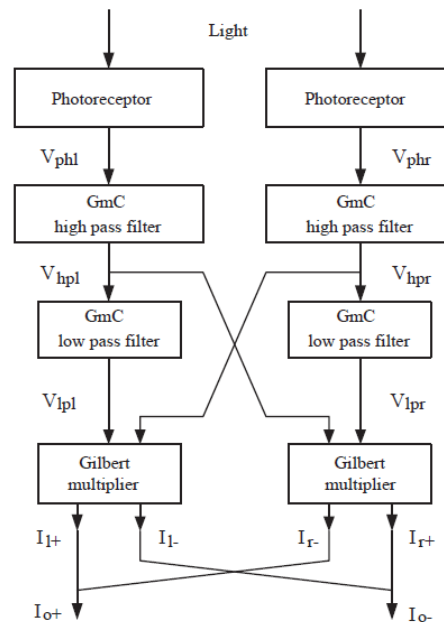


Fig. 1. Block diagram of EMD implementation.

The opuc now generated by the EMDS pass on to spatial filters. Each filter coefficient is programmed using nonvolatile storage in floating gate MOS. Bandyopadhyay et al. used a programmable floating-gate array to implement matrix transformations on images [8]. Here programming is accomplished

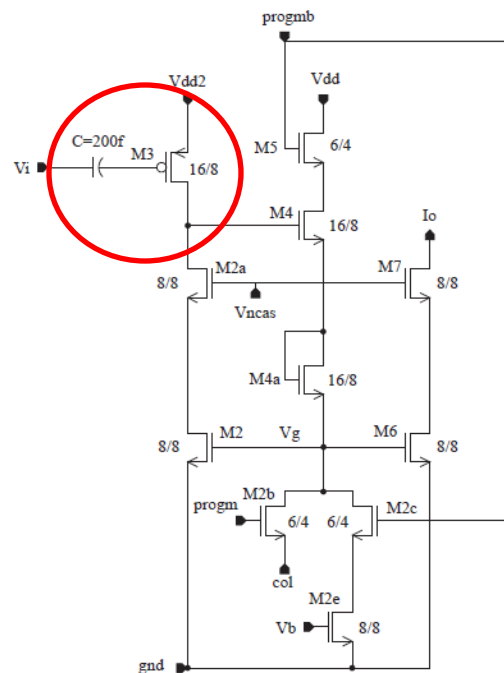


Fig. 2. Schematic of the PCE.

Programmable Current Element

current. $M3$ performs the multiplication operation, and the charge stored on its floating gate functions as the coefficient of the filter.

A Fully Integrated and Reconfigurable Architecture for Coherent Self-Testing of High Speed Analog-to-Digital Converters

Edinei Santin, *Student Member, IEEE*, Luís B. Oliveira, *Member, IEEE*, Blazej Nowacki, and João Goes, *Senior Member, IEEE*

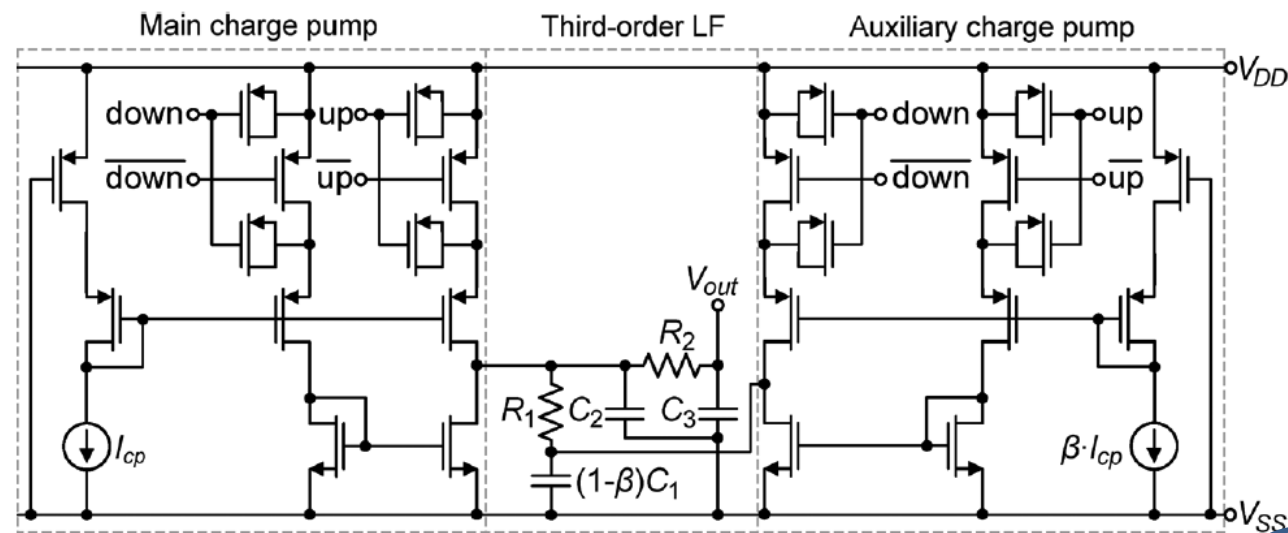


Fig. 5. Schematic of the charge pump and third-order loop filter.

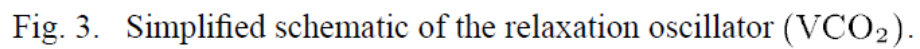


Fig. 3. Simplified schematic of the relaxation oscillator (VCO₂).

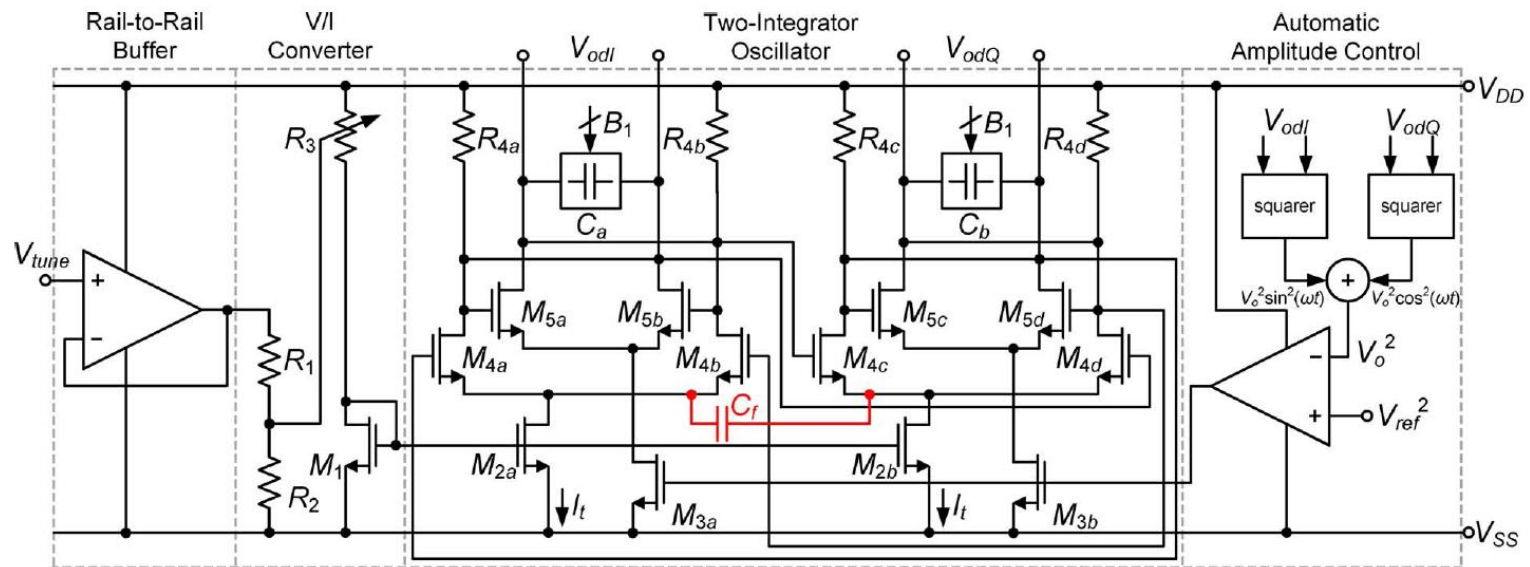


Fig. 4. Simplified schematic of the two-integrator oscillator (VCO₁).

Current-Mode, WCDMA Channel Filter With In-Band Noise Shaping

Alberto Pirola, *Student Member, IEEE*, Antonio Liscidini, *Member, IEEE*, and Rinaldo Castello, *Fellow, IEEE*

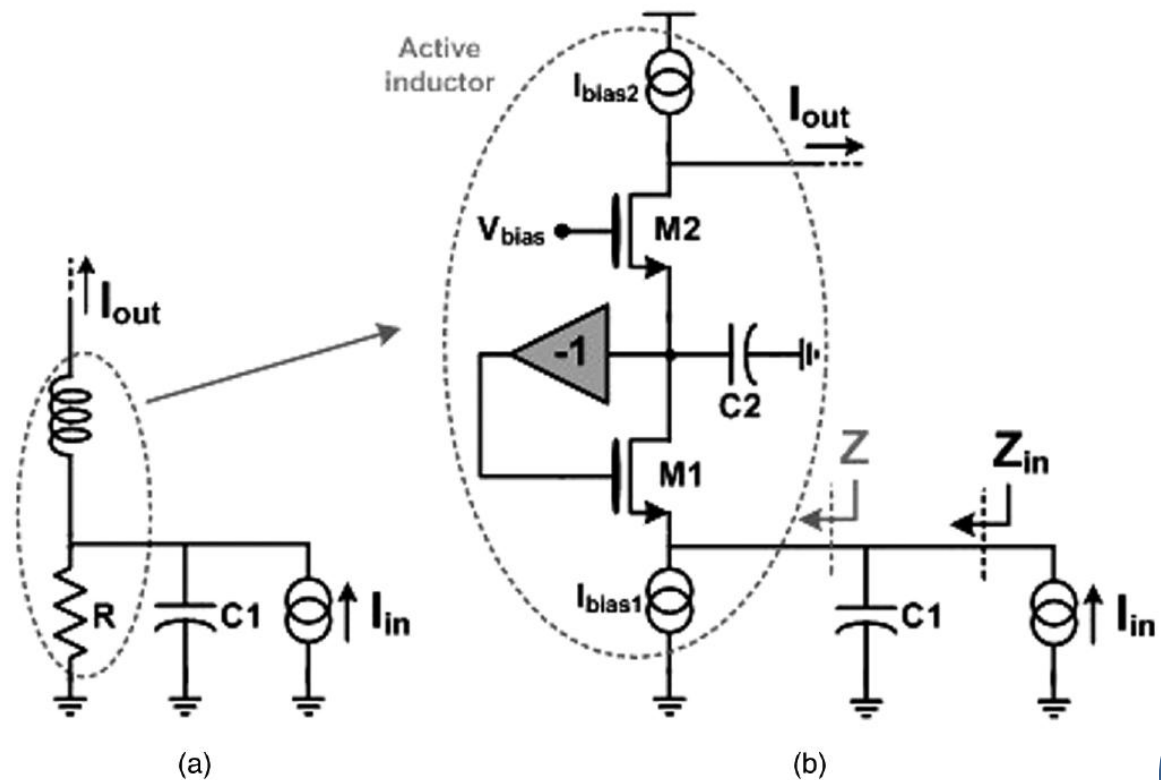


Fig. 4. Current biquad cell.

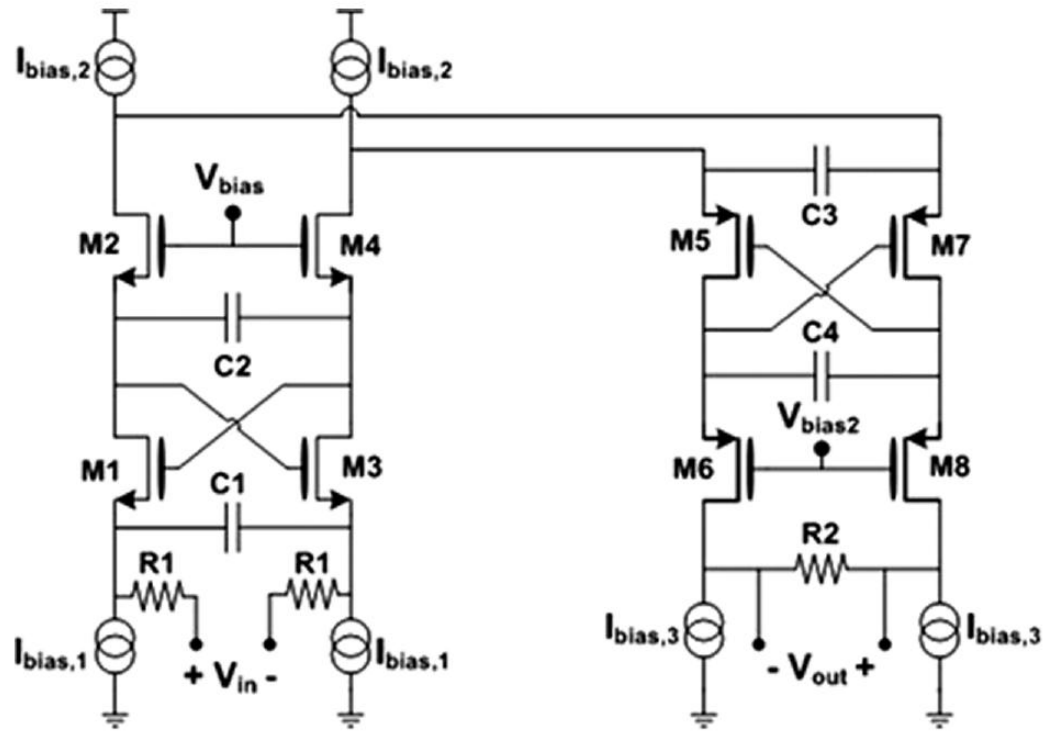
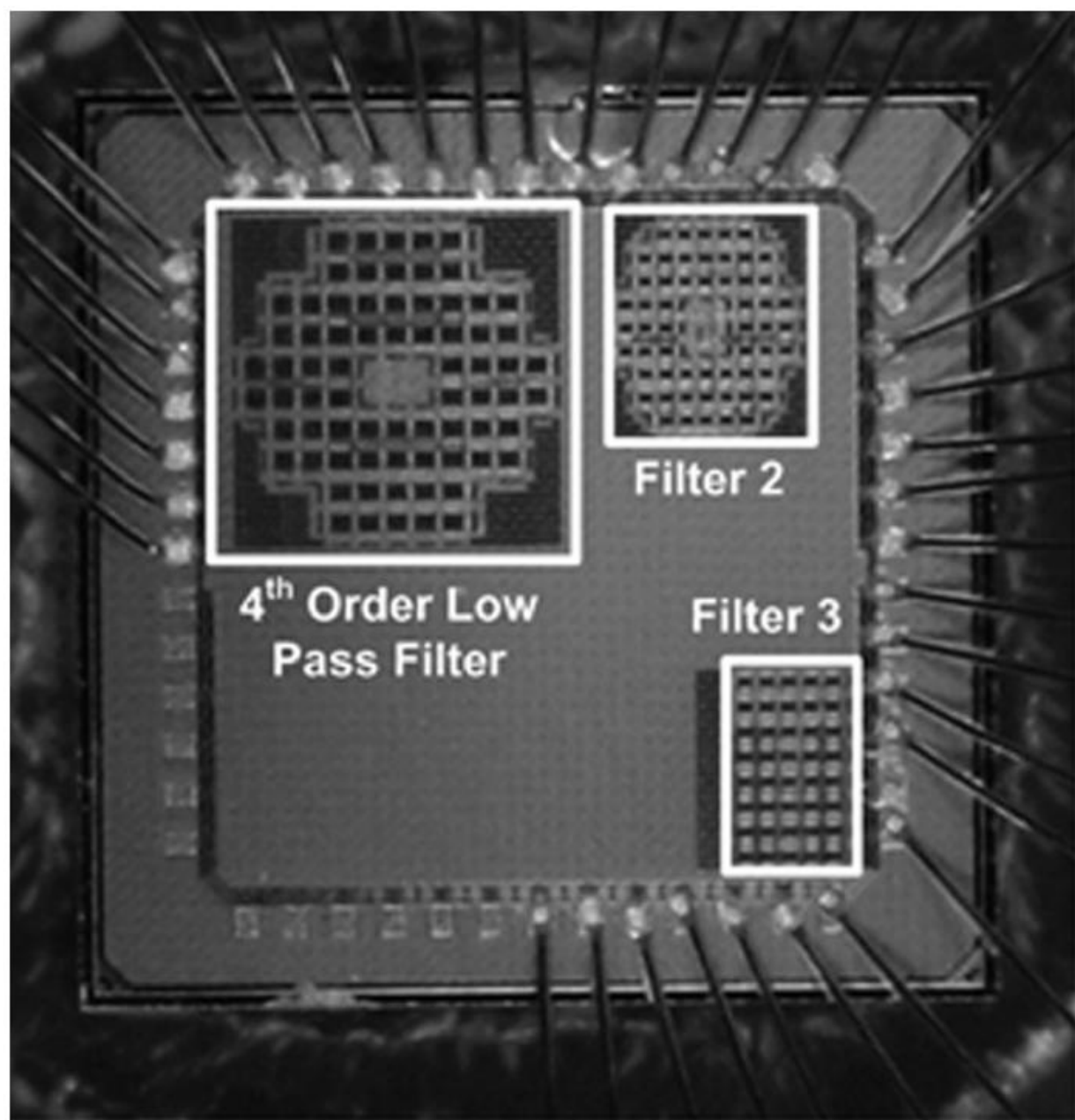


Fig. 8. Fourth-order filter schematic.

The chip micrograph of the filter prototype, fabricated in a 90 nm CMOS process, is shown in Fig. 10. All pads are ESD protected and the active die area is 0.5 mm². This area is dominated by low-density MiM capacitors (210 pF), whose placement could be further improved, resulting in a lower area occupation. Moreover, large on-chip MoM bypass capacitors are



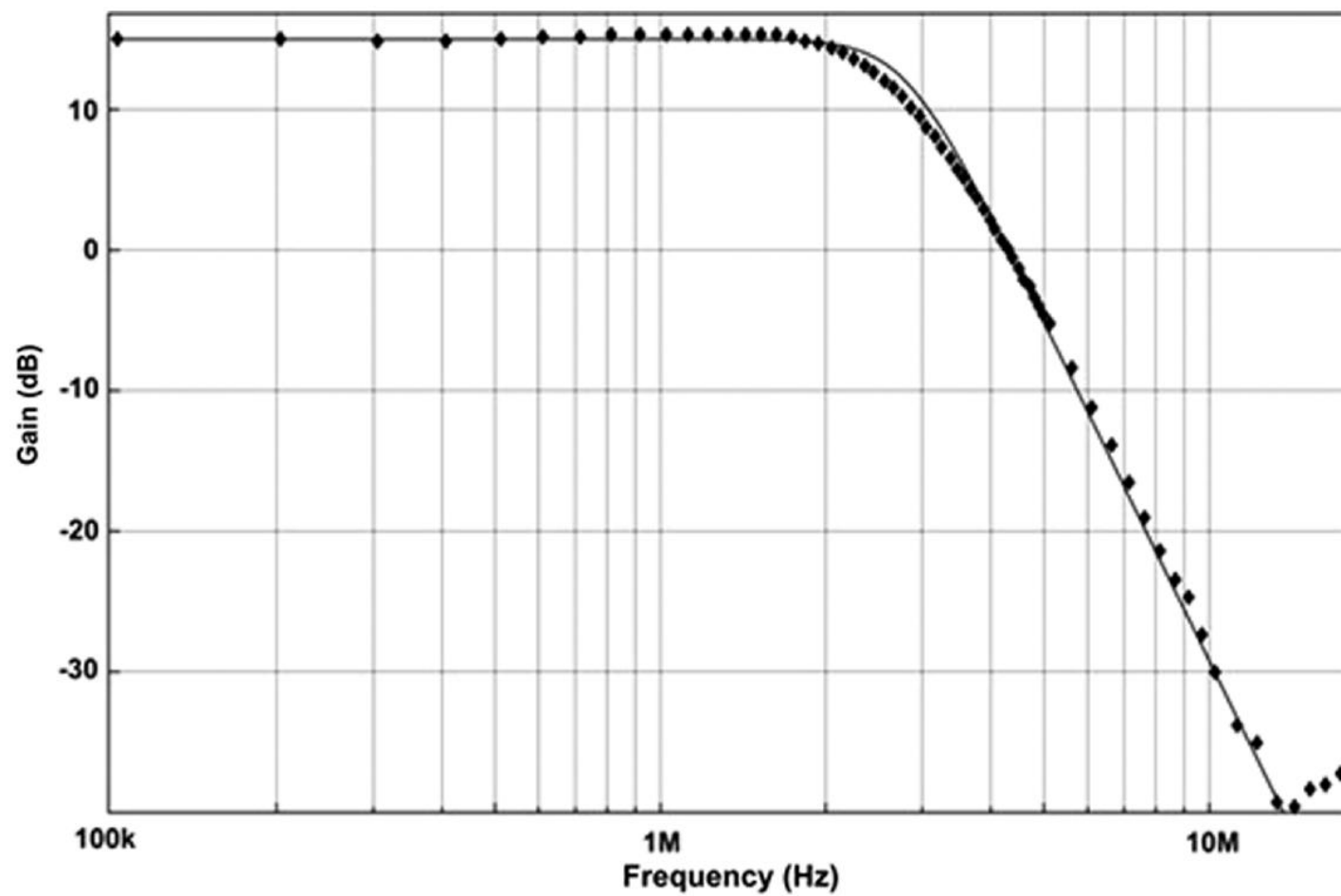


Fig. 11. Measured output transfer function.

Transformed lumped element integrated passive bandpass filters for gigahertz range spectrum monitor receivers

S. Liang and W. Redman-White

ELECTRONICS LETTERS 24th November 2011 Vol. 47 No. 24

Two integrated bandpass filters have been designed and fabricated on standard 130 nm CMOS technology. The lumped element, third-order Butterworth bandpass filters at 9.45 and 1.75 GHz are designed for sub-band filtering in a spectrum monitoring receiver function in a future cognitive radio. A series coupled resonator topology is selected and a novel delta–star transformation technique is applied to obtain element values suitable for reliable fabrication on an integrated circuit. Occupying die areas of $780 \times 200 \mu\text{m}$ and $1750 \times 500 \mu\text{m}$ each, the filters achieve insertion losses of 15.6 and 8.6 dB, and bandwidths of 1 GHz and 210 MHz, respectively, which are suitable for the chosen spectrum monitor receiver architecture.

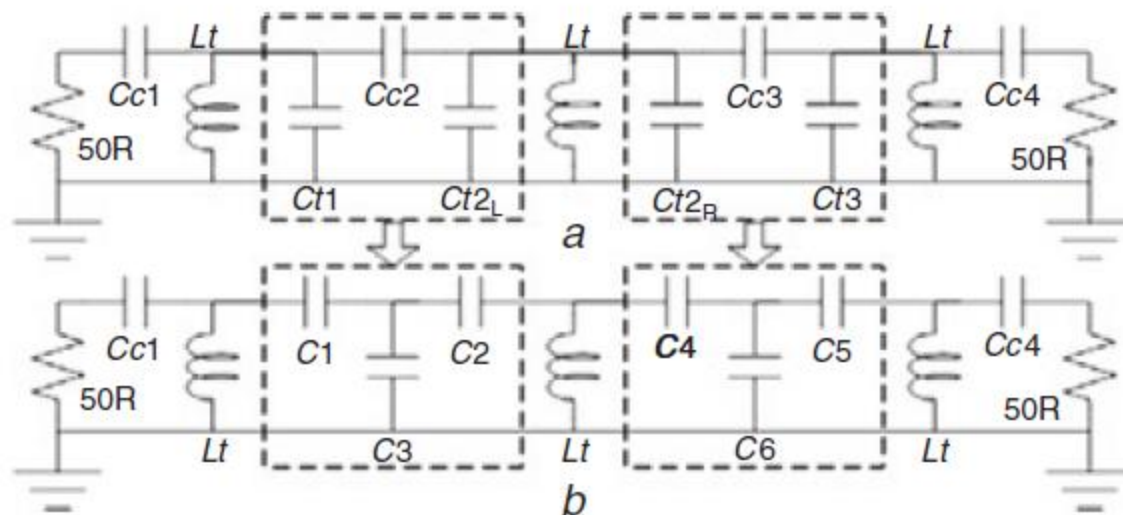


Fig. 2 Series coupled resonator filter topology and delta–star transformation

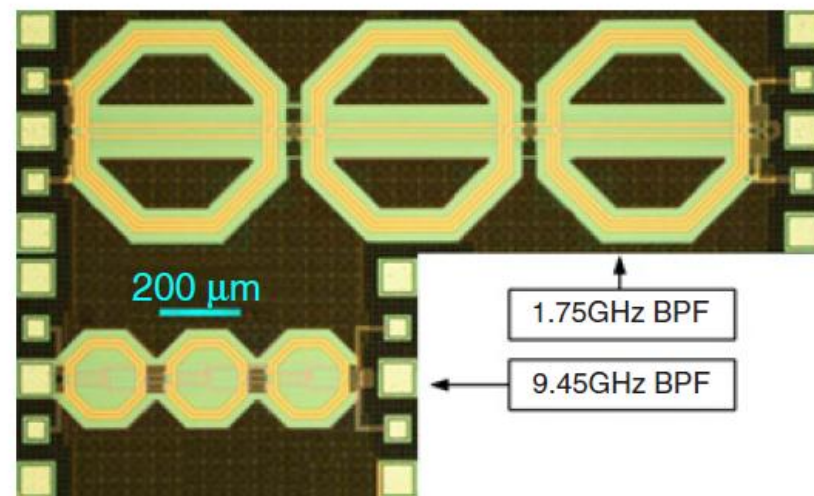


Fig. 3 Filter die photos including GSGSG pads

