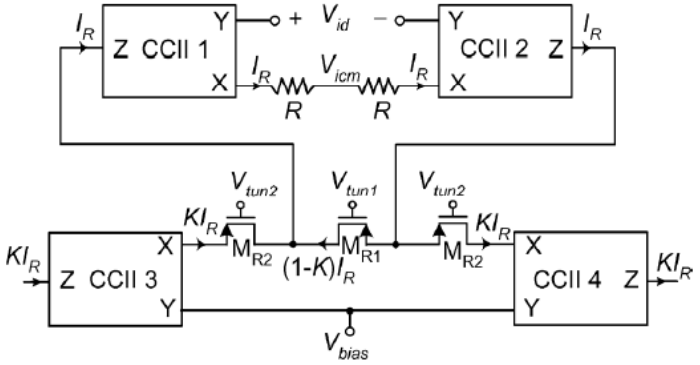
EE 508
Lecture 41

What filter architectures are really being used today?

Tunable Class AB CMOS Gm-C Filter Based on Quasi-Floating Gate Techniques

Coro Garcia-Alberdi, Antonio J. Lopez-Martin, *Senior Member, IEEE*, Lucia Acosta, Ramon G. Carvajal, *Senior Member, IEEE*, and Jaime Ramirez-Angulo, *Fellow, IEEE*

Manuscript received November 06, 2011; revised March 29, 2012, May 25, 2012; accepted July 24, 2012. This work was supported in part by the Spanish



ig. 2. Transconductor proposed.

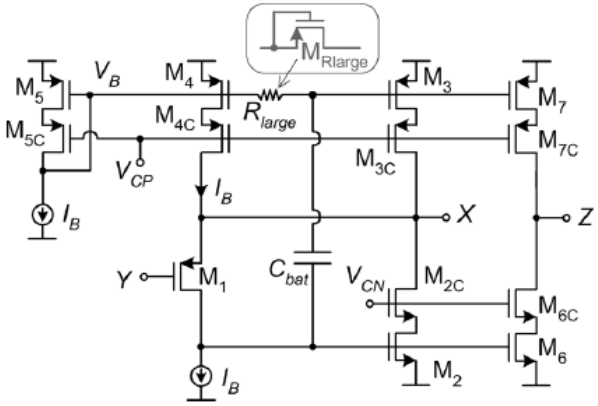


Fig. 3. Class AB CCII.

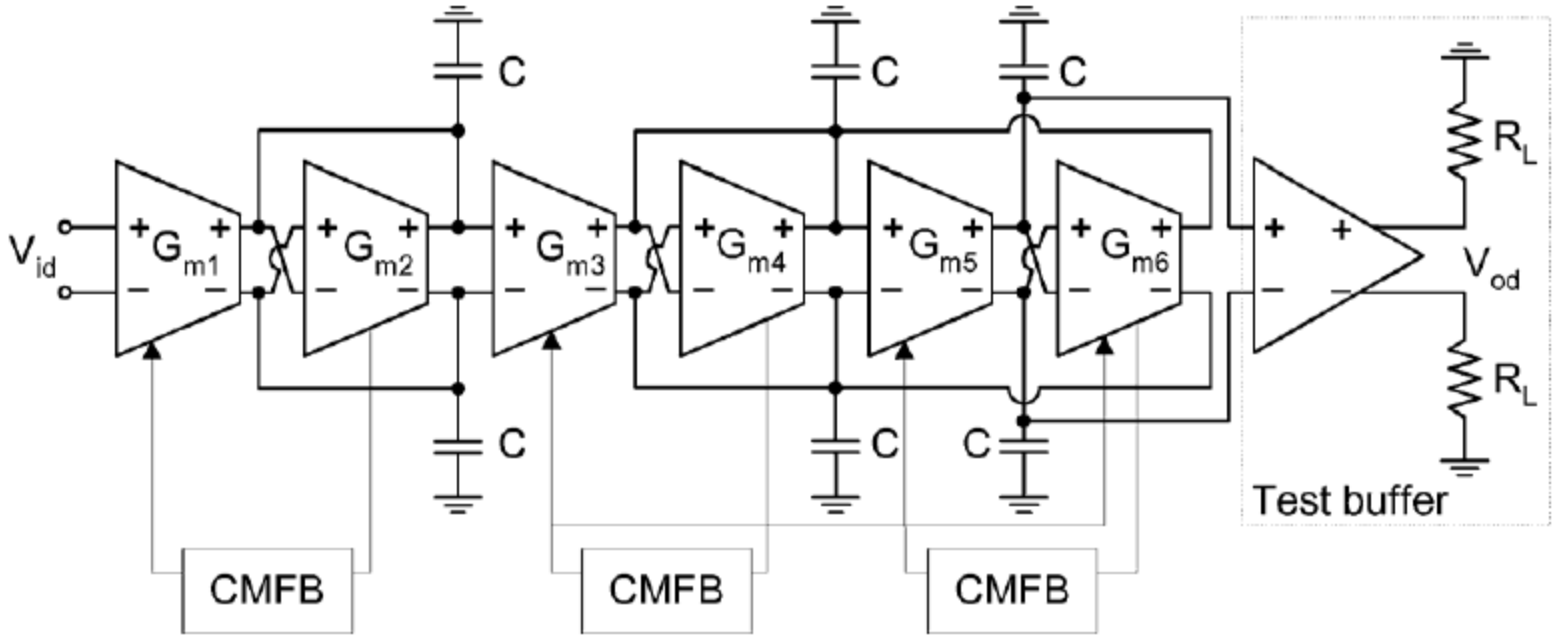


Fig. 5. Third-order Butterworth Gm-C channel filter.

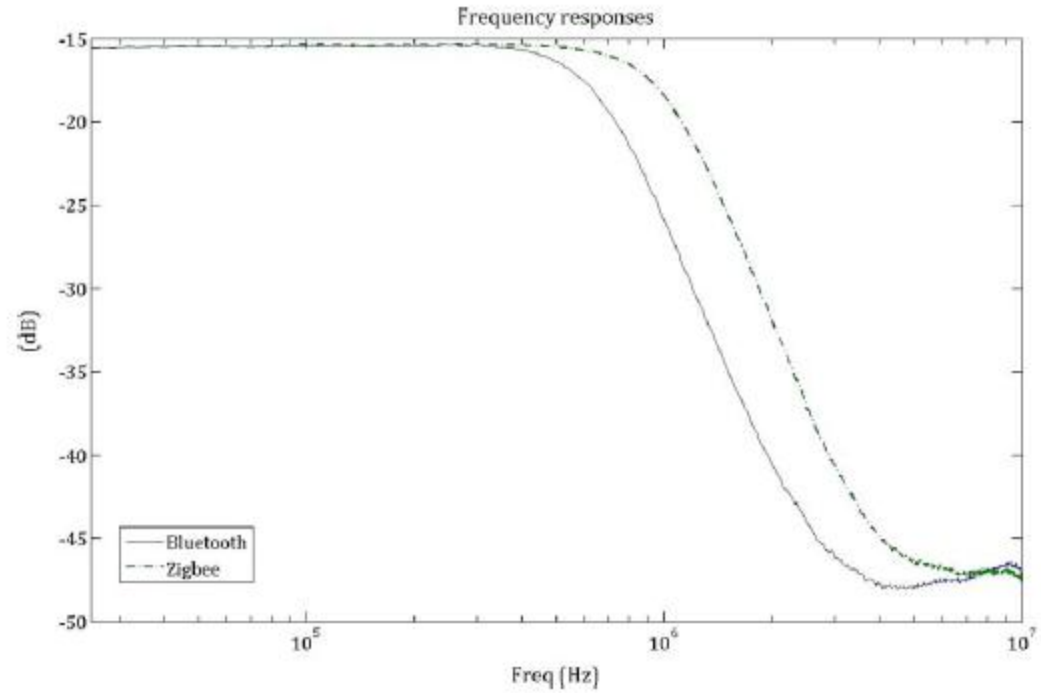
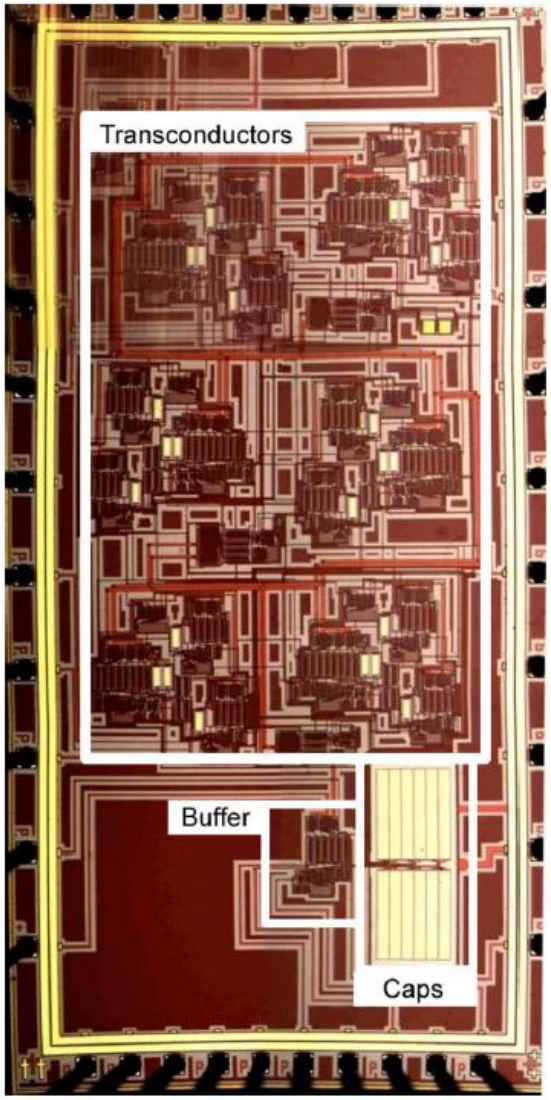


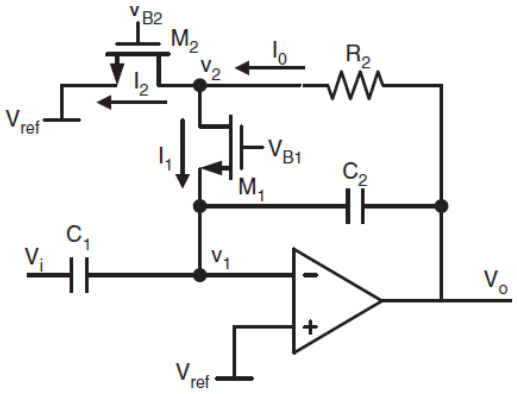
Fig. 10. Measured frequency response of the filter.


Transconductors
Buffer
Caps

5 mHz highpass filter with −80 dB total harmonic distortions

Haixi Li, Jinyong Zhang and Lei Wang

ELECTRONICS LETTERS 7th June 2012 Vol. 48 No. 12



a

Parameters	Values
C_1	1.5 pF
C_2	1.4 pF
R_2	297 kΩ
M_1	0.3 µm/9 µm
M_2	98 µm/0.3 µm
V_{B1} (at fc = 0.05 Hz)	1.25 V
V_{B2}	1.8 V
V_{ref}	0.9 V

b

Fig. 1 *Architecture and configuration of proposed first-order highpass filter*

a Architecture
b Configuration

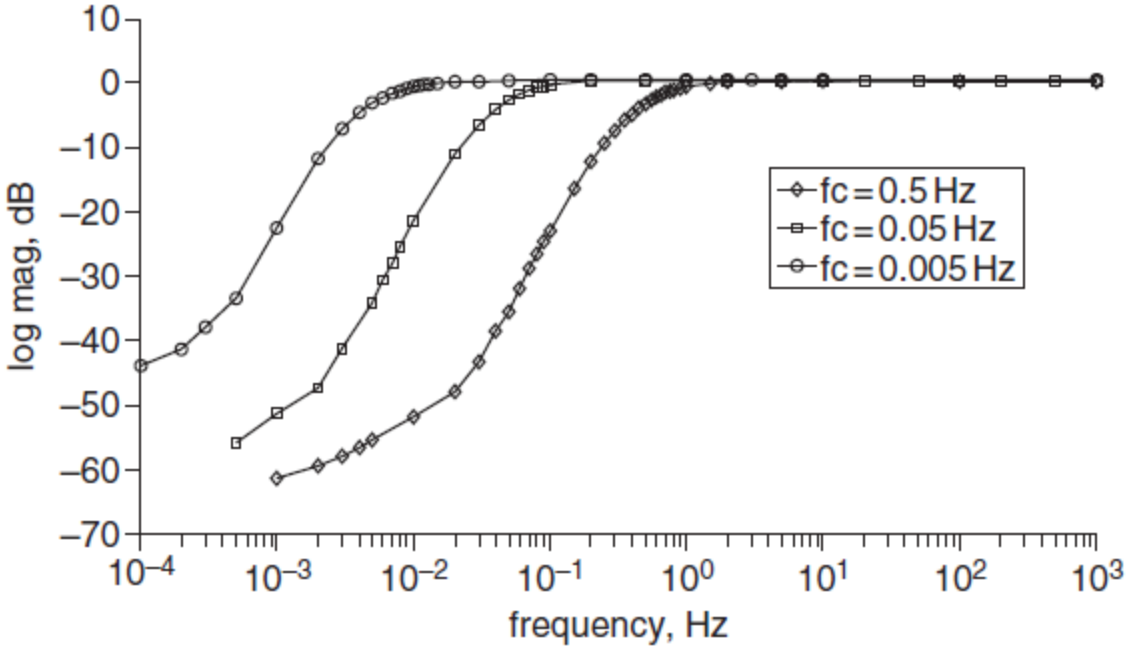


Fig. 2 *Frequency responses to three different −3 dB frequencies (fc) which are tuned by* V_{B1}

A 0.5-V R-MOSFET-C Filter Design Using Subthreshold R-MOSFET Resistors and OTAs With Cross-Forward Common-Mode Cancellation Technique

Phanumas Khumsat, *Member, IEEE*, and Apisak Worapishet, *Senior Member, IEEE*

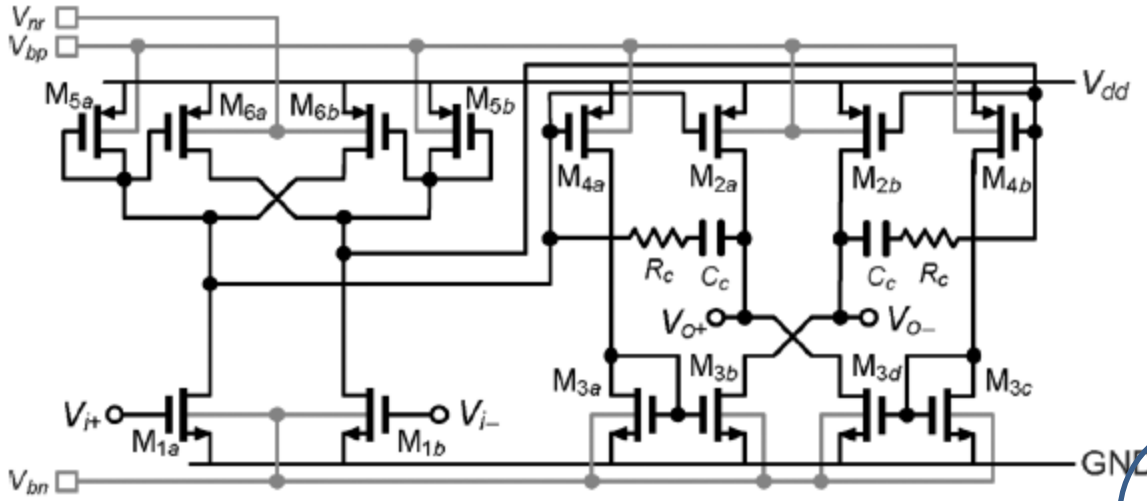
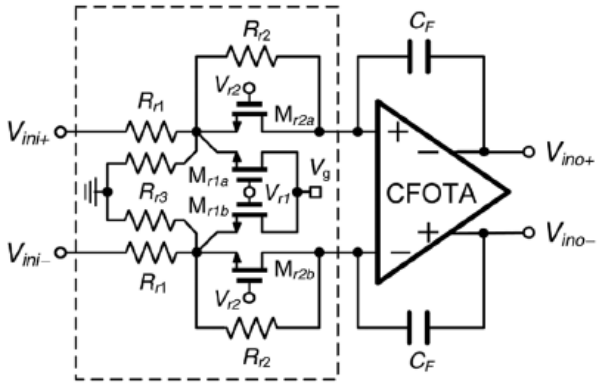


Fig. 1. Fully differential CFOTA with frequency compensation.



(a)

Mosfet-R integtator

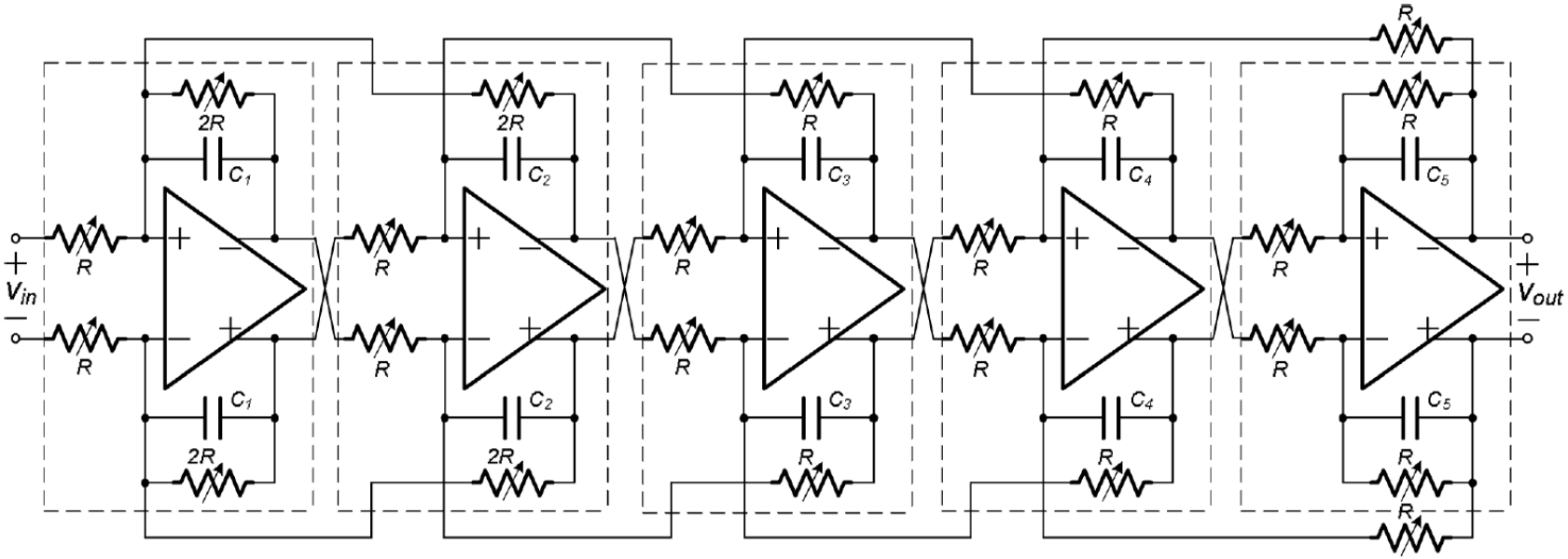


Fig. 9. Fifth-order Chebyshev R-MOSFET-C filter prototype. Each circuit in the dashed boxes is similar to Fig. 6.

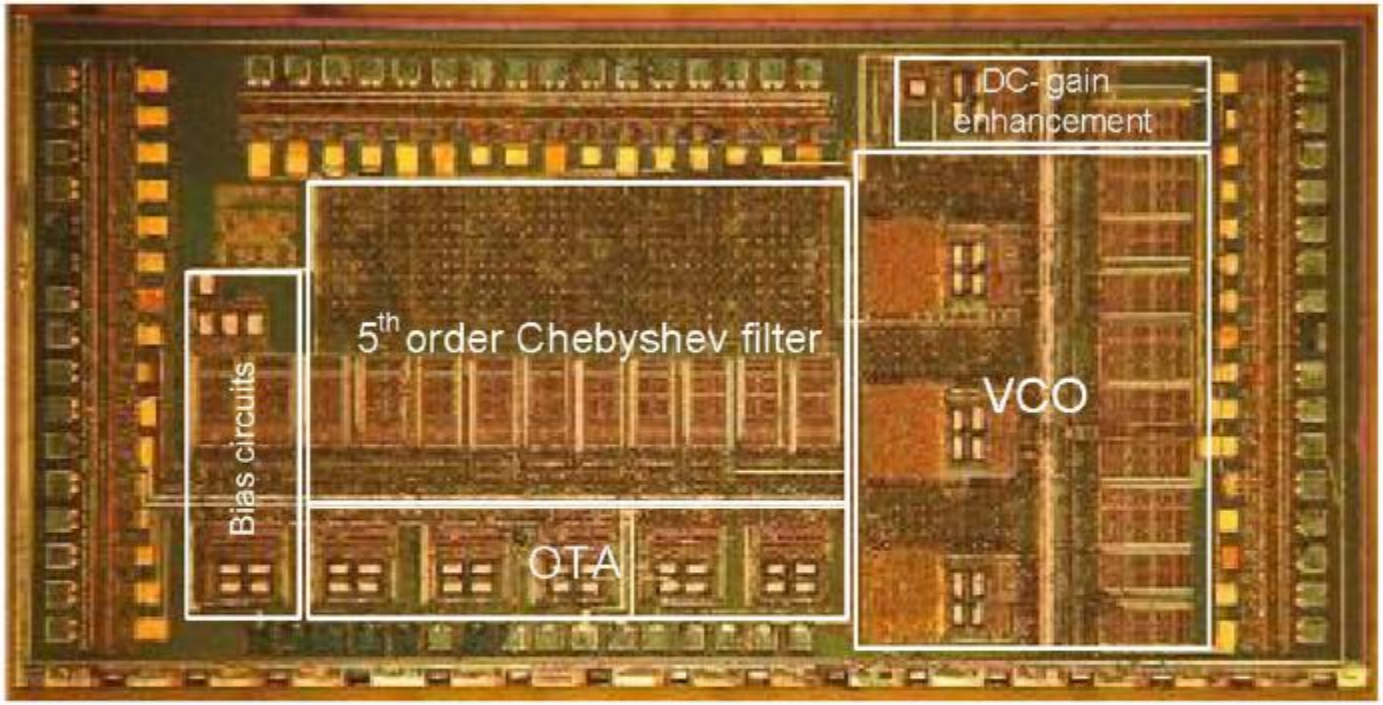
TABLE II
FILTER DESIGN PARAMETERS

Capacitor	Value	Capacitor	Value
C_1	11.31pF	C_5	22.62pF
C_2	16.31pF	Resistor	Value
C_3	33.70pF	R	75kΩ
C_4	16.31pF		

TABLE III
COMPONENTS PARAMETERS OF UNIT SUB-RMOS RESISTOR AND BIAS CIRCUITS [SEE FIG. 6] FOR A NOMINAL RESISTANCE VALUE OF 150 kΩ

Transistors	Sizes	Resistors	Values
M_{r1a}, M_{r1b}, M_{r2a}, M_{r2b}	100μm/1.8μm	R_{r1}, R_{r2}, R_{r3}	75kΩ
M_{c1}, M_{c2}, M_{c3}	192μm/0.36μm	R_{c4}	10kΩ
M_{c4}	30μm/0.48μm	R_g	75kΩ
M_g	48μm/0.48μm		

(a)



(b)

Fig. 10. Experimental 0.5-V filter. (a) Block diagram. (b) Chip microphotograph.

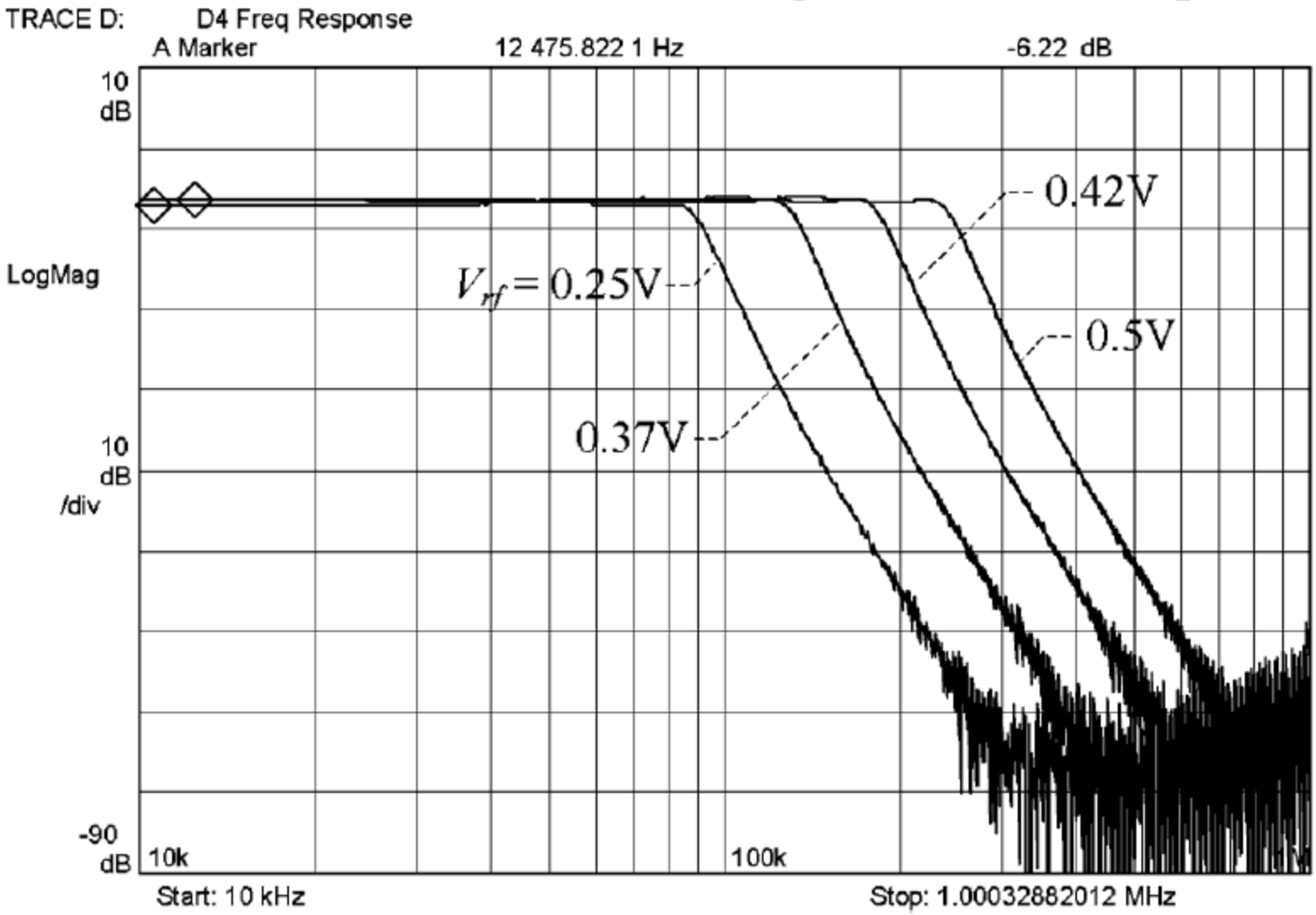


Fig. 11. Differential-to-single-ended frequency responses at different frequency tuning voltages V_{rf}.

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER VERY LOW-VOLTAGE FILTERS

	This work	[2]	[3]	[5]	[4]
Technology	0.18-μm	0.18-μm	0.18-μm	0.13-μm	0.18-μm
Threshold voltage, V_{th} with $V_b = V_s$	0.5 V	0.5 V	0.5 V	0.3 V	0.5 V
V_{dd}	0.5 V	0.5 V	0.6 V	0.55 V	0.6 V
V_{dd}/V_{th}	1.0	1.0	1.2	1.83	1.2
Filter type	5th-order Chebyshev	5th-order Elliptic	2nd-order Butterworth	4th-order Butterworth	5th-order Chebyshev
Filter structure	Leapfrog, active-*RC*	Leapfrog, active-*RC*	Leapfrog, active-*RC*	Cascaded biquadratic, active-G_m-*RC*	Leapfrog, companding
Nominal –3dB bandwidth	135 kHz	135 kHz	135 kHz	11.3 MHz	100 kHz
DC gain†	–0.3 dB	–0.35 dB	0 dB	–1.4dB	–2 dB
Input† (1%-THD)	219.2 mV_{rms} (@100 kHz)	50 mV_{rms} (@100 kHz)	212.2 mV_{rms} (@ 2kHz)	70.7 mV_{rms} (@ 1MHz)	-
Input-referred noise‡	195.4 μV_{rms}	74 μV_{rms}	-	110 μV_{rms}	-
Dynamic range (1%-THD)	61.0 dB	56.6 dB	64 dB (SNR)	60 dB	89 dB
In-band IIP3	+4 dBV_{rms}	–3 dBV_{rms}	+17 dBV_{rms}	–3 dBV_{rms}	–76 dBA_{rms}
Out-of-band IIP3	+14 dBV_{rms}	+5 dBV_{rms}	-	0 dBV_{rms}	–86 dBA_{rms}
In-band spurious-free dynamic range (SFDR)	53.7 dB (f_{in} = 50, 55kHz) 54.0 dB (f_{in} = 90, 95kHz)	-	-	-	-
Total current consumption	1.2 mA	2.2 mA	-	5.8 mA**	-
Total power consumption	0.6 mW 0.4 mW**	1.1 mW	1 mW	3.5 mW**	0.443 mW
Bandwidth tuning range	91 – 268 kHz	88 – 154 kHz	67 – 203 kHz	-	-
PLL lock range	190 – 400 kHz	-	-	-	-
PLL tone feed-through*	11.4 μV_{rms} @ 263 kHz 54.1 μV_{rms} @ 526 kHz 23.7 μV_{rms} @ 789 kHz	85 μV_{rms} @ 280kHz	-	-	-
Chip area (size breakdown) - OTAs - Filter resistors and capacitors - Bias circuits - VCO + DC Enhancement	0.25×1.17 mm^2 (0.29 mm^2) 0.7×1.17 mm^2 (0.82 mm^2) 0.75×0.25 mm^2 (0.19 mm^2) 1.07×0.77 mm^2 + 0.2×0.67 mm^2 (0.96 mm^2)	0.33×0.7 mm^2 (0.23 mm^2) 0.55×0.7 mm^2 (0.38 mm^2) 0.13×1.0 mm^2 (0.13 mm^2) 0.87×0.3 mm^2 (0.26 mm^2)	0.5×1.4 mm^2 (0.70$^{\delta}$ mm^2)	0.45$^{\delta}$ mm^2	2.128$^{\delta}$ mm^2
FOM	0.79 pJ 0.52 pJ**	2.41 pJ	2.34 pJ	0.0774 pJ**	0.0314 pJ

†: Differential
*: Measured at *single-ended* output with no input signal applied
‡: Integrated over 1 kHz to 1 MHz
**: No automatic-frequency tuning
$^{\delta}$: Total chip area

A 0.47mW 6th-Order 20MHz Active Filter Using Highly Power-Efficient Opamp

Le Ye, Congyin Shi, Huailin Liao*, and Ru Huang
Institute of Microelectronics, Peking University

978-1-4244-9474-3/11/$26.00 ©2011 IEEE

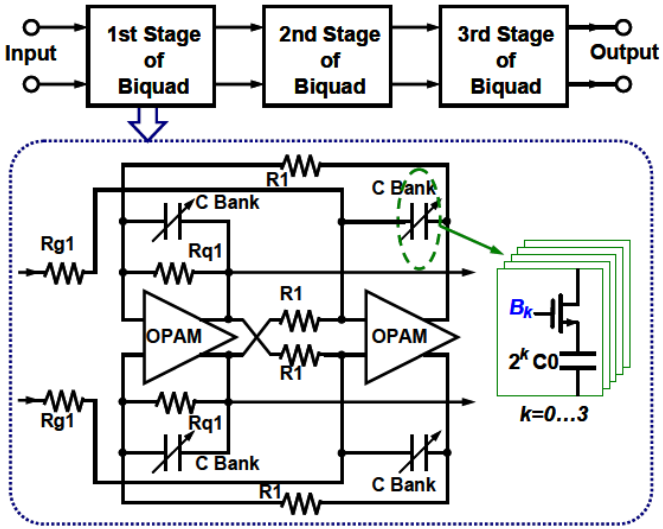


Figure. 5 The architecture of the proposed ultra-low power 6th-order active low-pass filte

Opamps. The tunable frequency bands are realized by switching the capacitor bank.

Authors claim Op Amp is highly power efficient

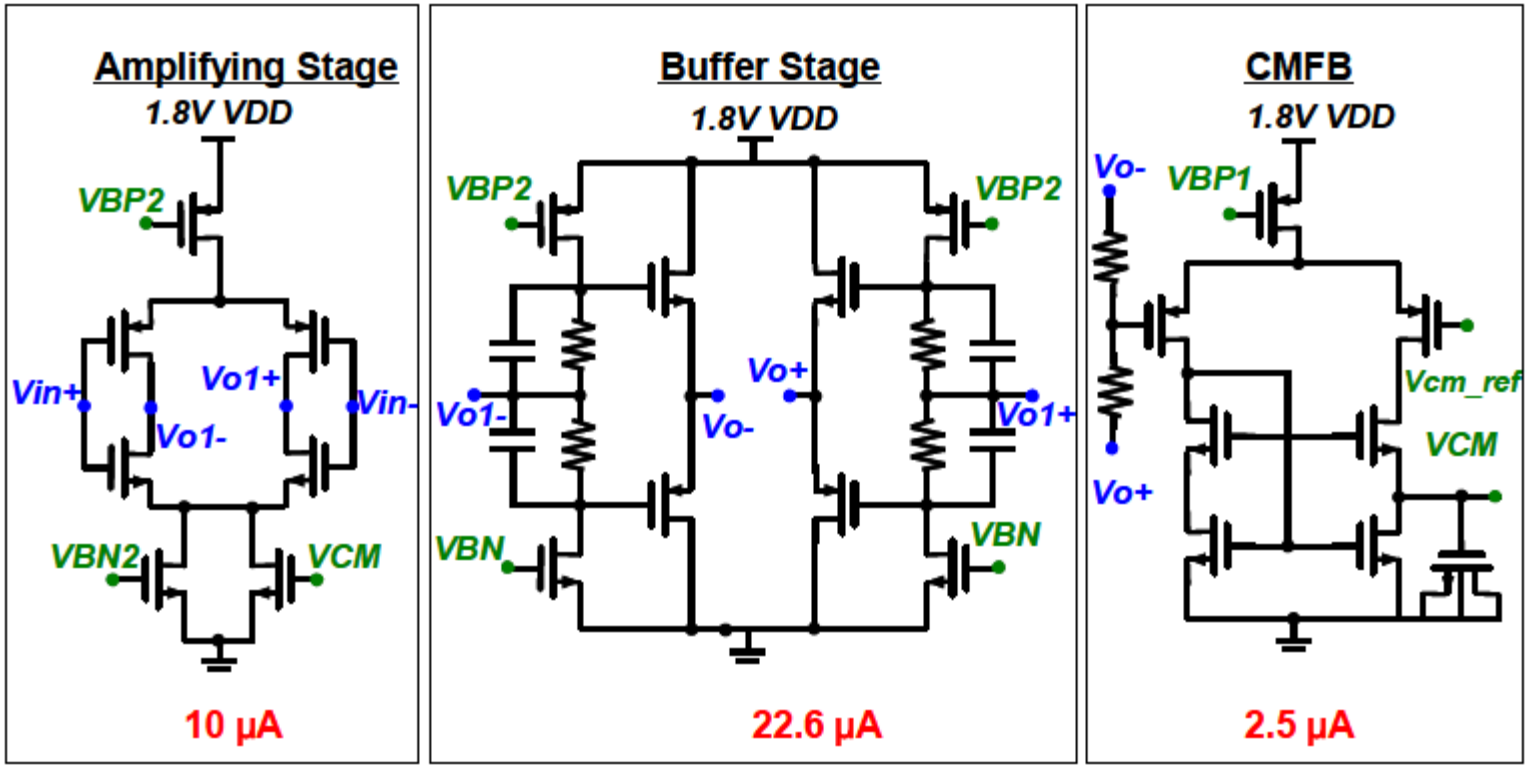


Figure. 4 The schematic of the proposed highly power-efficient Opamp

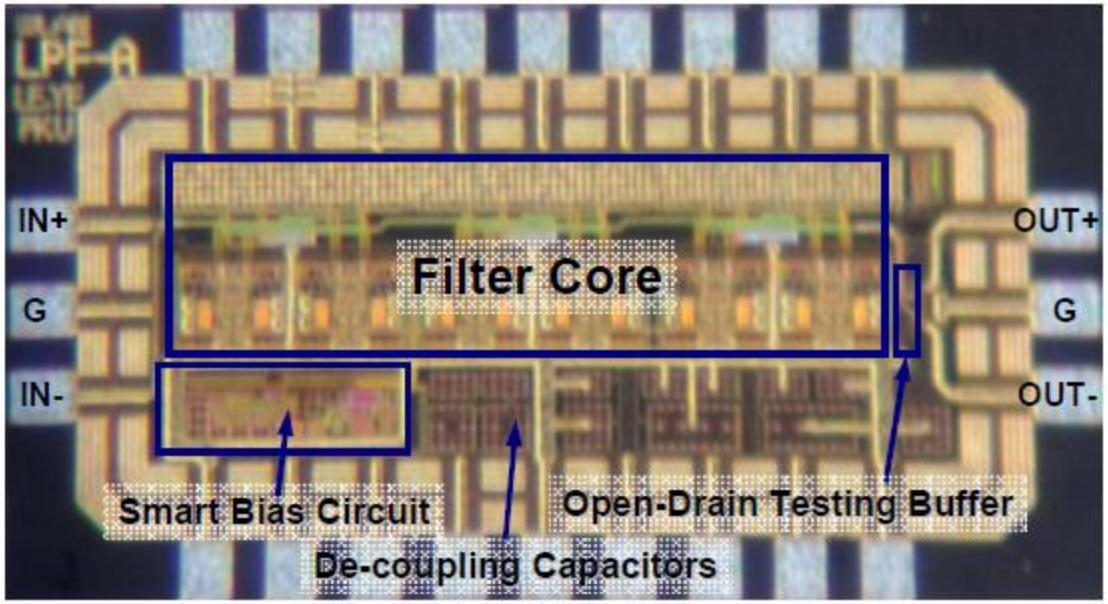


Figure. 6 The chip microphotograph.

Figure. 6 The chip microphotograph.

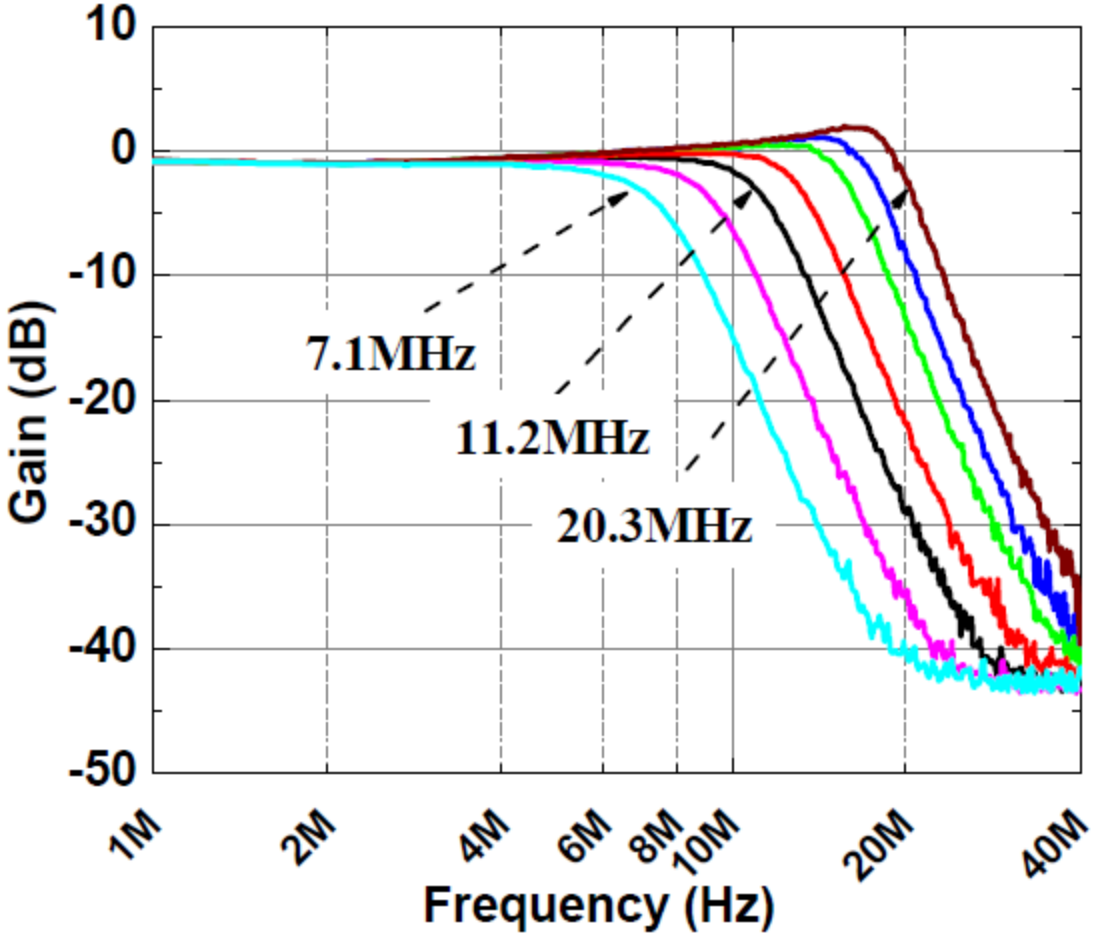


Figure. 7 The measured magnitude response of the filter with selected frequency tuning bands.

TABLE II. MEASURED PERFORMANCE SUMMARY

Technology	0.18 μm CMOS
Supply Voltage	1.8V ±10%
Filter Order	6
-3dB Cutoff Frequency	7.1 MHz ~ 20.3 MHz
DC voltage gain	-0.8 dB
Noise (100 kHz to 20 MHz)	298 μVrms
Noise Density	66.2 nV/√Hz
IIP3 @ 3 MHz, 5 MHz	20.9 dBm
Power Consumption	260 μA (0.47 mW)
Normalized Power	3.86 pW/Hz/pole
Silicon area without Pads	0.21 mm^2

TABLE I. PERFORMANCE COMPARISON OF THE PUBLISHED STATE-OF-THE-ART FILTERS

Ref	[3] RFIC 2005	[4] JSSC 2007	[5] ISCAS 2009	[6] JSSC 2006	[7] ISSCC 2006	This work
Technology	90nm CMOS	0.13 µm CMOS	65 nm CMOS	0.13µm CMOS	0.18 µm CMOS	**0.18 µm CMOS**
VDD	1.4 V	1.5 V	1.3 V	1.2 V	1.8 V	**1.8 V**
Topology	Gm-C	Active-RC	Active-RC	Active-Gm-RC	Source-follow-based	**Active-RC**
Filter Order	6	5	5	4	4	**6**
BW	10/100 MHz	19.7 MHz	9 MHz	11 MHz	10 MHz	**7.1 to 20.3MHz**
Noise Density	19 nV/√Hz	30 nV/√Hz	6.5 pA/√Hz	10.9 nV/√Hz (1)	7.5 nV/√Hz	**66.2 nV/√Hz**
In-band OIP3 (2)	15.5 dBm (3)	17.3 dBm (4)	--	21 dBm	13.5 dBm (5)	**20.1 dBm**
Filter Area	0.55 mm^2	0.20 mm^2	0.46 mm^2	0.9 mm^2	0.26 mm^2	**0.21 mm^2**
Power	13.5 mW	11.3 mW	12.4 mW	14.2 mW	4.1 mW	**0.47 mW**
Normalized Power	**22.5** pW/Hz/pole (6)	**115** pW/Hz/pole	**276** pW/Hz/pole	**323** pW/Hz/pole	**103** pW/Hz/pole	**3.86 pW/Hz/pole**
FOM	**440.6** (7)	**171.7**	--	**304.1**	**615.5**	**2779**

(1) Calculated from the reported 36 µVrms integrated input-referred noise; (2) For fear comparison, take the voltage gain into account; (3) calculated from the

Wide-Loading-Range Fully Integrated LDR With a Power-Supply Ripple Injection Filter

Edward N. Y. Ho and Philip K. T. Mok, *Senior Member, IEEE*

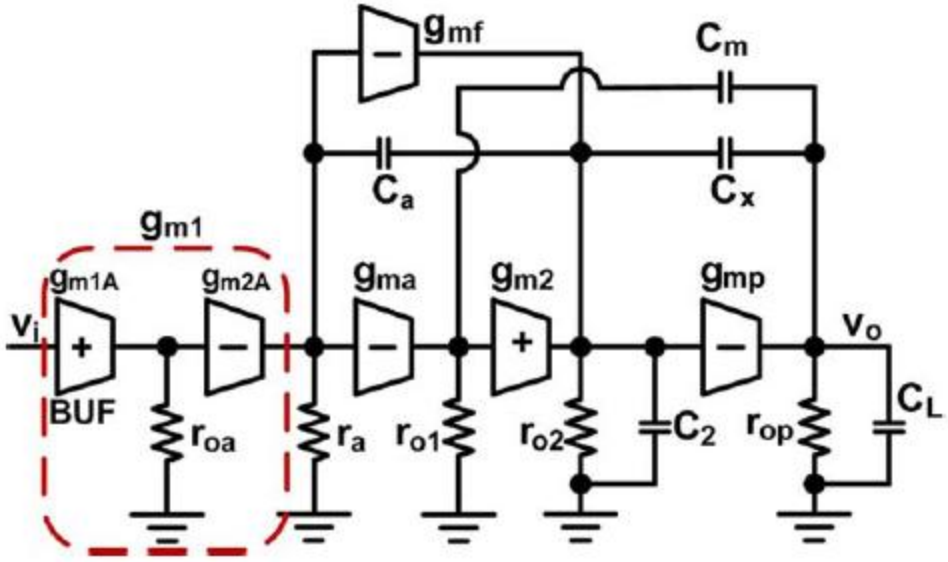


Fig. 3. Small-signal model of the proposed design.

A 30-MHz–2.4-GHz CMOS Receiver With Integrated RF Filter and Dynamic-Range-Scalable Energy Detector for Cognitive Radio Systems

Masaki Kitsunezuka, Hiroshi Kodama, Naoki Oshima, Kazuaki Kunihiro, Tadashi Maeda, *Member, IEEE*, and Muneo Fukaishi, *Member, IEEE*

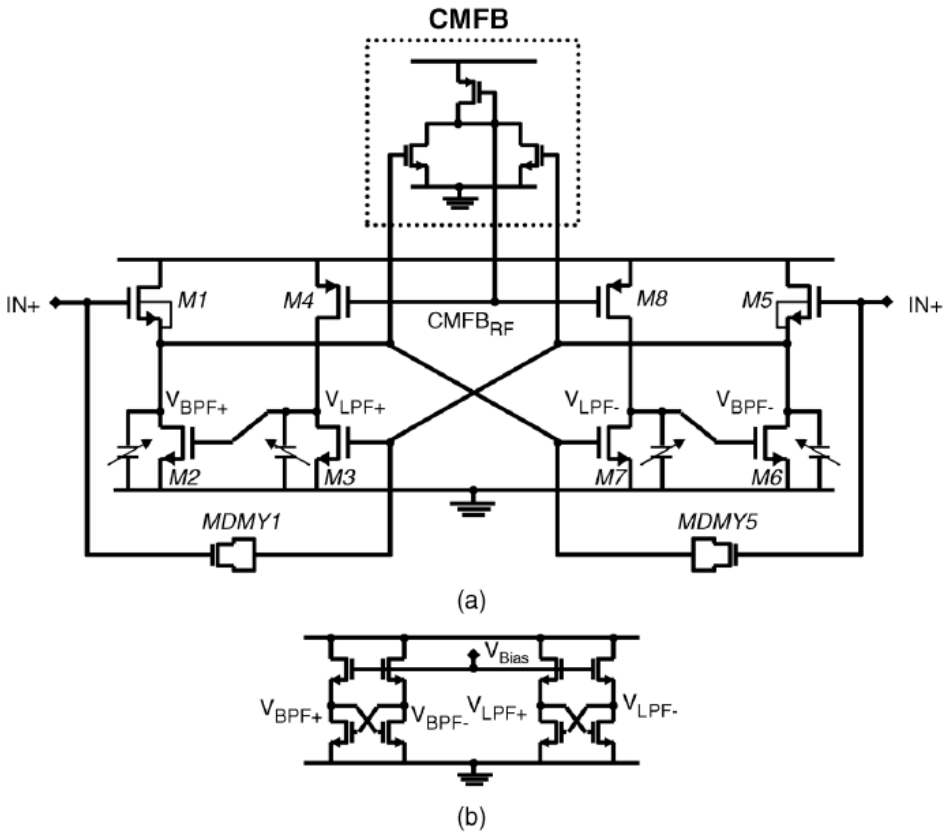


Fig. 4. (a) Circuit diagram of differential RF filter and (b) common-mode rejection/stabilization circuit.

To enable a wide tuning range (30 to 800 MHz) to be covered, 4-bit binary-weighted load-capacitor arrays are used to vary the filter characteristics. In addition, transconductance gain g_m is controlled by tuning the gate bias voltage of M1. Fig. 5

The transfer functions of the BPF and LPF are expressed as

$$H_{\mathrm{BPF}}(s) = \frac{V_{\mathrm{BPF}}}{V_{\mathrm{in}}} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}} \tag{1}$$

and

$$H_{\mathrm{LPF}}(s) = \frac{V_{\mathrm{LPF}}}{V_{\mathrm{in}}} = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s\frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}}, \tag{2}$$

respectively, where g_{mi} is the transconductance gain of transistor M_i. The cut-off (or center) frequency and quality factor are respectively written as

$$\omega_c = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}} \tag{3}$$

and

$$Q = \frac{\sqrt{g_{m2}g_{m3}}}{g_{m1}}\sqrt{\frac{C_1}{C_2}}. \tag{4}$$

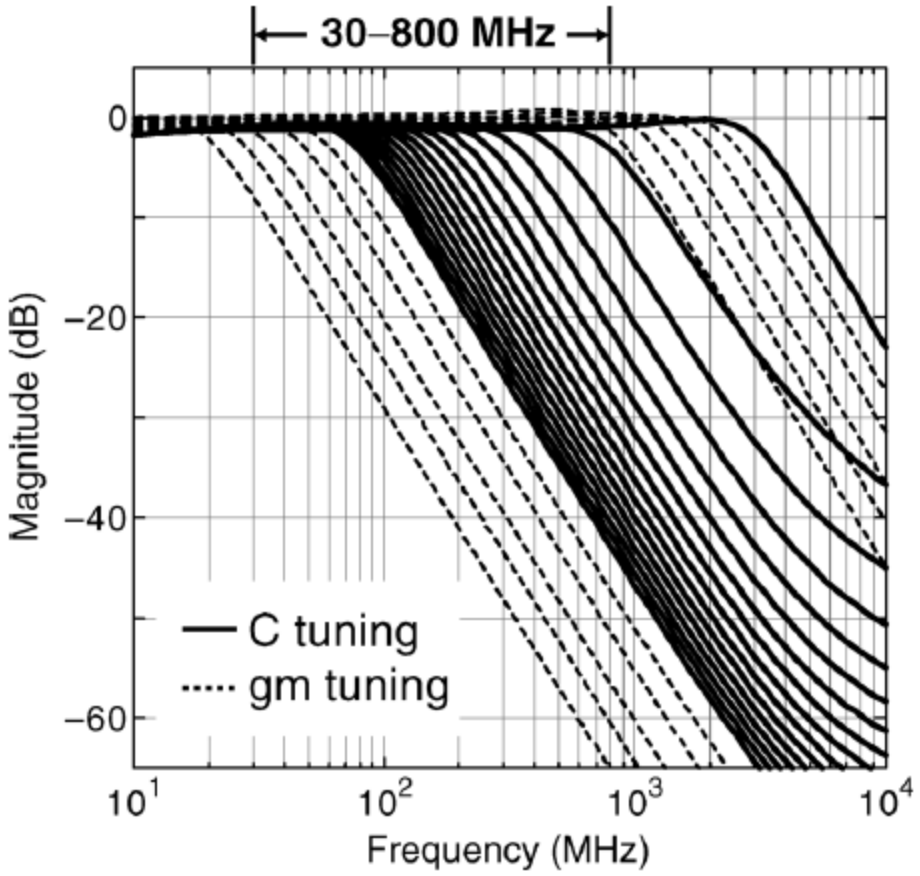
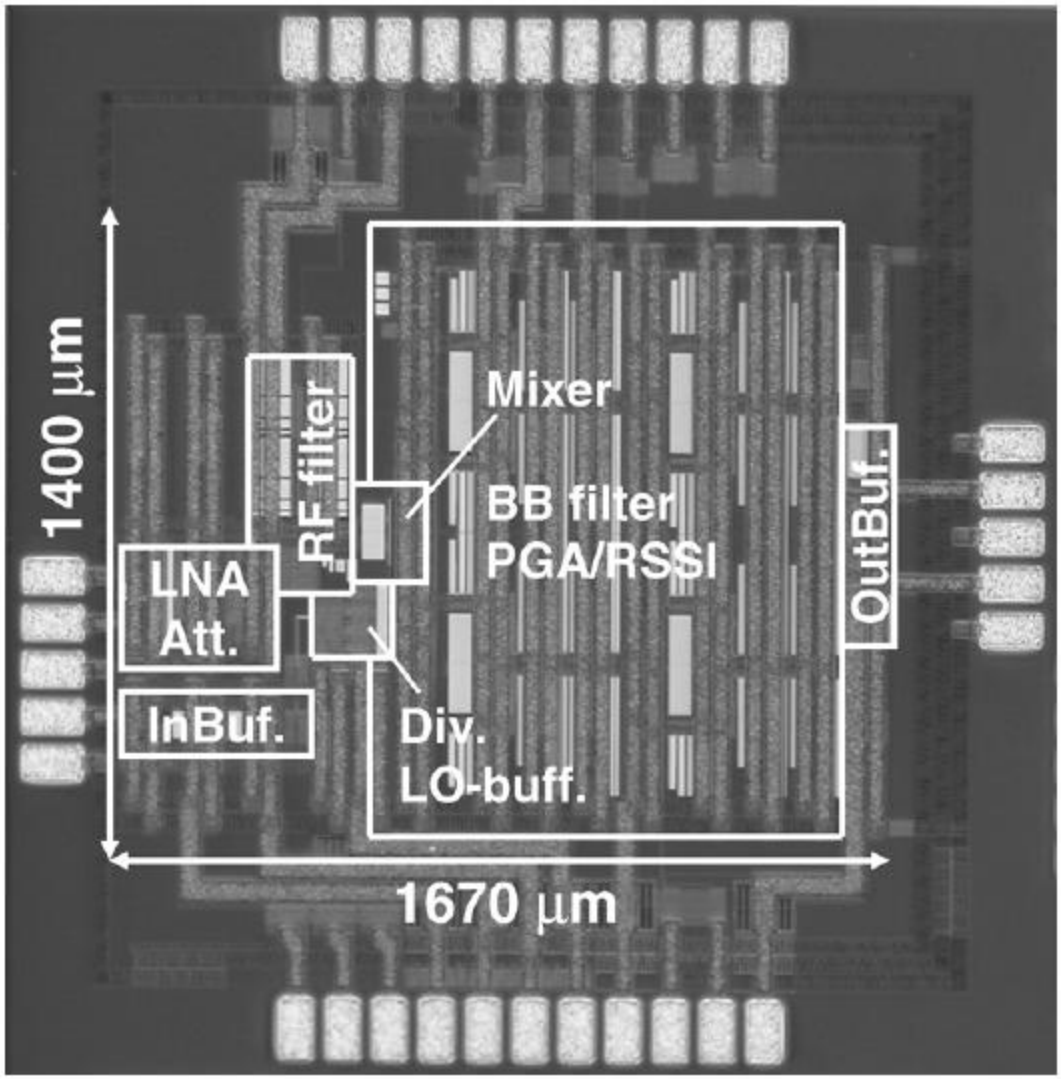


Fig. 5. Simulated frequency characteristics of RF filter.


1400 µm
1670 µm
RF filter
Mixer
BB filter
PGA/RSSI
LNA
Att.
InBuf.
Div.
LO-buff.
OutBuf.

A 4th-Order 84dB-DR CMOS-90nm Low-Pass Filter for WLAN Receivers

M. De Matteis[1], A. Pezzotta[2], A. Baschirotto[2]
[1]Innovation Engineering Department. University of Salento. Italy. [2]Department of Physics, University of Milano Bicocca. Italy
marcello.dematteis@unisalento.it, a.pezzotta1@campus.unimib.it, andrea.baschirotto@unimib.it

978-1-4244-9474-3/11/$26.00 ©2011 IEEE

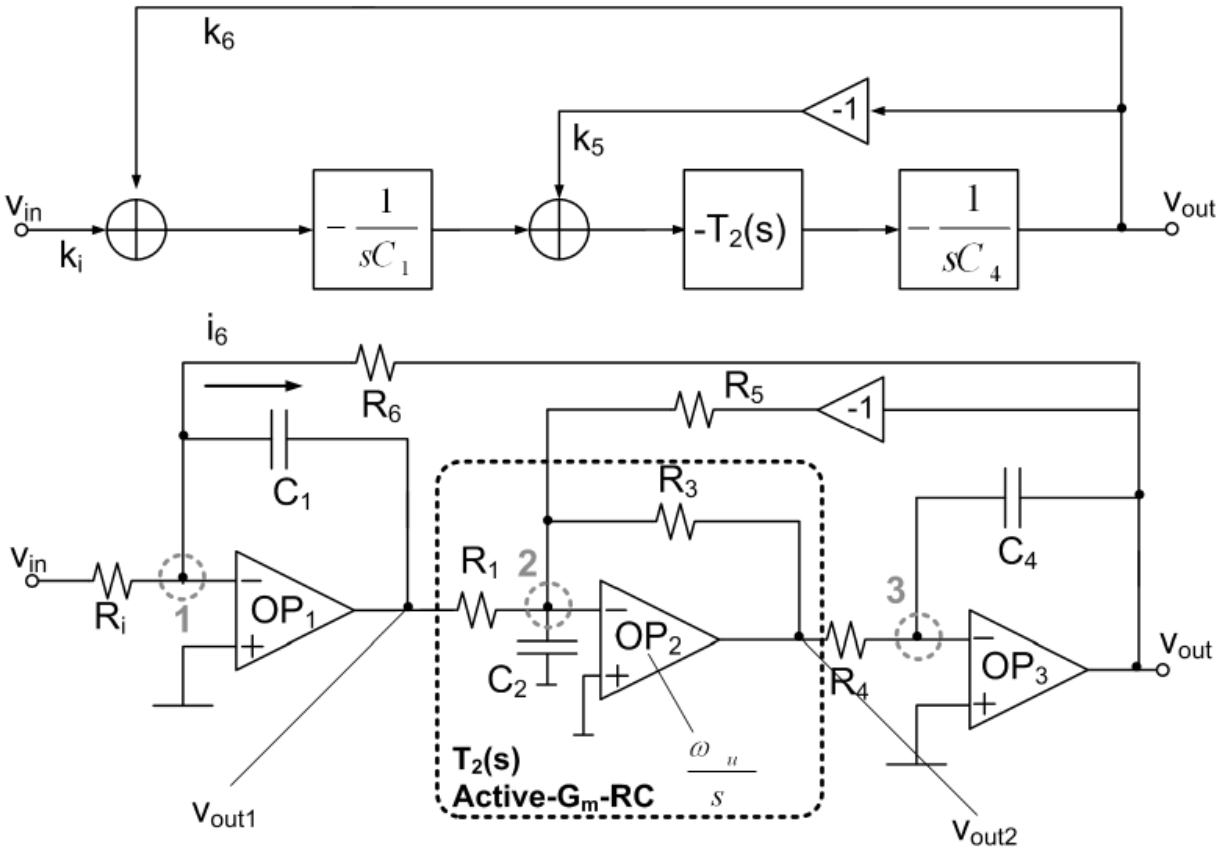


Fig. 1 - WLAN 4th Order Filter Block/Circuital Scheme

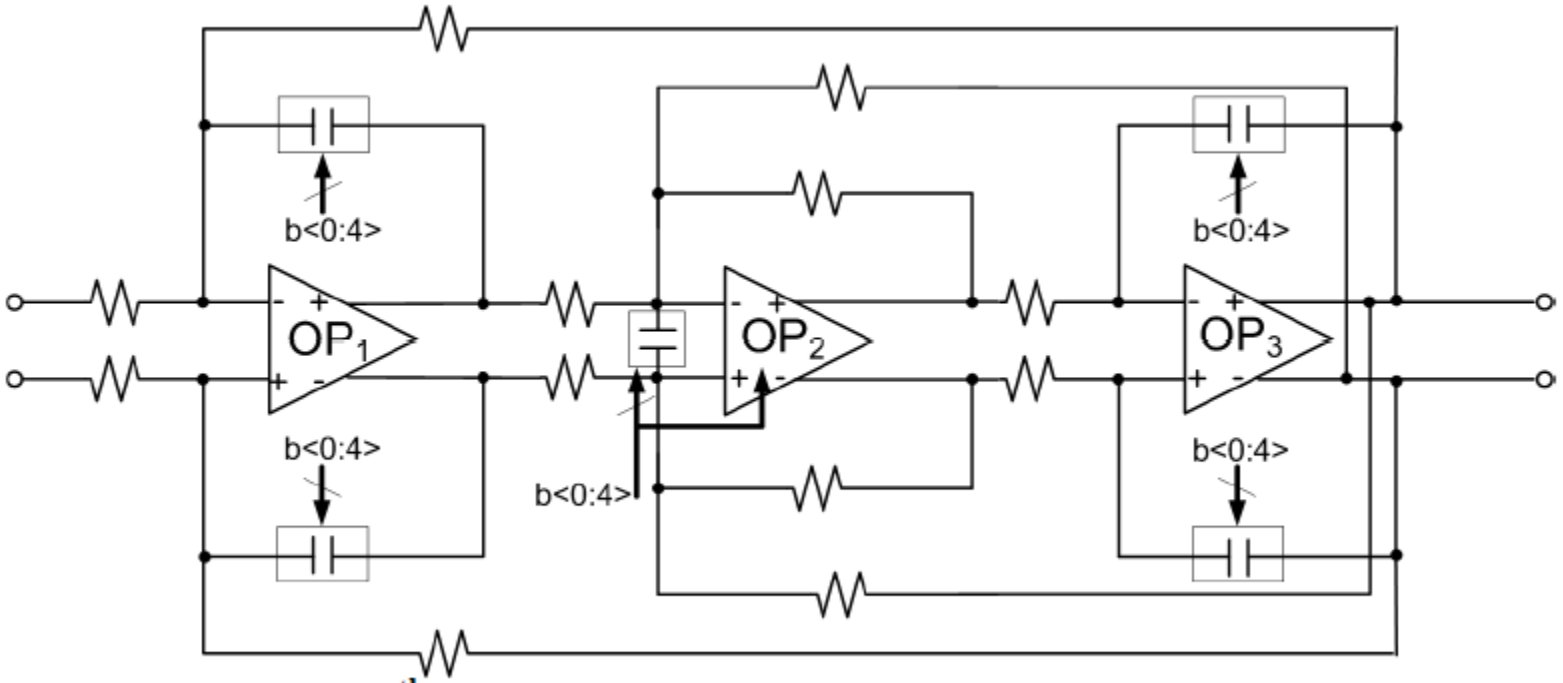


Fig. 5 – 4th Order WLAN Filter – Top-View Schematic

The uncertainty on the passive components nominal value due to the fabrication process and temperature variations can reach the 45%, affecting the filter frequency response. Any process variation and temperature dependencies can be compensated by tuning either the R's or the C's values. The

in the Fig. 6. The array value is, then, set by the external using a proper digital code.

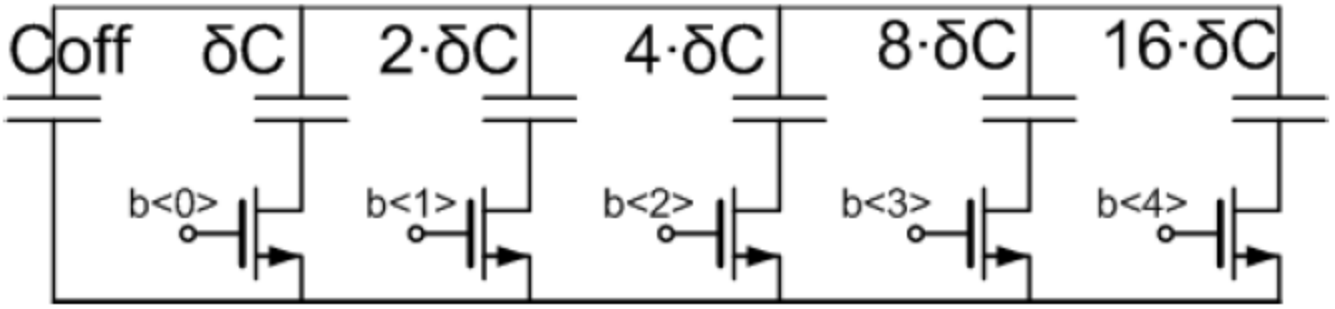


Fig. 6 – Capacitor Array

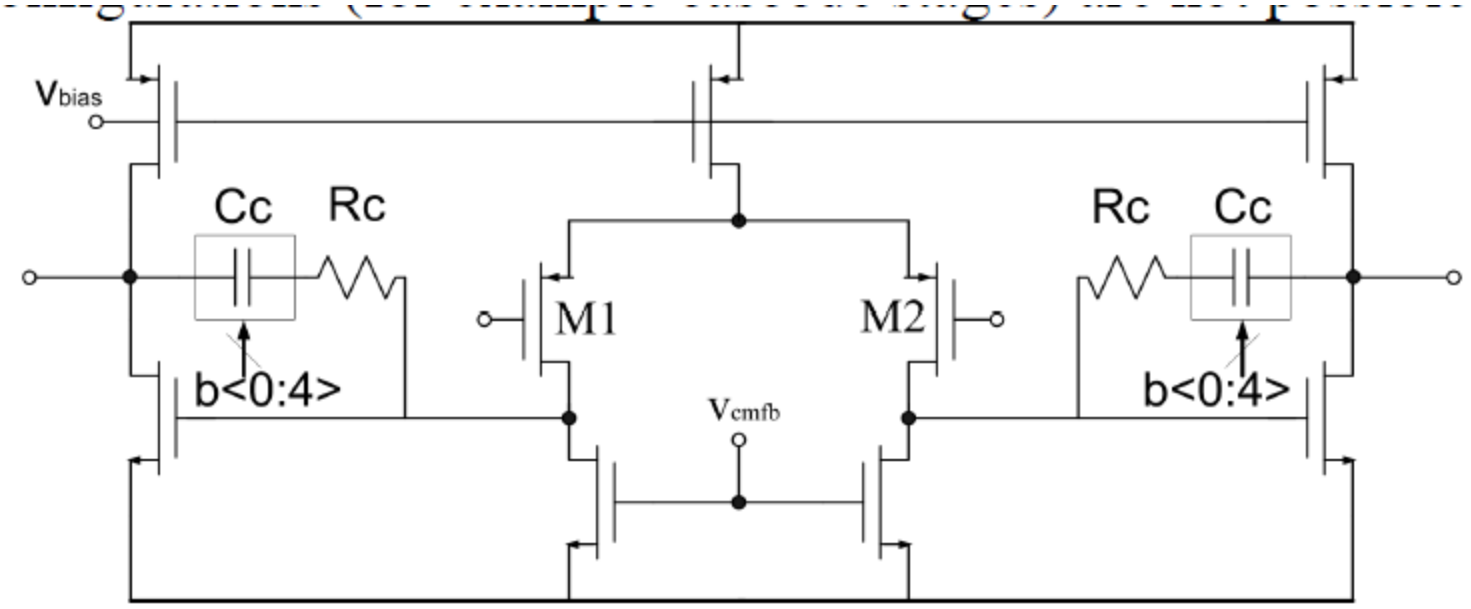


Fig. 7 – Opamp Schematic

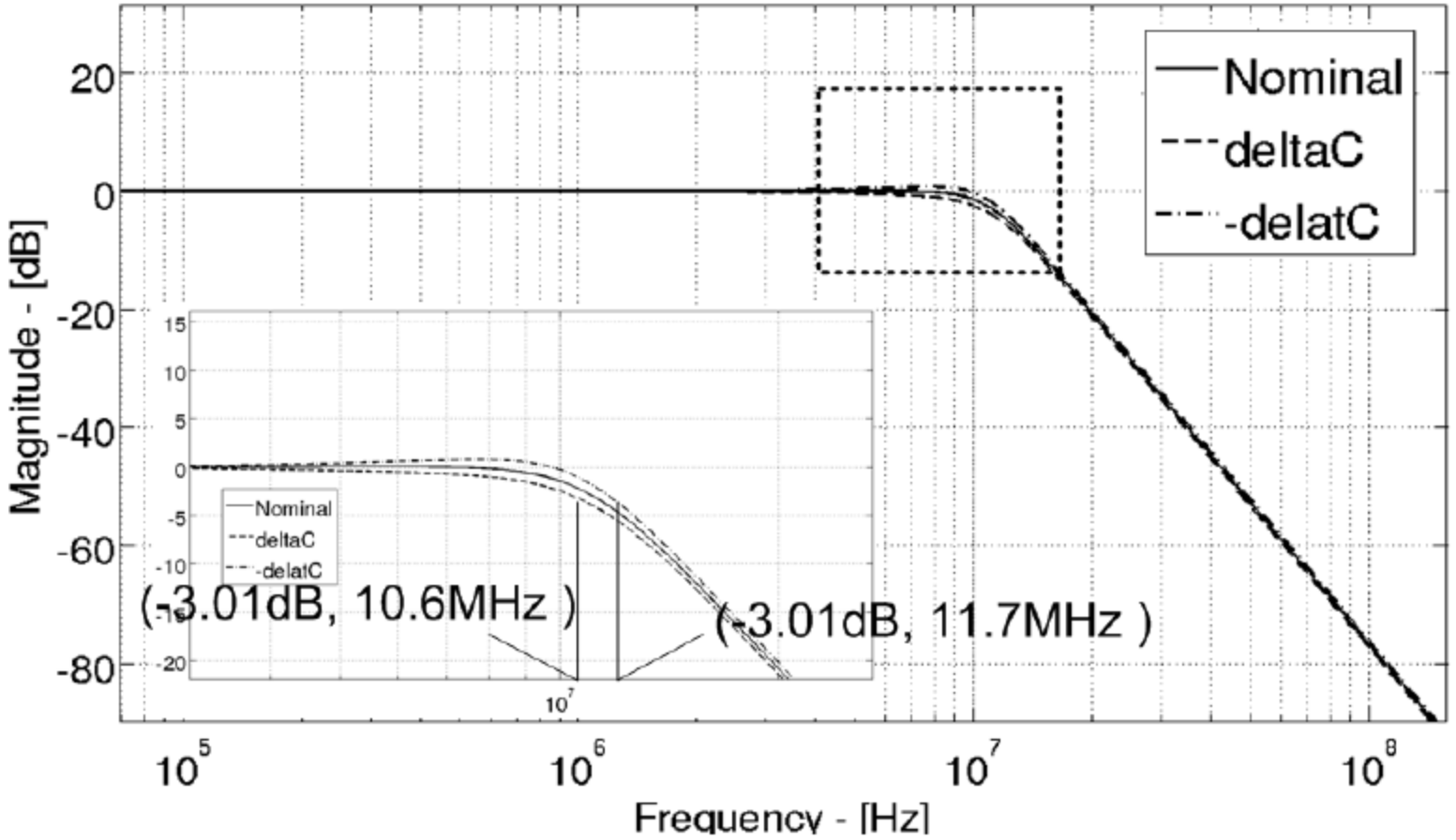


Fig. 8 – Filter Frequency Response

Parameter	Value
G[dB]	0
$f_{@-3dB}$[MHz]	11
avdd[V]	1.2
CMOS Technology	90nm
Power Consumption[mW]	14
Output Integrated Noise[μV_{rms}] - (100kHz÷20MHz)	48
IRN Spectral Density@2MHz [nV/√Hz]	5
THD[dBc] – v_{out}=1.05$V_{zero-peak}$@4MHz	40
DR@THD=40dBc - [dB]	84
IIP3 [dBm] - v_{in}=v_{in1}+v_{in2} - v_{in1}@4MHz, v_{in2}@5MHz	10

Tab. IV – Filter Performance Resume

A 23.4 mW 68 dB Dynamic Range Low Band CMOS Hybrid Tracking Filter for ATSC Digital TV Tuner Adopting RC and Gm-C Topology

Kuduck Kwon, *Member, IEEE*, and Kwyro Lee, *Senior Member, IEEE*

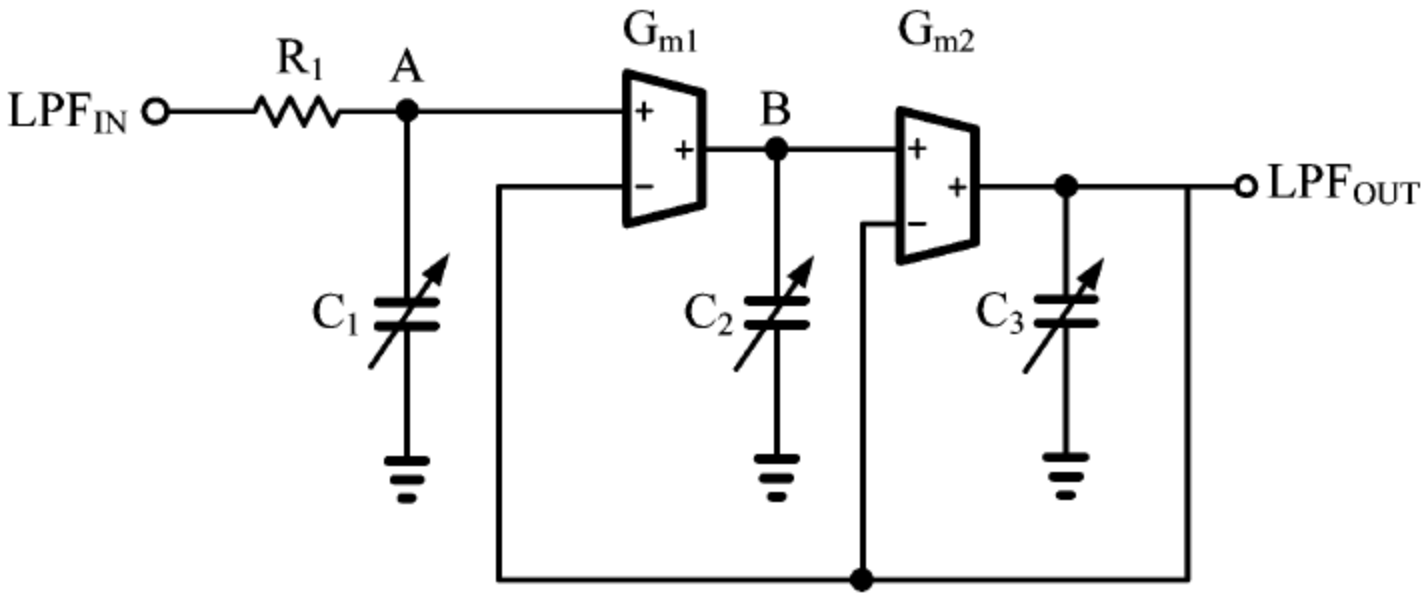


Fig. 3. Proposed third-order Chebyshev hybrid tracking low-pass filter.

A 23.4 mW 68 dB Dynamic Range Low Band CMOS Hybrid Tracking Filter for ATSC Digital TV Tuner Adopting RC and Gm-C Topology

Kuduck Kwon, *Member, IEEE*, and Kwyro Lee, *Senior Member, IEEE*

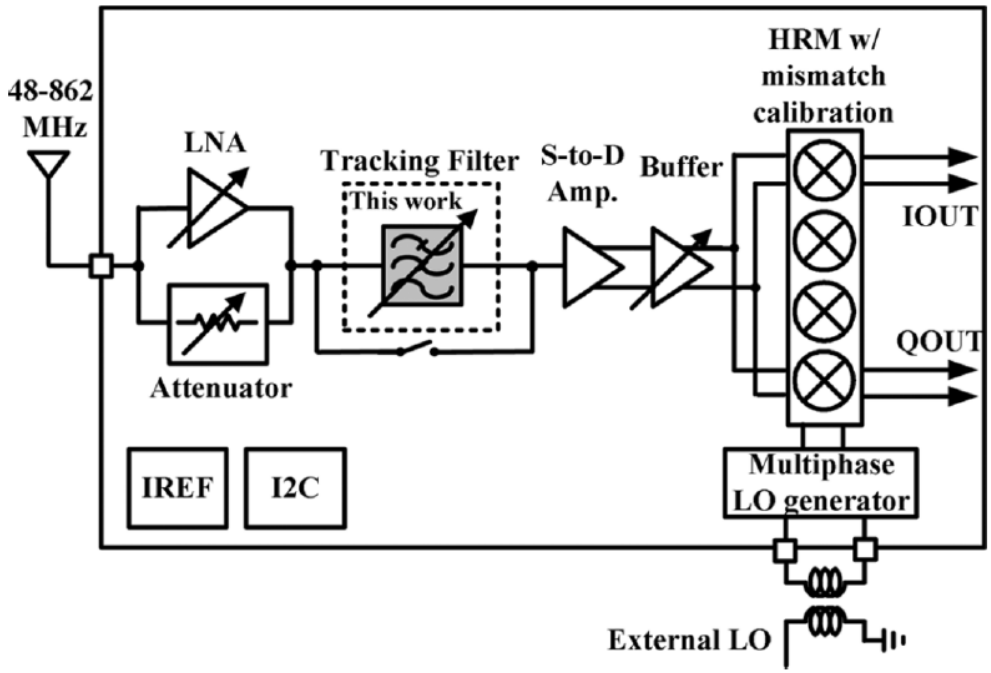


Fig. 1. Block diagram of RF front-end for ATSC terrestrial digital TV tuner.

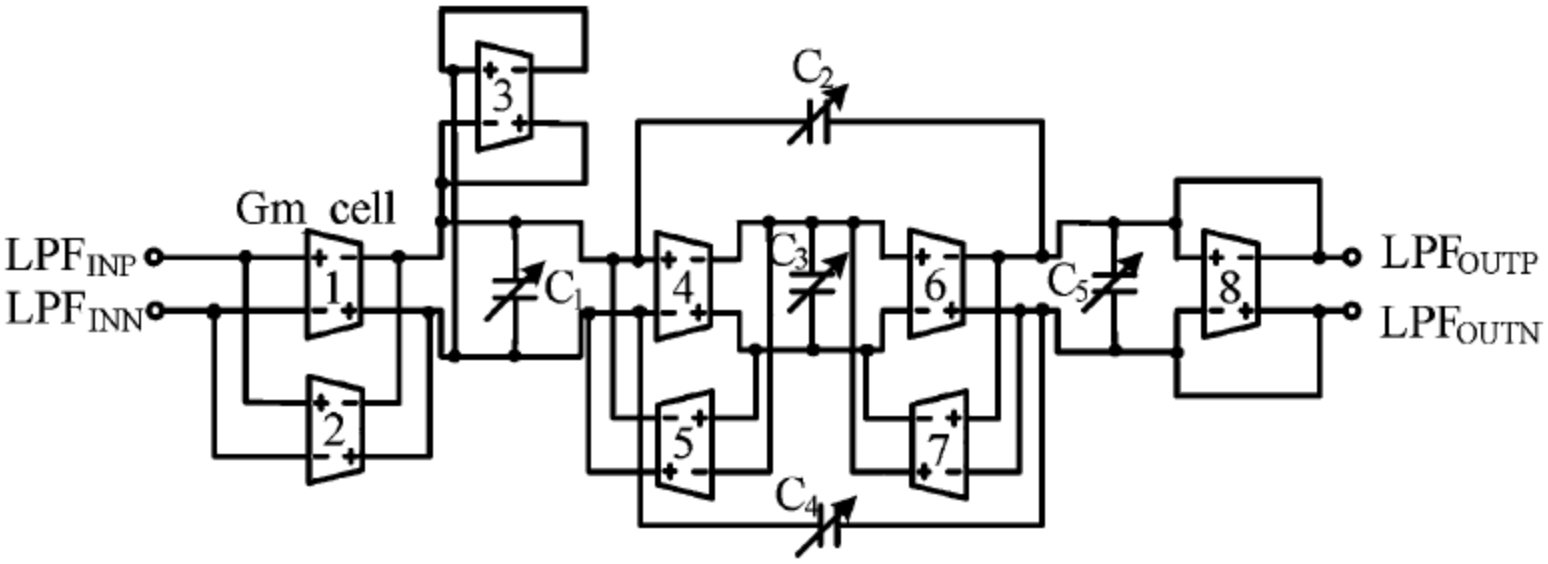


Fig. 2. Third-order elliptic transconductor-C low-pass filter based on ladder filter structure.

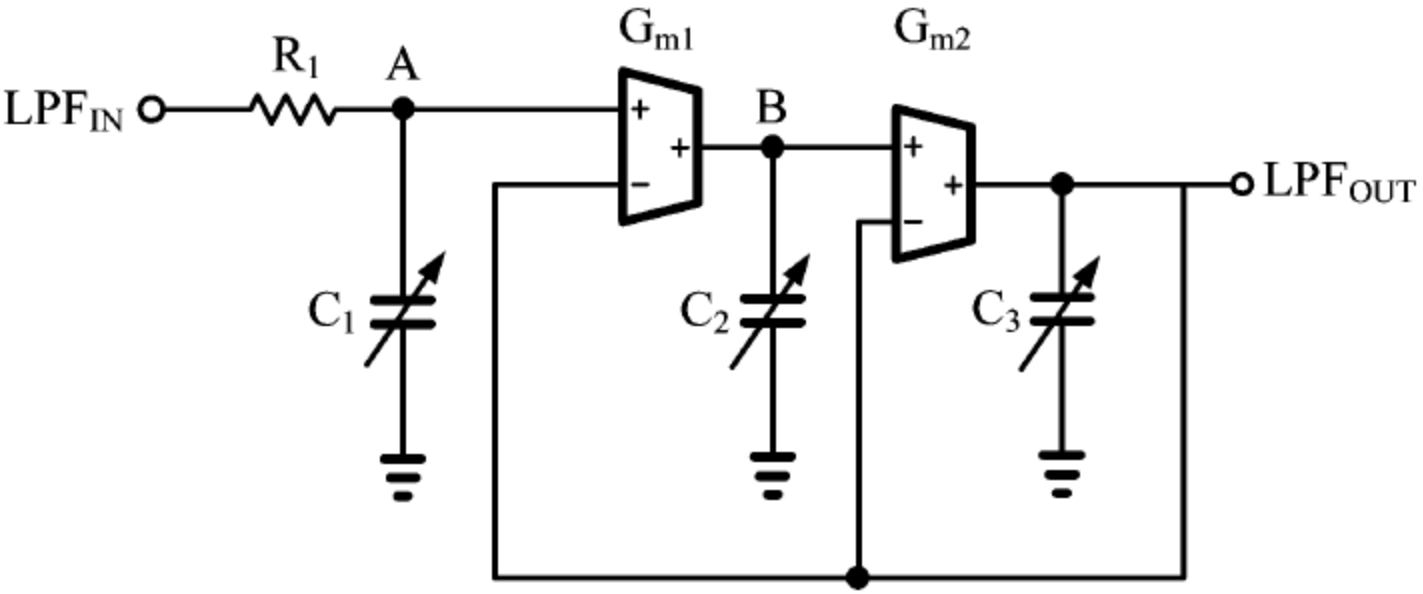


Fig. 3. Proposed third-order Chebyshev hybrid tracking low-pass filter.

COMPONENTS VALUES AND TRANSISTOR SIZES

Components	R_1	C_1*	C_2*	C_3*	G_{m1}	G_{m2}
Values	200 [Ω]	5 [pF]	19 [pF]	36 [pF]	16 [mS]	16 [mS]
Transistor	MT		ST		LT	
Sizes [W/L]	108μm /0.18μm		22μm /0.18μm		186μm /0.35μm	

*C1, C2, and C3 in Table II are values for 100MHz of -1dB cut-off frequency.

capacitor

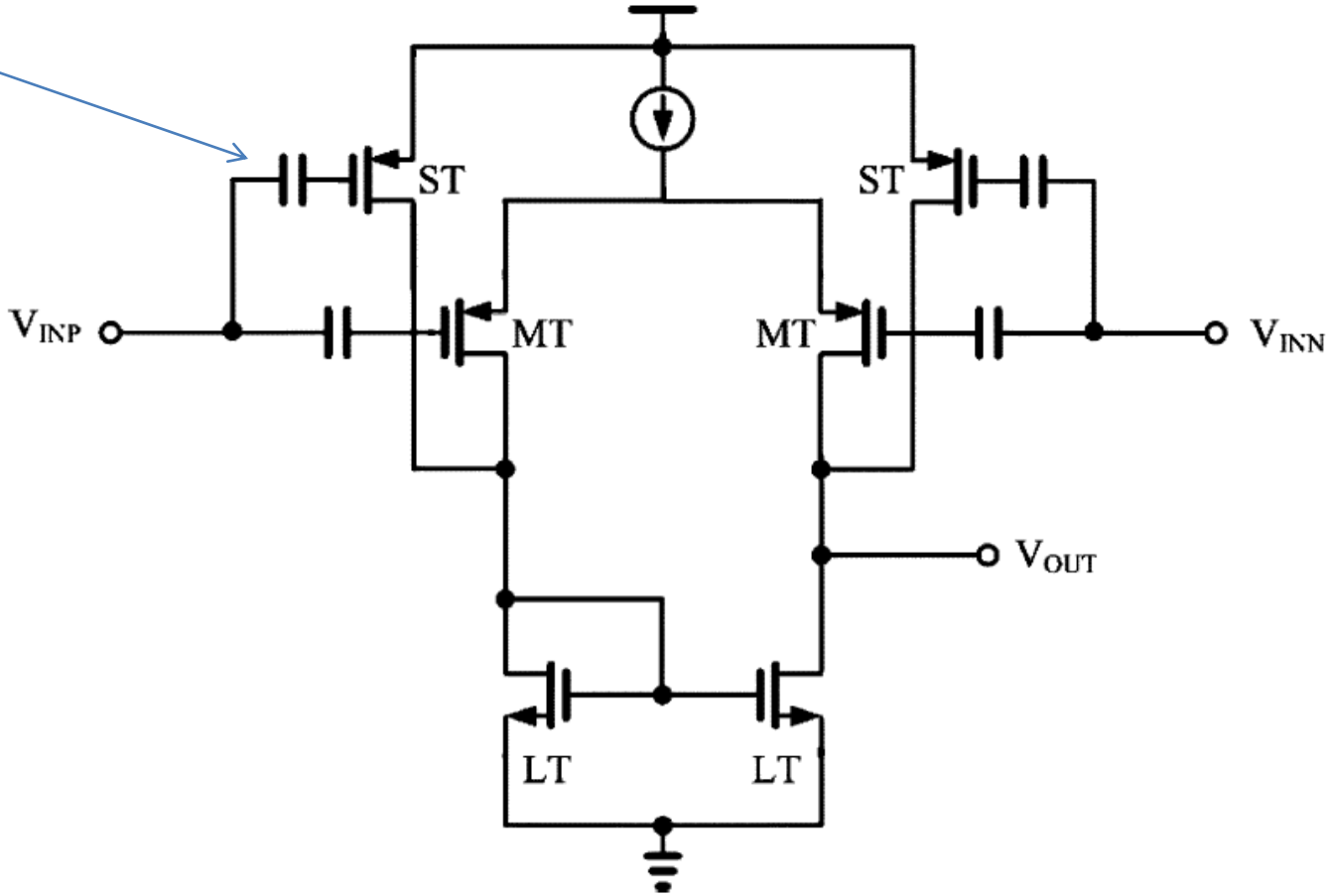
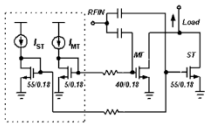


Fig. 4. Transconductor.

ST transistors operating in weak inversion provide linearization of basic transconductance stage. Transistor biasing not shown but described in [11]

For the robust characteristics to variations of process, supply voltage, and temperature, the MT and ST are biased with current-mirror bias circuitry [11].



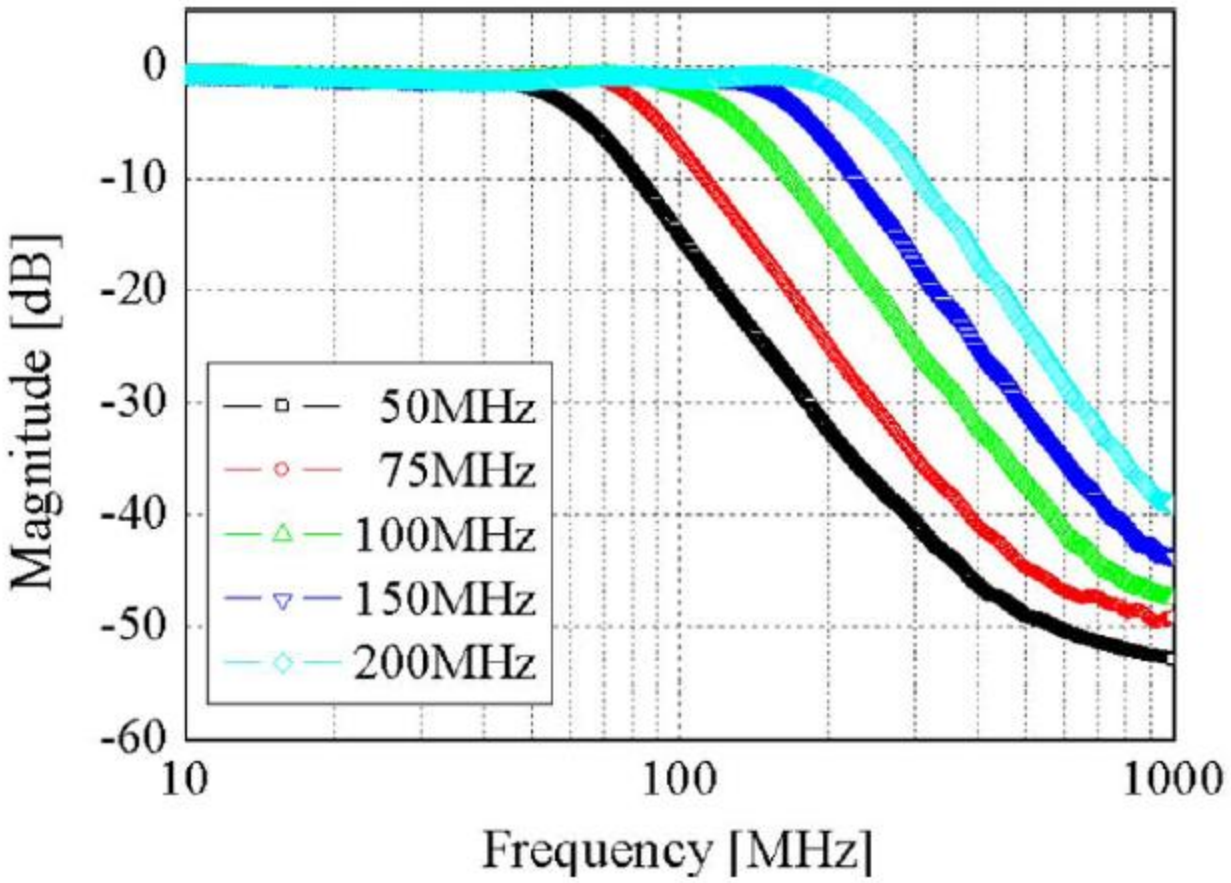

0
-10
-20
-30
-40
-50
-60
Magnitude [dB]
10
100
1000
Frequency [MHz]
50MHz
75MHz
100MHz
150MHz
200MHz

TABLE IV
COMPARISON WITH OTHER REPORTED FILTERS

	[1]	[18]	[19]*	[25]	[26]	[27]	[28]	This work
Technology	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	0.25μm CMOS	0.25μm CMOS	0.35μm CMOS	0.13μm CMOS	0.18μm CMOS
Cut-off freq.(*f*) [MHz]	50-300	50-300	50-300	80-200	30-120	200	200	50-200
OIP3 [dBm]	14	11	16.9	18.8	10.1	17	14	17.3
NF [dB]	17	20	14	-	-	-	32	15
Filter order (N)	4	4	3	7	8	7	2	3
Single (S) or Differential (D)	D	D	D	D	D	D	D	S
Pdc [mW]	72	7.6	72	210	120	60	20.8	23.4
FOM (FOM2**) (FOM3***)	51 (2511) (51)	120 (11926) (120)	152 (3673) (152)	- (1264) -	- (327) -	- (1170) -	0.3 (483) (0.3)	193 (5901) (96.5)

*[19] is our previous work of the tracking filter utilized for both ATSC terrestrial and Cable digital TV standards

**FOM2 is the equation excluding the (F-1) term in the FOM of equation (14) because [25]-[27] do not indicate the noise performance

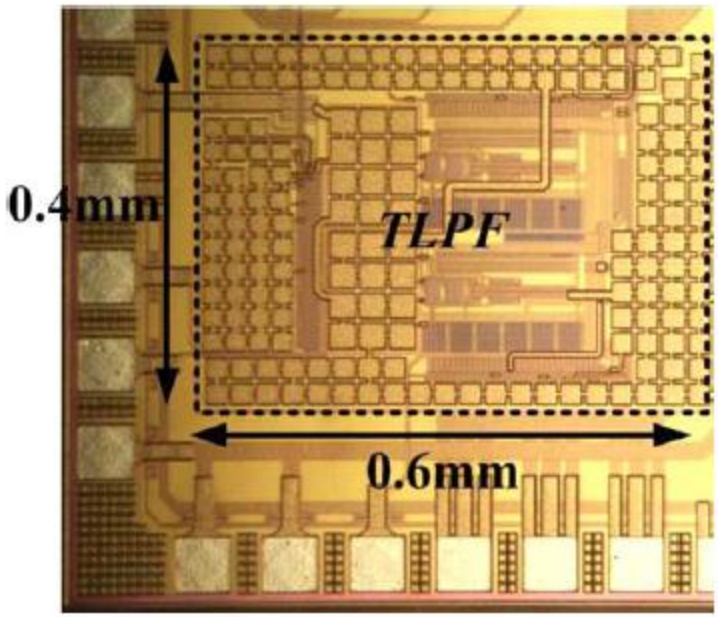
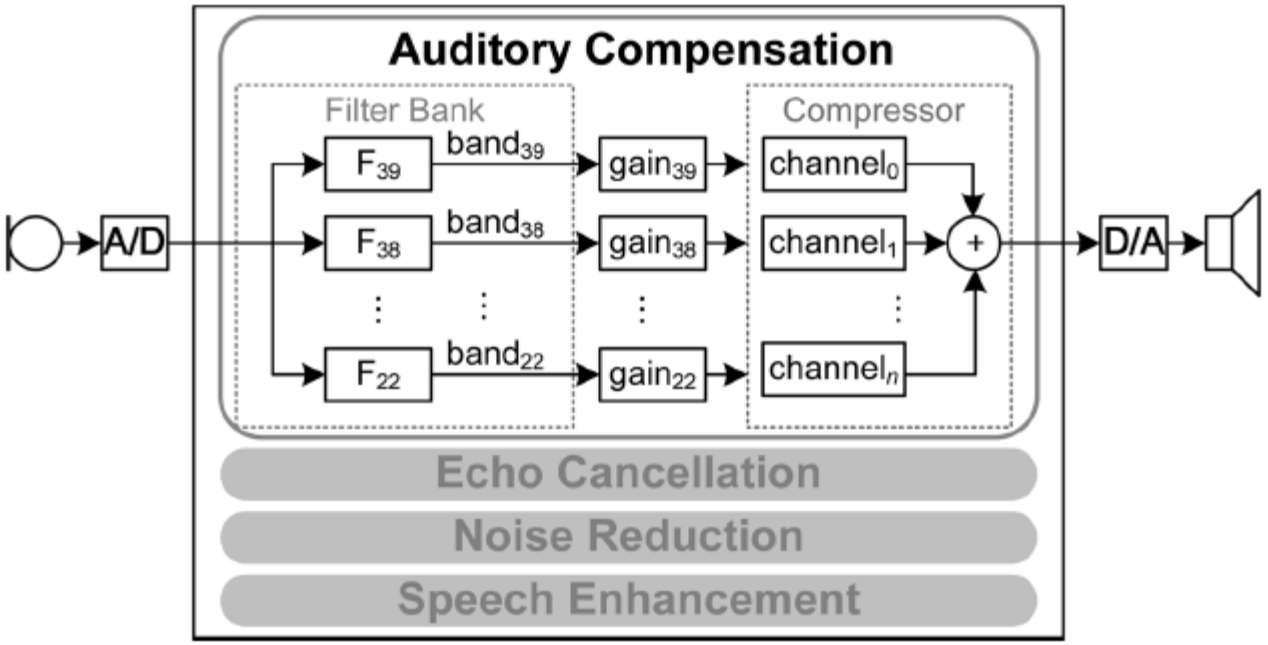


Fig. 7. Microphotograph of the hybrid tracking low-pass filter.

Design and Implementation of Low-Power ANSI S1.11 Filter Bank for Digital Hearing Aids

Yu-Ting Kuo, Tay-Jyi Lin, *Member, IEEE*, Yueh-Tai Li, and Chih-Wei Liu



ck diagram of the advanced hearing aid.

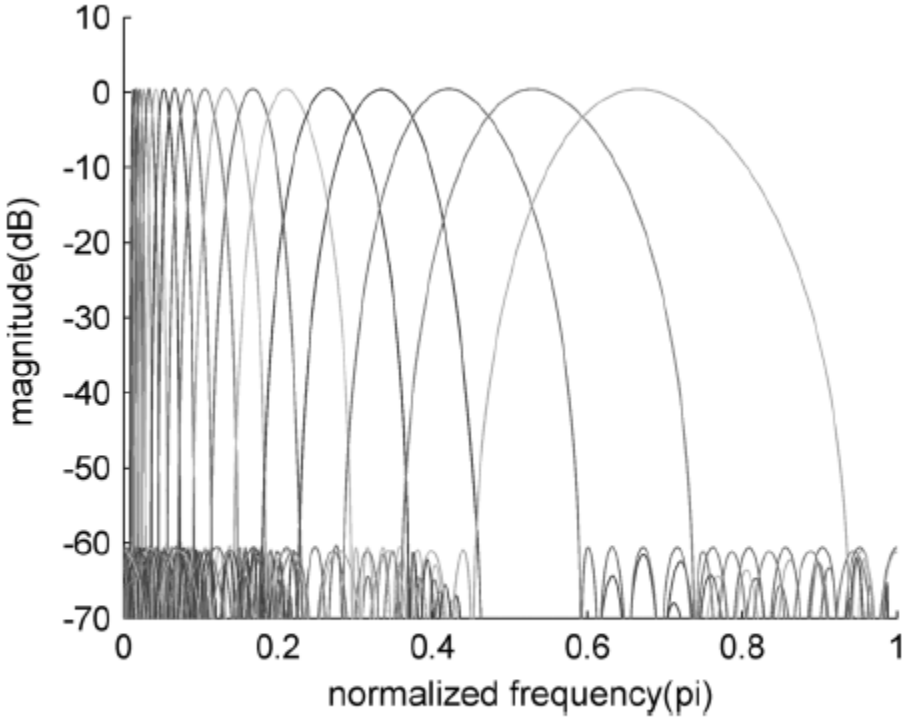
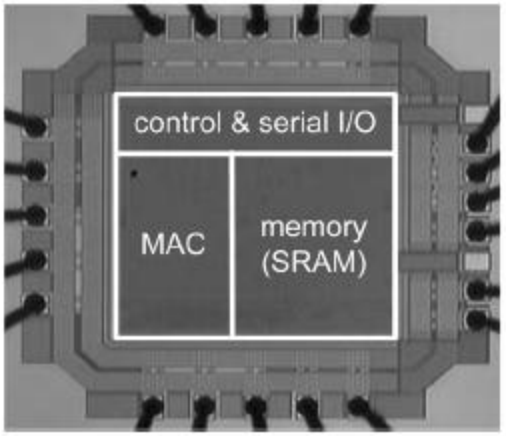


Fig. 14. Magnitude response of the proposed 18-band 1/3-octave filter bank.



Sub-modules	Gate count
MAC	2,847
memory	5,594
system controller	1,010
memory controller	301
serial I/O	1,103

This paper addresses the low-power filter bank design for advanced digital hearing aids. In the literature, the standard ANSI S1.11 1/3-octave filter bank is rarely adopted in hearing aids due to high computation complexity even though it has the advantage of well matching the human hearing characteristics. We develop an efficient multirate filter bank algorithm to implement an 18-band ANSI S1.11 1/3-octave FIR filter bank. The proposed architecture needs only 4% of multiplications and additions of a straightforward parallel FIR filter bank design. We also investigate and apply several lower-power

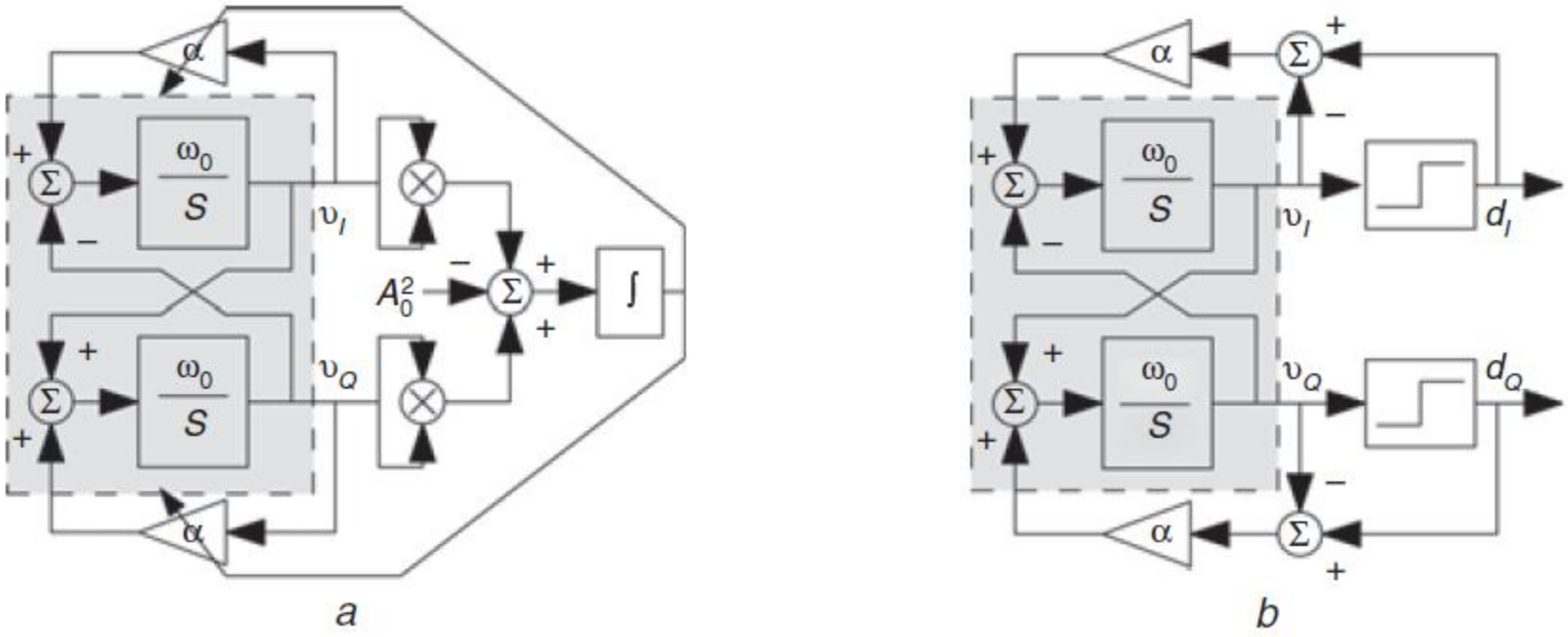
The test chip consumes only 87 μW,

Most existing ANSI S1.11 filter banks are implemented by infinite-impulse response (IIR) filters [8], [9]. Indeed, the researches in psychoacoustics had shown that human ear is not sensitive to phase-distortion. The filter bank with IIR filters may be a good design with low computation complexity; however, FIR filters are still preferred and adopted in [3]–[7], not only for their linear phase but also for the stability and regular structure. The round-off error of FIR filters is easier to analyze and

Simple quadrature oscillator for BIST

J. Raman, P. Rombouts and L. Weyten

ELECTRONICS LETTERS 18th February 2010 Vol. 46 No. 4



Two integrator loop oscillators – different methods for controlling the loss