EE 508 Lecture 41

Some Recent Filter Structures- Part 2
A 20kHz∼16MHz Programmable-Bandwidth 4th Order Active Filter using Gain-boosted Opamp with Negative Resistance in 65 nm CMOS

Jiye Lim, Student Member, IEEE, and Jintae Kim, Senior Member, IEEE

Accepted for TCAS II and pending publication Nov18

The prototype filter is fabricated in 65nm CMOS and occupies 0.098mm². It features three programmable cutoff frequencies of 20kHz, 2MHz, and 16MHz.
Review from Last Lecture

A 28.8-MHz 23-dBm-IIP3 3.2-mW Sallen-Key Fourth-Order Filter With Out-of-Band Zeros Cancellation Marcello De Matteis, Federica Resta, Alessandra Pipino, Stefano D’Amico, and Andrea Baschirotto

TCAS II Dec 16

Fig. 1. SK single-ended generic scheme, with auxiliary path.

The total area occupancy is 0.12 mm²

3.2-mW power consumption

0.18μm process
A 4th-Order Active-Gm-RC Reconfigurable (UMTS/WLAN) Filter  Stefano D’Amico, Vito Giannini, and Andrea Baschirotto

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 7, JULY 2006

\[
V_{IN}G_1 + V_{OUT}G_2 = V_x (G_1 + G_2 + sC)
\]

\[
V_{OUT} = V_x \frac{-A_0}{1 + \tau s}
\]

\[
\frac{V_{OUT}}{V_{IN}} = \frac{-A_0 G_1}{\tau C}
\]

\[
\frac{V_{OUT}}{V_{IN}} = \frac{G_1 + G_2 (1 + A_0)}{\tau C}
\]

Realizes 4\textsuperscript{th}-order filter

C1 and CC tunable,
R1 and R2 switchable

Operates in 2MHz and 20MHz ranges
A 63-dB DR 22.5-MHz 21.5-dBm IIP3 Fourth-Order FLFB Analog Filter
Marcello De Matteis, Alessandra Pipino, Federica Resta, Alessandro Pezzotta, Stefano D’Amico, and Andrea Baschirotto

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 7, JULY 2017

Follow the Leader Feedback (a slight variant on the MLF approach)

Cell 3 Realized with Gm-RC stage of previous slide
A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications

Sheng-Yu Peng, Member, IEEE, Yu-Hsien Lee, Tzu-Yun Wang, Student Member, IEEE, Hui-Chun Huang, Min-Rui Lai, Chiang-Hsi Lee, and Li-Han Liu

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 65, NO. 2, FEBRUARY 2018
Recall the basic two-integrator loop

\[ V_{01} sC_1 = G_x V_{01} + g_{m1} V_{IN} + g_{m4} V_{02} \]
\[ V_{02} sC_2 = g_{m3} V_{01} \]

\[
\begin{align*}
\frac{V_{01}}{V_{IN}} &= \frac{s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_x}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}} \\
\frac{V_{02}}{V_{IN}} &= \frac{\frac{g_{m3} g_{m1}}{C_1 C_2}}{s^2 + s \frac{g_x}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}}
\end{align*}
\]

\[
\begin{align*}
R_X &= \frac{1}{g_{m2}} \\
\frac{V_{01}}{V_{IN}} &= \frac{s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}} \\
\frac{V_{02}}{V_{IN}} &= \frac{\frac{g_{m3} g_{m1}}{C_1 C_2}}{s^2 + s \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}}
\end{align*}
\]
This is a fully-differential implementation of the standard two-integrator loop.

- MUX selects either LP or BP output.

\[
\begin{align*}
\frac{V_{01}}{V_{IN}} &= \frac{s^2 + s \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}}{s^2 + \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}} \\
\frac{V_{02}}{V_{IN}} &= \frac{s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}}
\end{align*}
\]
• This is a fully-differential implementation of the standard two-integrator loop
• MUX selects either LP or BP output

\[
\frac{V_{01}}{V_{IN}} = \frac{s g_{m1}}{C_1} \frac{1}{\frac{1}{s^2} + s \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}}
\]

\[
\frac{V_{02}}{V_{IN}} = \frac{g_{m3} g_{m1}}{C_1 C_2} \frac{1}{\frac{1}{s^2} + s \frac{g_{m2}}{C_1} + \frac{g_{m3} g_{m4}}{C_1 C_2}}
\]

OTAs operate in weak inversion
Adjust \(\omega_0\) by changing tail currents – claim in excess of 5 decades of adjustment
Target 2Hz to 20KHz though claim can go much lower (claim to 10mHz range) and higher
Bias current adjusted by changing charge on floating gate transistor
Each biquad requires 0.12mm\(^2\) of die area in 350nm process
Linearized OTA

Used computer iteration to size devices in OTA
Good linearity and low power dissipation claimed
A 28nm-CMOS 100MHz 1mW 12dBm-IIP3 4th-order Flipped-Source-Follower Analog Filter

F. Fary1, M. De Matteis1, T. Vergine1,2 and A. Baschirotto1

ESSCIRC 2018

Flipped-Source-Follower NMOS Biquadratic Cell

<table>
<thead>
<tr>
<th>Transfer Function</th>
<th>4th-Order Low-Pass</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc-Gain</td>
<td>0dB</td>
</tr>
<tr>
<td>Poles Frequency</td>
<td>1.306</td>
</tr>
<tr>
<td>Cell A Q Factor</td>
<td>1.8 mA/V</td>
</tr>
<tr>
<td>Cell B Q Factor</td>
<td>4.8 pF</td>
</tr>
<tr>
<td>Cell A - C1a</td>
<td>1.75 pF</td>
</tr>
<tr>
<td>Cell B - C1b</td>
<td>1.99 pF</td>
</tr>
</tbody>
</table>

A=0.026mm² for 4th order BW filter in 28nm process P approx. 1mW
\[
V_{OUT} (sC_1 + sC_2) + g_{m2} V_{GS2} - g_{m1} V_{GS1} = sC_1 V_{GS2} \\
V_{IN} = V_{GS1} + V_{OUT} \\
V_{GS2} sC_1 + g_{m1} V_{GS1} = V_{OUT} sC_1
\]

\[
\frac{V_{OUT}}{V_{IN}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1} g_{m2}}
\]

\[
\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}
\]

\[
Q = \sqrt{\frac{g_{m1} C_2}{g_{\partial m2} C_1}}
\]
End of Lecture 41