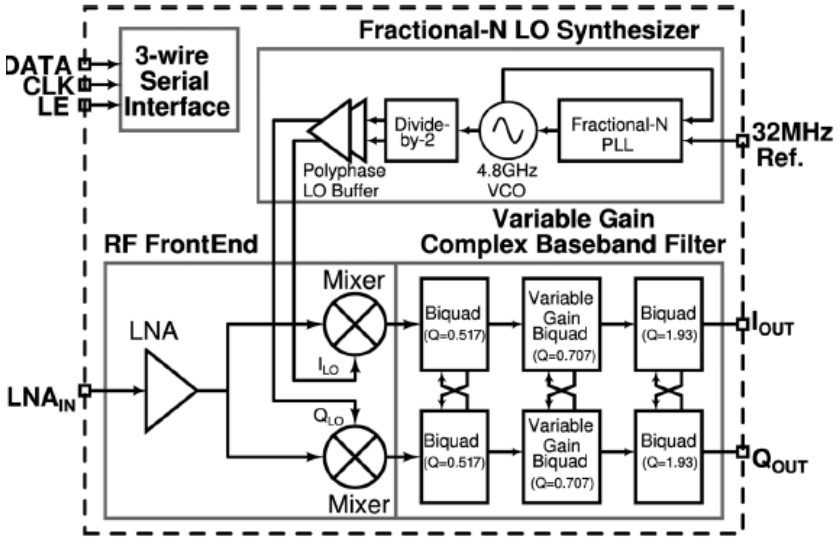
EE 508
Lecture 42

What filter architectures are really being used today?

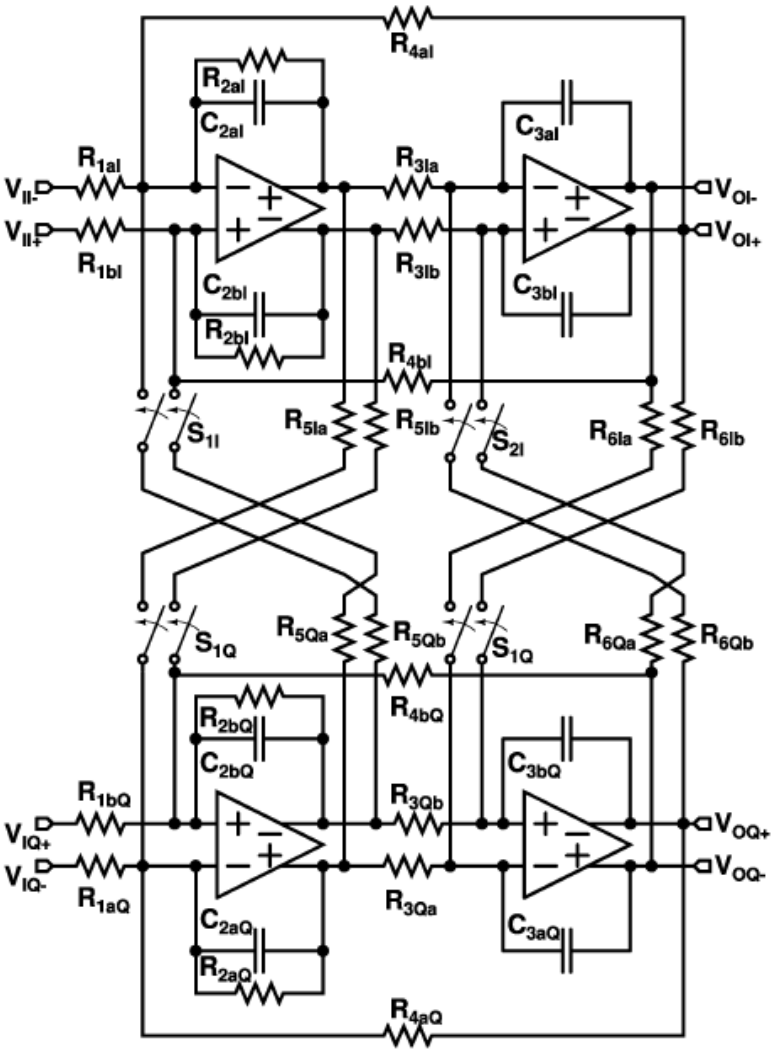
A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications

Ajay Balankutty, *Student Member, IEEE*, Shih-An Yu, *Student Member, IEEE*, Yiping Feng, *Student Member, IEEE*, and Peter R. Kinget, *Senior Member, IEEE*



filter is only 2. To reduce the number of OTAs required for implementing the filter, a lower-order filter transfer function would be preferred. However, biquad-based filters have the drawback that the filter characteristics are more easily affected by parasitics and OTA non-idealities and this sensitivity of the filter characteristics typically is a function of the Q of the filter poles [24]. To make the biquad more tolerant to parasitics and OTA non-idealities, a Tow–Thomas implementation for the biquad is used [25]. To further reduce the sensitivity to parasitics, low Q biquads are preferred. The 6th-order Butterworth filter is chosen for the channel select filter and is implemented as a cascade of three biquads with pole Qs of 0.515, 0.707 and 1.93. The ordering of the biquads has a significant impact on the baseband performance and is discussed in the next section. Even though

System requirements appear to not have played a role in defining the filter type


R4aI
R2aI
C2aI
C3aI
R1aI
R3Ia
VII-
VOI-
VII+
VOI+
R1bI
R3Ib
C2bI
C3bI
R2bI
R4bI
S1I
R5Ia
R5Ib
S2I
R6Ia
R6Ib
S1Q
R5Qa
R5Qb
S1Q
R6Qa
R6Qb
R4bQ
R2bQ
C2bQ
C3bQ
R1bQ
R3Qb
VIQ+
VOQ+
VIQ-
VOQ-
R1aQ
R3Qa
C2aQ
C3aQ
R2aQ
R4aQ

(b)

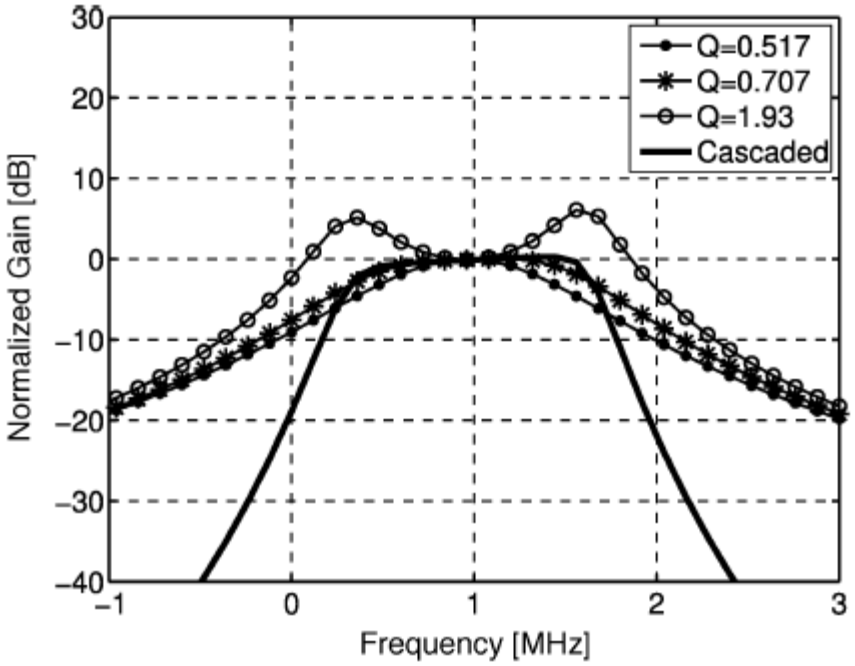
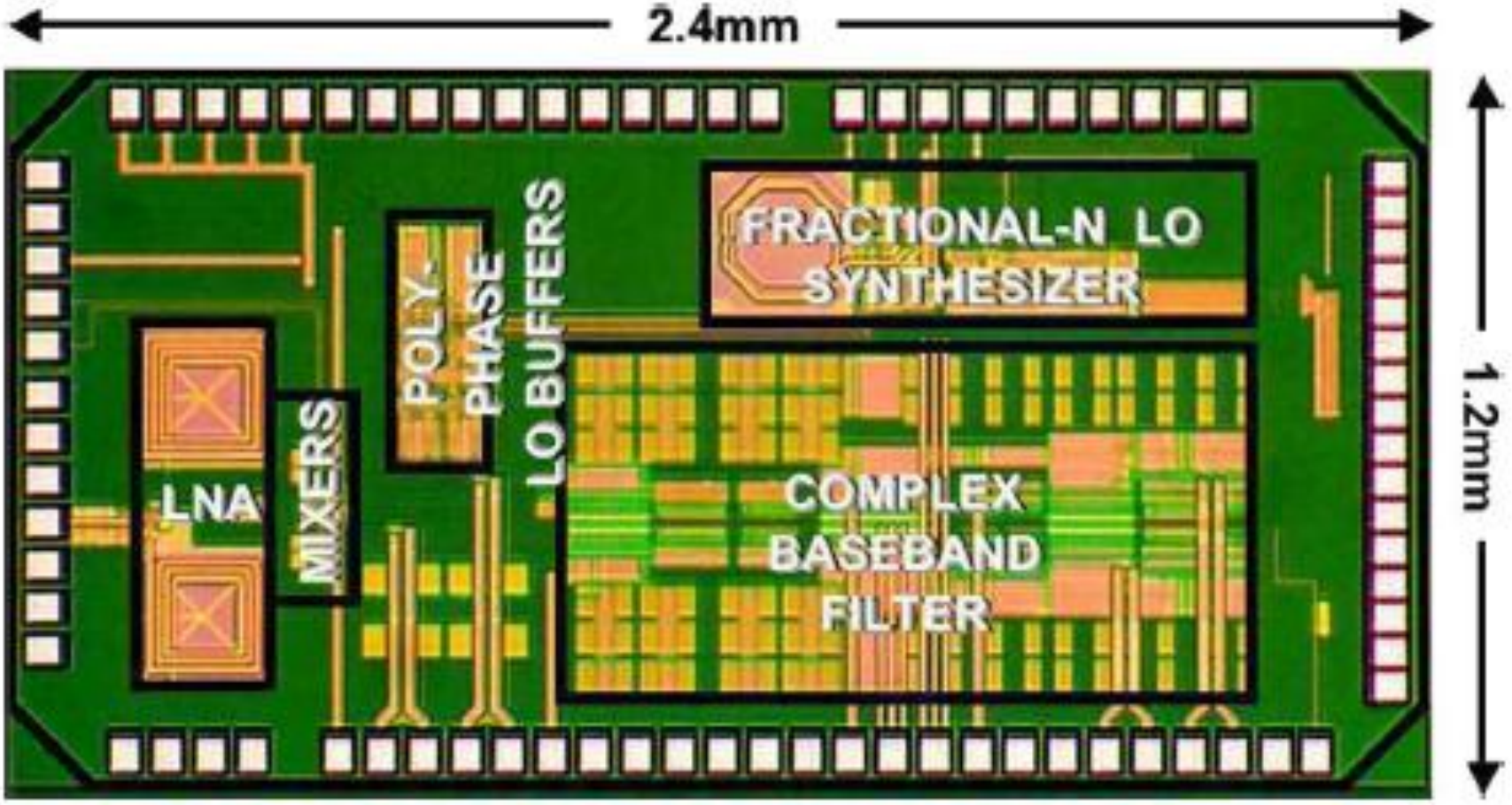


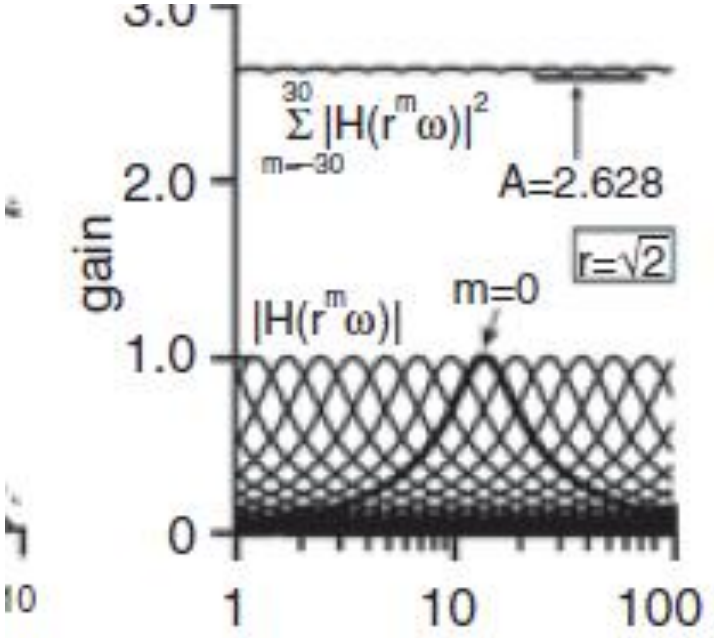
Fig. 5. Simulated frequency response for the different complex biquad stages. The ordering of the biquads is determined by their blocker attenuation. For maximal out-of-channel attenuation as early as possible, the biquads are ordered such that the biquad with $Q = 0.517$ is followed by the biquad with $Q = 0.707$ and biquad with $Q = 1.93$.


2.4mm
1.2mm
FRACTIONAL-N LO SYNTHESIZER
POLY-PHASE
LO BUFFERS
LNA
MIXERS
COMPLEX BASEBAND FILTER

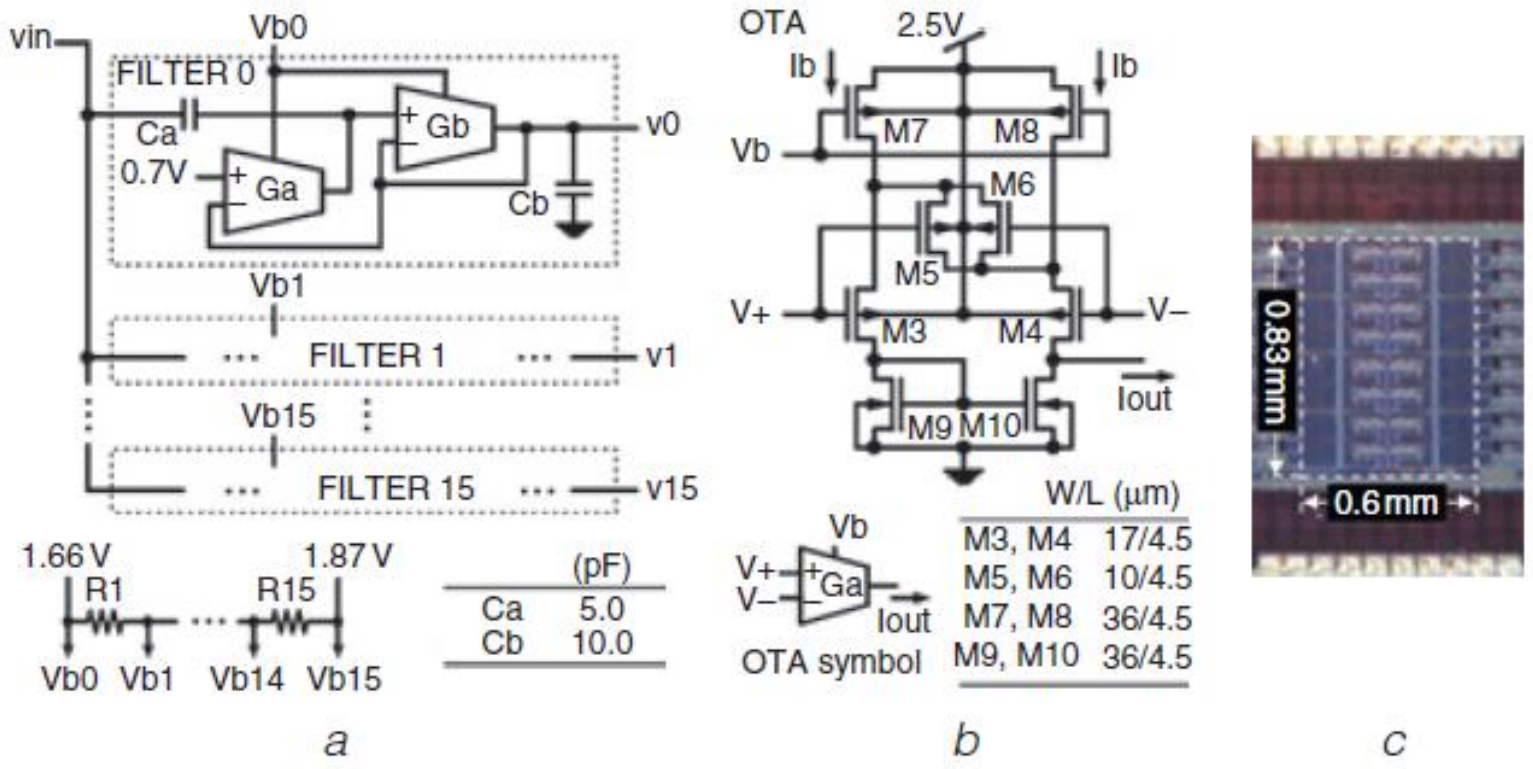
Analogue wavelet transform with single biquad stage per scale

M.A. Gurrola-Navarro and G. Espinosa-Flores-Verdad

ELECTRONICS LETTERS 29th April 2010 Vol. 46 No. 9



C

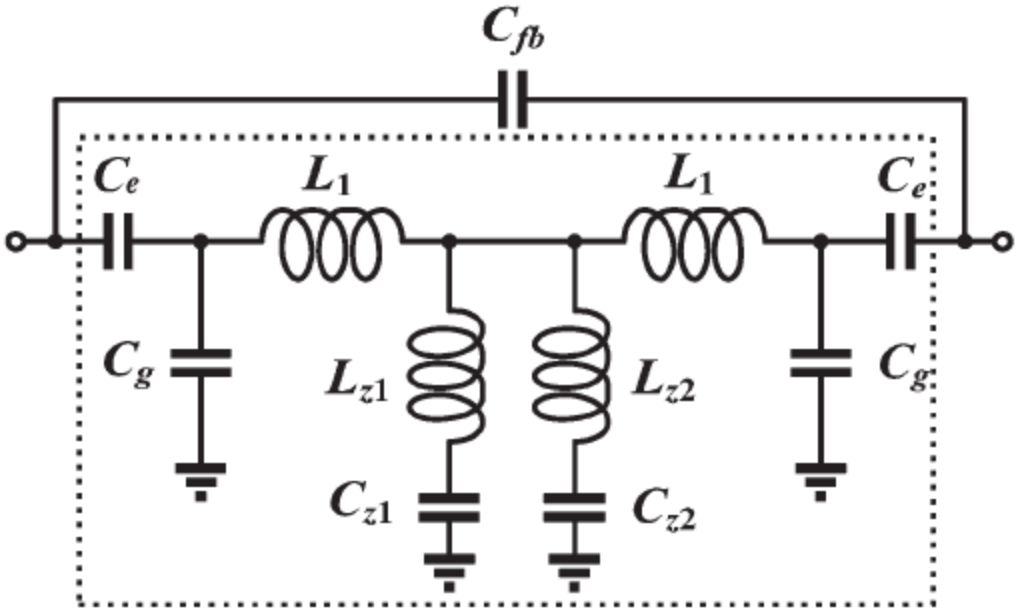


The OTAs are biased in the subthreshold region.

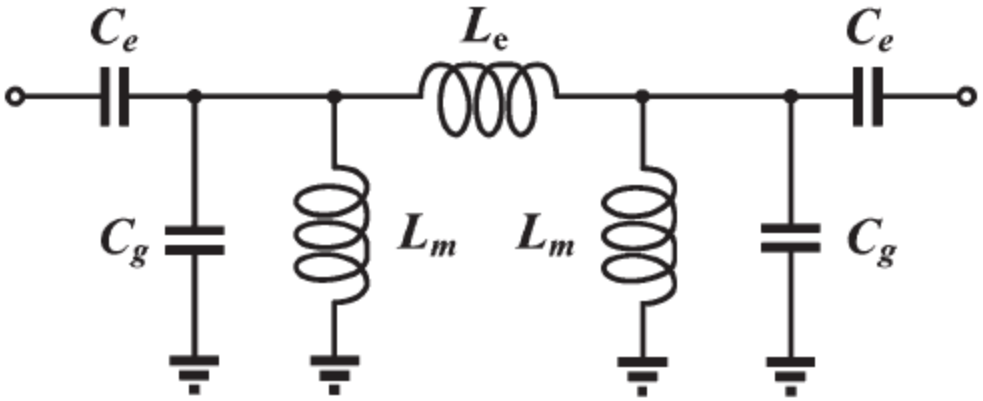
Design of a K-Band Chip Filter With Three Tunable Transmission Zeros Using a Standard 0.13-μm CMOS Technology

Chin-Lung Yang, Shin-Yi Shu, and Yi-Chyun Chiang, *Member, IEEE*

is presented for 24-GHz automotive ultrawideband (UWB) radar systems. The filter combines a second-order asymmetrically compact resonator filter with a source–load coupling mechanism to realize three transmission zeros; two zeros are arranged in the lower stopband, and one zero is located in the upper stopband. To achieve a compact layout size and a low insertion loss, a semi-lumped approach, which is accomplished with mixed utilization of high-impedance coplanar waveguide lines and lumped capacitors, is used to construct the chip filter. A K-band experimental proto-



(a)



(b)

Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures

Pei-Yu Chen, *Student Member, IEEE*, Lan-Da Van, *Member, IEEE*, I-Hung Khoo, *Member, IEEE*, Hari C. Reddy, *Fellow, IEEE*, and Chin-Teng Lin, *Fellow, IEEE*

***Abstract*—This paper presents two-dimensional (2-D) VLSI digital filter structures possessing various symmetries in the filter magnitude response. For this purpose, four Type-1 and four Type-2 power-efficient and cost-effective 2-D magnitude sym-**

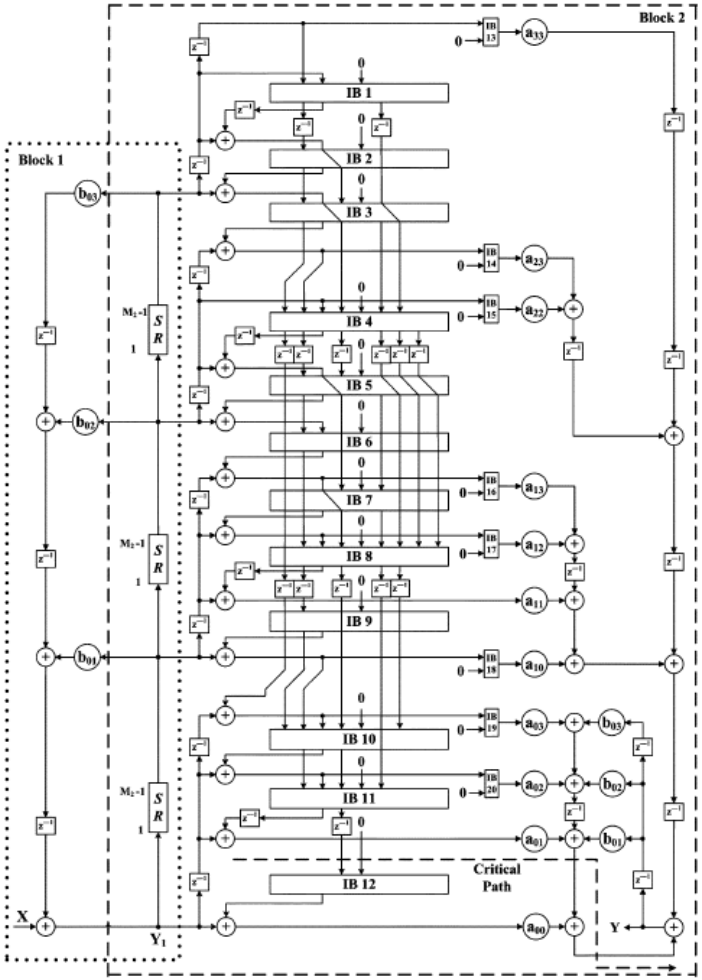


Fig. 11. Proposed multimode 2-D filter architecture with four symmetries for $N = 3$.

area size of 718.95 μm $\times$ 711.05 μm. The corresponding power consumption of the proposed multimode 2-D filter is 29.34 mW on average. In terms of power comparison, the DSM, FRSM,

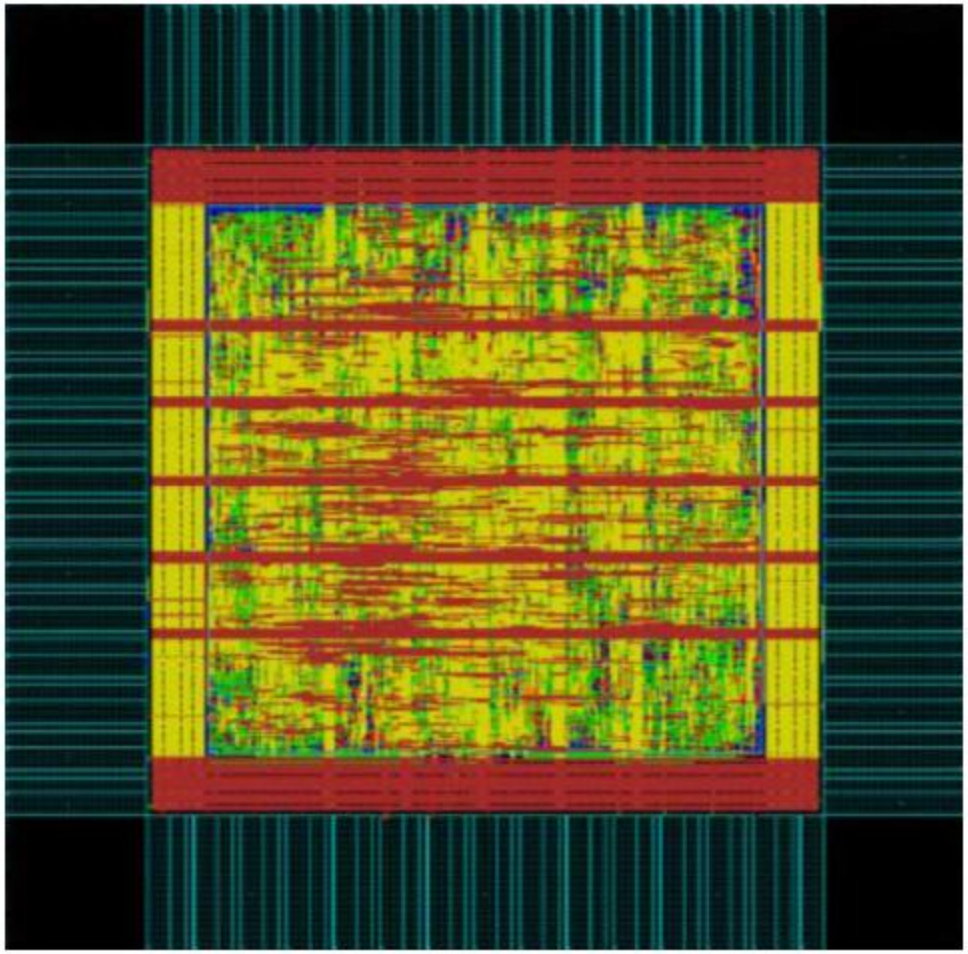


Fig. 18. Layout of the proposed multimode symmetry filter for $N = 3$.

A Subharmonic Receiver in SiGe Technology for 122 GHz Sensor Applications

Klaus Schmalz, Wolfgang Winkler, Johannes Borngräber, Wojciech Debski, Bernd Heinemann, and J. Christoph Scheytt, *Member, IEEE*

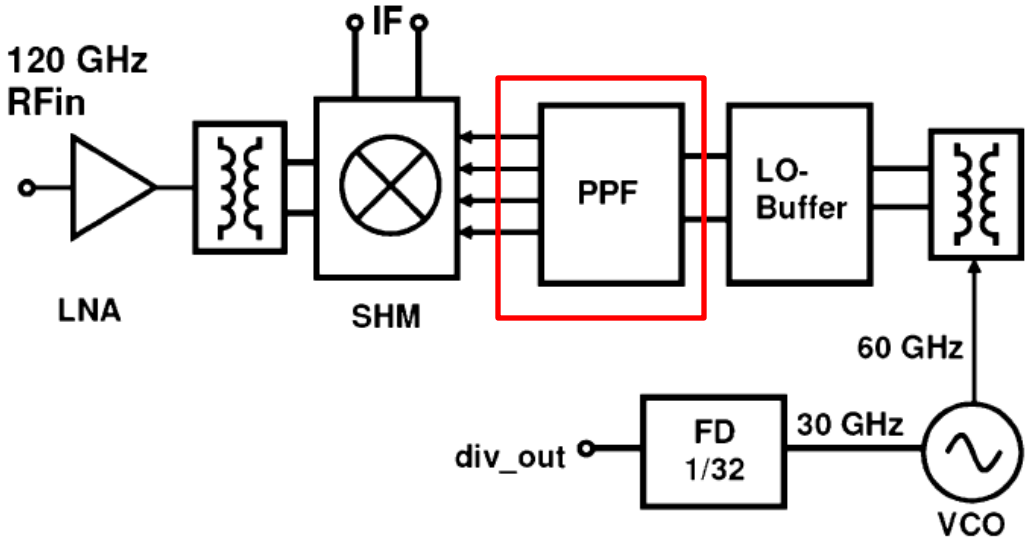


Fig. 1. Topology of the subharmonic receiver.

is fabricated in SiGe:C BiCMOS technology with $f_T/f_{\max}$ of 255 GHz/315 GHz. The receiver was optimized by an

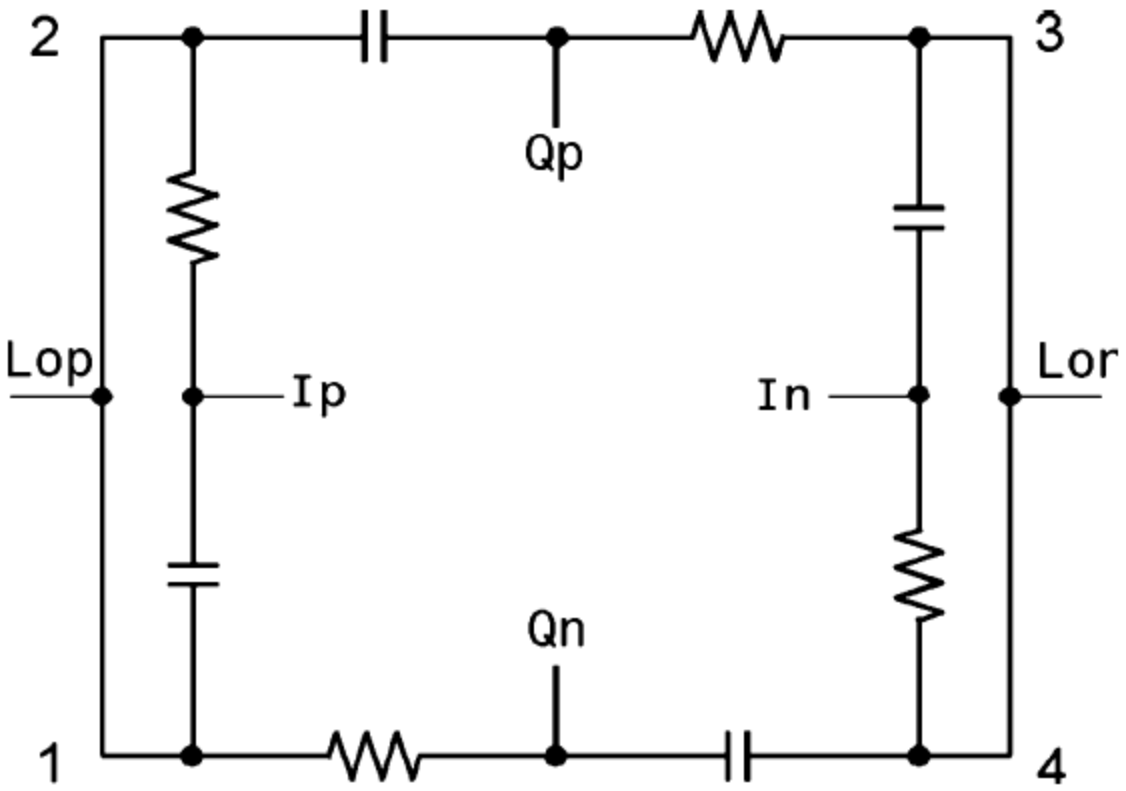


Fig. 4. Schematic of 5 GHz polyphase filter

$$R = 67\ \Omega \text{ and } C = 40 \text{ fF}$$

unsalicided, p-doped gate polysilicon as resistor

MIM capacitors with 1 fF/μm^2.

Low-Power and Widely Tunable Linearized Biquadratic Low-Pass Transconductor-C Filter

Armin Tajalli, *Member, IEEE*, and Yusuf Leblebici, *Fellow, IEEE*

***Abstract*—A sixth-order low-pass transconductor-C filter with a very wide tuning range ($f_c = 100$ Hz to 10 MHz) is presented. The wide tuning range has been achieved without using switchable components or programmable building blocks.**

ı 0.18-μm CMOS technology

the input devices are biased in the subthreshold regime

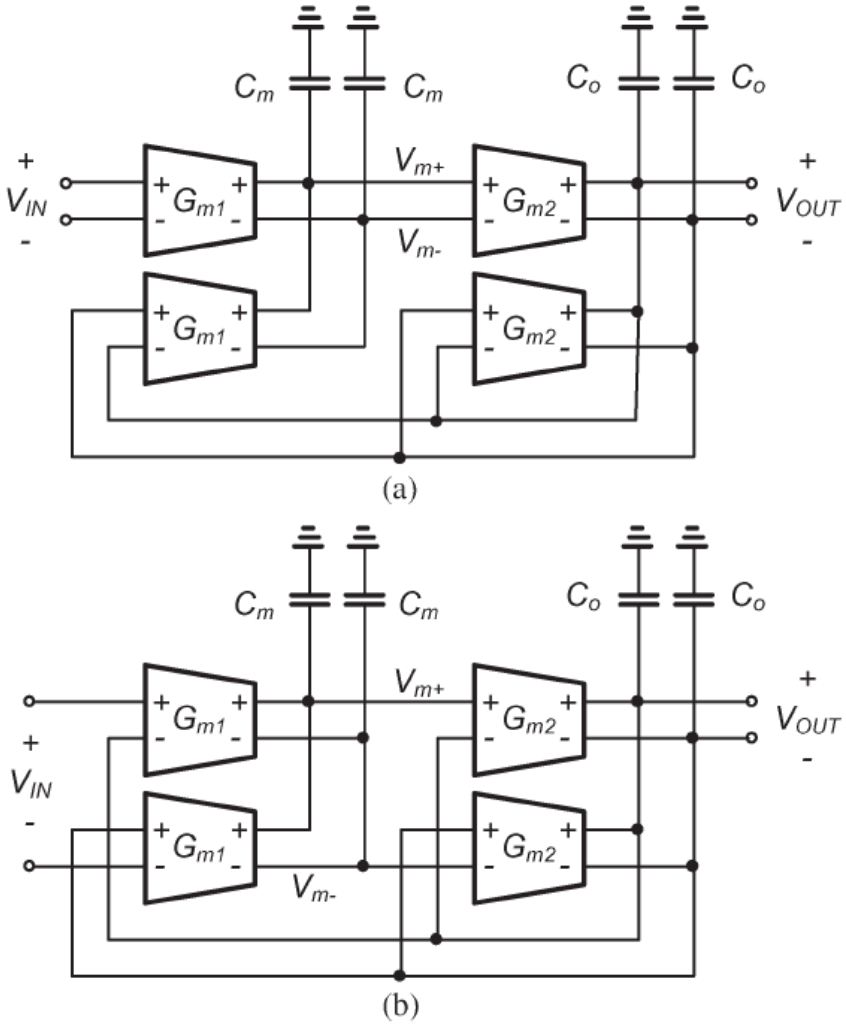


Fig. 2. Biquadratic g_m-C filter. (a) Conventional topology. (b) Modified topology with improved linearity performance.

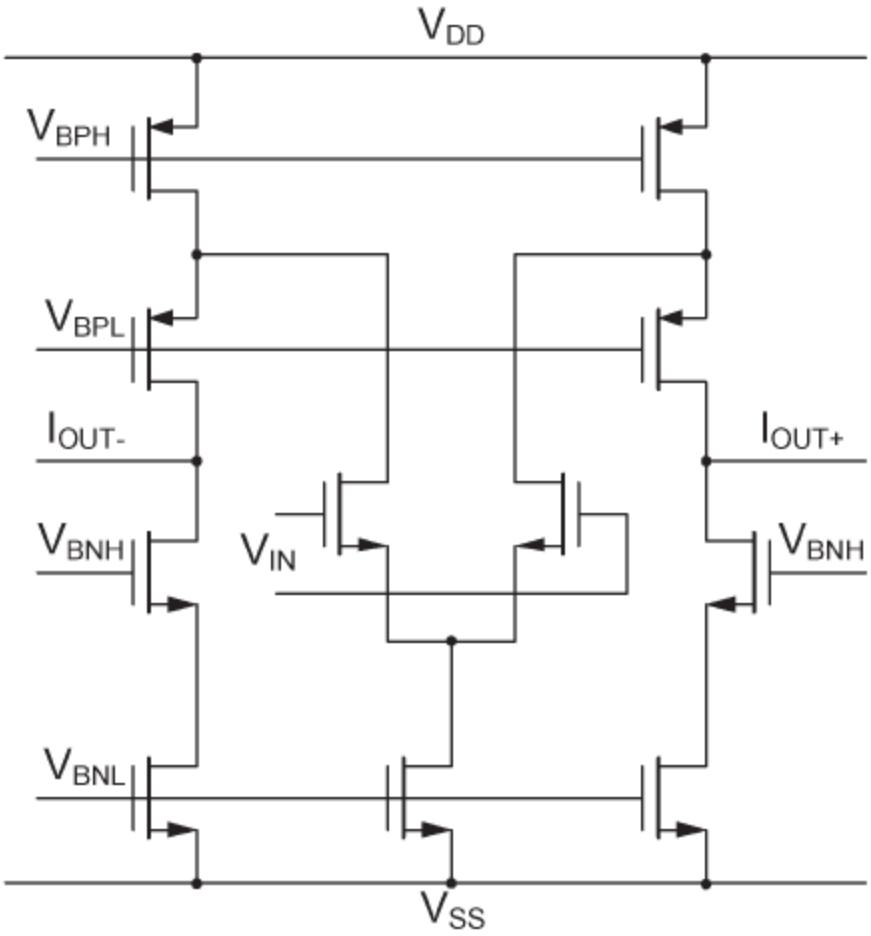
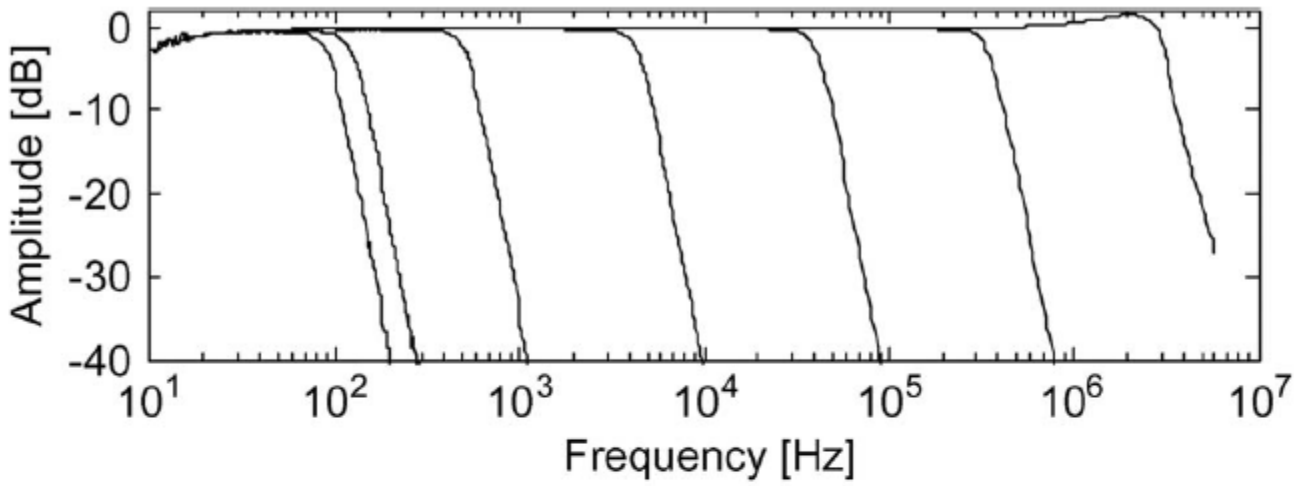
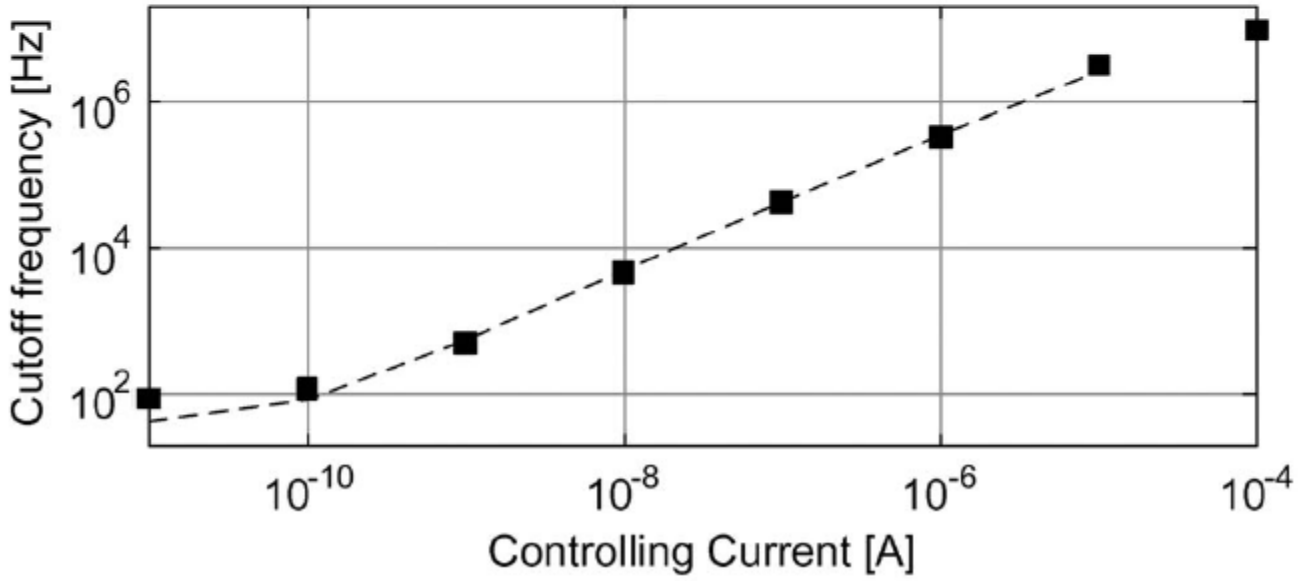


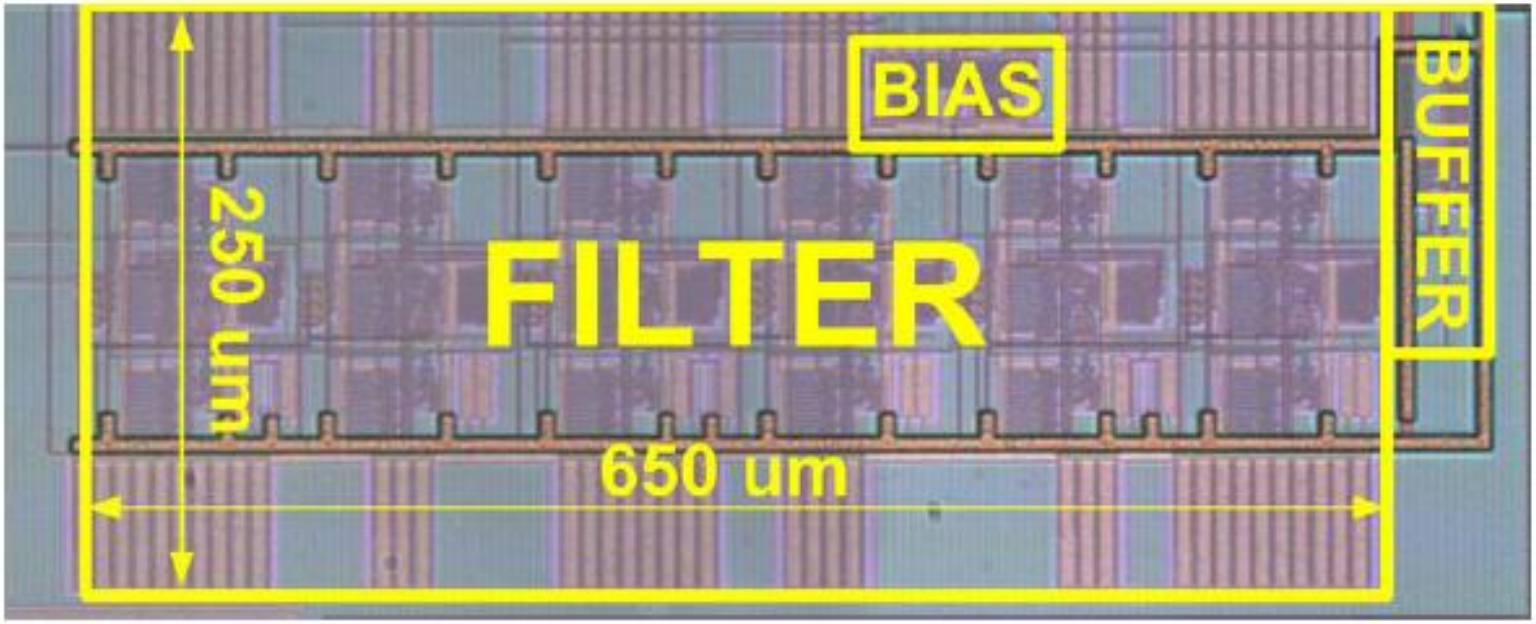
Fig. 4. Schematic of the folded cascode transconductor used to implement the widely tunable filter.


Amplitude [dB]
0
-10
-20
-30
-40
10^1
10^2
10^3
10^4
10^5
10^6
10^7
Frequency [Hz]

(a)


Cutoff frequency [Hz]
10^6
10^4
10^2
10^{-10}
10^{-8}
10^{-6}
10^{-4}
Controlling Current [A]

(b)


BIAS
BUFFER
FILTER
250 um
650 um

CMOS on-chip active RF tracking filter for digital TV tuner ICs

Y. Sun, C.J. Jeong, S.K. Han and S.G. Lee

ELECTRONICS LETTERS 17th March 2011 Vol. 47 No. 6

The fabricated tracking filter based on a 0.13 μm CMOS process shows 48–780 MHz tracking range with 15–60 MHz bandwidth,

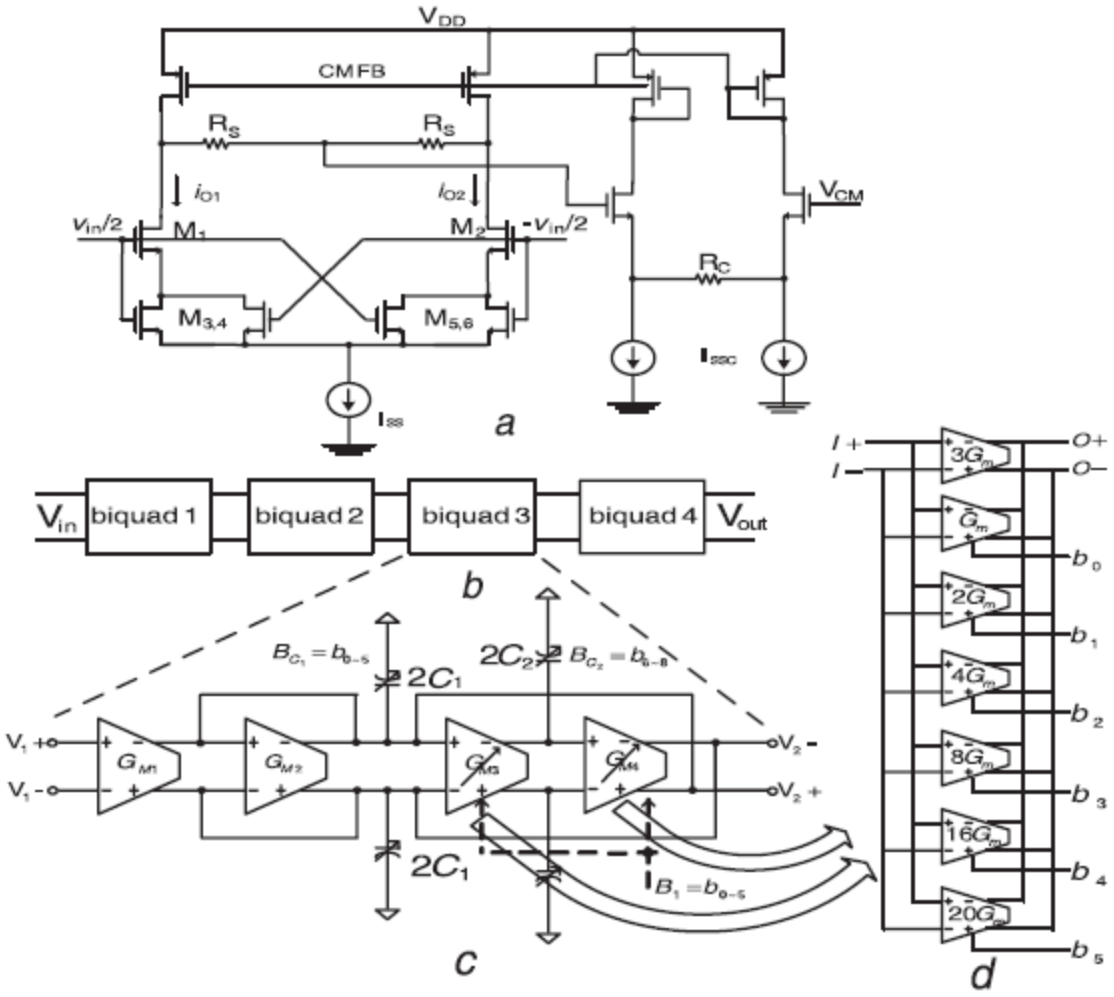


Fig. 1 *Proposed RF tracking filter design*

a Schematic of unit G_m-cell used in proposed RF tracking filter
b RF tracking filter architecture
c Biquad architecture
d G_M-cell in biquad

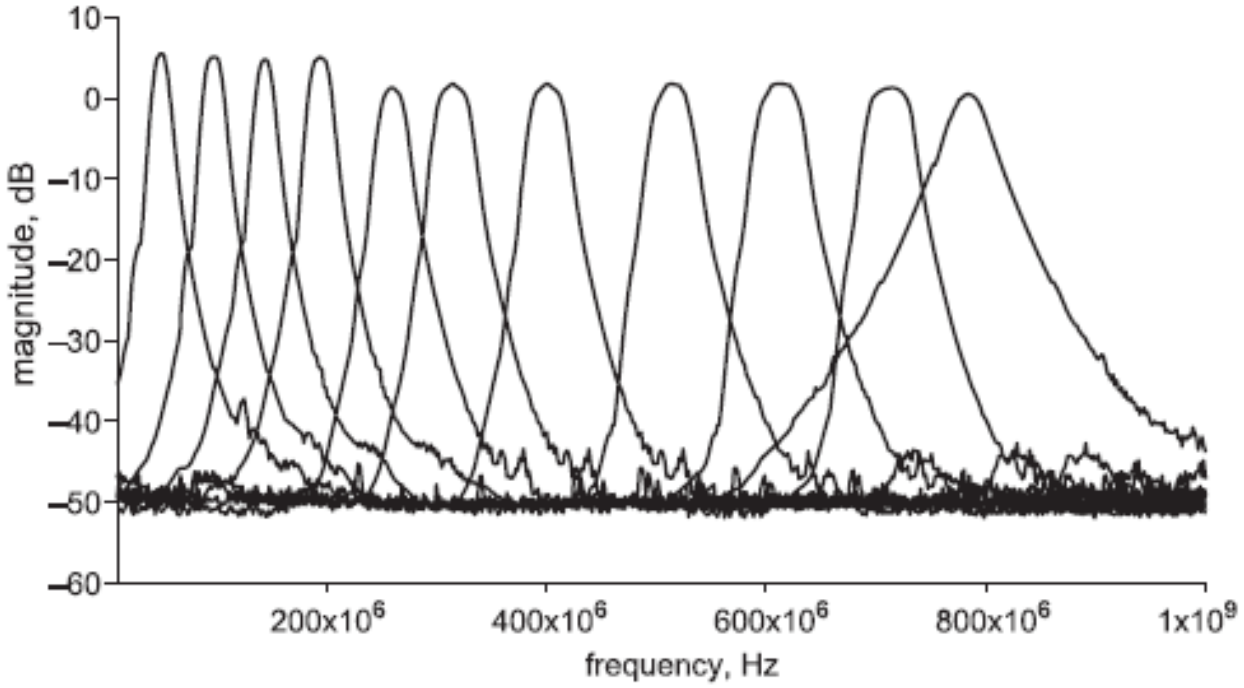


Fig. 2 *Measured frequency tuning and rejection performance*

Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification

Amir Ghaffari, *Student Member; IEEE*, Eric A. M. Klumperink, *Senior Member; IEEE*, Michiel C. M. Soer, *Student Member; IEEE*, and Bram Nauta, *Fellow, IEEE*

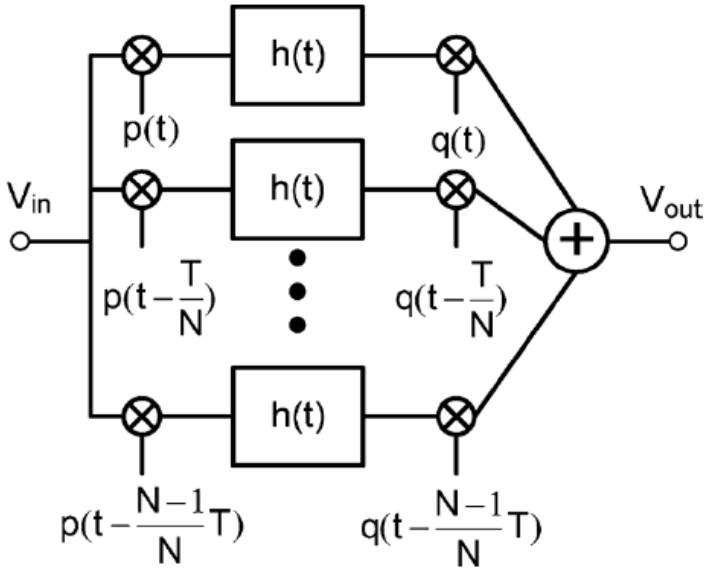


Fig. 1. Architecture of an N-path filter [5] (p and q are the mixing functions and T is the period of the mixing frequency).

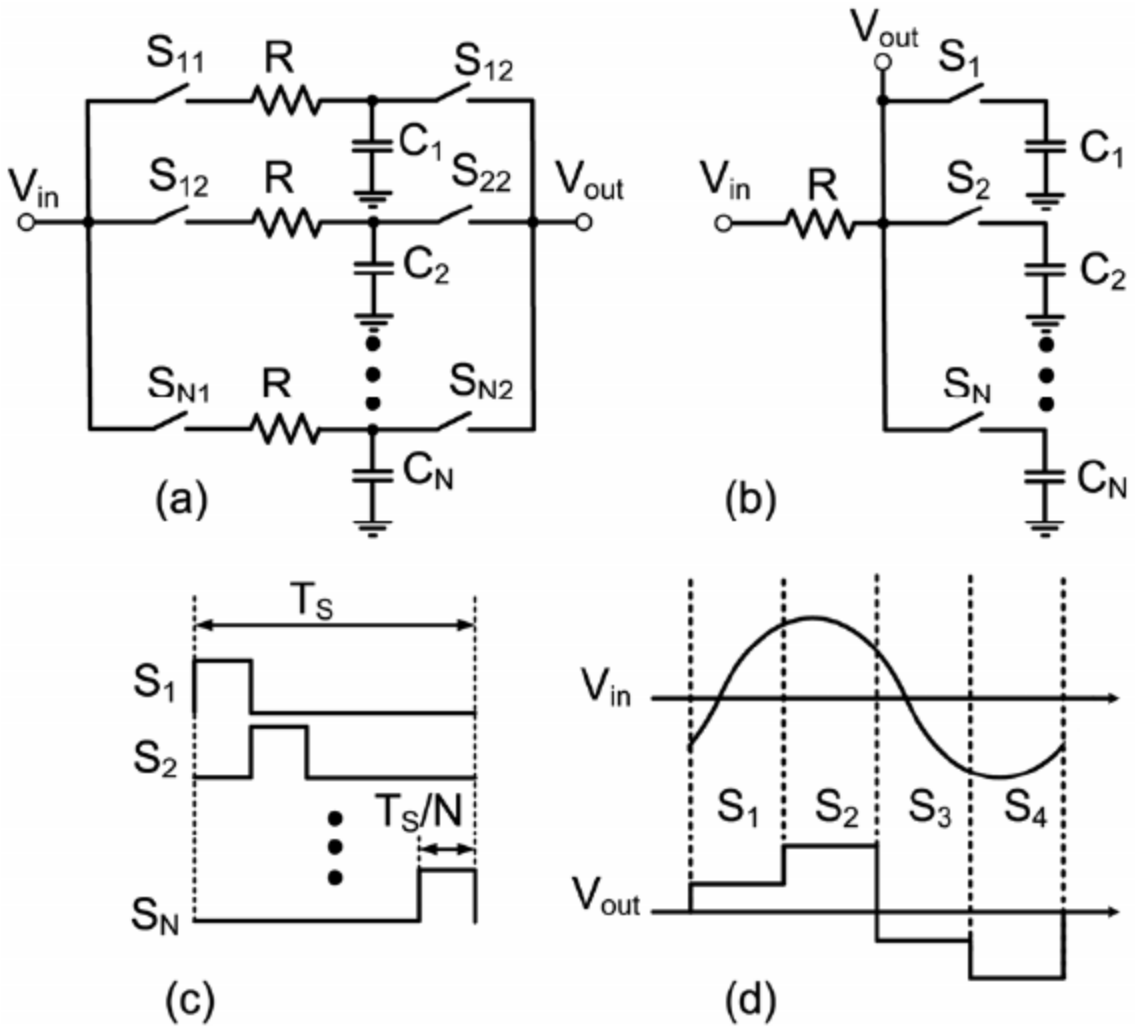
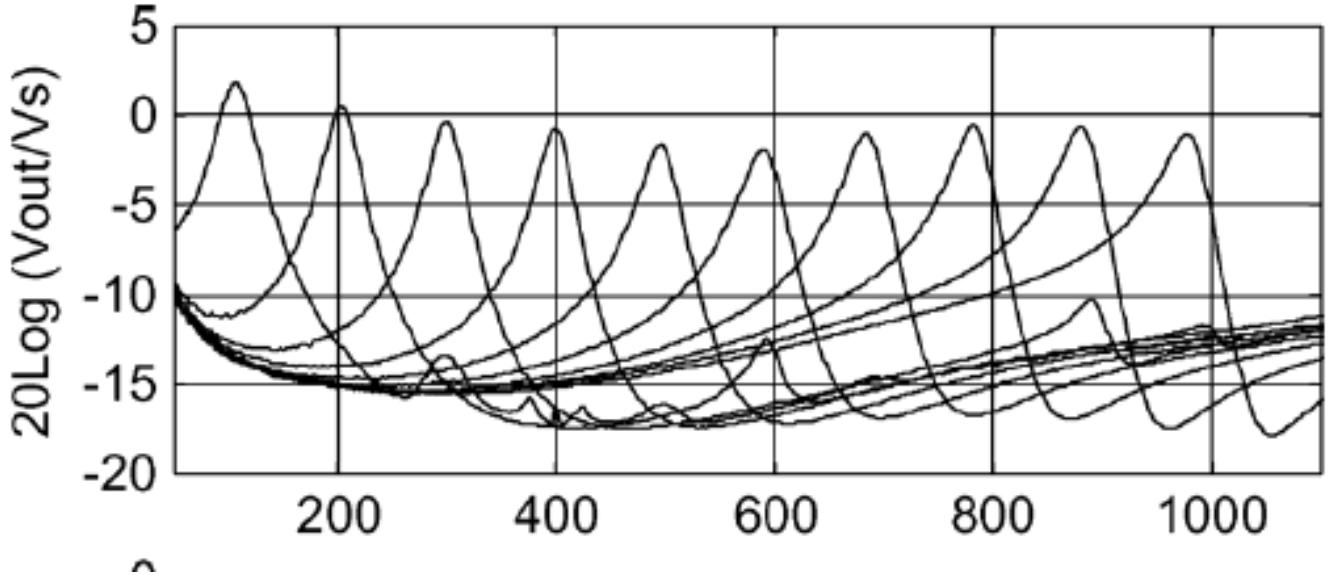


Fig. 2. (a) Switched-RC N-path filter. (b) Single port, single ended N-path filter. (c) Multiphase clocking. (d) Typical (in-band) input and output signal.


20Log (Vout/Vs)
5
0
-5
-10
-15
-20
200
400
600
800
1000

Performance	This Work	[9]	[4]
Process	65nm CMOS	0.35um CMOS	0.18um CMOS
Active Area	$0.07mm^2$	$1.9mm^2$	$0.81mm^2$
Power Consumption	2 to 16mW	63mW	17mW
Frequency Tuning Range	0.1 to 1GHz	240 to 530MHz	2 to 2.06GHz
-3dB Band Width	35MHz	1.75 to 4.6MHz	130MHz
Voltage Gain	-2dB	-2dB	0dB
Quality Factor (Q)	3 to 29	301 to 114	15.4 to 15.8
P_{1dB}	2dBm	-5dBm	-6.6dBm
IIP3	14dBm	NA	2.5dBm
Noise Figure	3-5dB	9dB	15dB

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 58, NO. 7, JULY 2011 1561

A 400 μW Hz-Range Lock-In A/D Frontend Channel for Infrared Spectroscopic Gas Recognition

Stepan Sutula, *Student Member, IEEE*, Carles Ferrer, and Francisco Serra-Graells, *Member, IEEE*

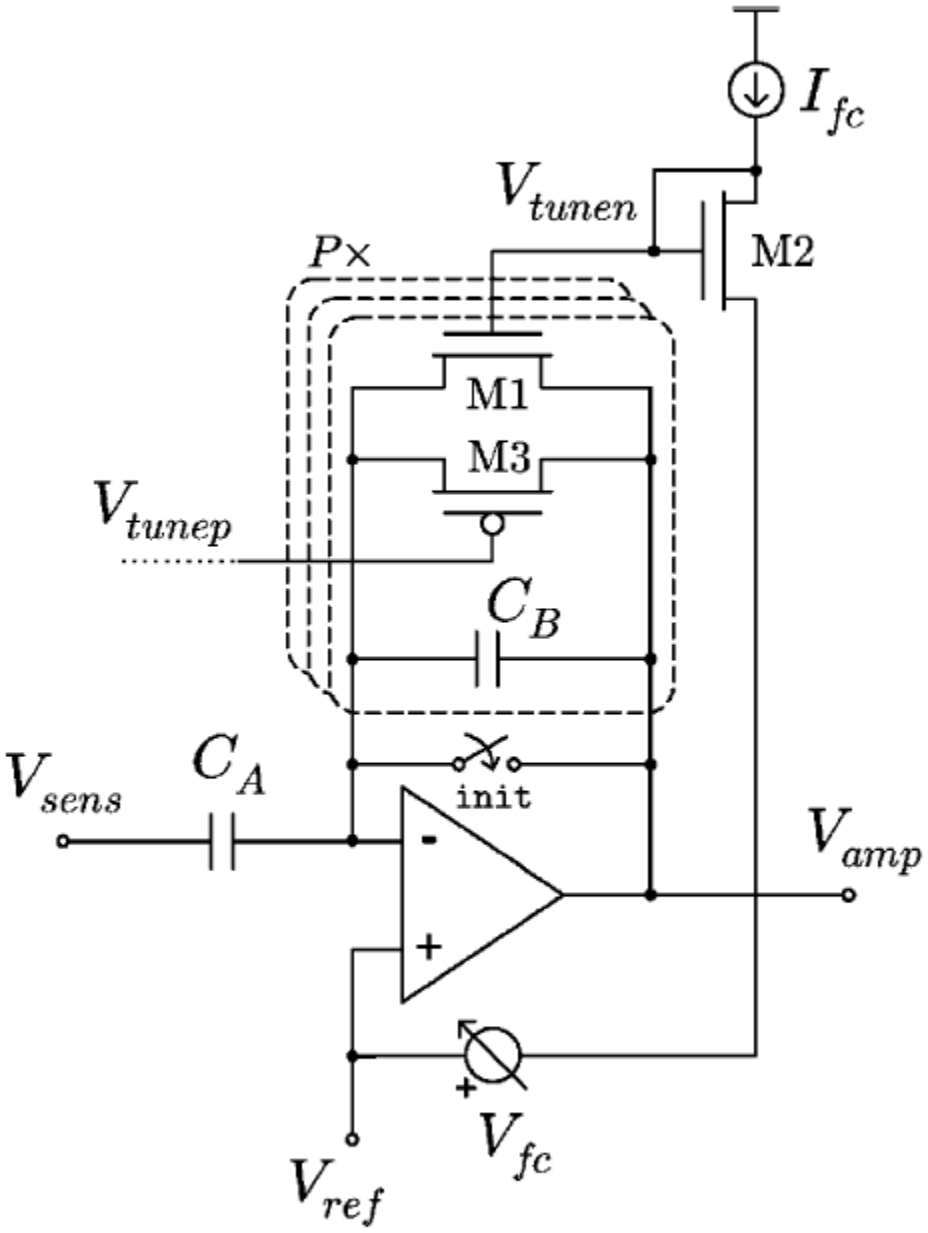


Fig. 3. Proposed sub-Hz programmable MOS-C high-pass preamplifier.

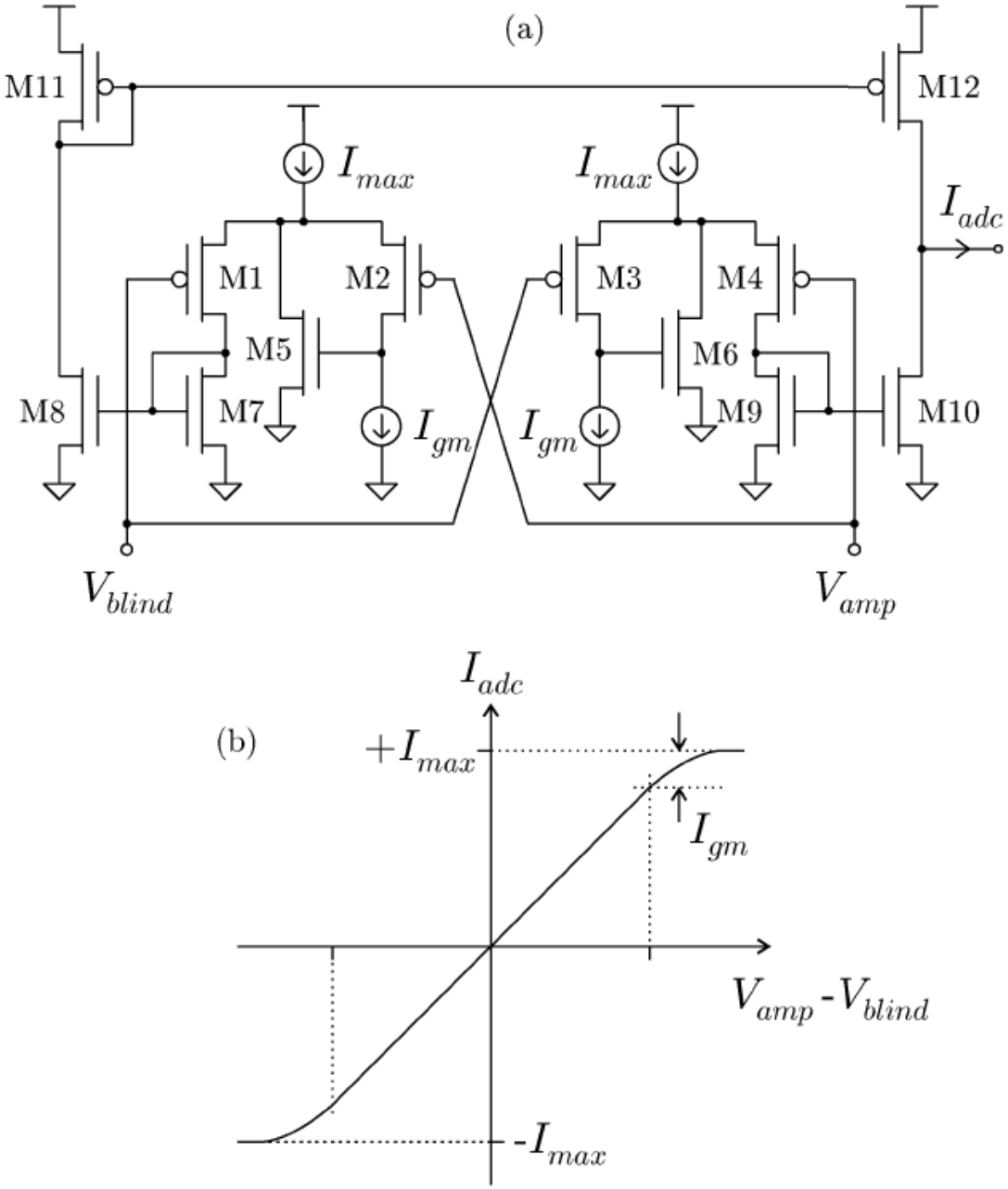
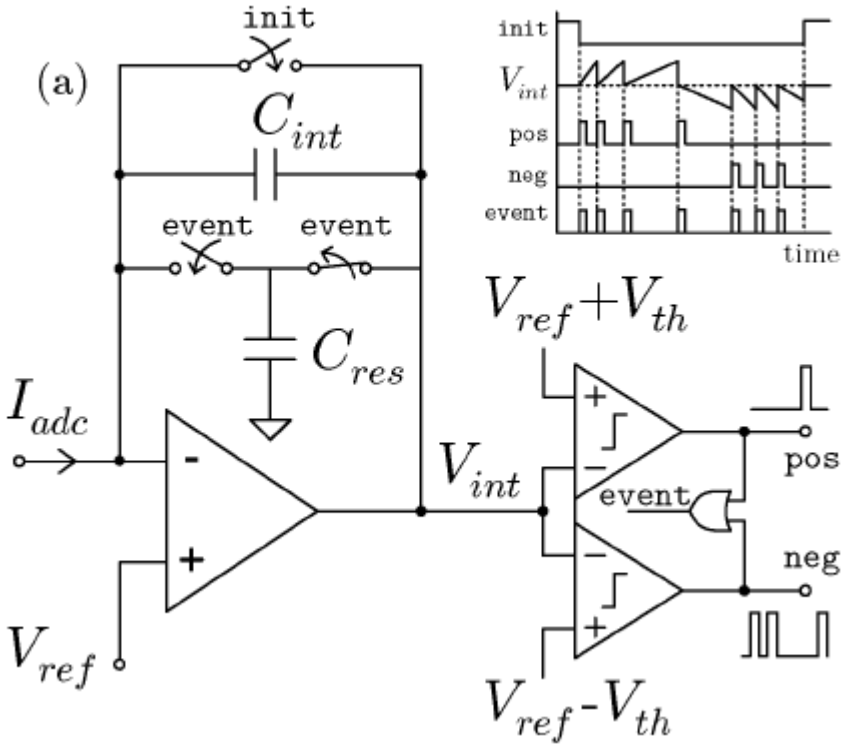
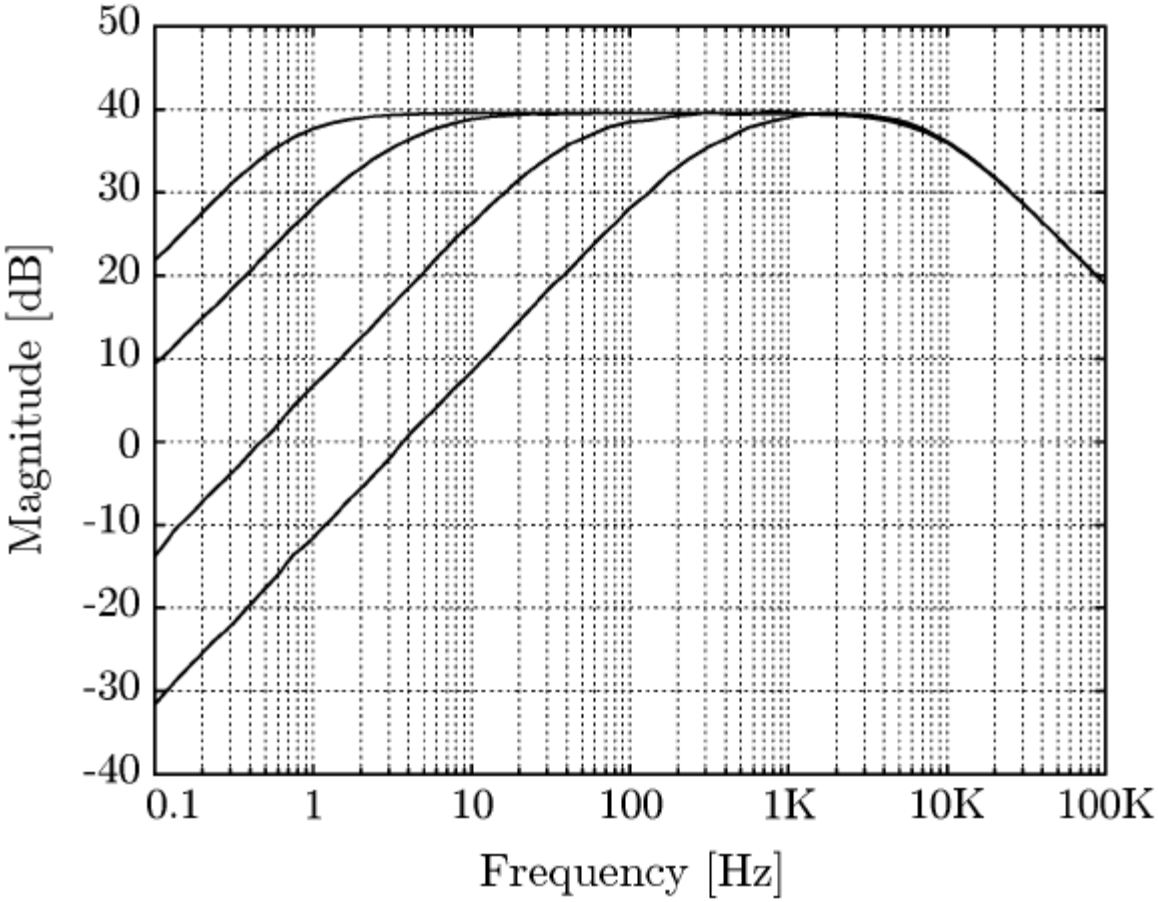


Fig. 6. (a) Proposed linear transconductor and (b) equivalent built-in limiter


(a)
init
C_{int}
event
event
C_{res}
I_{adc}
V_{ref}
V_{int}
$V_{ref}+V_{th}$
$V_{ref}-V_{th}$
event
pos
neg
init
V_{int}
pos
neg
event
time



9. Experimental transfer function of the high-pass preamplifier stage for pendent gain (top) and corner frequency (bottom) digital programming.

An Electronically Fine-Tunable Multi-Input–Single-Output Universal Filter

Indrit Myderrizi, *Member, IEEE*, Shahram Minaei, *Senior Member, IEEE*, and Erkan Yuce, *Member, IEEE*

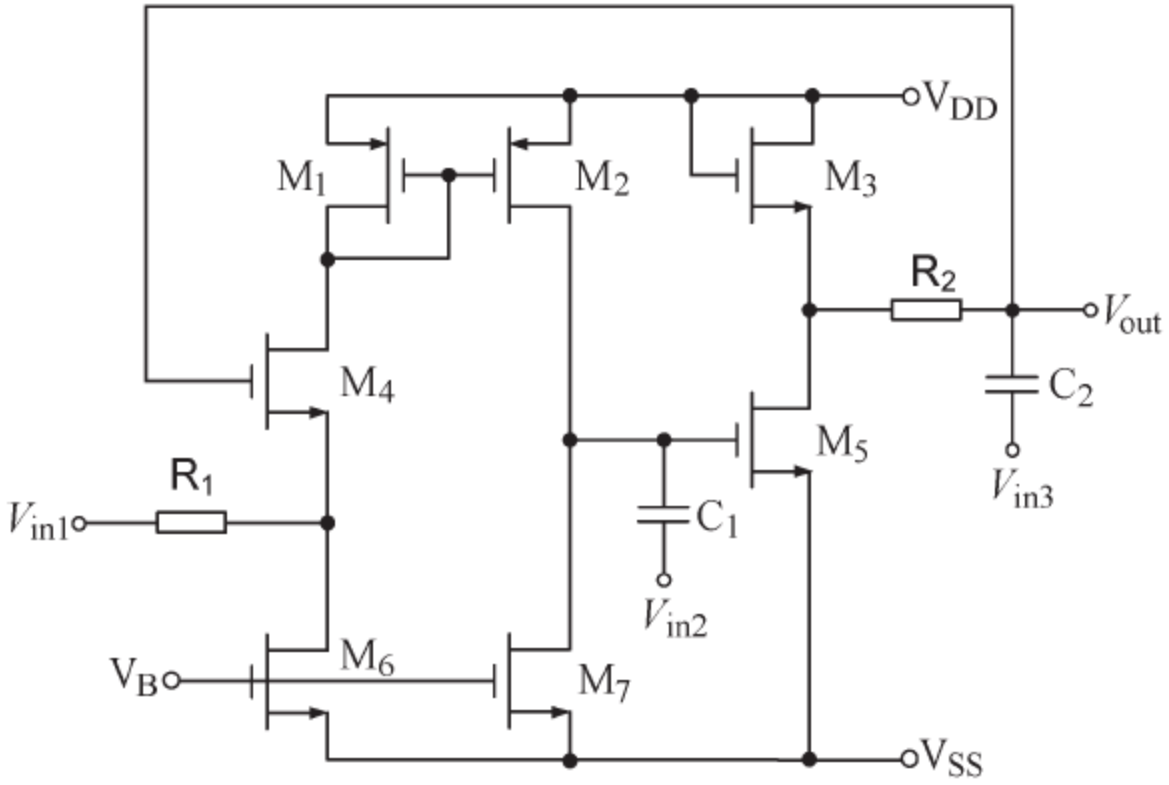


Fig. 1. CMOS realization of the proposed VM MISO universal filter.

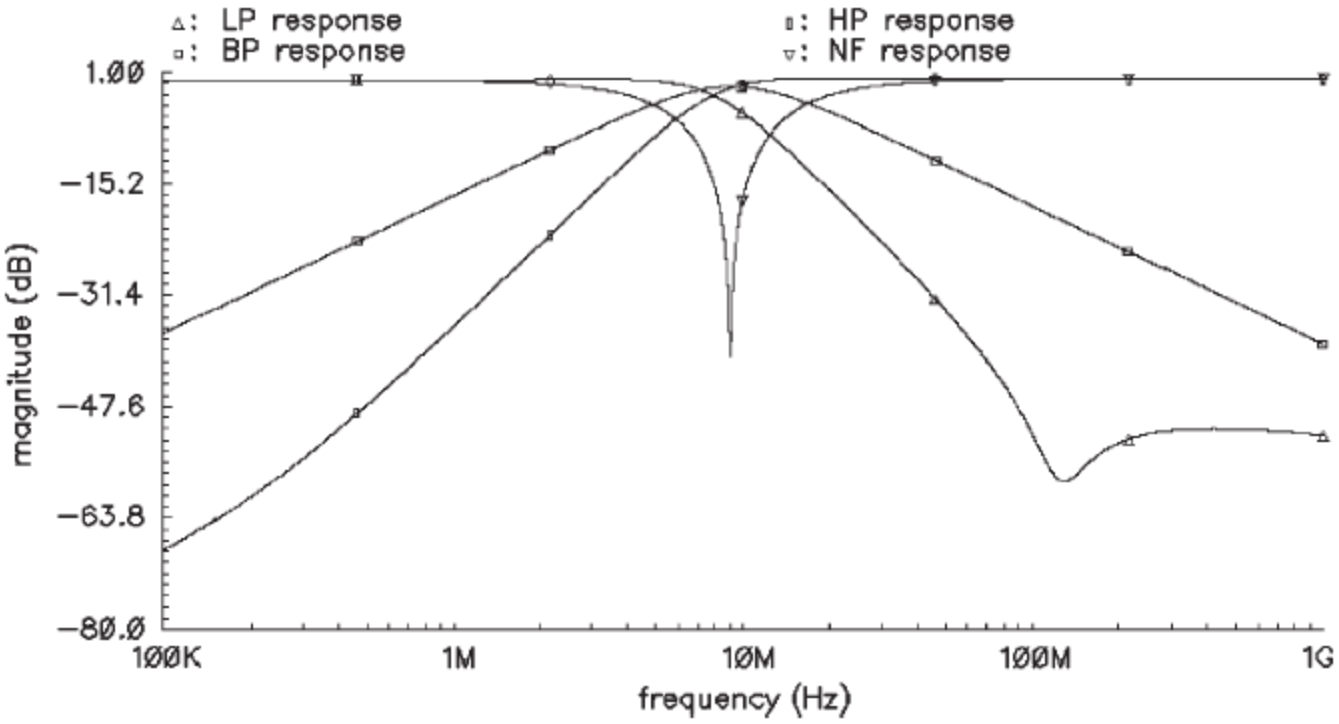


Fig. 3. Magnitude frequency responses of the MISO multifunctional filter.

for a high-Q BP response of the filter. In this case, $Q = 5$, and the component values are selected as $C_1 = 0.457$ pF, $C_2 = 2$ pF, $R_1 = 6.5$ kΩ, and $R_2 = 37.2$ kΩ.

A 16-Channel Low-Noise Programmable System for the Recording of Neural Signals

Carolina Mora López, Dries Braeken, Carmen Bartic, Robert Puers*, Georges Gielen* and Wolfgang Eberle
Imec, Leuven, Belgium

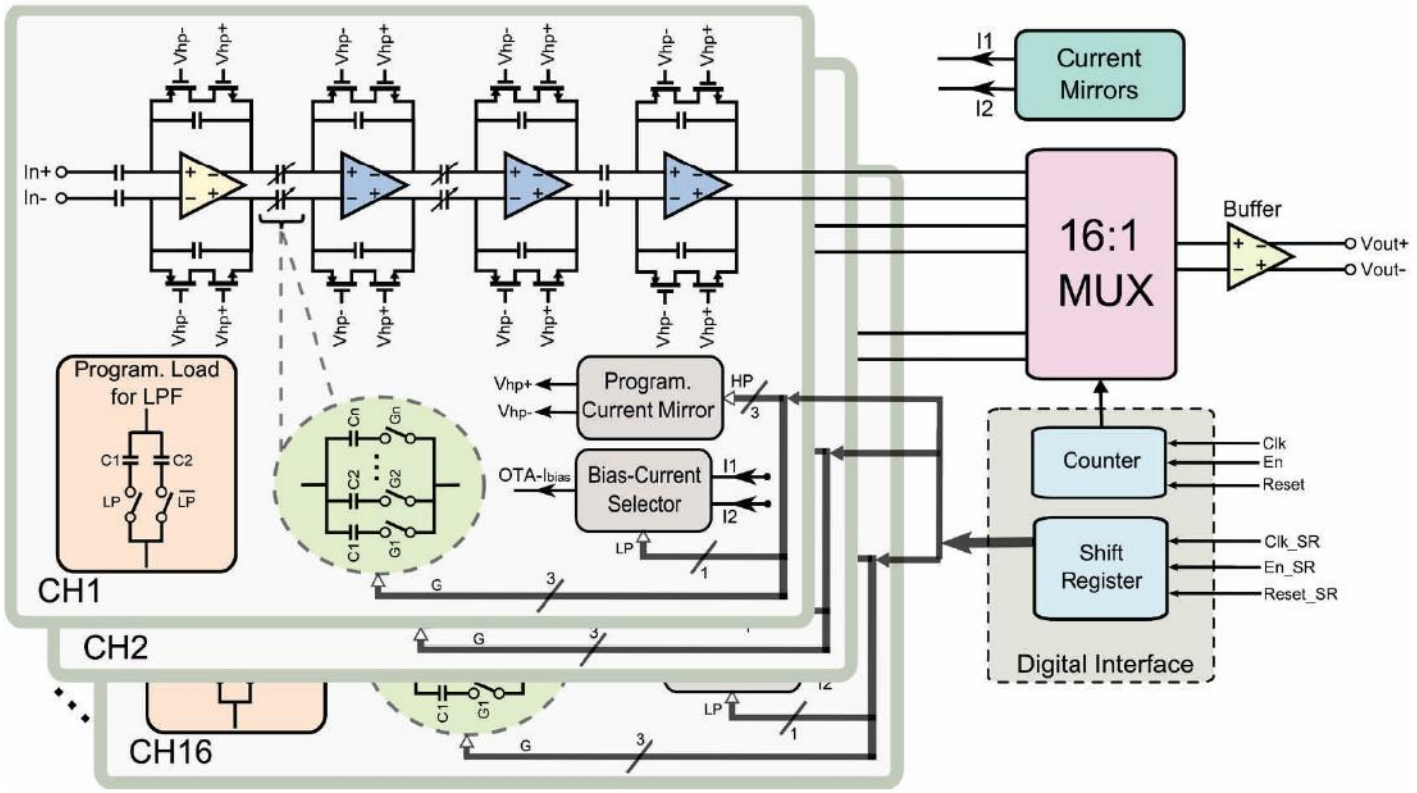


Figure 1. Architecture of the 16-channel neural recording system.

The high-pass filtering characteristic in each channel is achieved by the parallel combination of the feedback capacitors and the feedback MOS-bipolar pseudoresistors (formed by a NMOS and a PMOS transistors). These voltage-controlled pseudoresistor elements [7] can achieve very high resistance values in the order of 10^{12} Ω, providing an area-efficient way to implement very low frequency filters. The cutoff frequency can be tuned via a current-mode digital-to-analog converter (Fig. 3) that changes the gate voltages of the transistors (i.e. the resistance), in order to accept or reject the LFP signal frequencies. This circuit consists of a wide-swing cascode current mirror that copies the selected current to the transistors *Mn* and *Mp*, which are diode-connected and sized with large *W/L*. A similar method was previously described by Yin *et al* [8].

The fourth-order low-pass filter characteristic is implemented by the cascade of first-order voltage integrators, consisting of an OTA and a load capacitor. The load capacitor is implemented as a capacitor array that allows the selection of two different frequency ranges: one for the LFP signals and another for the AP signals. Also, for low-frequency LFP recordings, the supply current of the amplifiers is lowered to save power.

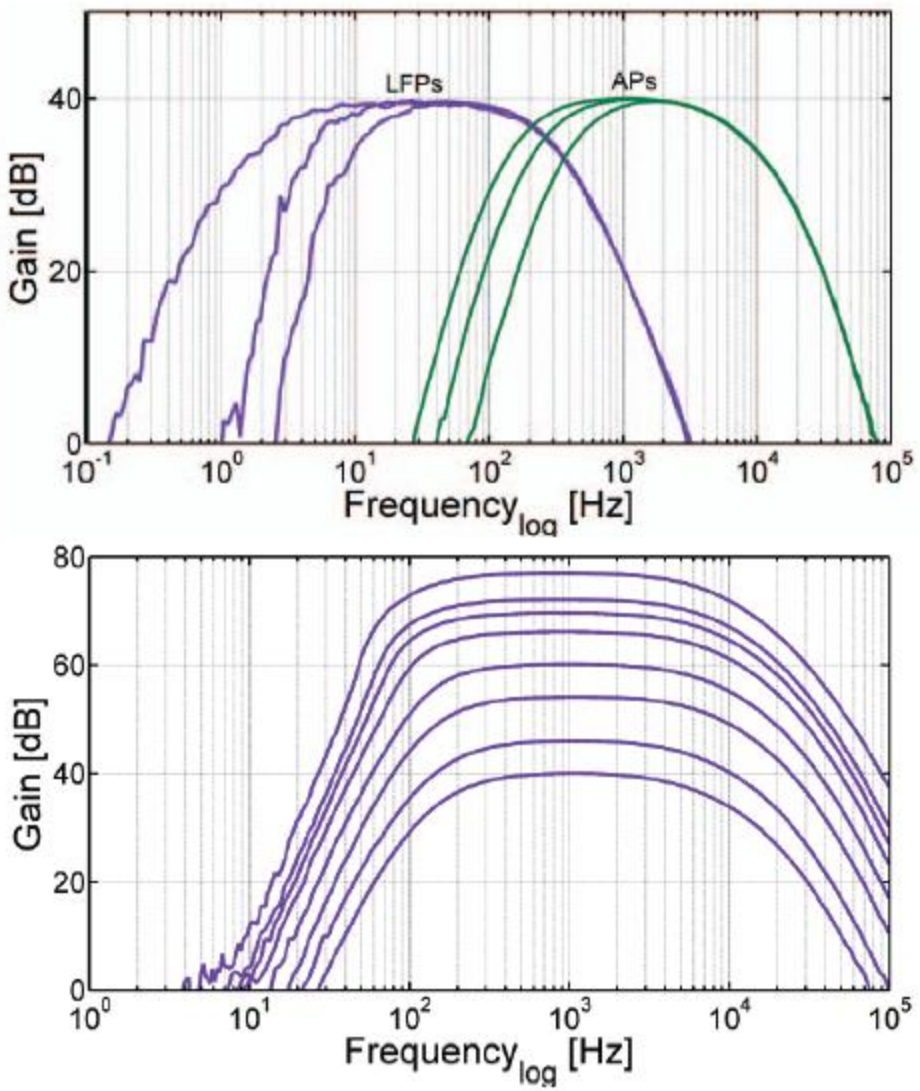


Figure 5. Transfer function of one channel, measued for different bandwiths and gains.

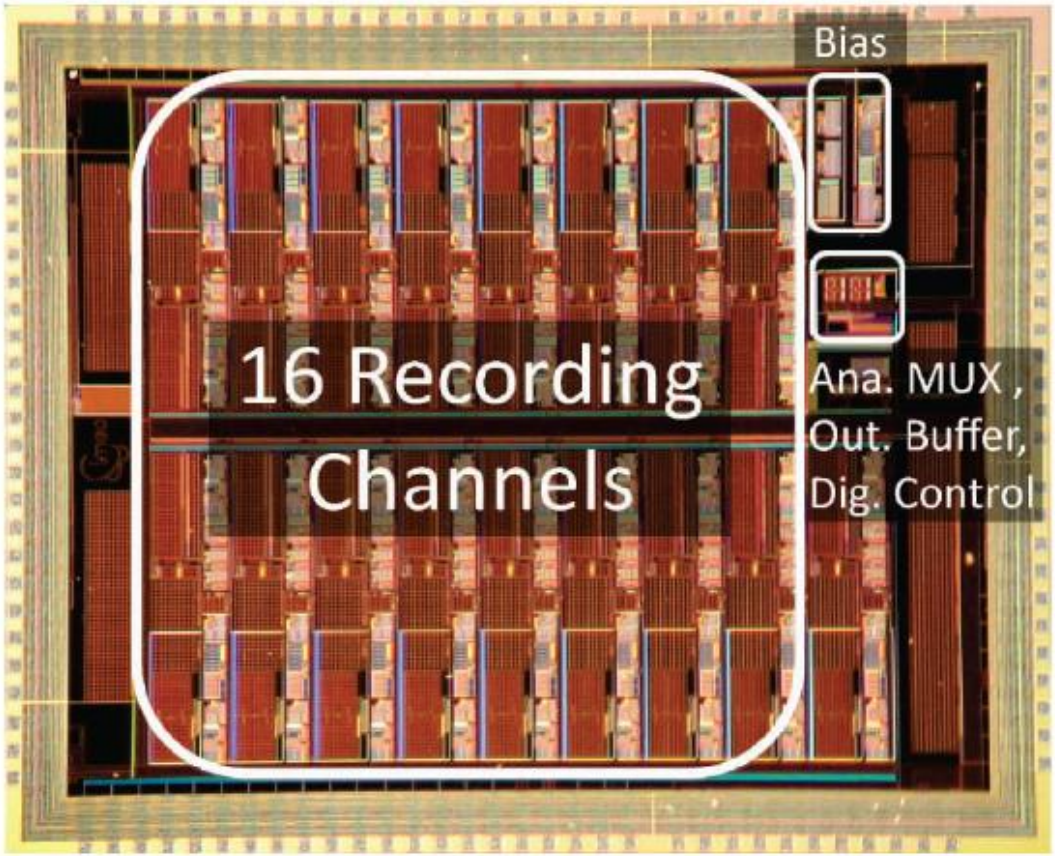


Figure 4. Die photo of the 16-channel neural recording system. The total area is 5.6 mm × 4.5 mm and the core area is 4.1mm × 3.8 mm.

The 16-channel neural recording system in Fig.1 has been implemented and fabricated in a 0.35 μm On Semiconductor CMOS technology. The capacitors are implemented as metal-insulator-metal capacitors and the resistors as polysilicon resistors. The die (Fig. 4) occupies a core area of 4.1 × 3.8 mm^2 and a total area of 5.6 × 4.5 mm^2. The area of one channel is 0.76 mm^2.

A High-Performance PLL With a Low-Power Active Switched-Capacitor Loop Filter

Yu Song, *Student Member, IEEE*, and Zeljko Ignjatovic, *Member, IEEE*

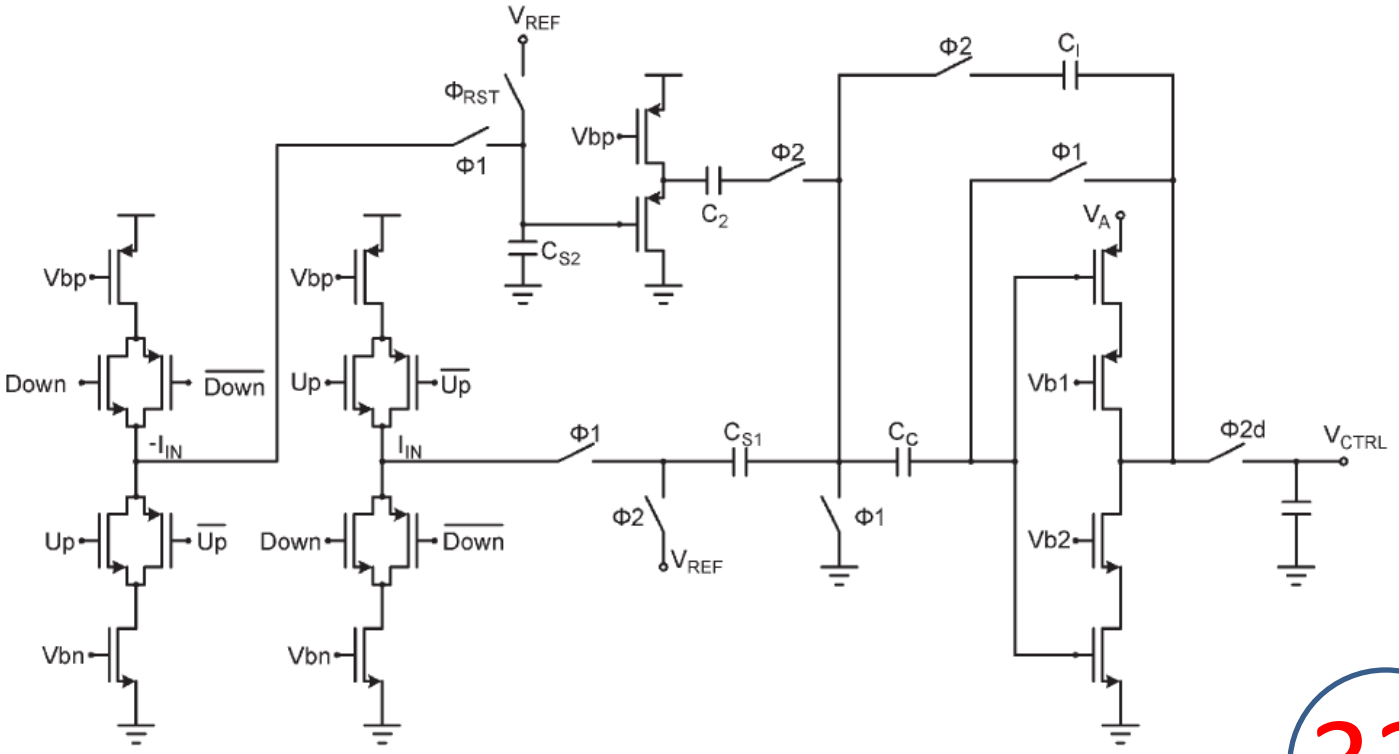


Fig. 1. Proposed SC PLL loop filter with complimentary charge pumps, single-ended shown.

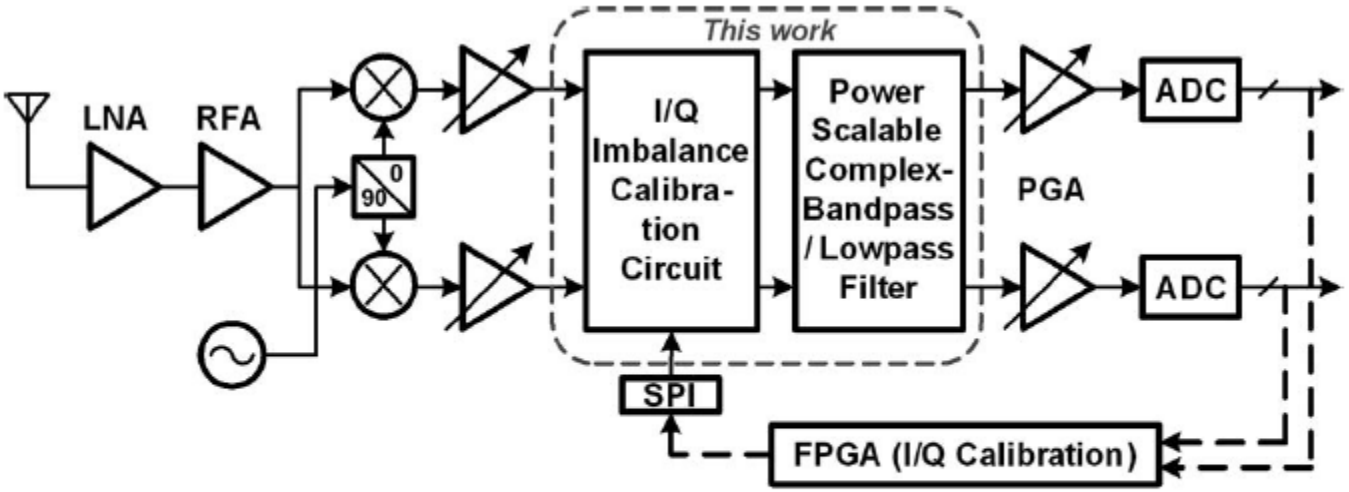
A low-power low-noise differential SC loop filter is designed based on the above analysis, with another filter, as shown in Fig. 1, sharing the complimentary charge pumps. The input reference frequency is selected to be 10 MHz, and the loop bandwidth is around 350 kHz. The discrepancy between the

TABLE I
PLL PERFORMANCE COMPARISON

	[1]	[3]	[4]	This Work
Freq. (GHz)	2.4	2.4	3.6	2.5
Technology	0.25μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Loop Filter Structure	Passive SC	Passive SC	Hybrid	Active SC
Reference Frequency	1MHz	12MHz	50MHz	10MHz
Power (mW)	?	48.8 (core)	110 (core)	16
Area (mm^2)	?	4.8	2.7 (acitve)	0.36
Reference Spur	-62dBc	-70dBc	-45dBc	-64dBc
Phase Noise	-126dBc/Hz @2MHz	-125dBc/Hz @3MHz	-155dBc/Hz @20MHz	-124dBc/Hz @3MHz

Power-Scalable, Complex Bandpass/Low-Pass Filter With I/Q Imbalance Calibration for a Multimode GNSS Receiver

Yang Xu, Baoyong Chi, *Member, IEEE*, Xiaobao Yu, Nan Qi, Patrick Chiang, *Member, IEEE*, and Zhihua Wang, *Senior Member, IEEE*



Mode	GPS			Compass			GLONASS		Galileo		
Channel	L1	L2	L5	B1	B2	B3	L1	L2	E1	E5a	E5b
BW (MHz)	2.2/18	18	18	4.2	4.2/18	18	10/18	8/18	2.2	18	18

Fig. 1. Low-IF/zero-IF multimode GNSS receiver.

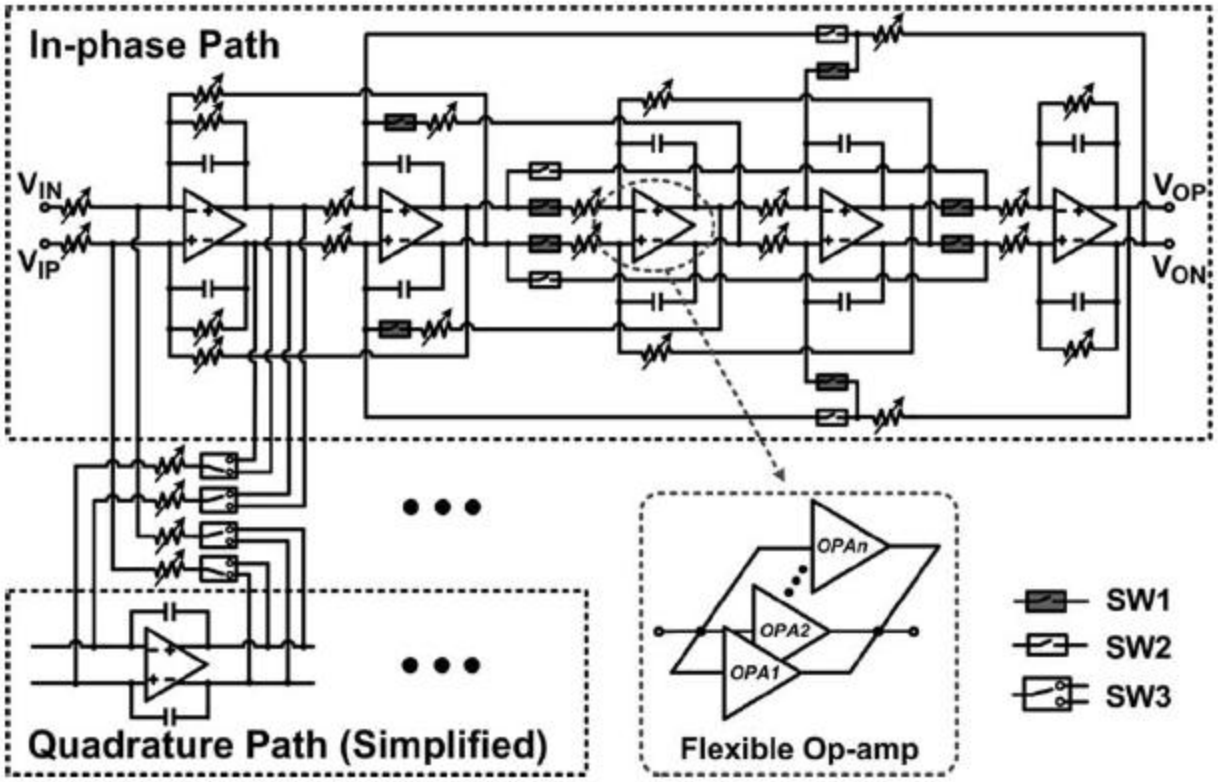


Fig. 2. Architecture of the reconfigurable fifth-order CBPF/third-order LPF.

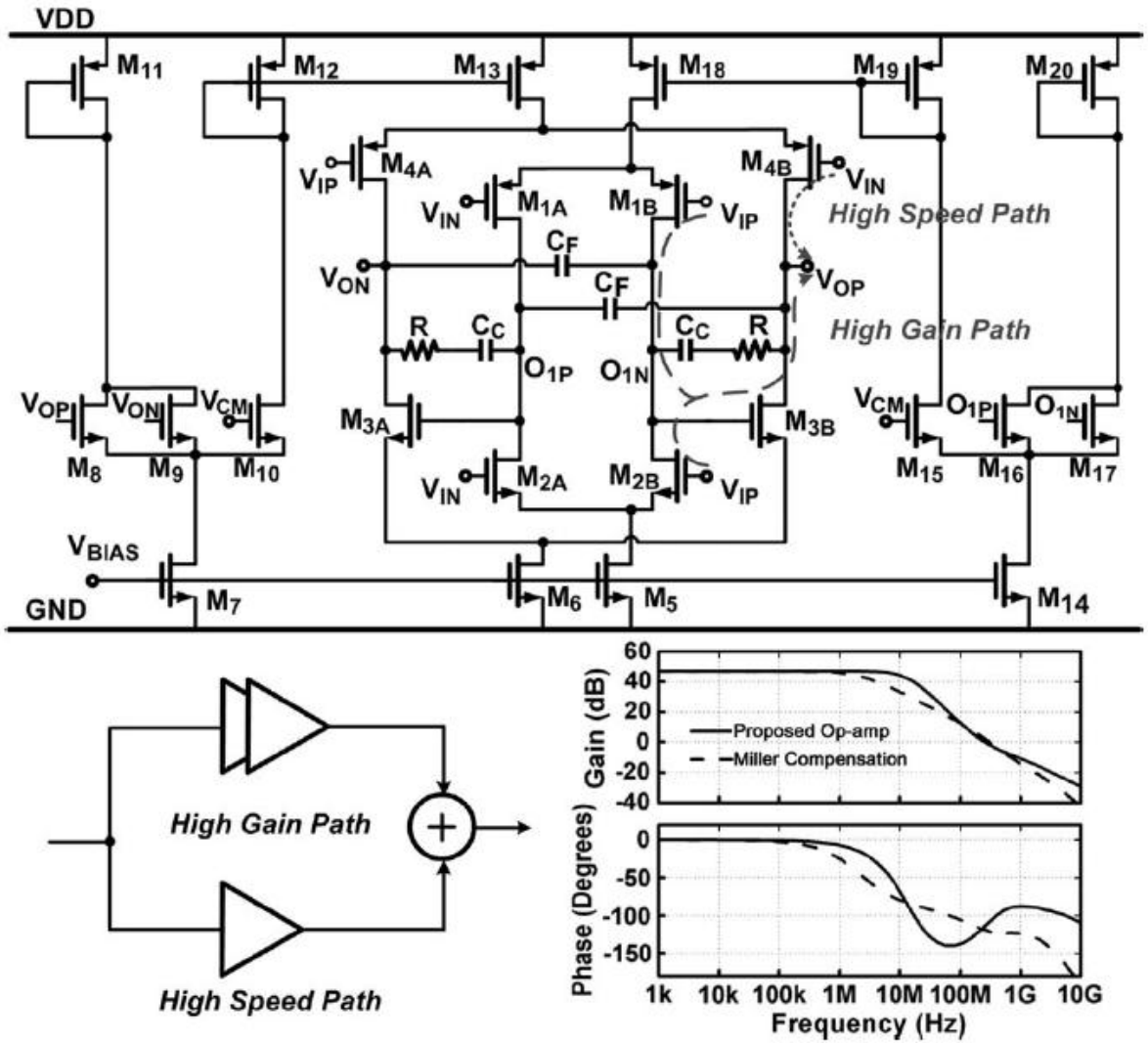


Fig. 3. Simplified op-amp cell of the FLOA.

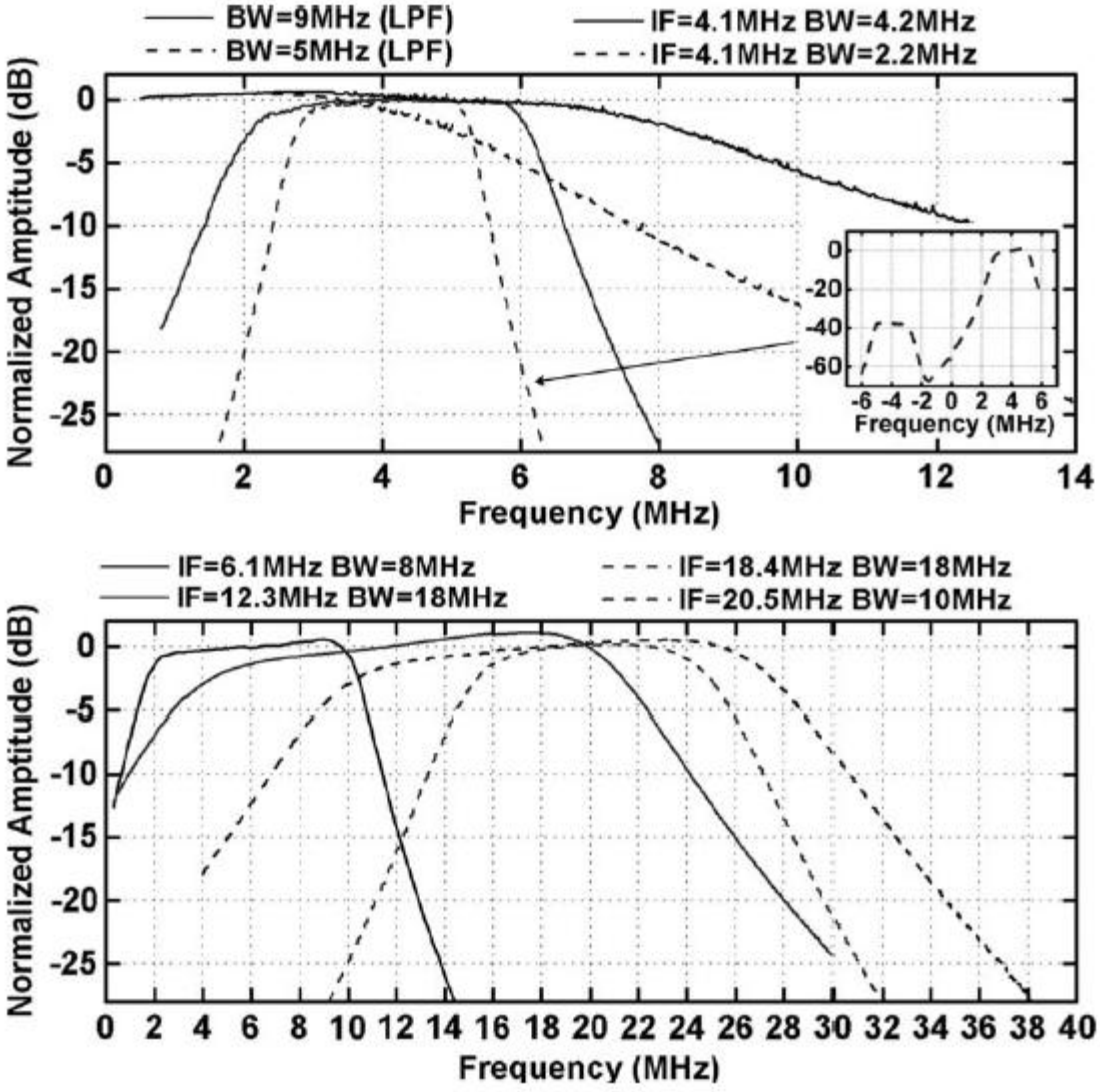


Fig. 7. Measured ac response of the LPF and the CBPF.