expensive to detect. In fact, questions about whether some complicated circuits are even testable arise. It is now an accepted responsibility of the designers to address the testing problem at the design stage. ICs often contain additional circuitry, which is used in the testing of the circuit itself. The testing question is definitely not trivial for complicated designs, and it represents an active area of research. Related to this problem is the field of fault-tolerant technology, also an active area of research, in which circuits are designed so that they remain functional even if some faults do exist.

The probability of having one or more hard faults on any die associated with particulate material or crystal defects generally increases with both die area and circuit complexity. The reason for the increase with die area should be apparent; it is more likely that a die will contact some fixed defects on a wafer if the die area is increased. This is illustrated in simplified form in Fig. 1.5-1, where varying die sizes are considered with a fixed defect distribution. It should be apparent from this example that with 52 potential dies, 45 will be free of defects (Fig. 1.5-1*b*). With 12 potential dies (Fig. 1.5-1*c*), 7 will be free of defects, and with 4 potential dies none will be free of defects (Fig. 1.5-1*d*). In this example, yield decreases from 86% to 0% as the die size increases.

Although not accounted for in the previous example, the density of defects which will cause die failure also increases with die complexity. If a die is

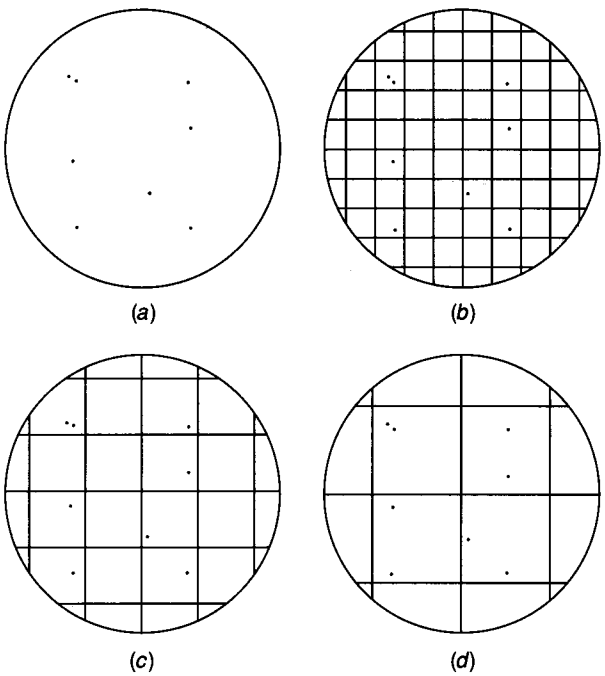

FIGURE 1.5-1
Effects of defects on yield: (a) Defect locations, (b) Small die size, (c) Larger die size, (d) Die size with zero yield.

not heavily utilized, some defects may occur in areas where no components or interconnections exist, so die failure will not result. Likewise, some types of defects are more likely to cause a fault if they occur where a transistor is located than where interconnections are made. It can be shown, however, that for a fixed circuit schematic overall yield decreases with increasing die size and increases if the devices are densely packed on the die. The reader is thus cautioned not to draw the conclusion that the yield can be improved by decreasing the density if more silicon area for a given circuit is used. In general, the decrease in failure density on a die with a loosely packed circuit will be more than offset by the total number of defects anticipated in the die with larger area.

Several models are used to predict yield associated with crystal- and particulate-related defects. A simple model based upon using the Poisson distribution to predict the probability of K defects in a die area, A, with an average defect density of D defects per unit area results in the expression for the probability that a given die of area A has zero defects:

$$P = e^{-AD} \tag{1.5-1}$$

The defect density, D, is typically in the range of 1 to 2/cm^2.

Since many defects cause a failure only if the defect occurs in an active area, it may be preferable to use the active area and the corresponding average active area defect density in Eq. 1.5-1. Alternatively, even better results should be obtainable if the active and interconnection defects are considered separately. If A_A and A_I denote the active and interconnect areas, respectively, and D_A and D_I denote the average defect densities in those two regions, then the probability that a die is good can be obtained by modifying Eq. 1.5-1

$$P = e^{-(A_A D_A + A_I D_I)} \tag{1.5-2}$$

Example 1.5-1. If the average defect density is 1/cm^2, what is the average cost per good die for a 4" wafer if the die size is 1 cm^2? 0.2 cm^2? What would be the price per good die if the average defect density increased to 2/cm^2? Neglect die losses associated with the wafer edges. Assume the cost for the 4" wafer and processing is \$200 and that Eq. 1.5-1 models the probability that a device is good.

Solution. The average cost per good die is $200/NP$ where P is the probability the die is good and N is the number of potential dies per wafer. The number of potential 1 cm^2 dies in a 4" wafer is (neglecting edge losses)

$$N_{1\text{cm}} = \frac{\pi[(2\text{ in})(2.5\text{ cm/in})]^2}{1\text{ cm}^2} = 81$$

Likewise

$$N_{0.2\text{cm}} = 405$$

For a 1/cm^2 defect density, it follows from Eq. 1.5-1 that the probability that the 1 cm^2 die is good is 36%, whereas the probability that the 0.2 cm^2 die is good is 82%. The corresponding cost per good 1 cm^2 die is thus \$6.86. The cost per good 0.2 cm^2 die is 60¢. If the defect density were to increase to 2/cm^2, the average

cost per good 1 cm^2 die increases to \$18.24 and the 0.2 cm^2 die increases to 74¢. From this example it should be apparent that increasing either the defect density or die area significantly increases the average die cost once the product of A and D exceeds unity.

Example 1.5-2. If the average defect density is $1.5/cm^2$, what is the yield if the die size is increased to that of an entire 4" wafer? On the average, how many such wafers must be fabricated to give one good die? If the cost of each wafer is \$200, what would be the average cost per good die? Use the simple model of Eq. 1.5-1 to predict yield.

Solution. From Eq. 1.5-1, the probability that the die is good is

$$P = e^{-\pi(2\text{ in})^2(2.54\text{ cm/in})^2(1.5)/\text{cm}^2}$$

$$P = 1.53 \times 10^{-53}$$

It thus requires, on the average, $1/P = 6.5 \times 10^{52}$ wafers to yield one good die. At a cost of \$200/wafer, the average cost per good die would be $\$1.3 \times 10^{55}$.

Two important observations can be made from the simplified calculations of the previous example. First, the effective cost of good large die is very high. Second, the concept of using the entire wafer as a single IC is totally impractical if the circuit is not tolerant of any faults. The concept of using the entire wafer as a single IC (termed wafer scale integration or WSI), is sufficiently attractive, however, that considerable effort has been devoted to research in this area. These circuits must, of course, provide for a mechanism of repair—either through inherent redundancy or some form of mechanical reconfiguration (e.g., laser trimming)—to be viable, since some defects will occur during processing.

For large devices the yield predicted by Eq. 1.5-1 is somewhat pessimistic. Two other models used are the Seeds model[14] and Murphy model[15], which are characterized respectively by the following expressions for the probability that a given die is good:

$$P = e^{-\sqrt{AD}} \tag{1.5-3}$$

$$P = \left(\frac{1 - e^{-AD}}{AD}\right)^2 \tag{1.5-4}$$

Additional information about yield prediction can be found in references 16–19.

Soft faults due to parameter drifts also affect yield in a statistical sense. The soft faults play a major role in yield of analog circuits. The effects of parameter drifts can best be appreciated by considering Fig. 1.5-2, in which the statistical distributions of the parameter X are shown. In Fig. 1.5-2*a* the statistical distribution of the average of the parameter over repeated processing runs is shown. X_{MAX} and X_{MIN} define a process window within which the average value of the parameter must reside. Both design and processing groups must agree on an acceptable process window. The cost of fabricating an IC increases with a decreasing process window and approaches infinity as the width of the process window converges to zero. It is often the case that X_{MAX} and X_{MIN} differ from

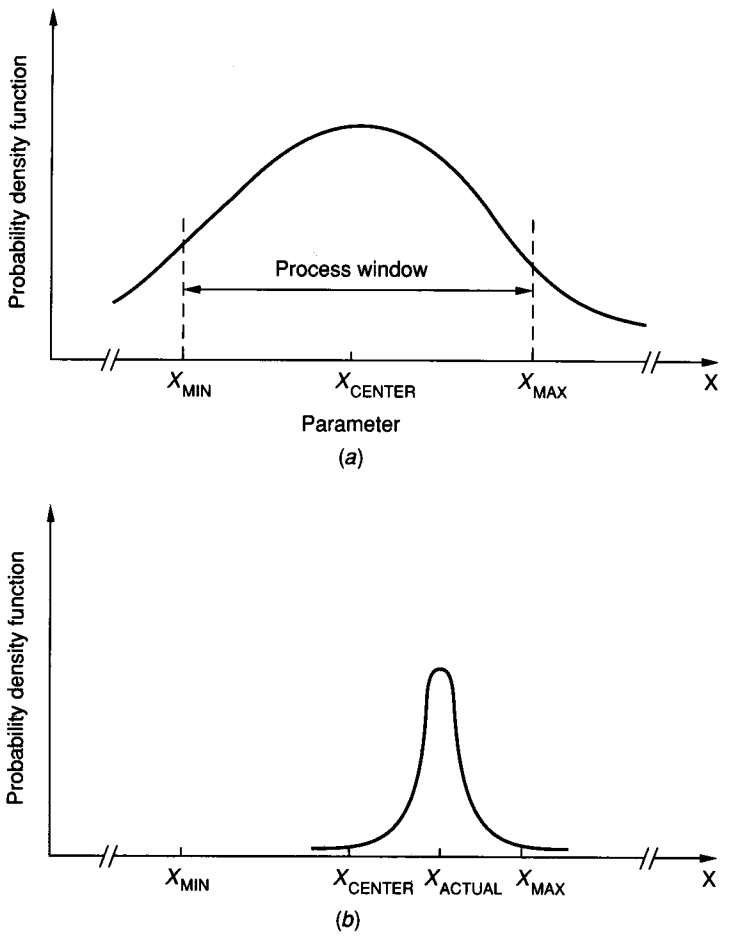

FIGURE 1.5-2
Statistical parameter spreads in a variable X: (a) Process window, (b) Wafer level variations.

X_{CENTER} by 10% to 50% for most of the major process parameters. More details about parameter spreads can be found in Chapter 2. Good designs will meet specifications over a wide process window. It often requires considerable effort on the part of the designer to produce designs that meet specifications over a wide process window. This is particularly true of analog designs.

Even at the wafer level, statistical variations in the parameter occur across the wafer. These variations are somewhat dependent on proximity of devices and, because of the way parameters are defined, the symmetry in layout. This variation, not including either device proximity or layout, is shown in Fig. 1.5-2*b*, where X_{ACTUAL} represents the average value of the parameter X on a given wafer. X_{ACTUAL} is thus considered a random variable relative to processing but a fixed parameter once processing is complete. The statistical variance at the wafer level is generally much smaller than the variance at the processing level.

For example, the capacitance density of oxide capacitors may have a processing variation (variance) of 10% of the mean whereas the wafer-level variation may be less than 0.1% of the mean. Two interesting observations can be made from the curves in Fig. 1.5-2. First, after fabrication the parameters are distributed around X_{ACTUAL} rather than the process center, X_{CENTER}. In fact, after processing the probability that a parameter is close to X_{CENTER} may be quite small. Second, it should be apparent that designs should meet specifications over *both* process window and wafer-level variations.

Most good digital designs are functionally tolerant to large process parameter variations of all key parameters and are quite insensitive to wafer-level variations. This insensitivity is inherent in most of the basic digital circuit structures. These variations, however, play a major role in the speed specifications of digital circuits, with faster circuits commanding a premium price in the marketplace.

The analog designer, on the other hand, must pay considerable attention to both process window and wafer-level variations. The process window variations are actually so large that many design approaches used in discrete component design are totally impractical in monolithic designs. For reasons that will become apparent in later chapters, the performance of many analog designs is strongly dependent on close matching of devices and device characteristics and relatively tolerant of nominal parameter variations within the process window. Consequently, the curve of Fig. 1.5-2*b* plays a key role in many analog designs.

Although the exact shape of the parameter distributions shown in Fig. 1.5-2 is of interest, that information is not widely distributed. Rather, a single parameter that in some sense characterizes the parameter distribution is more commonly available. For example, a comment about the threshold voltage, V_T, such as $V_T = 0.5\ V \pm 20\%$ means that the value of V_T after processing will "usually" be within $\pm 20\%$ of 0.5 V. Actually, depending on the process acceptance criteria, the average value of V_T may be within this window for all accepted wafers. Correspondingly, a comment such as "V_T matching is to 5 mV" means that the wafer-level parameter variations such as those shown in Fig. 1.5-2*b* typically differ by less than 5 mV from the measured average value. Whereas the bounds on the process window may be fixed due to rejection of wafers that do not meet the acceptance criterion, the wafer-level variations are essentially not bounded. Unless stated differently, it will be assumed throughout this text that a wafer-level or process window distribution as specified above corresponds to a window within which *99.73% of the devices* will fall. This corresponds to a ± 3 standard deviation window if the random variable is normally distributed—an assumption that is often made.

Example 1.5-3. Assume the die of a circuit is 6 mm on a side with a defect density of $0.7/cm^2$. Assume also that the die includes an analog section, which includes 100 transistors in which the characteristics must all be matched to within 0.5% of the die average value to meet specifications. Assume that the matching characteristics of the transistor are dominated by a single parameter that is normally distributed with a ± 3 standard deviation window, characterized by a variation from the die average of $\pm 0.5\%$.

(*a*) Using the Seeds model for defect density, determine the approximate yield if potential soft faults in the analog section are neglected.

(*b*) Estimate the yield if both hard and soft faults are considered.

(*c*) Repeat (*b*) if matching to 0.25% is required in the analog section.

Solution. (a) From (Eq. 1.5-3), the hard yield is the probability that a die is good, which is given by

$$P_H = e^{-\sqrt{AD}} = e^{-\sqrt{(6\text{mm})^2(7\times10^{-3})/\text{mm}^2}} = 60.5\%$$

(*b*) The probability that a die has no soft faults is equal to the probability that *all* 100 transistors meet the matching specifications. The probability that each transistor meets the matching requirements is $P = .9973$. Thus, the probability that all 100 transistors meet the specifications is

$$P_S = (.9973)^{100} = .763$$

The overall yield is thus the product of the hard and soft fault yield, which is

$$P = P_H P_S = 46\%$$

(*c*) For a matching to 0.25%, it follows from a standard investigation of the normal distribution that the probability that a given transistor meets the specifications is equal to the probability that the normal random variable is within $\pm$ 1.5 standard deviations of the mean. From a probability density table for the normal distribution, it follows that the probability that any one transistor meets the specifications is 0.8664. Thus, the probability that all 100 transistors meet specifications is

$$P_S = (0.8664)^{100} = 5.9 \times 10^{-7}$$

Thus, from part (*a*), the overall yield is

$$P = P_S P_H = 3.5 \times 10^{-6} = 3.5 \times 10^{-5}\%$$

Note that this modest increase in matching requirement from 0.5% to 0.25% results in a yield that is so small as to make such a design totally impractical.

The previous example demonstrates a very important point. If very much matching is required in analog circuit design, then the matching requirements must not be too severe if the yield is to be high enough to make the circuit economically feasible.

Since considerable variation from the process center occurs, as indicated in Fig. 1.5-2*a*, one naturally asks the question: What value should be used for the parameters at the design stage? Stated alternately, the problem is to find the design target, or the design center, for each parameter. The process center is widely used for the design center. It can, however, be shown that in some cases, the yield can be improved if something other than the process center is used for the design center. The field of design centering and yield optimization addresses these questions. Unless stated otherwise, it will be assumed throughout this book that the desired design center corresponds to the process center.

The reader should be cautioned to avoid the temptation of using experimental parameter centers obtained from measurements made on one or two wafer lots

in lieu of the design center that has evolved with the process itself. It should be apparent from Fig. 1.5-2 that using experimentally measured parameters rather than the process center as design centers will statistically bias designs in a way that will often be accompanied by a decrease in yield.

Industry is keenly aware of the relationship among the specified process window (which dictates the design specification range), the actual wafer-level variations, and the corresponding yield. A *capability index*, which relates these variables for any process parameter, is defined by the expression[20]

$$C_p = \frac{\text{Design specification width}}{\text{Process width}} \tag{1.5-5}$$

where the process width is generally defined to be ± 3 standard deviations (σ) about the mean. Assuming a normally distributed process around the mean in which the process width is characterized by the $\pm 3\sigma$ window, it follows that if the process window is centered in the design specification window, then the probability that a parameter of a device lies inside the design specification window is

$$P = \frac{1}{\sqrt{2\pi}} \int_{-3C_p}^{3C_p} e^{-(x^2/2)} dx \tag{1.5-6}$$

This error function, erf (x), integral is readily obtainable from tables of the normal probability distribution, which appear in most elementary statistics texts. If C_p is small, the probability that a device parameter is actually within the process window is small; the yield will be poor and will deteriorate even more if the mean of a parameter for a wafer is not centered within the design specification window. Correspondingly, if C_p is large, the yield will be high and the process will be reasonably tolerant to small shifts in the wafer-level parameter center from the design specification center. Setting the design specification width so that $C_p = 2$ will result in reasonable yield in many applications, although this may place unrealistic performance demands on the designer for some design projects.

Example 1.5-4 clearly demonstrates the yield implications associated with properly establishing the capability index.

Example 1.5-4. If 1000 devices on a chip must have a specific parameter within the specified design process window, determine the soft yield if the process has been characterized by a capability index of (*a*) $C_p = 0.5$, (*b*) $C_p = 1.0$, (*c*) $C_p = 1.5$, and (*d*) $C_p = 2.0$.

Solution. With $C_p = 0.5$, it follows from Eq. 1.5-6 and a normal random variable table that $P = .8664$. Thus, the probability that all 1000 devices have a parameter within the design specification window is $P_{1000} = (.8664)^{1000} \approx 0$. If $C_p = 1.0$, $P = .9973$ and $P_{1000} = .067$, which represents about a 6.7% yield. If $C_p = 1.5$, $P = .999993$ and $P_{1000} \approx .993$. Finally, if $C_p = 2.0$, $P = .999999998$ and $P_{1000} \approx 1.0$, indicating essentially a 100% yield.

1.6 TRENDS IN VLSI DESIGN

Several trends in the production of VLSI circuits are readily identifiable. Some of these have already been discussed in this chapter. The most visible is the continual shrinking of the minimum geometrical feature size. Although this trend will continue, the rate at which the minimum feature size decreases is slowing. This slowing is partially attributable to inherent physical limitations in the photolithographic process and the rapidly increasing costs associated with very fine resolution processing equipment. Problems associated with power dissipation density, the effects of additional diffusion in small devices due to subsequent heat cycle steps during processing, and concerns about a practical alternative to the widely used standard local oxidation (LOCOS) processing step are all becoming significant in submicron processes. The size of the silicon atom and the silicon dioxide molecule will also be of increasing concern in submicron processes. These concerns about size place very real lower bounds on the conventional approach to integrated circuit design.

A trend in increasing speed in digital circuits is readily identifiable. Some research efforts with gallium arsenide (GaAs) suggest that this material may ultimately supplant silicon at very high frequencies. GaAs is attractive because of higher electron mobility and, in some applications, because of reduced sensitivity to radiation. Continual improvement in the performance of silicon circuits raises doubts, however, about when and if a transition to GaAs will occur. The increase in speed and increase in circuit complexity are direct results of the reduction in feature size.

A third trend is the increasing complexity of circuit function and device count on a die. This trend is crucial for the development of new markets for integrated circuits.

A fourth trend is toward increased designer productivity and an ever-growing dependence on the computer in the design process. Design methods that were standard a decade ago would be totally unworkable in many current design projects.

A fifth trend is the continual shift of where design, production, and markets are geographically located. A decade ago most major and innovative design efforts and a significant portion of the production were done in the United States and Western Europe, with more mature technologies being transferred to the Far East. Production was generally most profitable in countries where labor costs were low. An increasing shift in the design efforts to the more developed Far Eastern countries has occurred in recent years, with the mature production shifting more into the less-developed Far Eastern countries, where labor costs remain low. The marketplace is also shifting, with a large number of less-developed countries now experiencing the data processing and telecommunications revolution that swept the West a decade earlier. A trend of the design and production activities geographically following the marketplace is also observable.

A sixth trend is a growing coupling of a specific process and its processing equipment. As feature sizes shrink and processes become more complex, the process is becoming increasingly dependent on the performance of specific pieces of equipment.

Other trends include the use of more powerful CAD tools, which extends VLSI design to the realm of the systems designer, and increasing the complexity of processes by using silicon on insulator (SOI) or combining both MOS and bipolar technologies into a single process.

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PROBLEMS

Section 1.1

1.1. How many SiO_2 molecules will be required to form the insulating layer under the gate of a MOSFET that has a 3 $\mu \times$ 3 μ gate area if the silicon dioxide thickness is 800 Å? Repeat if the gate is 0.5 $\mu \times$ 0.5 μ with a 100 Å SiO_2 layer.

1.2. What is the average number of vertically stacked SiO_2 molecules in an 80 Å gate oxide layer?

Section 1.4

1.3. If the average resistance density (resistance/unit area) is 1.2 Ω/μ^2 and the capacitance density is 0.7 fF/μ^2(1 fF = 10^{-3} pf = 10^{-15} F) and if a 5 inch wafer costs \$250 to produce, what is the cost (based upon area) of a 250 kΩ resistor? What is the cost of a 100 pF capacitor? How many 2 $\mu \times 2$ μ transistors can be placed in the area required for the 250 kΩ resistor? For the 100 pF capacitor? What is the cost per transistor if spacing and interconnection area are neglected? What is the cost per transistor if spacing and interconnection increase the area per transistor by a factor of 10?

Section 1.5

1.4. If a 4 inch wafer costs \$200 and the defect density is $D = 2/cm^2$, what is the maximum permissible die area that can be used if the effective die cost (cost per good die) must not exceed 45¢? Assume the Seeds model characterizes the yield of the process and neglect area losses associated with placing square dies on a round wafer.

1.5. If an 8-bit flash A/D converter has 2^8 comparators and all must have an offset voltage less than 40 mV (-40 mV $< V_{offset} <$ 40 mV) for the device to operate properly, and if the offset voltage for the comparators in this process is 20 mV, what percentage of the dies will fail due to soft faults associated with the offset voltage? If the same approach is used to build a 10-bit converter, the offset voltage requirement is more stringent (10 mV). If the same process is used, what percentage of the dies will now fail due to soft faults associated with the process?

1.6. Derive an expression for and plot the effective die cost (cost per good die) versus die area if the defect density is $2/cm^2$ for both the simple model of Eq. 1.5-1 and Seeds model. Also obtain an expression for and plot the cost per unit area and the cost per good unit area versus die area for both models. Assume the wafer size is 4 inch and the wafer cost after processing is \$200.

1.7. What is the average cost per good 24-pin plastic DIP package of a die that is 0.1 inch on a side if it is fabricated on a 5 inch wafer and the average defect density is $1.5/cm^2$? Assume that wafer probing is used to eliminate defective dies and that the packaging yield is 85%. Use the typical processing costs listed in Table 1.4-2 for your calculations.

1.8. Repeat Example 1.4-1 if the die size is decreased to 0.2 cm $\times$ 0.2 cm and the defect density is $1.5/cm^2$. Assume the yield model of Eq. 1.5-1 and a packaging yield of 95%.

1.9. Assume an integrated circuit has a die size of 0.8 cm $\times$ 0.8 cm, defect density of $2/cm^2$, a wafer size of 4 inch, a package requirement of 64 pins, and a packaging yield of 90%.

(*a*) Calculate the average cost per good package if wafer probing is used and parts are packaged in plastic DIP packages.

(*b*) Compare the results of part (*a*) with the average cost per good package if wafer probing is omitted and parts are packaged in ceramic side brazed packages.

Use the processing and packaging cost estimates of Table 1.4-2.

1.10. A 5 inch wafer is yielding 85% at wafer probe with a die size of 0.2 cm $\times$ 0.2 cm. Determine the defect density assuming the process is characterized by the Seeds model.

1.11. Assume an area overhead per die of 250,000 μ^2 to allow for interconnection of a die to the outside world. Assume that a minimum size transistor is 3 μ^2 and an additional 60 μ^2 is needed for spacing and internal interconnection for each transistor. Assume also that the die is fabricated on a 4 inch wafer and that production costs are characterized by the values given in Table 1.4-2.

(*a*) Calculate and plot the average cost of fabrication per transistor on this die as the number of transistors on the die ranges between 1 and 100,000.

(*b*) Calculate and plot the average cost per good transistor on good dies if the fatal defect density in the external interconnection area is $0.1/cm^2$ and that in the area devoted to transistors (transistor, spacing, and interconnection) is $1.5/cm^2$. Use the model of Eq. 1.5-2.

1.12. Determine the minimum acceptable capability index for characterizing a process if a soft yield of 95% must be maintained on a die that contains 2000 devices.