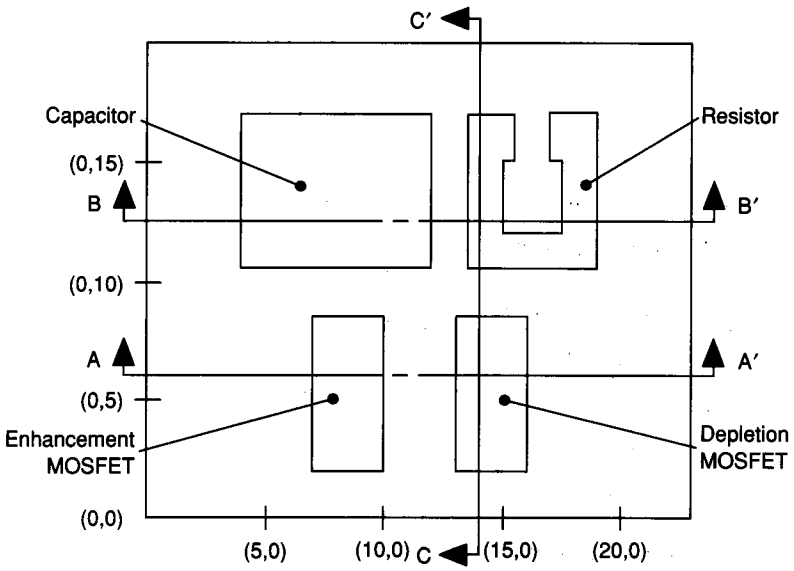
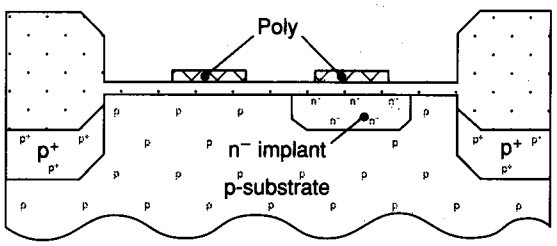
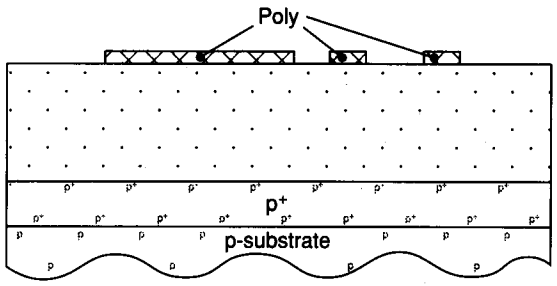


Mask #3 POLY 1



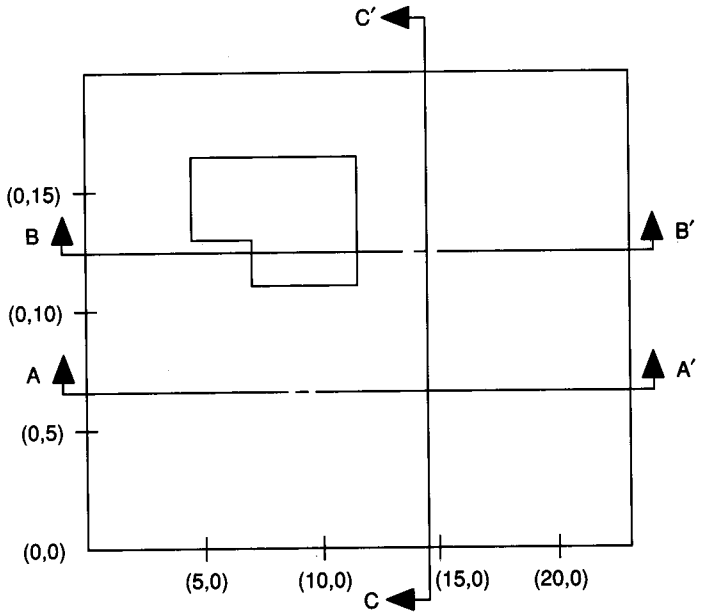
A-A′ Following Patterning POLY I



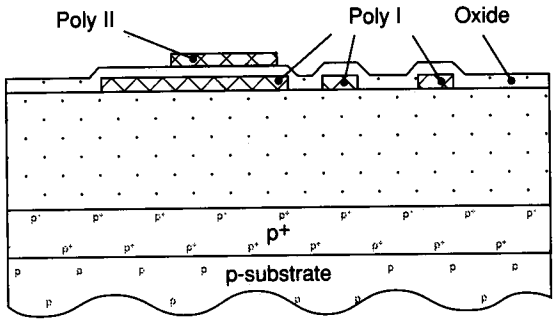
B-B′ Following Patterning POLY I

(*c*)

FIGURE 2A.1
(Continued)



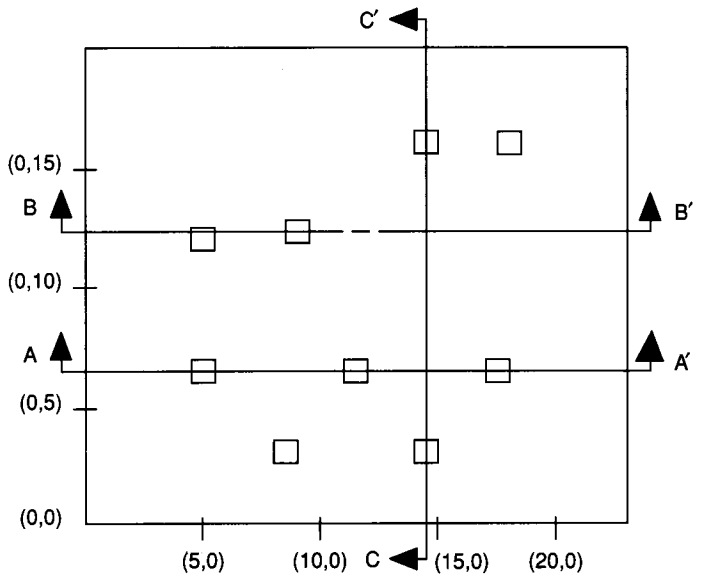
Mask B POLY II



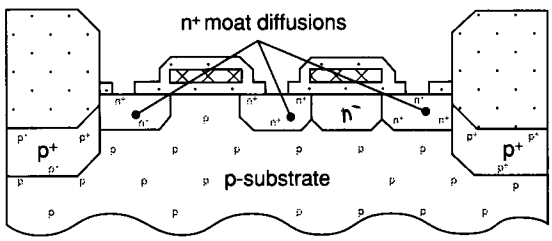
B-B′ Following Patterning POLY II

(*d*)

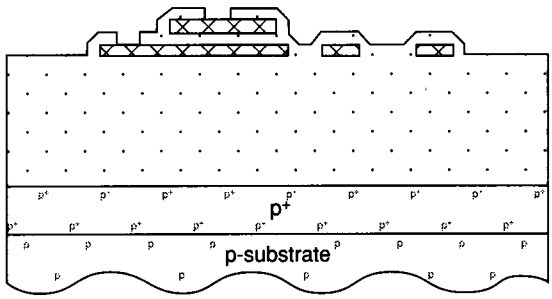
FIGURE 2A.1
(Continued)



Mask #4 Contact Openings



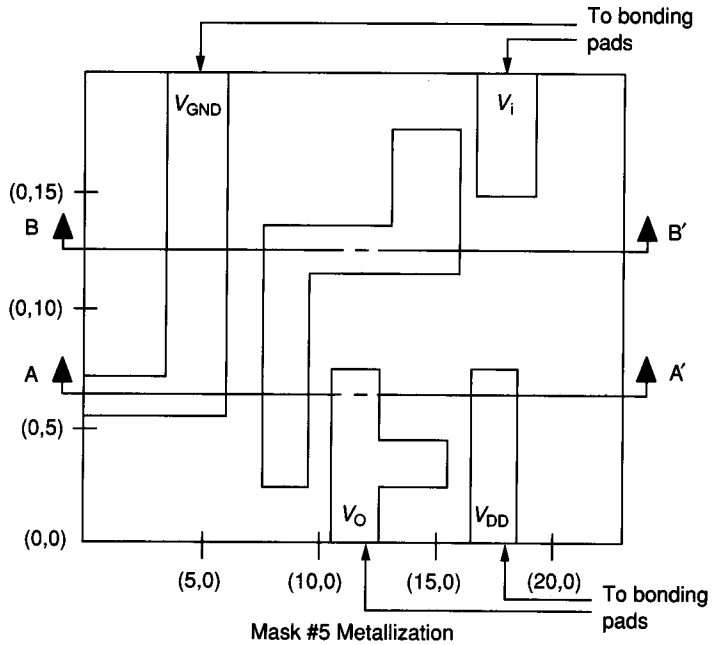
A-A′ Following Moat Diffusion and Contact Openings

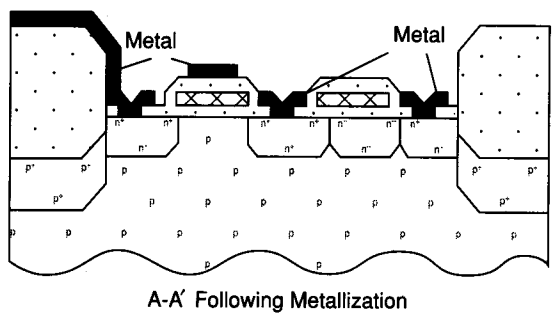


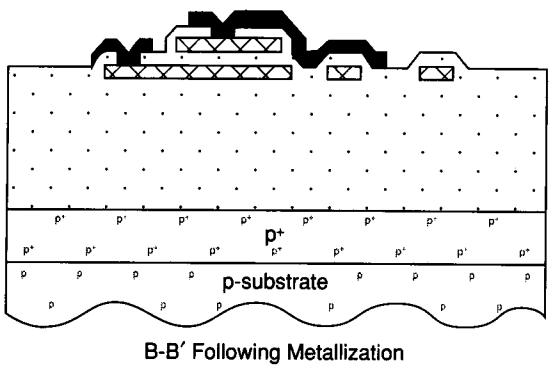
B-B′ Following Moat Diffusion and Contact Openings

(*e*)

FIGURE 2A.1
(Continued)







(*f*)

FIGURE 2A.1
(Continued)

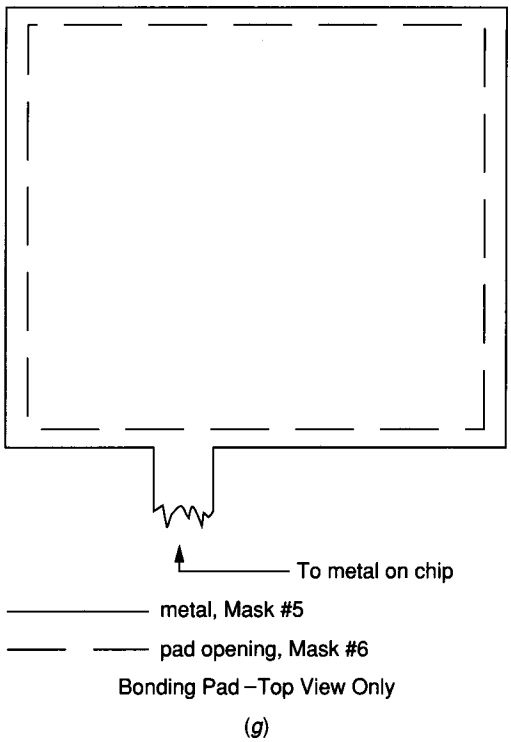


FIGURE 2A.1
(Continued)

APPENDIX 2B
PROCESS CHARACTERIZATION OF A GENERIC CMOS PROCESS

TABLE 2B.1
Process scenario of major process steps in typical p-well CMOS process[a]

1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN P-WELL	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffuse p-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT (n-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	
25.	Strip photoresist	
	Optional steps for double polysilicon process	
	B.1 Strip thin oxide	
	B.2 GROW THIN OXIDE	
	B.3 POLYSILICON DEPOSITION (POLY II)	
	B.4 Apply photoresist	
	B.5 PATTERN POLYSILICON	(MASK #B1)
	B.6 Develop photoresist	
	B.7 ETCH POLYSILICON	
	B.8 Strip photoresist	
	B.9 Strip thin oxide	

TABLE 2B.1
(Continued)

26.	Apply photoresist	
27.	PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts)	(MASK #4)
28.	Develop photoresist	
29.	p^+ IMPLANT	
30.	Strip photoresist	
31.	Apply photoresist	
32.	PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate)	(MASK #5)
33.	Develop photoresist	
34.	n^+ IMPLANT	
35.	Strip photoresist	
36.	Strip thin oxide	
37.	Grow oxide	
38.	Apply photoresist	
39.	PATTERN CONTACT OPENINGS	(MASK #6)
40.	Develop photoresist	
41.	Etch oxide	
42.	Strip photoresist	
43.	APPLY METAL	
44.	Apply photoresist	
45.	PATTERN METAL	(MASK #7)
46.	Develop photoresist	
47.	Etch metal	
48.	Strip photoresist	
	Optional steps for double metal process	
	C.1 Strip thin oxide	
	C.2 DEPOSIT INTERMETAL OXIDE	
	C.3 Apply photoresist	
	C.4 PATTERN VIAS	(MASK #C1)
	C.5 Develop photoresist	
	C.6 Etch oxide	
	C.7 Strip photoresist	
	C.8 APPLY METAL (Metal 2)	
	C.9 Apply photoresist	
	C.10 PATTERN METAL	(MASK #C2)
	C.11 Develop photoresist	
	C.12 Etch metal	
	C.13 Strip photoresist	
49.	APPLY PASSIVATION	
50.	Apply photoresist	
51.	PATTERN PAD OPENINGS	(MASK #8)
52.	Develop photoresist	
53.	Etch passivation	
54.	Strip photoresist	
55.	ASSEMBLE, PACKAGE AND TEST	

[a]Major functional steps shown in capital letters.

TABLE 2B.2
Design rules for a typical p-well CMOS process (See Table 2B.3 in color plates for graphical interpretation)

		Dimensions	
		Microns	**Scalable**
1.	p-well (CIF Brown, Mask #1[a])		
1.1	Width	5	4λ
1.2	Spacing (different potential)	15	10λ
1.3	Spacing (same potential)	9	6λ
2.	Active (CIF Green, Mask #2)		
2.1	Width	4	2λ
2.2	Spacing	4	2λ
2.3	p^+ active in n-subs to p-well edge	8	6λ
2.4	n^+ active in n-subs to p-well edge	7	5λ
2.5	n^+ active in p-well to p-well edge	4	2λ
2.6	p^+ active in p-well to p-well edge	1	λ
3.	Poly (POLY I) (CIF Red, Mask #3)		
3.1	Width	3	2λ
3.2	Spacing	3	2λ
3.3	Field poly to active	2	λ
3.4	Poly overlap of active	3	2λ
3.5	Active overlap of poly	4	2λ
4.	p^+ select (CIF Orange, Mask #4)		
4.1	Overlap of active	2	λ
4.2	Space to n^+ active	2	λ
4.3	Overlap of channel[b]	3.5	2λ
4.4	Space to channel[b]	3.5	2λ
4.5	Space to p^+ select	3	2λ
4.6	Width	3	2λ
5.	Contact[c] (CIF Purple, Mask #6)		
5.1	Square contact, exactly	3 × 3	2λ × 2λ
5.2	Rectangular contact, exactly	3 × 8	2λ × 6λ
5.3	Space to different contact	3	2λ
5.4	Poly overlap of contact	2	λ
5.5	Poly overlap in direction of metal 1	2.5	2λ
5.6	Space to channel	3	2λ
5.7	Metal 1 overlap of contact	2	λ
5.8	Active overlap of contact	2	λ
5.9	p^+ select overlap of contact	3	2λ
5.10	Subs./well shorting contact, exactly	3 × 8	2λ × 6λ
6.	Metal 1[d] (CIF Blue, Mask #7)		
6.1	Width	3	2λ
6.2	Spacing	4	3λ
6.3	Maximum current density	0.8 mA/μ	0.8 mA/μ

TABLE 2B.2
(Continued)

		Dimensions	
		Microns	**Scalable**
7.	Via [e](CIF Purple Hatched, Mask #C1)		
7.1	Size, exactly	3 × 3	2λ × 2λ
7.2	Separation	3	2λ
7.3	Space to poly edge	4	2λ
7.4	Space to contact	3	2λ
7.5	Overlap by metal 1	2	λ
7.6	Overlap by metal 2	2	λ
7.7	Space to active edge	3	2λ
8.	Metal 2 (CIF Orange Hatched, Mask #C2)		
8.1	Width	5	3λ
8.2	Spacing	5	3λ
8.3	Bonding pad size	100 × 100	100 μ × 100 μ
8.4	Probe pad size	75 × 75	75 μ × 75 μ
8.5	Bonding pad separation	50	50 μ
8.6	Bonding to probe pad	30	30 μ
8.7	Probe pad separation	30	30 μ
8.8	Pad to circuitry	40	40 μ
8.9	Maximum current density	0.8 mA/μ	0.8 mA/μ
9.	Passivation[f] (CIF Purple Dashed, Mask #8)		
9.1	Bonding pad opening	90 × 90	90 μ × 90 μ
9.2	Probe pad opening	65 × 65	65 μ × 65 μ
10.	Metal 2 crossing coincident metal 1 and poly[g]		
10.1	Metal 1 to poly edge spacing when crossing metal 2	2	λ
10.2	Rule domain	2	λ
11.	Electrode (POLY II)[h] (CIF Purple Hatched, Mask #A1)		
11.1	Width	3	2λ
11.2	Spacing	3	2λ
11.3	POLY I overlap of POLY II	2	λ
11.4	Space to contact	3	2λ

[a]Mask numbers are relative to the process scenario of Table 2B.1. CIF format discussed in footnote of Table 2A.2.
[b]Add 2.5 microns for a source/drain width of 3μ for worst-case mask misalignment.
[c]No contact to poly inside active.
[d]For single metal process, pads are made with metal 1 following design rules 8.3–8.8.
[e]Via must be on a flat surface; metal 1 must be under a via.
[f]There must be metal 2 under the pad openings in a double-metal process.
[g]Objective: Avoidance of too large a step for metal 2.
[h]POLY I must always be under POLY II.

TABLE 2B.3
Graphical interpretation of CMOS design rules.

(See color plate 6 in insert section)

TABLE 2B.4
Process parameters for a typical[a] p-well CMOS process

	Typical	Tolerance[b]	Units
Square law model parameters			
V_{T0} (threshold voltage)			
n-channel (V_{TN0})	0.75	± 0.25	V
p-channel (V_{TP0})	−0.75	± 0.25	V
K'(conduction factor)			
n-channel	24	± 6	$\mu A/V^2$
p-channel	8	± 1.5	$\mu A/V^2$
γ(body effect)			
n-channel	0.8	± 0.4	$V^{1/2}$
p-channel	0.4	± 0.2	$V^{1/2}$
λ(channel length modulation)			
n-channel	0.01	± 50%	V^{-1}
p-channel	0.02	± 50%	V^{-1}
ϕ(surface potential)			
n- and p-channel	0.6	± 0.1	V
Process parameters			
μ (channel mobility)			
n-channel	710		$cm^2/(V \cdot s)$
p-channel	230		$cm^2/(V \cdot s)$
Doping[c]			
n^+ active	5	±4	$10^{18}/cm^3$
p^+ active	5	±4	$10^{17}/cm^3$
p-well	5	±2	$10^{16}/cm^3$
n-substrate	1	±0.1	$10^{16}/cm^3$
Physical feature sizes			
T_{OX} (gate oxide thickness)	500	± 100	Å
Total lateral diffusion			
n-channel	0.45	± 0.15	μ
p-channel	0.6	± 0.3	μ
Diffusion depth			
n^+ diffusion	0.45	± 0.15	μ
p^+ diffusion	0.6	± 0.3	μ
p-well	3.0	± 30%	μ
Insulating layer separation			
POLY I to POLY II	800	± 100	Å
Metal 1 to Substrate	1.55	± 0.15	μ
Metal 1 to Diffusion	0.925	± 0.25	μ
POLY I to Substrate (POLY I on field oxide)	0.75	± 0.1	μ
Metal 1 to POLY I	0.87	± 0.7	μ
Metal 2 to Substrate	2.7	± 0.25	μ
Metal 2 to Metal I	1.2	± 0.1	μ
Metal 2 to POLY I	2.0	± 0.07	μ

Note: $K' = \mu C_{ox}$ $24E-6 \neq (710)(69) \simeq 49.7E-6$

TABLE 2B.4
(Continued)

	Typical	Tolerance[b]	Units
Capacitances[d]			
C_{OX} (gate oxide capacitance, n- and p-channel)	0.7	±0.1	fF/μ^2
POLY I to substrate, poly in field	0.045	±0.01	fF/μ^2
POLY II to substrate, poly in field	0.045	±0.01	fF/μ^2
Metal 1 to substrate, metal in field	0.025	±0.005	fF/μ^2
Metal 2 to substrate, metal in field	0.014	±0.002	fF/μ^2
POLY I to POLY II	0.44	±0.05	fF/μ^2
POLY I to Metal 1	0.04	±0.01	fF/μ^2
POLY I to Metal 2	0.039	±0.003	fF/μ^2
Metal 1 to Metal 2	0.035	±0.01	fF/μ^2
Metal 1 to diffusion	0.04	±0.01	fF/μ^2
Metal 2 to diffusion	0.02	±0.005	fF/μ^2
n^+ diffusion to p-well (junction, bottom)	0.33	±0.17	fF/μ^2
n^+ diffusion sidewall (junction, sidewall)	2.6	±0.6	fF/μ
p^+ diffusion to substrate (junction, bottom)	0.38	±0.12	fF/μ^2
p^+ diffusion sidewall (junction, sidewall)	3.5	±2.0	fF/μ
p-well to substrate (junction, bottom)	0.2	±0.1	fF/μ^2
p-well sidewall (junction, sidewall)	1.6	±1.0	fF/μ
Resistances			
Substrate	25	±20%	Ω-cm
p-well	5000	±2500	Ω/□
n^+ diffusion	35	±25	Ω/□
p^+ diffusion	80	±55	Ω/□
Metal	0.003	±25%	Ω/□
Poly	25	±25%	Ω/□
Metal 1–Metal 2 via (3 μ × 3 μ contact)	<0.1		Ω
Metal 1 contact to POLY I (3 μ × 3 μ contact)	<10		Ω
Metal 1 contact to n^+ or p^+ diffusion (3 μ × 3 μ contact)	<5		Ω
Breakdown voltages, leakage currents, migration currents and operating conditions			
Punchthrough voltages (Gate oxide, POLY I to POLY II)	>10		V
Diffusion reverse breakdown voltage	>10		V
p-well to substrate reverse breakdown voltage	>20		V
Metal 1 in field threshold voltage	>10		V
Metal 2 in field threshold voltage	>10		V
Poly-field threshold voltage	>10		V
Maximum operating voltage	7.0		V
n^+ diffusion to p-well leakage current	0.25		fA/μ^2
p^+ diffusion to substrate leakage current	0.25		fA/μ^2
p-well leakage current	0.25		fA/μ^2
Maximum metal current density	0.8		mA/μ width
Maximum device operating temperature	200		°C

[a] Parameters based upon a 3μ ($\lambda = 1.5\mu$) CMOS process.

[b] The tolerance is in terms of the absolute value of the parameter relative to processing variations from run to run. Matching characteristics on a die are much better. For example, chip-level matching of V_{T0} is in the 1 mV to 20 mV range, and K′ matching is in the 0.5% to 5% range.[18–22]

[c] Impurity concentration varies with depth.

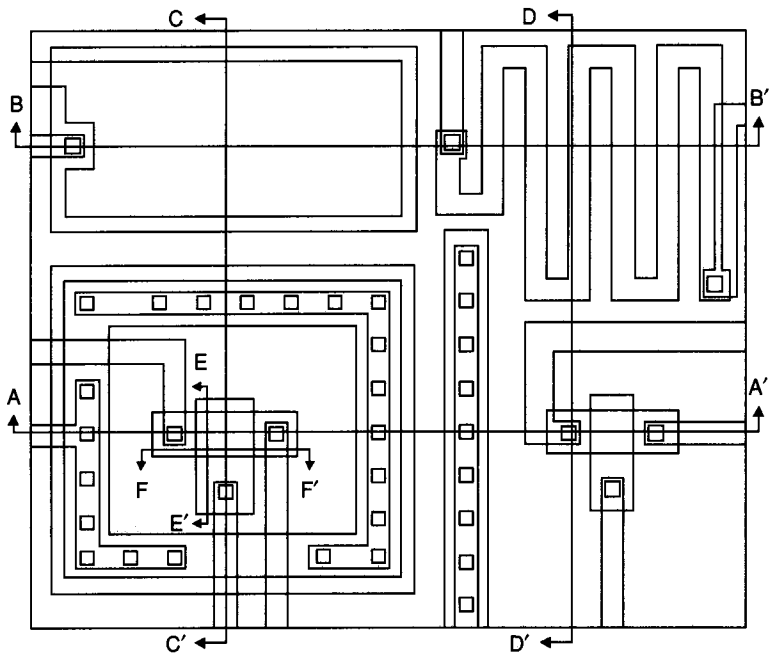
[d] Junction capacitances at zero bias.

TABLE 2B.5
SPICE MOSFET model parameters of a typical p-well CMOS process (MOSIS[a])

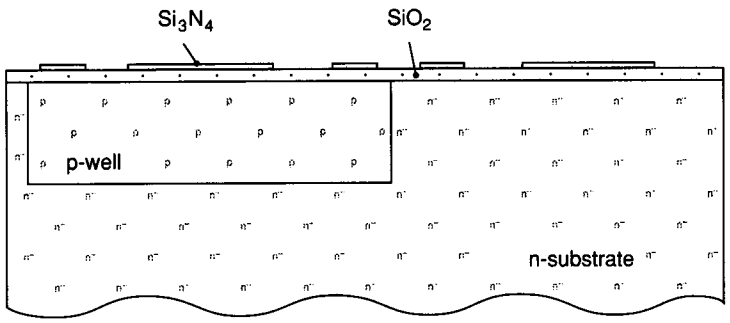
Parameter (Level 2 model)	n-channel	p-channel	Units
VTO	0.827	−0.895	V
KP	32.87	15.26	$\mu A/V^2$
GAMMA	1.36	0.879	$V^{1/2}$
PHI	0.6	0.6	V
LAMBDA	1.605E−2	4.709E−2	V^{-1}
CGSO	5.2E−4	4.0E−4	fF/μ width
CGDO	5.2E−4	4.0E−4	fF/μ width
RSH	25	95	$\Omega/\square$
CJ	3.2E−4	2.0E−4	p/fF/μ^2
MJ	0.5	0.5	
CJSW	9.0E−4	4.5E−4	p/fF/μ perimeter
MJSW	0.33	0.33	
TOX	500	500	Å
NSUB	1.0E16	1.12E14	$1/cm^3$
NSS	0	0	$1/cm^2$
NFS	1.235E12	8.79E11	$1/cm^2$
TPG	1	−1	
XJ	0.4	0.4	μ
LD	0.28	0.28	μ
UO	200	100	$cm^2/(V \cdot s)$
UCRIT	9.99E5	1.64E4	V/cm
UEXP	1.001E−3	0.1534	
VMAX	1.0E5	1.0E5	m/s
NEFF	1.001E−2	1.001E−2	
DELTA	1.2405	1.938	

verify units before final corrections

[a] The SPICE parameters were obtained by assuming them to be empirical parameters and then fitting measured device characteristics to the mathematical equations which comprise the model by using a numerical optimization algorithm. This approach gives good fit to the model but causes a deviation from the typical parameters of Table 2A.4 and results in parameter relationships which may not be self-consistent with some of the fundamental relationships developed in Chapters 3 and 4.



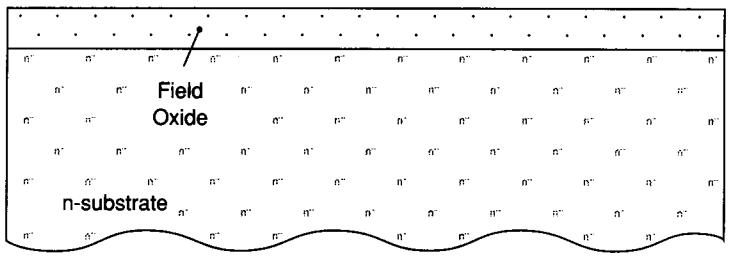
(*a*) Top View (color version appears in plate 3)



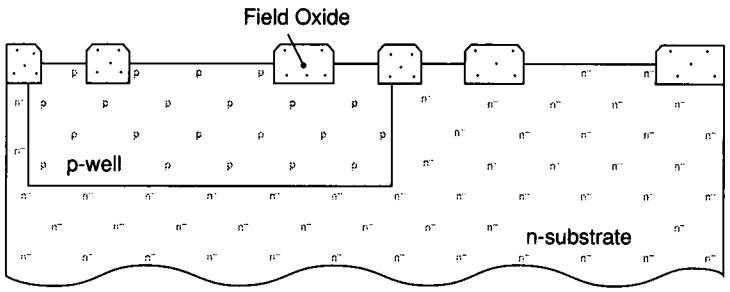
A-A′ Following Moat Patterning

(*b*)

FIGURE 2B.1
Process description for the CMOS process.

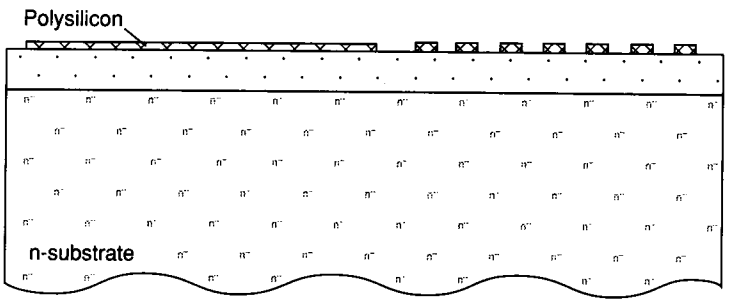


B-B Following Field Oxide Growth

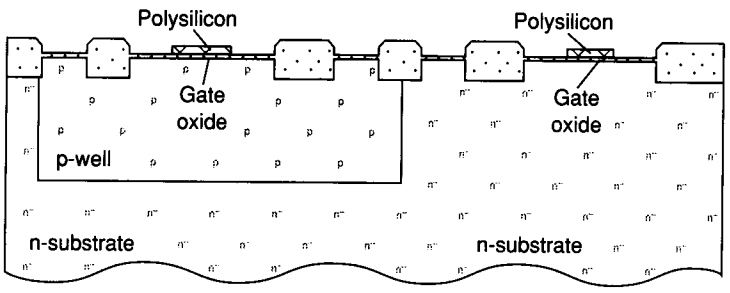


A-A′ Following Field Oxide Growth

(*c*)



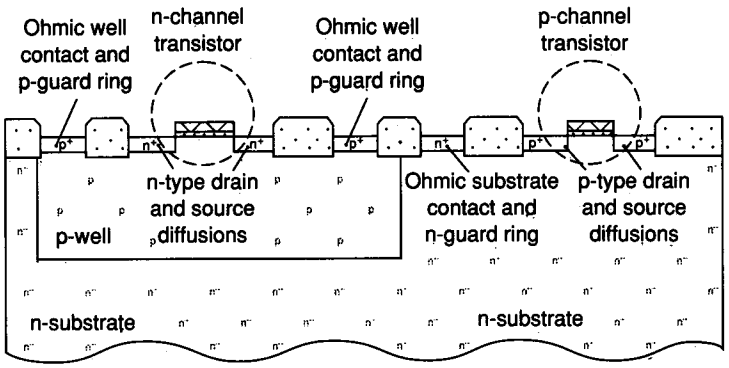
B-B′ Following Polysilicon Patterning



A-A′ Following Polysilicon Patterning

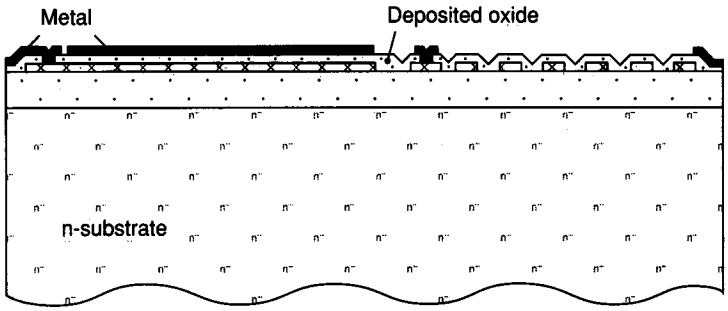
(*d*)

FIGURE 2B.1
(Continued)

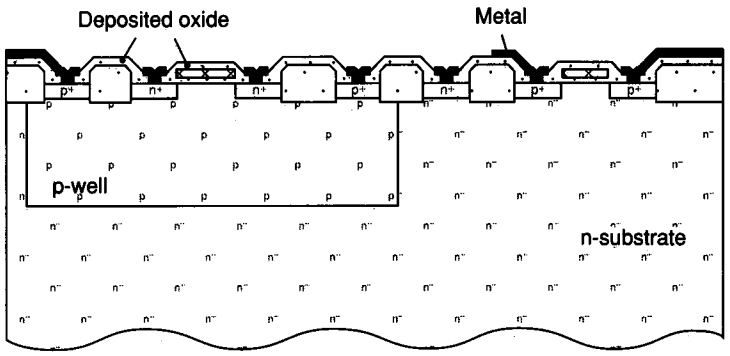


A-A′ Following p+ and n+ Diffusions

(*e*)



B-B′ Following Metal Patterning



A-A′ Following Metal Patterning

(*f*)

FIGURE 2B.1
(Continued)

APPENDIX 2C
PROCESS CHARACTERIZATION OF A GENERIC BIPOLAR PROCESS

TABLE 2C.1
Process scenario of major process steps in typical bipolar process[a]

1.	Clean wafer (p-type)	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n^+ BURIED LAYER	(MASK #1)
5.	Develop photoresist	
6.	DEPOSITION AND DIFFUSION OF n-BURIED LAYER	
7.	Strip photoresist	
8.	Strip oxide	
9.	GROW EPITAXIAL LAYER (n-type)	
10.	Grow oxide	
11.	Apply photoresist	
12.	PATTERN p^+ ISOLATION REGIONS	(MASK #2)
13.	Develop photoresist	
14.	Etch oxide	
15.	DEPOSITION AND DIFFUSION OF p^+ ISOLATION	
16.	Strip photoresist	
17.	Grow oxide	
	Optional high-resistance p-diffusion	
	A.1 Apply photoresist	
	A.2 PATTERN p-RESISTORS	(MASK #A)
	A.3 Develop photoresist	
	A.4 Etch oxide	
	A.5 DEPOSITION AND DIFFUSION OF p-RESISTORS	
	A.6 Strip photoresist	
	A.7 Grow oxide	
18.	Apply photoresist	
19.	PATTERN BASE REGIONS	(MASK #3)
20.	Develop photoresist	
21.	Etch oxide	
22.	DEPOSITION AND DIFFUSION OF p-TYPE BASE	
23.	Strip photoresist	
24.	Grow oxide	
25.	Apply photoresist	
26.	PATTERN n-TYPE EMITTER REGIONS	(MASK #4)
27.	Develop photoresist	
28.	Etch Oxide	
29.	n^+ DEPOSITION AND DIFFUSION	
30.	Strip photoresist	
31.	Grow oxide	
32.	Apply photoresist	
33.	PATTERN CONTACT OPENINGS	(MASK #5)
34.	Develop photoresist	
35.	Etch oxide	
36.	Strip Photoresist	
37.	APPLY METAL	
38.	Apply photoresist	
39.	PATTERN METAL	(MASK #6)

TABLE 2C.1
(Continued)

40.	Develop photoresist	
41.	ETCH METAL	
42.	Strip photoresist	
43.	APPLY PASSIVATION	
44.	Apply photoresist	
45.	PATTERN PAD OPENINGS	(MASK #7)
46.	Develop photoresist	
47.	Etch passivation	
48.	Strip photoresist	
49.	ASSEMBLE, PACKAGE, AND TEST	

[a]Major functional steps shown in capital letters.

TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5\ \mu$)
(See Table 2C.3 in color plates for graphical interpretation)

	Dimension
1. n^+ buried collector diffusion (Yellow, Mask #1)	
1.1 Width	3λ
1.2 Overlap of p-base diffusion (for vertical npn)	2λ
1.3 Overlap of n^+ emitter diffusion (for collector contact of vertical npn)	2λ
1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp)	2λ
1.5 Overlap of n^+ emitter diffusion (for base contact of lateral pnp)	2λ
2. Isolation diffusion (Orange, Mask #2)	
2.1 Width	4λ
2.2 Spacing	24λ
2.3 Distance to n^+ buried collector	14λ
3. p-base diffusion (Brown, Mask #3)	
3.1 Width	3λ
3.2 Spacing	5λ
3.3 Distance to isolation diffusion	14λ
3.4 Width (resistor)	3λ
3.5 Spacing (as resistor)	3λ
4. n^+ emitter diffusion (Green, Mask #4)	
4.1 Width	3λ
4.2 Spacing	3λ
4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
4.4 Spacing to isolation diffusion (for collector contact)	12λ
4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ
5. Contact (Black, Mask #5)	
5.1 Size (exactly)	$4\lambda \times 4\lambda$
5.2 Spacing	2λ
5.3 Metal overlap of contact	λ
5.4 n^+ emitter diffusion overlap of contact	2λ
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
5.7 Spacing to isolation diffusion	4λ

TABLE 2C.2
(Continued)

	Dimension
6. Metalization (Blue, Mask #6)	
6.1 Width	2λ
6.2 Spacing	2λ
6.3 Bonding pad size	100 μ × 100 μ
6.4 Probe pad size	75 μ × 75 μ
6.5 Bonding pad separation	50 μ
6.6 Bonding to probe pad	30 μ
6.7 Probe pad separation	30 μ
6.8 Pad to circuitry	40 μ
6.9 Maximum current density	0.8 mA/μ width
7. Passivation (Purple, Mask #7)	
7.1 Minimum bonding pad opening	90 μ × 90 μ
7.2 Minimum probe pad opening	65 μ × 65 μ

TABLE 2C.3
Graphical interpretation of bipolar design rules.

(See color plate 7 in insert section)

TABLE 2C.4
Process parameters for a typical bipolar process[a]

Parameter	Typical	Tolerance[b]	Units
Ebers-Moll model parameters			
β_F (forward β)			
npn—vertical	100	50 to 200	
pnp—lateral			
(at I_C = 500 μA)	10	±20%	
(at I_C = 200 μA)	6	±20%	
β_R (reverse β)			
npn—vertical	1.5	±0.5	
pnp—lateral			
(at I_C = 500 μA)	5	±20%	
(at I_C = 200 μA)	3	±20%	
V_{AF} (forward Early voltage)			
npn—vertical	100	±30%	V
pnp—lateral	150	±30%	V
V_{AR} (reverse Early voltage)			
npn—vertical	150	±30%	V
pnp—lateral	150	±30%	V
J_S (saturation current density)			
npn—vertical	2.6×10^{-7}	−50%to + 100%	pA/μ^2
pnp—lateral	1.3×10^{-5}	−50%to + 100%	pA/μ emitter perimeter

TABLE 2C.4
(Continued)

Parameter	Typical	Tolerance[b]	Units
	Doping		
n^+ emitter	10^4	±30%	$10^{16}/cm^3$
p-base			
Surface	10^5	±20%	$10^{16}/cm^3$
Junction	1	±20%	$10^{16}/cm^3$
Epitaxial layer	0.3	±20%	$10^{16}/cm^3$
Substrate	0.08	±25%	$10^{16}/cm^3$
	Physical feature size		
Diffusion depth			
n+ emitter diffusion	1.3	±5%	μ
p-base diffusion	2.6	±5%	μ
p-resistive diffusion	0.3	±5%	μ
n-epitaxial layer	10.4	±5%	μ
n^+buried collector diffusion			
Into epitaxial	3.9	±5%	μ
Into substrate	7.8	±5%	μ
Oxide thickness			
Metal to epitaxial	1.4	±30%	μ
Metal to p-base	0.65	±30%	μ
Metal to n^+ emitter	0.4	±30%	μ
	Capacitances		
Metal to epitaxial	0.022	±30%	fF/μ^2
Metal to p-base diffusion	0.045	±30%	fF/μ^2
Metal to n^+ emitter diffusion	0.078	±30%	fF/μ^2
n^+ buried collector to substrate (junction, bottom)	0.062	±30%	fF/μ^2
Epitaxial to substrate (junction, bottom)	0.062	±30%	fF/μ^2
Epitaxial to substrate (junction, sidewall)	1.6	±30%	fF/μ perimeter
Epitaxial to p-base diffusion (junction, bottom)	0.14	±30%	fF/μ^2
Epitaxial to p-base diffusion (junction, sidewall)	7.9	±30%	fF/μ perimeter
p-base diffusion to n^+ emitter diffusion (junction, bottom)	0.78	±30%	fF/μ^2
p-base diffusion to n^+ emitter diffusion (junction, sidewall)	3.1	±30%	fF/μ perimeter

TABLE 2C.4
(Continued)

Parameter	Typical	Tolerance[b]	Units
Resistance and resistivity			
Substrate resistivity	16	±25%	Ω · cm
n^+ buried collector diffusion	17	±35%	Ω / □
Epitaxial layer	1.6	±20%	Ω · cm
p-base diffusion	160	±20%	Ω / □
p-resistive diffusion (optional)	1500	±40%	Ω / □
n^+ emitter diffusion	4.5	±30%	Ω / □
Metal	0.003		Ω / □
Contacts ($3\mu \times 3\mu$)	<4		Ω
Metal-n^+ emitter (contact plus series resistance to BE junction)	<1		Ω
Metal-p-base[c] (contact plus series resistance)	70		Ω
Metal-Epitaxial[d] (contact plus series resistance to BC junction)	120		Ω
Breakdown voltages, leakage currents, migration currents, and operating conditions			
Reverse breakdown voltages			
n^+ emitter to p-base	6.9	±50 mV	V
p-base to epitaxial	70	±10	V
Epitaxial to substrate	>80		V
Maximum operating voltage	40		V
Substrate leakage current	0.16		fA/μ^2
Maximum metal current density	0.8		mA/μ width
Maximum device operating temperature (design)	125		°C
Maximum device operating temperature (physical)	225		°C

[a] Process parameters based on the process of Tables 2C.1 and 2C.2.

[b] The tolerance is in terms of the absolute value of the parameter relating to processing variation from run to run. Matching characteristics on a die are much better. For example, β_F matching for identical devices on the same die to ±5% and J_S matching to ±5% are achievable.

[c] The base series resistance is strongly dependent on layout. Value given is for double base contact.

[d] The collector series resistance is strongly layout-dependent. It is primarily dependent on the vertical distance between contact and buried layer and buried layer to base.

TABLE 2C.5
SPICE model parameters of typical bipolar process

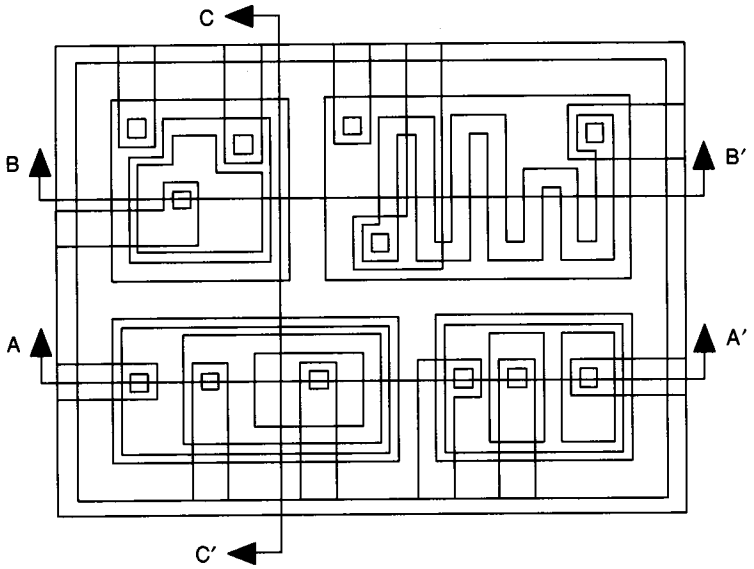
Parameter[a,b,c]	Vertical npn	Lateral pnp	Units
IS[c]	0.1	0.78	fA
BF	80	225	
NF	1	1	
VAF	100	150	V
IKF	100	0.1	mA
ISE	0.11	0.15	fA
NE	1.44	1.28	
BR	1.5		
NR	1	1	
VAR[b]	19	38	V
ISC		1.5	fA
NC	1.44	1.28	
RB	70	250	Ω
RE	1	4	Ω
RC	120	130	Ω
CJE	0.62	0.48	pF
VTE	0.69	0.65	V
MJE	0.33	0.40	
TF	0.45	40	ns
CJC	1.9	0.48	pF
VJC	0.65	0.65	V
MJC	0.4	0.4	
XCJC	0.5	0	
TR	22.5	2000	ns
CJS[d]	1.30	0	pF
VJS	0.49	0	pF
MJS	0.38	0	

[a] Parameters are defined in Chapters 3 and 4.

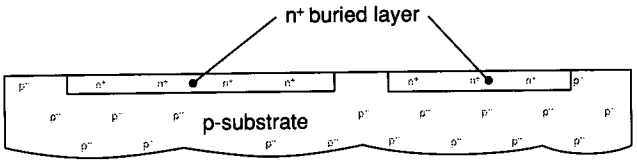
[b] Some of these Gummel-Poon parameters differ considerably from those given in Table 2C.4. They have been obtained from curve fitting and should give good results with computer simulations. The parameters of Table 2C.4 should be used for hand analysis.

[c] Parameters that are strongly area-dependent are based upon an npn emitter area of 390 μ^2 and perimeter of 80 μ, a base area of 2200 μ^2 and perimeter of 200 μ, and a collector area of 10,500 μ^2 and perimeter of 425 μ. The lateral pnp has rectangular collectors and emitters spaced 10 μ apart with areas of 230 μ^2 and perimeters of 60 μ. The base area of the pnp is 7400 μ^2 and the base perimeter is 345 μ.

[d] CJS is set to zero for the lateral transistor because it is essentially nonexistent. The parasitic capacitance from base to substrate, which totals 1.0 pF for this device, must be added externally to the BJT.

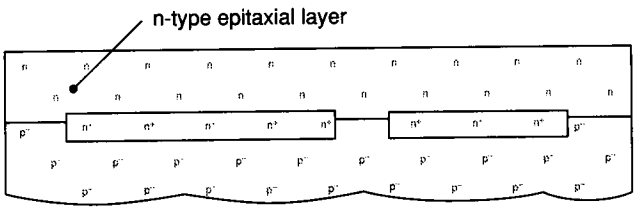


(*a*) Top View of Bipolar Die[a] (color version appears in Plate 4)



A-A′ Following Fabrication of Buried Layer

(*b*)

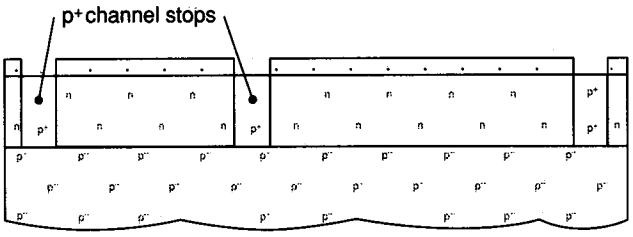


A-A′ Following Epitaxy

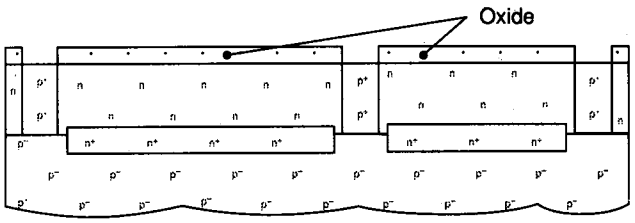
(*c*)

FIGURE 2C.1
Process description for the bipolar process.

[a] The base-emitter junction which must be reversed biased forms the capacitor in the upper left. A p-base diffused resistor is in the upper right. The vertical npn transistor and lateral pnp appear in the lower left and lower right respectively.

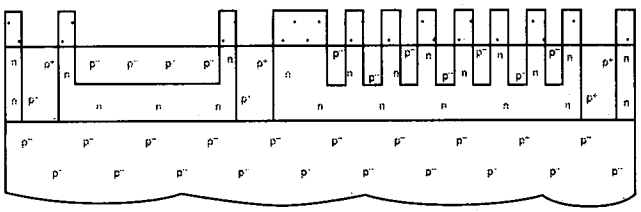


B-B′ Following Isolation Diffusion

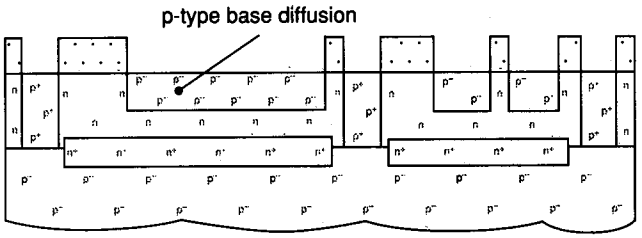


A-A′ Following Isolation Diffusion

(*d*)



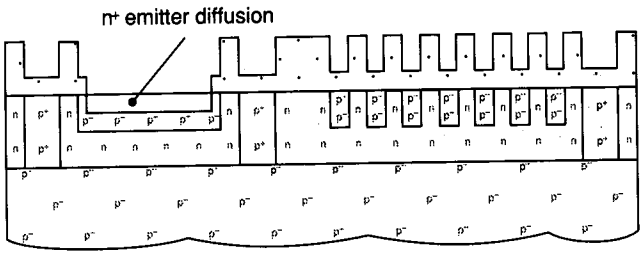
B-B′ Following p-type Base Diffusion



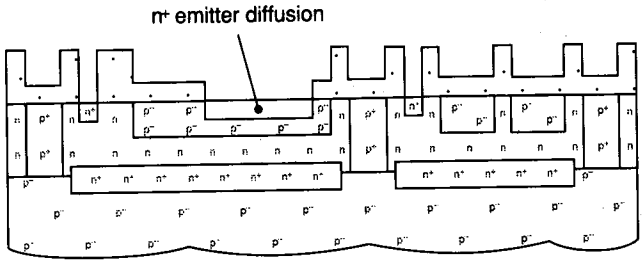
A-A′ Following p-type Base Diffusion

(*e*)

FIGURE 2C.1
(Continued)

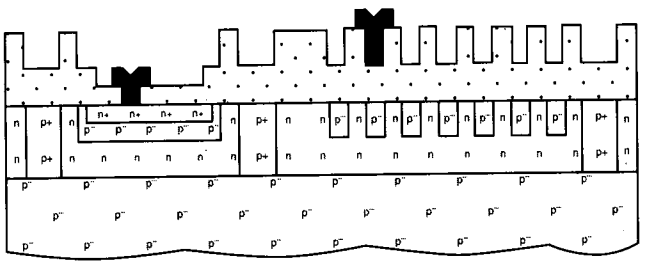


B-B′ Following n+ Emitter Diffusion

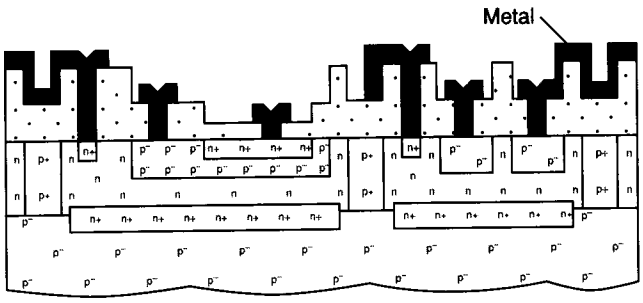


A-A′ Following n+Emitter Diffusion

(*f*)



B-B′ Following Metallization



A-A′ Following Metallization

(*g*)

FIGURE 2C.1
(Continued)

APPENDIX 2D
PROCESS CHARACTERIZATION OF A GENERIC THICK FILM PROCESS

TABLE 2D.1
Process scenario of major process steps in typical thick film process

1. Screen conductor material	(Screen 1)
2. Fire conductor material	
3. Screen resistive layer 1	(Screen 2)
4. Screen resistive layer 2	(Screen 3)
5. Screen resistive layer 3	(Screen 4)
6. Screen dielectric—first pass	(Screen 5)
7. Fire dielectric	
8. Screen dielectric—second pass	(Screen 6)
9. Fire dielectric	
10. Screen second conductor	(Screen 7)
11. Fire circuit	

TABLE 2D.2
Design rules for a typical thick film process

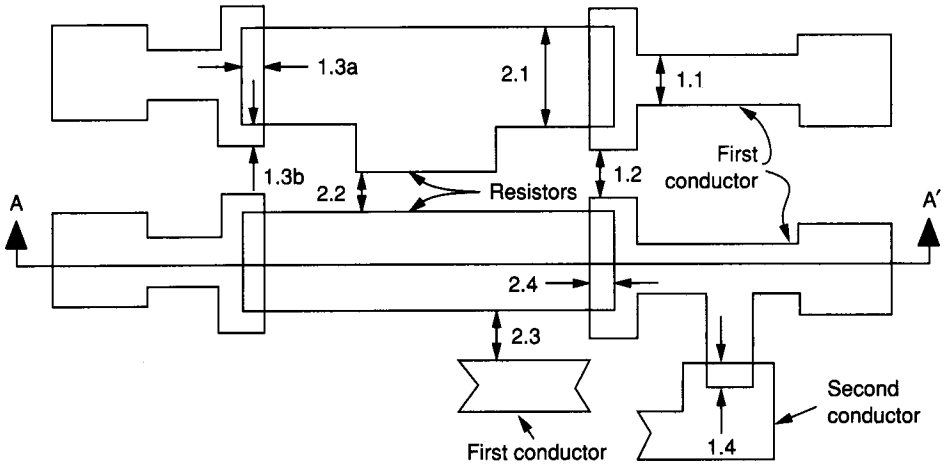
	Minimum dimension[a]
1. Conductor	
1.1 Width	2λ
1.2 Spacing	2λ
1.3 Metal larger than contacting resistor	
1.3*a* In direction of resistor	λ
1.3*b* Perpendicular to resistor	λ
1.4 Overlap of second contacting conductor	λ
1.5 Spacing to edge of substrate	2λ
2. Resistors	
2.1 Width or length	5λ
2.2 Spacing (same or different screenings)	2λ
2.3 Spacing to unconnected conductor	2λ
2.4 Overlap of conductor	λ
2.5 Spacing to resistor or conductor in trim region	
2.5*a* For laser trims	λ
2.5*b* For abrasive trims	4λ
2.6 Spacing to edge of substrate	2λ
3. Dielectric	
3.1 Dielectric larger than upper conductor (on top of lower conductor)	λ
4. Pad size	4λ

[a] λ is typically around 250 μ. Design rules depicted graphically in Fig. 2D.1.

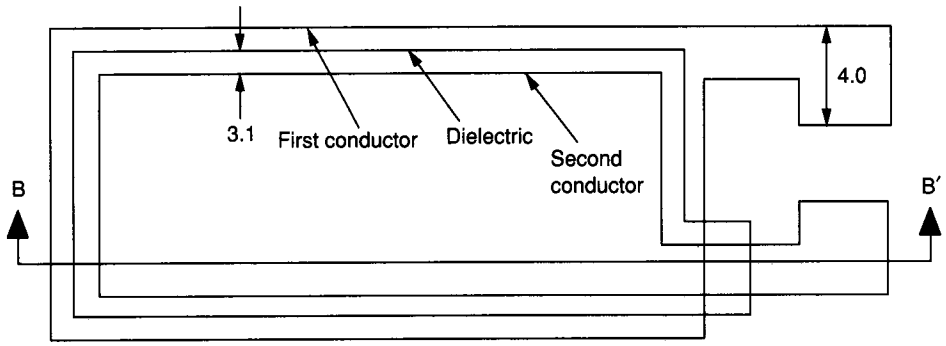
TABLE 2D.3
Process parameters for a typical thick film process

Parameter	Typical	Tolerance	Units
Conductor sheet resistance (after firing)	0.5	±40%	Ω/□
First resistor sheet resistance (after firing)	100	±30%	Ω/□
Second resistor sheet resistance (after firing)	1000	±30%	Ω/□
Third resistor sheet resistance (after firing)	10,000	±30%	Ω/□
Screen mesh size	200		per inch
Thickness after firing (resistors and conductors)	20	±20%	μ
Dielectric thickness	40	±30%	μ
Capacitance density[a]	0.8	±40%	pF/cm^2
TCR_1	−150	±20%	ppm/°C
TCR_2	+50	±20%	ppm/°C
TCR_3	200	±20%	ppm/°C
TCC	10	±10%	ppm/°C
VCR (all resistors)	≤ 60		ppm/V

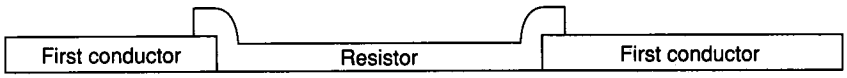
[a] The capacitance density is strongly a function of the characteristics of the material used for the dielectric.



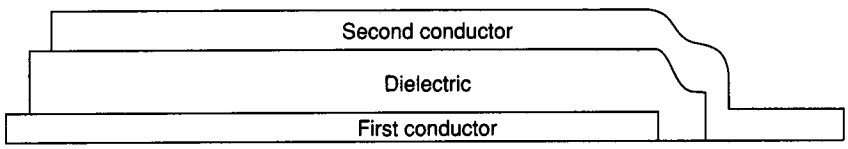
(*a*) Top view



(*b*) Top view



(*c*) Cross section A-A′



(*d*) Cross section B-B′

FIGURE 2D.1
Process description for the thick film process.

APPENDIX 2E
PROCESS CHARACTERIZATION OF A GENERIC THIN FILM PROCESS

TABLE 2E.1
Process scenario of major process steps in a typical resistive thin film process

1. Deposit resistive film	
2. Deposit conductive film	
3. Apply photoresist and pattern conductor	(Mask #1)
4. Etch conductor	
5. Apply photoresist and pattern resistor (and conductor)	(Mask #2)
6. Etch resistor	
7. Apply passivation	
8. Apply photoresist and pattern pad openings	(Mask #3)

TABLE 2E.2
Design rules for a typical thin film process

	Minimum dimensions
1. Conductor	
1.1 Width	200 μ
1.2 Spacing	200 μ
2. Resistor	
2.1 Width	20 μ
2.2 Spacing	20 μ
2.3 Spacing to conductor	200 μ
3. Pads	
3.1 Pad size	200 $\mu \times$ 200 μ
3.2 Passivation	180 $\mu \times$ 180 μ

Note: Design rules depicted graphically in Fig. 2E.1.

TABLE 2E.3
Process parameters for a typical thin film process

Parameter	Typical	Tolerance	Units
Conductor sheet resistance	0.25	±20%	Ω/□
Resistor sheet resistance	100	±20%	Ω/□
Temperature coefficient of resistance	100		ppm/°C
Voltage coefficient of resistance	5		ppm/V/mm length
Resistor matching (untrimmed)	±5%		
Conductor film thickness	1000		Å
Resistor film thickness	1000		Å

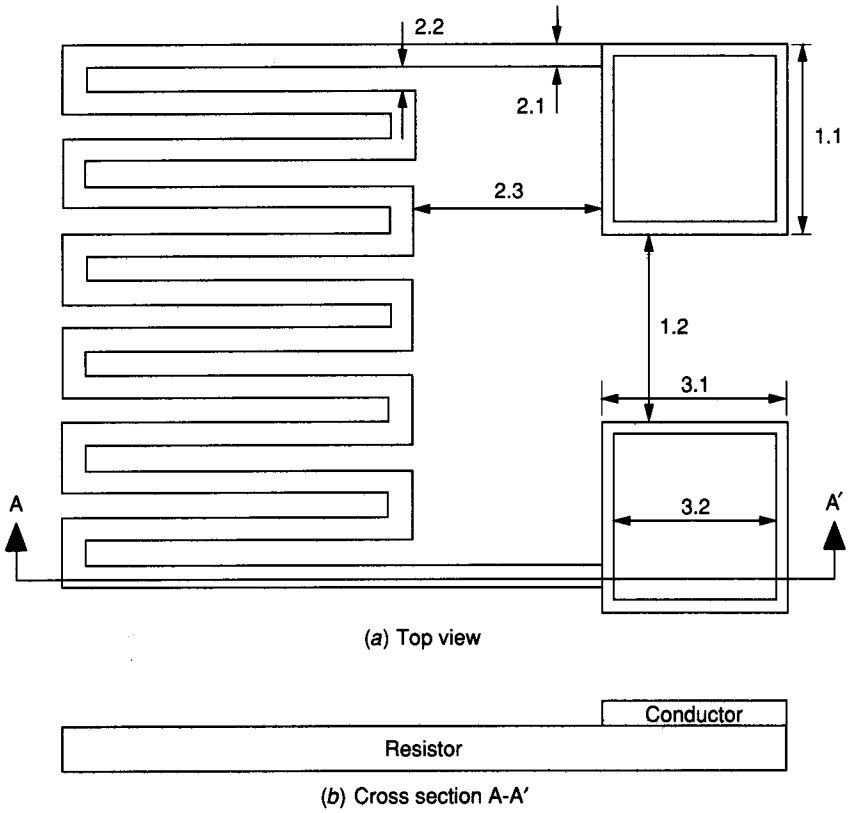


FIGURE 2E.1
Process description for the thin film process.