is often adequate for biasing applications and operating point calculations when the device is operating in the forward active region. In the reverse active region the simplified model becomes

$$V_{BC} = 0.6 \text{ V} \tag{3.3-25}$$

$$I_E = \beta_R I_B \tag{3.3-26}$$

The reader should be cautioned, however, not to attempt to use the value of V_{BE} or V_{BC} as given by (3.3-23) or (3.3-25) directly in the Ebers-Moll equations to obtain I_C or I_B. Small errors in these junction voltages will result in large errors in the currents because of the exponential relationship of the model.

SATURATION REGION. It will be seen later that most (although not all) digital applications involve switching the BJT between the saturation and cutoff regions. When the device is operating in the saturation region with large positive base and collector currents, it is operating near the forward active region. The base–emitter voltage will be near 0.7 V and the base–collector voltage near 0.5 V. The device can thus be modeled by two voltage sources, $V_{BE} = 0.7$ V and $V_{CE} = 0.2$ V, when operating in this region. This collector–emitter voltage in saturation is often termed V_{CESAT}. When the device is operating in saturation with a large positive base current and a large negative collector current, the device is operating near the reverse active region. The base–collector voltage will be near 0.7 V and the base–emitter voltage near 0.5 V. In this case the device will be modeled by two voltage sources, $V_{BC} = 0.7$ V and $V_{CE} = -0.2$ V. This simple modeling approach for the saturation region will be adequate for most hand manipulations. The reader again must be cautioned that these are approximate junction voltage values and thus cannot be used to obtain I_C and I_E in the Ebers-Moll equations since small changes or errors in V_{BC} and V_{BE} cause large changes in the corresponding currents. When the collector and base currents must be accurately determined for devices operating in the saturation region, they are often obtained from equations describing the network itself (KVL or KCL) rather than directly from the Ebers-Moll equations. This situation is illustrated in the following example.

Example 3.3-2. Determine good approximations (± 5% accuracy is close enough) for the base current, collector current, V_{BE}, and V_{CE} for the circuit of Fig. 3.3-4

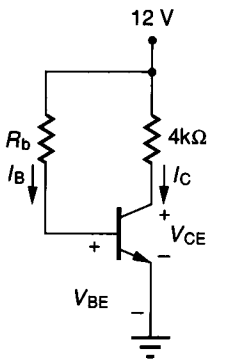


FIGURE 3.3-4
Example 3.3-2.

if (*a*) $R_b = 500\ \text{k}\Omega$, (*b*) $R_b = 100\ \text{k}\Omega$. Also obtain an accurate expression for V_{BE}. Assume the transistor has an emitter area of 4 mil^2, $\beta_F = 100$, $\beta_R = 0.2$, $J_S = 6 \times 10^{-10}\ \mu\text{A/mil}^2$, and $T = 300\ ^\circ\text{K}$.

Solution. Assume initially that I_B is in the 0.1 μA to 1 mA range. From Example 3.3-1 it can be concluded that $V_{BE} \simeq 0.6$ V and consequently the current through R_b, which is also the base current, can be approximated by $I_b \simeq (11.4\ \text{V})/R_b$.

(*a*) With $R_b = 500\ \text{k}\Omega$, it follows that $I_B \simeq 0.0228$ mA, which satisfies the criterion established in Example 3.3-1 on I_B and thus justifies the initial assumption $V_{BE} \simeq 0.6$ V. If it is now assumed (a fact that must later be verified) that the device is operating in the forward active region, it follows from (3.3-15) that $I_C \simeq 2.28$ mA. With $I_C \simeq 2.28$ mA it follows that $V_{CE} = 12 - (4\ \text{k}\Omega)(2.28\ \text{mA}) = 2.88$ V. With V_{BE} in the 0.6 V range, it thus can be concluded that $V_{BC} < 0$, thus verifying the initial assumption of operation in the forward active region. It remains to accurately determine V_{BE}. Since I_C is now approximately known, it follows from (3.3-13) with $V_t = 26$ mV that

$$V_{BE} = (.026\ \text{V})\ln(I_C/I_S)$$

$$= (.026\ \text{V})\ln[2.28\ \text{mA}/(6 \times 10^{-10} \cdot 4\ \mu\text{A})] = 0.717\ \text{V}$$

(*b*) With $R_b = 100\ \text{k}\Omega$, it follows that $I_B \simeq (11.4\ \text{V})/(100\ \text{k}\Omega) = 0.114$ mA. If we were to assume, as in part (*a*), that the transistor were operating in the forward active region, we would conclude that $I_C = 11.4$ mA. Consequently, $V_{CE} = -33.6$ V, yielding a value for V_{BC} of 34.2 V, which is in strong violation of the assumption $V_{BC} < 0.3$ V that was necessary to obtain (3.3-15). It can thus be concluded that the collector current is too large for operation in the forward active region and thus the device is operating in saturation near the forward active region. From the above modeling in the saturation region it can be concluded that

$$V_{BE} \simeq 0.7\ \text{V}$$

$$I_B \simeq \frac{12\ \text{V} - 0.7\ \text{V}}{100\ \text{k}\Omega} = 0.113\ \text{mA}$$

$$V_{CE} \simeq 0.2\ \text{V}$$

$$I_C \simeq \frac{12\ \text{V} - 0.2\ \text{V}}{4\ \text{k}\Omega} = 2.95\ \text{mA}$$

CUTOFF. When the BJT is operating in cutoff, the collector and base currents are very small compared to those which typically flow in the active and saturation regions. In many applications it is adequate to model the device with $I_C = 0$ and $I_B = 0$ when operating in the cutoff region. The relative magnitude of the currents in the BJT when operating in cutoff to those when operating in the forward active region are shown in Example 3.3-3.

BJT MODEL SUMMARY. A summary of the simplified dc model for the BJT in the four major regions of operation—forward active, reverse active, saturation, and cutoff—appears in Table 3.3-2. This simplified model should be adequate for most hand calculations except in the seldom used transition region (between cutoff and forward or reverse active) indicated by the lightly shaded region in

TABLE 3.3-2
Simplified dc model for bipolar transistors

npn			
$I_C = J_S A e^{(V_{BE}/V_t)}[1 + (V_{CE}/V_{AF})]$	(1)	Forward active	$V_{BE} > 0.5$ V
$I_B = \frac{J_S}{\beta_F} A e^{(V_{BE}/V_t)}$	(2)		$V_{BC} < 0.3$ V
$I_E = J_S A e^{(V_{BC}/V_t)}[1 - (V_{CE}/V_{AR})]$	(3)	Reverse active	$V_{BC} > 0.5$ V
$I_B = \frac{J_S}{\beta_R} A e^{(V_{BC}/V_t)}$	(4)		$V_{BE} < 0.3$ V
$I_B = I_C = 0$	(5)	Cutoff	$(V_{CE} < 0, V_{BC} < 0)$
$V_{BE} = 0.7$ V, $V_{CE} = 0.2$ V	(6)	Forward saturated	
$V_{BC} = 0.7$ V, $V_{CE} = -0.2$ V	(7)	Reverse saturated	
pnp			
$I_C = -J_S A e^{-(V_{BE}/V_t)}[1 - (V_{CE}/V_{AF})]$	(8)	Forward active	$V_{BE} < -0.5$ V
$I_B = -\frac{J_S A}{\beta_F} e^{-(V_{BE}/V_t)}$	(9)		$V_{BC} > -0.3$ V
$I_E = -J_S A e^{-(V_{BC}/V_t)}[1 + (V_{CE}/V_{AR})]$	(10)	Reverse active	$V_{BC} < -0.5$ V
$I_B = -\frac{J_S A}{\beta_R} e^{-(V_{BC}/V_t)}$	(11)		$V_{BE} > -0.3$ V
$I_B = I_C = 0$	(12)	Cutoff	$(V_{CE} > 0, V_{BC} > 0)$
$V_{BE} = -0.7$ V, $V_{CE} = -0.2$ V	(13)	Forward saturated	
$V_{BC} = -0.7$ V, $V_{CE} = +0.2$ V	(14)	Reverse saturated	

Design parameters: A
Process parameters: $J_S, \beta_F, \beta_R, V_{AR}, V_{AF}$
Environmental parameter: V_t
All design, process, and environmental parameters are positive for both npn and pnp transistors.

Fig. 3.3-3. For operation in this transition region, the more complicated Ebers-Moll equations 3.3-1 and 3.3-2 are needed.

For biasing or operating point calculations, an even simpler model is often adequate. This model is summarized in Table 3.3-3. An equivalent circuit appears in Fig. 3.3-5. This model can be used in place of the model of Table 3.3-2 to reduce computational complexity with minimal loss of accuracy in most biasing applications. This simplified model is generally justified if the base current can be reasonably accurately determined from the circuit in which the BJT is embedded (as in Example 3.3-2) rather than from the exponential relationship between I_B and V_{BE} (as in Problem 3.38*b*).

Early voltage effects can be readily included in the Ebers-Moll equations 3.3-1 and 3.3-2 by multiplying I_C by $(1 + V_{CE}/V_{AF})$ for $V_{CE} > 0$ or multiplying I_E by $(1 - V_{CE}/V_{AR})$ for $V_{CE} < 0$. Since the BJT is inherently a good current amplifier, it is common to look at the collector current versus V_{CE} for different

TABLE 3.3-3
Simplified model of BJT used for biasing and operating point calculations

Region	npn		pnp	
Forward active	$I_C = \beta_F I_B$	(1)	$I_C = \beta_F I_B$	(11)
	$V_{BE} = 0.6$ V	(2)	$V_{BE} = -0.6$ V	(12)
Reverse active	$I_E = \beta_R I_B$	(3)	$I_E = \beta_R I_B$	(13)
	$V_{BC} = 0.6$ V	(4)	$V_{BC} = -0.6$ V	(14)
Forward saturated	$V_{BE} = 0.7$ V	(5)	$V_{BE} = -0.7$ V	(15)
	$V_{CE} = 0.2$ V	(6)	$V_{CE} = -0.2$ V	(16)
Reverse saturated	$V_{BC} = 0.7$ V	(7)	$V_{BC} = -0.7$ V	(17)
	$V_{CE} = -0.2$ V	(8)	$V_{CE} = 0.2$ V	(18)
Cutoff	$I_C = 0$	(9)	$I_C = 0$	(19)
	$I_B = 0$	(10)	$I_B = 0$	(20)

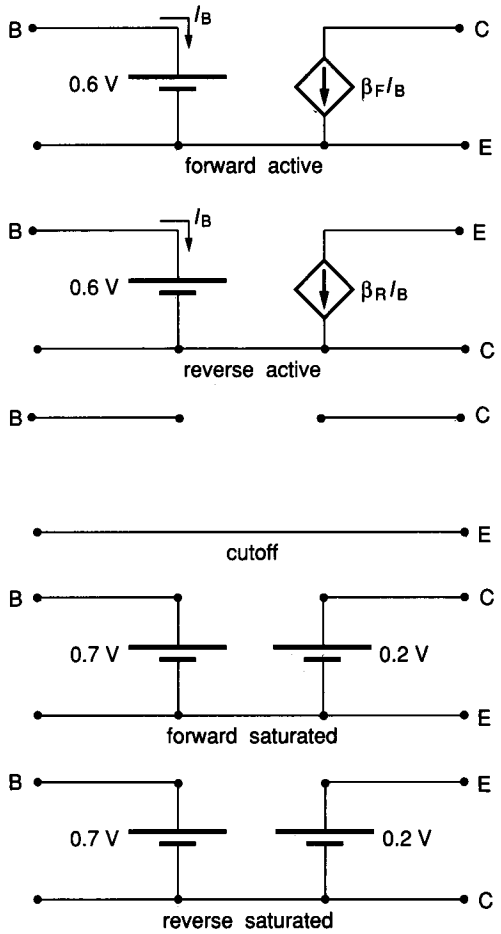


FIGURE 3.3-5
Equivalent circuits of npn BJT for biasing and operating point calculations.

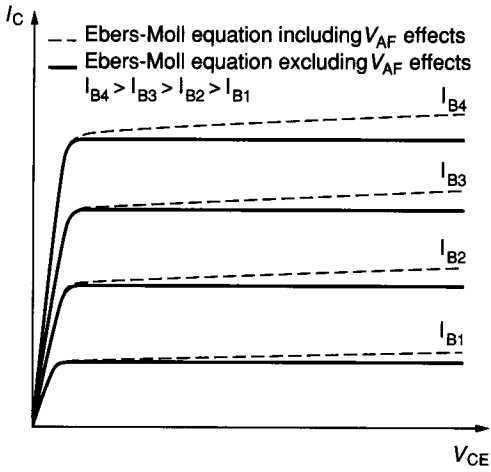


FIGURE 3.3-6
Typical output characteristics of npn BJT based upon Ebers-Moll model.

values of the base current, I_B. Such a plot describes what are termed the *output characteristics*. A plot of the output characteristics for a typical BJT is shown in Fig. 3.3-6 for operation in Quadrant 1 of the I_C–V_{CE} plane. The same basic relationship (except curves are spaced closer together) is obtained in Quadrant 3. Results are shown with and without Early voltage effects. The regions of operation of the BJT in the I_C–V_{CE} plane are shown in Fig. 3.3-7. Comparison of the nomenclature used to define the regions of operation of the BJT in Fig. 3.3-7 to that used to identify the corresponding regions for the MOSFET of Fig. 3.1-7 shows that the term *saturation* is used to define *nonanalogous* regions for the BJT and MOSFET. As mentioned when the terminology for the operating regions of the MOSFET was discussed, the reader should be aware of this nomenclature to avoid possible confusion.

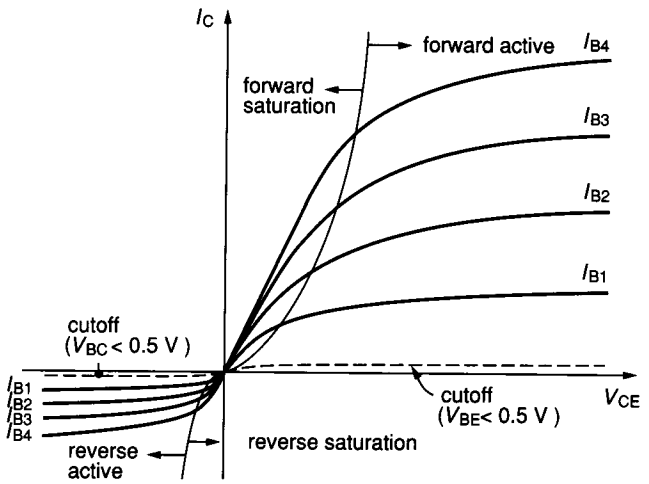


FIGURE 3.3-7
Regions of operation for BJT in I_C–V_{CE} plane.

Example 3.3-3. Compare, using the Ebers-Moll model, the collector and base currents in the forward active region to those in cutoff for a transistor with 1 mil^2 emitter area if $V_{BE} = 0.66$ V, $V_{BC} = -10$ V in the forward active region, and $V_{BE} = -0.3$ V, $V_{BC} = -10$ V in the cutoff region. Use the typical process parameters of Table 3.3-1.

Solution. From (3.3-1) and (3.3-2), I_C and I_B in cutoff are 1.4×10^{-9} μA and 1.406×10^{-9} μA respectively. In the forward active region, it follows from the same equations that $I_C = 63.4$ μA and $I_B = 0.641$ μA. The relative "smallness" of the device currents in the cutoff region should be apparent from these calculations.

3.3.2 Small Signal BJT Model

The small signal model of the bipolar transistor will now be obtained. From Sec. 3.0.2 it can be concluded that the small signal model can be obtained directly from the dc model introduced in the last section. Since there are four regions of operation that have been previously identified in the dc model, there is a different small signal model of the BJT corresponding to each of these regions. The BJT is biased to operate in the forward active region for most small signal applications. The small signal model developed here will be restricted to this region of operation. In the forward active region the collector and base currents can be obtained from

$$I_C = J_S A e^{(V_{BE}/V_t)}\left(1 + \frac{V_{CE}}{V_{AF}}\right) \tag{3.3-27}$$

$$I_B = \frac{J_S A}{\beta_F} e^{(V_{BE}/V_t)} \tag{3.3-28}$$

Since the BJT is modeled as a three-terminal device, it remains to find y_{11}, y_{12}, y_{21}, and y_{22}, as defined in Sec. 3.0 to obtain the small signal BJT model. Convention has resulted in the selection of the emitter node as the reference. For notational convenience b and c rather than 1 and 2 will be used to denote the base and collector nodes of the BJT, respectively. The parameter y_{cb}, often termed g_m, is generally the dominant parameter in the model. From (3.0-5) and (3.3-27) it follows that

$$y_{cb} = g_m = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{\substack{V_{CE}=V_{CEQ} \\ V_{BE}=V_{BEQ}}} = \frac{J_S A}{V_t} e^{(V_{BEQ}/V_t)}\left(1 + \frac{V_{CEQ}}{V_{AF}}\right) \tag{3.3-29}$$

Evaluating (3.3-29) at the Q-point and observing that $V_{CEQ}/V_{AF} << 1$, it follows from (3.3-27) and (3.3-29) that

$$g_m = \frac{I_{CQ}}{V_t} \tag{3.3-30}$$

The balance of the y parameters can be readily obtained from (3.0-5), (3.3-27), and (3.3-28). These parameters are summarized in Table 3.3-4. Also listed in this table is the equivalent h parameter model. The h parameter model has been included since it is also widely used. The small signal model equivalent circuits appear in Fig. 3.3-8.

TABLE 3.3-4
Small signal model parameters for the BJT

y Parameters	*h* Parameters
$y_{cb} = g_m = \frac{I_{CQ}}{V_t}$	$h_{fe} = \beta_F$
$y_{be} = g_\pi = \frac{g_m}{\beta_F}$	$h_{ie} = \frac{\beta_F V_t}{I_{CQ}}$
$y_{bc} = 0$	$h_{re} = 0$
$y_{cc} = g_o = \frac{g_m V_t}{V_{AF}} = \frac{I_{CQ}}{V_{AF}}$	$h_{oe} = \frac{I_{CQ}}{V_{AF}}$

Fundamental parameter relationships

$$r_\pi = 1/g_\pi = h_{ie}$$

$$r_o = 1/g_o = 1/h_{oe}$$

$$\beta_F = g_m r_\pi$$

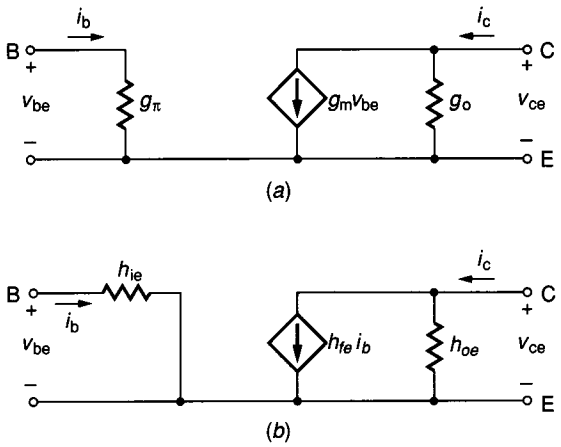


FIGURE 3.3-8
Small signal model of bipolar transistor: (*a*) *y* parameter model (Note: $r_\pi = 1/g_\pi, r_o = 1/g_o$ and $\beta_F = g_m r_\pi$), (*b*) *h* parameter model.

Example 3.3-4. For the circuit shown in Fig. 3.3-9, determine (*a*) the quiescent output voltage, (*b*) the small signal steady state output voltage, and (*c*) the total output voltage. Use the typical process parameters of Table 3.3-1 to characterize the BJT.

Solution

(*a*) To obtain the Q-point it suffices to use the equivalent circuits of Fig. 3.3-5. If it is assumed that the BJT is operating in the forward active region, the circuit of Fig. 3.3-10*a* is obtained. From Ohm's law, it follows that

$$I_{BQ} = (12\text{ V} - 0.6\text{ V})/(600\text{ k}\Omega) = 19\ \mu\text{A}$$

so that

$$I_{CQ} = \beta_F I_{BQ} = 1.9\text{ mA}$$

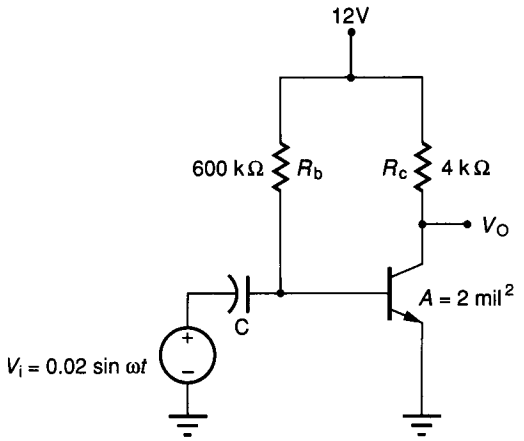


FIGURE 3.3-9
Example 3.3-4.

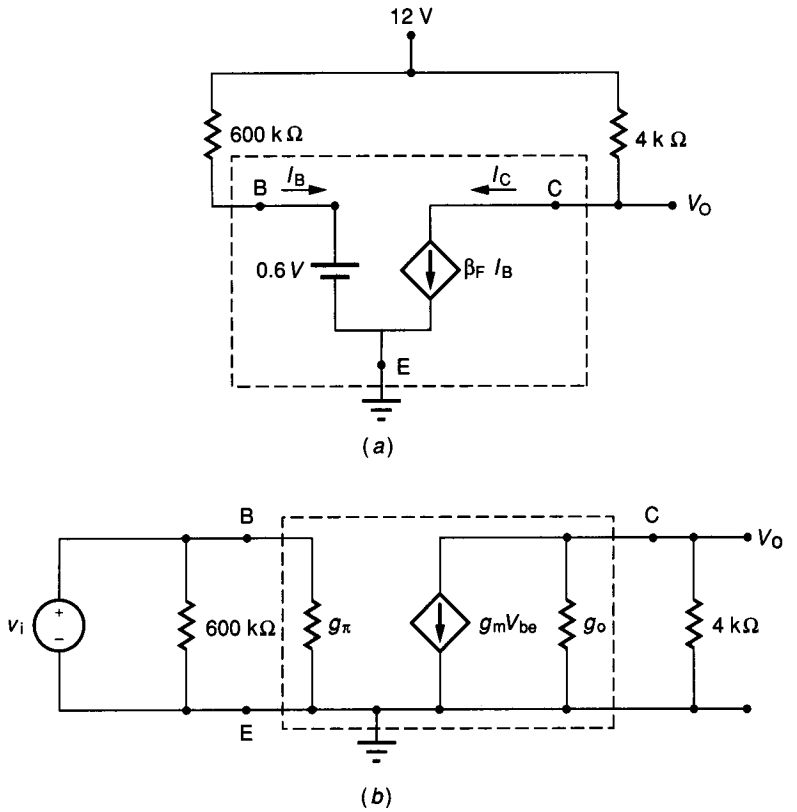


FIGURE 3.3-10
Solution of Example 3.3-4: (*a*) Equivalent circuit for biasing, (*b*) Small signal equivalent circuit.

Hence the quiescent output voltage, V_{OQ}, is given by $V_{OQ} = 12\text{ V} - I_{CQ}R_c = 4.4$ V. With $V_O = 4.4$ V it follows that the assumption of operation in the forward active region is valid.

(*b*) Assuming C is large enough to act as a short circuit for ac signals, it follows from the model of Fig. 3.3-8 that the circuit can be drawn as in Fig. 3.3-10b. From Table 3.3-4 it follows that the small signal transistor g parameters at room temperature ($V_t = 26$ mV) are

$$g_m = 73.1 \text{ mmho}$$

$$g_\pi = 0.731 \text{ mmho}$$

$$g_o = 9.5\ \mu\text{mho}$$

From Ohm's law

$$v_o = (-g_m v_i)\left(\frac{1}{g_o + 1/(4\text{k}\Omega)}\right)$$

$$v_o/v_i = -282$$

The small signal steady state output voltage thus becomes

$$v_o(t) = 5.64 \sin \omega t$$

(*c*) The total output voltage is the sum of the quiescent and small signal steady state values; hence

$$V_O(t) = 4.4\text{ V} - (5.64 \sin \omega t)\text{ V}$$

The minus sign appears in the sum to maintain the correct phase relationship between V_O and I_I in this example.

3.3.3 High-Frequency BJT Model

At high frequencies both the dc and small signal models of the BJT introduced in the previous sections are generally considered inadequate. These limitations are primarily attributable to the unavoidable parasitic capacitances inherent in existing bipolar integrated circuits.

These capacitances are of two types. The first type is composed of pn junction capacitances. These capacitances, which are voltage dependent, can be modeled as in the MOSFET and diode cases by (3.1-14) and (3.2-8) provided the junction is not forward biased by any more than $\phi_B/2$ or about 0.35 V. Since the BJT is typically operated with at least one junction forward biased, it is necessary to model the parasitic junction capacitances under forward bias.

For forward biases greater than $\phi_B/2$, it follows from (3.2-9) that the ~~charge~~ depletion ~~storage~~ region capacitance can be approximated by[12]

$$C_j = 2^n C_{j0} A\left[2n\frac{V_F}{\phi_B} + (1 - n)\right] \tag{3.3-31}$$

where V_F is the forward bias on the junction. This linear approximation is a continuous extension of (3.1-14) across $V_F = \phi_B/2$ that also agrees in slope at the transition point (see Problem 3.31). The model of the BJT junction capacitances is identical to that of the pn junction diode given in (3.2-8) and (3.2-9).

The cross sections of a vertical npn and a lateral pnp transistor are shown in Fig. 3.3-11. The parasitic junction capacitors for all junctions are identified. Note that the vertical structure has parasitic base–collector, base–emitter, and collector–substrate capacitances, whereas the lateral structure has base–emitter, base–collector, and base–substrate parasitics.

The second type of capacitance is due to majority carrier charge accumulation in the base region, which occurs under forward bias near the emitter junction and introduces a second parasitic between the base and emitter. This capacitance, which is also voltage dependent, can be modeled by

$$C_{AC} = \frac{q t_f I_{CQ}}{kT} = t_f g_m \tag{3.3-32}$$

where t_f is the forward base transit time and I_{CQ} is the quiescent collector current. The process parameter t_f is related to the base width, W_B, and the electron diffusion constant, D_n, by the expression

$$t_f = \frac{W_B^2}{2D_n} \tag{3.3-33}$$

The capacitance C_{AC} is added to the base–emitter junction capacitance to obtain the total base–emitter parasitic capacitance. Typical values of t_f range from 0.1 to 1 ns for vertical npn transistors and from 20 to 40 ns for lateral pnp transistors.[13] The parasitic capacitors for both the vertical and lateral BJT are summarized in Table 3.3-5.

A high-frequency small signal equivalent circuit for the BJT is shown in Fig. 3.3-12. In addition to the parasitic capacitors discussed above, four resistive parasitics are shown. These resistive parasitics are present at all frequencies. The resistance R_C, R_E, and R_B represent the ohmic resistance between the metal contact and the junctions in the transistor. Layouts that minimize the distance between the contacts and junctions minimize these resistors. Note that a "primed"

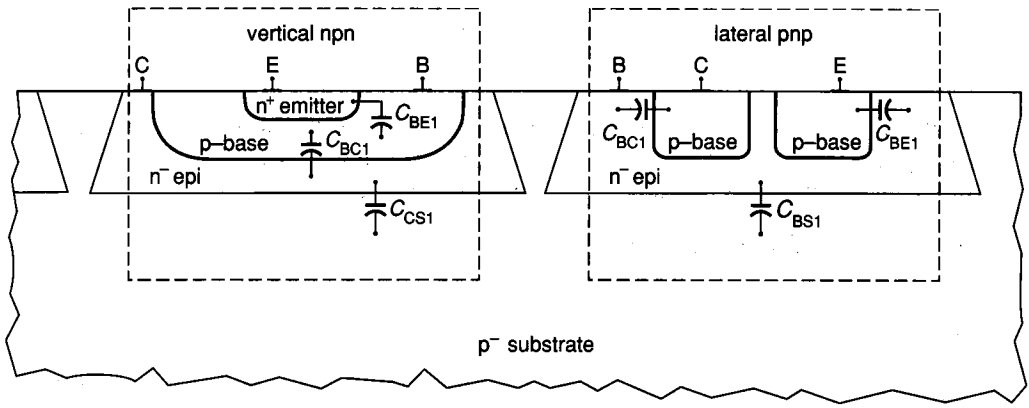


FIGURE 3.3-11
Parasitic junction capacitors in vertical npn and lateral pnp transistors.

TABLE 3.3-5
Parasitic capacitance for the BJT

	Transistor type		
	Alternate notation	**Lateral**	**Vertical**
C_{BE}	C_π	$C_{BE1} + C_{AC}$	$C_{BE1} + C_{AC}$
C_{BC}	C_μ	C_{BC1}	C_{BC1}
C_{BS}		C_{BS1}	0
C_{CS}		0	C_{CS1}

notation has been used to denote the E, B, and C terminals of the effective BJT. The distinction between the "primed" terminals and the actual terminals is necessary since the series ohmic resistances in the emitter, base, and collector leads were neglected when the model of the BJT was derived.

R_E is in the 1 Ω range and is essentially voltage independent. This low value is due to the shallow depth and high doping density of the emitter region. Although the value is small, the reader must be cautioned that even small resistors in the emitter circuit can significantly affect circuit performance (see Problem 3.44). The resistors R_C and R_B are typically in the 100 Ω range. They are both somewhat voltage dependent.

The resistor r_μ, which appears from the base to collector, is large in value and can be approximated by[13]

$$r_\mu \simeq 10\beta_F/g_o \tag{3.3-34}$$

In many applications r_μ can be ignored.

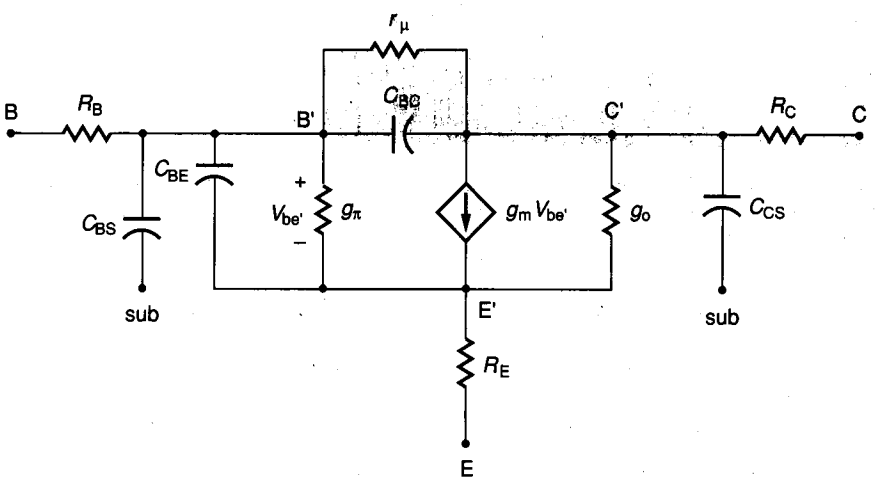


FIGURE 3.3-12
High-frequency small signal equivalent circuit of BJT.

3.3.4 Measurement of BJT Model Parameters

As stated in Section 3.1.4, experimentally measured process parameters are of considerable use to the circuit designer. As in the MOS case, automated measurement equipment is available for bipolar process characterization. In the absence of such equipment, several of the more important BJT device parameters can be measured with reasonable accuracy in the laboratory using standard laboratory equipment. Techniques for measuring J_S, β_F, β_R, V_{AF}, and V_{AR} will be discussed in this section.

From Table 3.3-2, the expressions for the collector and base currents of the npn transistor in the forward active region are

$$I_C = J_S A e^{(V_{BE}/V_t)} \left(1 + \frac{V_{CE}}{V_{AF}}\right) \tag{3.3-35}$$

and

$$I_B = \frac{J_S}{\beta_F} A \exp\left(\frac{V_{BE}}{V_t}\right) \tag{3.3-36}$$

These expressions will serve as a guide for measuring J_S, β_F, and V_{AF}. Measurements of the parameters should be made with I_C close to the intended operating point if possible.

Measurement of V_{AF}. Equation 3.3-35 (extended by Eq. 3.3-1 for small V_{CE}) is plotted in Fig. 3.3-13 for several different values of V_{BE}. Note that all extended curves intersect the V_{CE} axis at $V_{CE} = -V_{AF}$. The parameter V_{AF} can thus be determined by fixing V_{BE} and measuring the V_{CE} axis intercept. If I_{C1} and I_{C2} are the collector currents corresponding to the two different collector–emitter voltages V_{CE1} and V_{CE2} respectively, as depicted in Fig. 3.3-13, then

$$V_{AF} = \frac{I_{C2}V_{CE1} - I_{C1}V_{CE2}}{I_{C1} - I_{C2}} \tag{3.3-37}$$

The circuit of Fig. 3.3-14 with S1 closed can be used for making this measurement. Initially set V_{CE} at V_{CE2} (10 V would be reasonable) and adjust $V_1 = V_{BE}$ so that the desired collector current, I_{C2}, flows ($I_C = -V_O/R$). Leav-

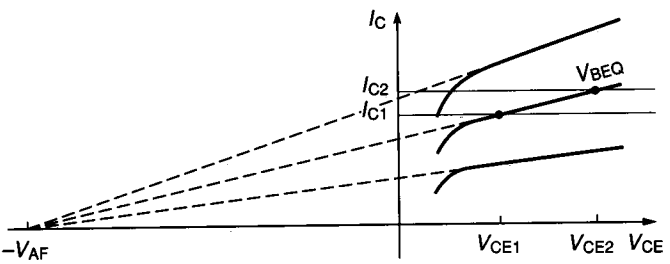
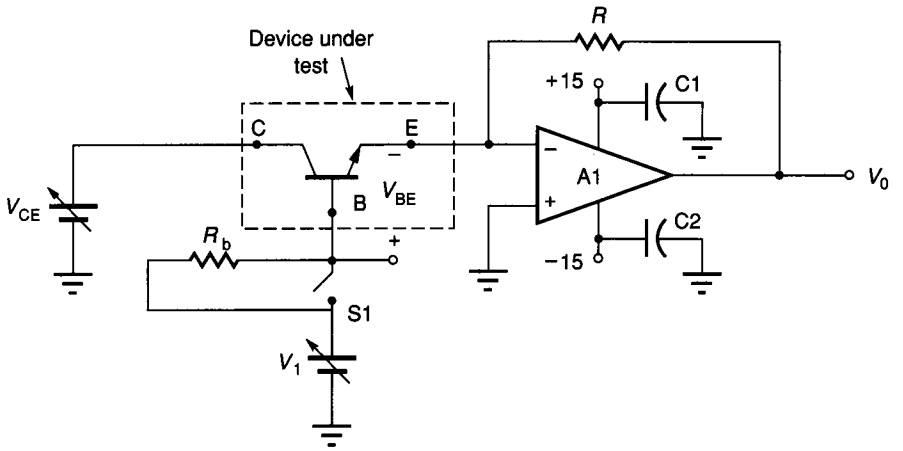


FIGURE 3.3-13
Projection of I–V characteristics of BJT into second quadrant.



A 356 op amp is a reasonable choice for A1. C1 and C2, which may be needed for stability, should be as close as possible to the supply terminals of the op amp to prevent oscillation. A value of 1μF for these capacitors is reasonable. Note: Care should be taken to avoid ever making $V_1 > V_{CE}$ with S1 closed, as this will permanently damage the transistor since no mechanism is provided to limit current flow when the base-collector junction is forward biased.

FIGURE 3.3-14
Circuit for measuring bipolar transistor parameters.

ing V_{BE} fixed ($V_{BE} = V_{BEQ}$), reduce V_{CE} (2 V would be reasonable) to V_{CE1} and measure the current I_{C1}. V_{AF} now follows from (3.3-37). Reasonably wide separation between V_{CE1} and V_{CE2} should be maintained to reduce the sensitivity to the measured voltages and currents.

Measurement of J_S. The previous circuit with S1 closed can be used for measuring $I_S = J_S A$. By measuring the temperature in °K, V_t can be calculated from Eq. 3.3-3. If I_{C2} and V_{CE2} are the initial collector current and collector–emitter voltage used in the measurement of V_{AF}, then it follows from (3.3-35) that it remains to accurately measure $V_{BE} = V_1$ to obtain I_S from the expression

$$I_S = \frac{I_{C2}\exp(-V_{BE}/V_t)}{1 + V_{CE2}/V_{AF}} \tag{3.3-38}$$

Once I_S is obtained, J_S can be determined by dividing by the emitter area, A.

For measuring J_S little accuracy would be lost by either neglecting V_{AF} or using a typical value of V_{AF} in (3.3-38). Accurate measurement of V_{BE} is, however, required.

Measurement of β_F. The circuit of Fig. 3.3-14 with S1 open can be used to measure β_F. Adjust V_1 to obtain the desired collector current, $I_C = -V_O/R$, and adjust V_{CE} to obtain the desired collector–emitter voltage. Measure $I_B = (V_1 - V_{BE})/R_b$. From (3.3-34) and (3.3-35) it thus follows that

$$\beta_F = \frac{I_C/I_B}{1 + V_{CE}/V_{AF}} \tag{3.3-39}$$

As in the case of the measurement of J_S, little accuracy is lost if V_{AF} is neglected or replaced by its nominal value. Since β_F is quite current dependent, it is *particularly important* that it be measured at a value close to the intended operating point.

Methods of measuring β_R and V_{AR} parallel those discussed for β_F and V_{AF} and are left to the reader, as are modifications for measuring parameters of pnp transistors. Information about the parasitic capacitors is generally required for high-frequency applications. Because of their small size, direct measurement with an acceptable degree of accuracy using standard laboratory equipment is not possible. Special test circuits, which either have exceptionally large test devices or which can be used to measure these parasitics indirectly through an investigation of the frequency response of the circuit, are often used.

3.4 PASSIVE COMPONENT MODELS

Discrete passive components are quite easy to model. Resistors and capacitors can generally be modeled by ideal resistors and capacitors respectively. The major limitations are manufacturing tolerances and temperature deviations—both of which can be reduced to acceptable levels in most applications through judicious component selection/specification.

Monolithic resistors and capacitors are far from ideal. They are typically both temperature and voltage dependent. The practical range of values is seriously limited by area constraints. Large resistor or capacitor values are impractical. Process deviations preclude accurate control of absolute component values. Parasitic effects are often quite significant. Relative accuracy (ratioing) between passive components is, however, often quite good.

The following figures of merit are used to characterize passive components.

Resistors

1. Sheet resistance
2. Resistance density
3. Temperature coefficient of resistance
4. Voltage coefficient of resistance
5. Absolute accuracy
6. Relative (ratio) accuracy

Capacitors

1. Capacitance density
2. Temperature coefficient of capacitance
3. Voltage coefficient of capacitance
4. Absolute accuracy
5. Relative (ratio) accuracy

The sheet resistance, temperature coefficients, and voltage coefficients were discussed in Chapter 2. The resistance density is generally a function of the process parameters and layout design rules. The capacitance density is a process parameter. The absolute accuracy is a measure of how accurately the actual resistor and capacitor values can be controlled during processing.

The relative (ratio) accuracy is a measure of how closely two resistors or capacitors can be matched. The ratio accuracy is affected by component placement on a die, device geometry, the physical size of the components, and the nominal relative values of the components themselves.

The parasitic effects were not listed above in the figures of merit primarily because of the difficulty in obtaining a single figure with which to meaningfully quantify the parasitic effects. Nevertheless, parasitic effects include contact resistance and distributed capacitances for resistors. Contact resistance, overlap stray capacitances, and edge capacitances are considered as parasitic effects for capacitors.

3.4.1 Monolithic Capacitors

Any structure in which a voltage-induced separation of charge occurs can serve as a capacitor. Some of the structures used for capacitors, along with their characteristics[14] are shown in Table 3.4-1. In a MOS process, the most common capacitors are formed by sandwiching a thin oxide layer between two conductive polysilicon layers. These capacitors are nearly independent of applied voltage and can be modeled as ideal capacitors. The major limitation is the large parasitic capacitor that is always formed between the lower plate and the substrate. This parasitic limits how these capacitors can be used although clever design techniques, such as stray-insensitive SC filters,[15–16] often evolve to minimize these effects.

When the luxury of the double polysilicon layers is not present in MOS processes, metal–poly, metal–diffusion (lower plate formed by a diffused region in the substrate), or poly–diffusion capacitors with an SiO_2 dielectric are used. These capacitors typically have a lower capacitance density and/or increased voltage dependence and/or a less conductive lower plate than the double poly capacitors.

In the bipolar process, the most desirable common capacitors are metal–diffusion capacitors with an SiO_2 dielectric. The heavily doped emitter diffusion is used for the lower diffusion plate. The characteristics are quite good, but an additional mask step is required for forming the dielectric region. Alternatives include the voltage-dependent junction capacitances formed by either the B–C or B–E junction. These capacitors are modeled by (3.1-14) and (3.3-31). The B–E junction offers reasonable capacitance density at the expense of a limited reverse breakdown voltage (typically 5 to 7 V). The B–C junction reverse breakdown voltage is quite high (typically in the 30 V range), but the capacitance density is quite low. All junction capacitors are limited by requirements that the junctions remain reverse biased (actually, not forward biased by more than a few tenths of a volt).

TABLE 3.4-1
Characteristics of monolithic capacitors

Capacitor type	Process	Dielectric	Absolute accuracy	Ratio accuracy	Voltage characteristic	Temperature	Comments
Poly–Poly	MOS	SiO_2	±20%	±0.06%	−5 ppm/V	25 ppm/°C	Most popular MOS, best characteristic
Poly–Diffusion	MOS	SiO_2	±10%	±0.06%	−20 ppm/V	25 ppm/°C	Lower plate potential often fixed
Metal–Diffusion (with thin oxide)	MOS/Bipolar	SiO_2	±10%	±0.06%	−20 ppm/V	25 ppm/°C	Most desirable bipolar
Moat–Substrate	MOS	Si					Voltage dependent
Base–Collector	Bipolar	Si					Must be reverse biased, low density
Base–Emitter	Bipolar	Si					Must be reverse biased
Conductor–Conductor	Thin film	Varies					Good characteristics
Screened	Thick film	Varies					Chip capacitors often preferred

3.4.2 Monolithic Resistors

Considerably more options exist for monolithic resistors. Some monolithic resistors are passive devices and others contain active devices. Major tradeoffs must be made between linearity, area, biasing complexity, and temperature characteristics in monolithic resistors. Table 3.4-2 lists the characteristics of some of the structures that are used for resistors.

In standard MOS processes, the most ideal resistors are merely strips of polysilicon. Diffusion strips are also used for resistors but exhibit an undesirable nonlinear relationship between voltage and current. Ion implants offer some advantages over depositions for the introduction of impurities to control absolute resistance values in diffused resistors. Thin film resistors with excellent characteristics are added in some specialized processes. For each of these types of resistors, a serpentine pattern is often used to improve packing density. The major limitations of these resistors are the low resistance densities, which limit the total resistance to quite small values; the high deviations in resistance due to process variations; and large temperature coefficients.

In bipolar processes epitaxial strips or diffusion strips are commonly used for resistors. These devices are quite linear. The base diffusion is often used because of its reasonably high sheet resistance. A base-diffused resistor is shown in Fig. 3.4-1a. To prevent forward biasing of the "base–collector" junction, a contact is needed to the epitaxial layer. This will be typically connected to the most positive power supply voltage used for the circuit.

It can be argued that the resistance of the base-diffused resistor could be increased if the depth of the p-base diffusion could be decreased. The depth of this diffusion, however, is generally determined to optimize performance of the BJTs themselves. An alternative is to place an n^+ emitter diffusion in the p base region. This masking step already exists and will result in a significant increase of the sheet resistance of the underlying p diffusion. Such a device, which is termed a *pinch* resistor, is shown in Fig. 3.4-1*b*. Contact must be made to both the n^+ emitter diffusion and the n^- epitaxial region. These regions are typically both connected to the most positive power supply voltage used for the circuit. Although the resistance increases significantly due to this pinching, the variance in emitter and base diffusion depths due to process variations makes the tolerances of pinch resistors quite wide. They also exhibit an increased voltage dependent nonlinearity and are limited in voltage range to circumvent breakdown of the reverse-biased base–emitter junction. Other types of pinch resistors (e.g., epitaxial pinch) can also be made.

Several *active resistors* are shown in Fig. 3.4-2. These active resistors often offer considerable reductions in area requirements compared to passive resistors at the expense of increased nonlinearity and/or reduced signal swing and/or complicated biasing requirements. A more detailed discussion of the active resistor structures appears in Chapter 5.

The circuit of Fig 3.4-2*a* is merely a MOSFET biased to operate in the ohmic region. From (3) of Table 3.1-1, the relationship between I_D and V_{GS} is

$$I_D = \frac{K'W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{3.4-1}$$

TABLE 3.4-2
Characteristics of MOS Resistors

Device	Characterizing equation	Ideal resistance†
Poly Strip	$V = I R_{\square}\frac{L}{W}$	$R = R_{\square}\frac{L}{W}$
Diffusion	$V = I R_{\square}\frac{L}{W}$	$R = R_{\square}\frac{L}{W}$
MOSFET (Ohmic region, Fig. 3.4-2*a*)	$I = \frac{K'W}{L}[(V_{GS} - V_T) - \frac{V}{2}]V$	$R = \frac{L}{K'W(V_{GS} - V_T)}$
MOSFET (Saturated region, Fig. 3.4-2*b*)	$I = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V)$	$R_{SS} = \frac{2L}{\lambda K'W(V_{GS} - V_T)^2}$
MOS depletion (Fig. 3.4-2*c*)	$I = \begin{cases} \frac{K'W}{L}(-V_T)V & V < -V_T \\ \frac{K'W}{2L}V_T^2(1 + \lambda V) & V > V_T \end{cases}$	$R = \frac{L}{K'W \mid V_T \mid}$ $R_{SS} = \frac{2L}{K'W V_T^2 \lambda}$
MOS Enhancement (Fig. 3.4-2*d*)	$I = \frac{K'W}{2L}(V - V_T)^2(1 + \lambda V)$	$R_{SS} = \frac{L}{K'W(V_Q - V_T)}$
Linearity Compensated[18] (Fig. 3.4-2*e*)	$I = \begin{cases} \frac{2K'W}{L}(-V_T)V & V < -V_T \\ \frac{K'W}{L}V_T^2(1 + \lambda V) & V > -V_T \end{cases}$	$R = \frac{L}{2K'W \mid V_T \mid}$ $R_{SS} = \frac{L}{K'W V_T^2 \lambda}$
Bootstrapped Budak[17] (Fig. 3.4-2*f*)	$I = \frac{K'W}{L}(V_C - V_T - V\frac{[\theta + 1]}{2})(1 - \theta)V$ $V < V_C - V_T$	$R = \frac{L}{K'W(1 - \theta)}$

If $V_{DS} << (V_{GS} - V_T)$, then, as seen in Eq. 3.4-1, the relationship between I_D and V_{DS} is linear (assuming V_{GS} is independent of V_{DS}), resulting in an equivalent resistance of

$$R_{eq} \simeq \frac{L}{K'W(V_{GS} - V_T)} \tag{3.4-2}$$

This approximation is quite good for $V_{DS} < 0.5(V_{GS} - V_T)$. A model that includes the nonlinearity is

$$R_{eq} \simeq \frac{L}{K'W[(V_{GS} - V_T) - V_{DS}/2]} \tag{3.4-3}$$

The resistance density (resistance per unit area) of the MOS resistor will now be calculated. Assume d_1 is the minimum moat width, d_2 the minimum

Resistance density‡	Temperature characteristic	Absolute accuracy	Relative accuracy	Comments
$\frac{R_\square}{d_4(d_5 + d_4)}$	1500 ppm/°C	±30%	±2%	Linear, low resistance density
$\frac{R_\square}{d_3(d_5 + d_4)}$	1500 ppm/°C	±35%	±2%	Somewhat voltage dependent
$\frac{1}{K'(V_{GS} - V_T)d_1(d_1 + 2d_2 + d_3)}$				To minimize distortion, $V < (V_{GS} - V_T)/2$
$\frac{1}{\lambda\frac{K'}{2}(V_{GS} - V_T)^2 d_1(d_1 + 2d_2 + d_3)}$				Small signal impedance only, high impedance values
$\frac{1}{K' \mid V_T \mid d_1(d_1 + 2d_2 + d_3)}$				Popular load device
$\frac{1}{\lambda\frac{K'}{2}V_T^2 d_1(d_1 + 2d_2 + d_3)}$				Quite nonlinear
$\frac{1}{K'(V_Q - V_T)d_1(d_1 + 2d_2 + d_3)}$				Quite nonlinear, good resistance density
$\frac{1}{2K' \mid V_T \mid d_1(d_1 + 2d_2 + d_3)}$				Major improvement in density
$\frac{1}{\lambda K' V_T^2 d_1(d_1 + 2d_2 + d_3)}$				
Depends upon how θV is realized				Good linearity potential

†R denotes large signal impedance; R_{SS} denotes small signal impedance only.

‡Assuming a minimum size layout, see Fig. 3.4-3 d_1, d_2, d_3, and d_4 as defined in Sec. 3.4.2.

required overlap of poly over moat, and d_3 the minimum poly–poly spacing as defined by the design rules of the process. If a large serpentine MOS device is constructed with minimum moat width and with separate polysilicon strips for each diffusion strip in the serpentine and if the incremental area required by the corners is neglected, then the diagram of Fig. 3.4-3 can be used to calculate the resistance density of this device. The section of length h has a resistance of

$$R = \frac{h}{K' d_1 (V_{GS} - V_T)} \tag{3.4-4}$$

and an area of

$$A = h(d_3 + d_1 + 2d_2) \tag{3.4-5}$$

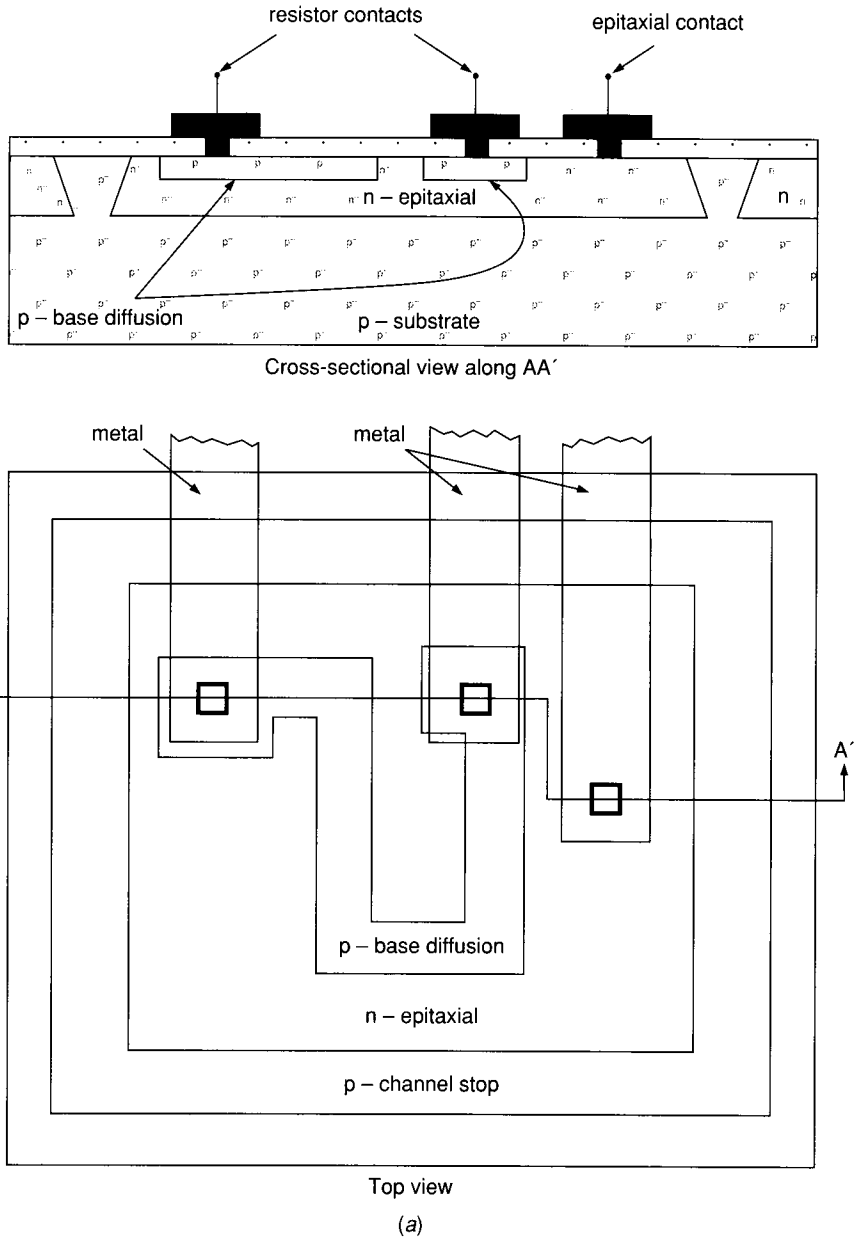
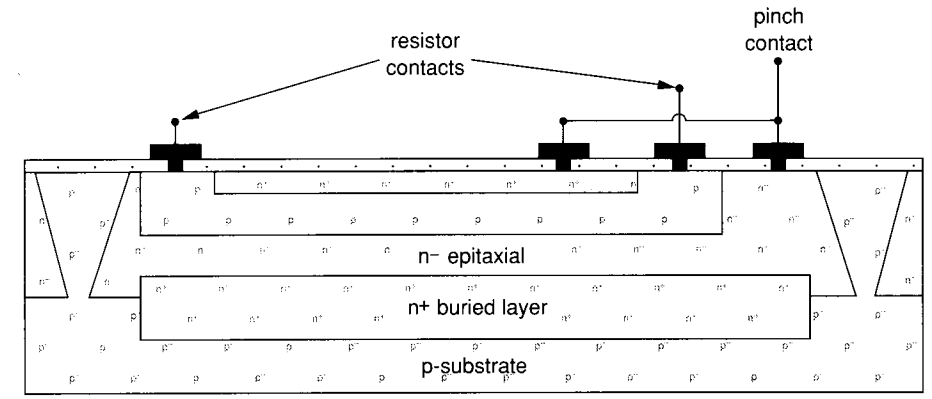
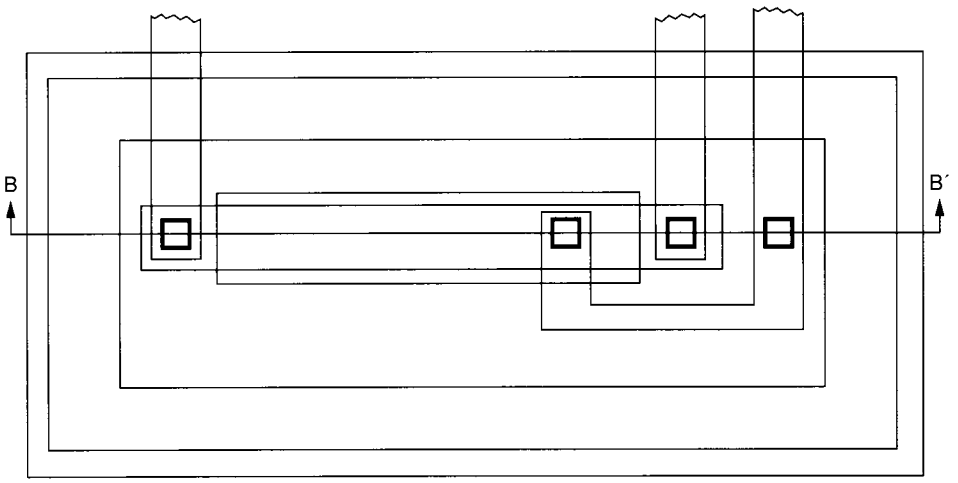


FIGURE 3.4-1
Monolithic resistors: (*a*) Base diffused, (*b*) Base-pinch.



Cross-sectional view along BB′



Top view

(*b*)

FIGURE 3.4-1
(*continued*)

so a resistance density of

$$R_d = \frac{1}{K'(V_{GS} - V_T)(d_1 + 2d_2 + d_3)d_1} \tag{3.4-6}$$

Although making V_{GS} close to V_T can make R_d very high, it is generally impractical due to process variations to directly make $V_{GS} - V_T < 1$ V. Some improvements in resistance density can be realized if the polysilicon strips are merged into one large rectangular region. In this case, the minimum diffusion spacings will determine how close the serpentined strips can be placed. If the MOSFET is a depletion device, it is particularly convenient to make $V_{GS} = 0$ as shown in Fig. 3.4-2*c*, thus eliminating the need for a voltage source.

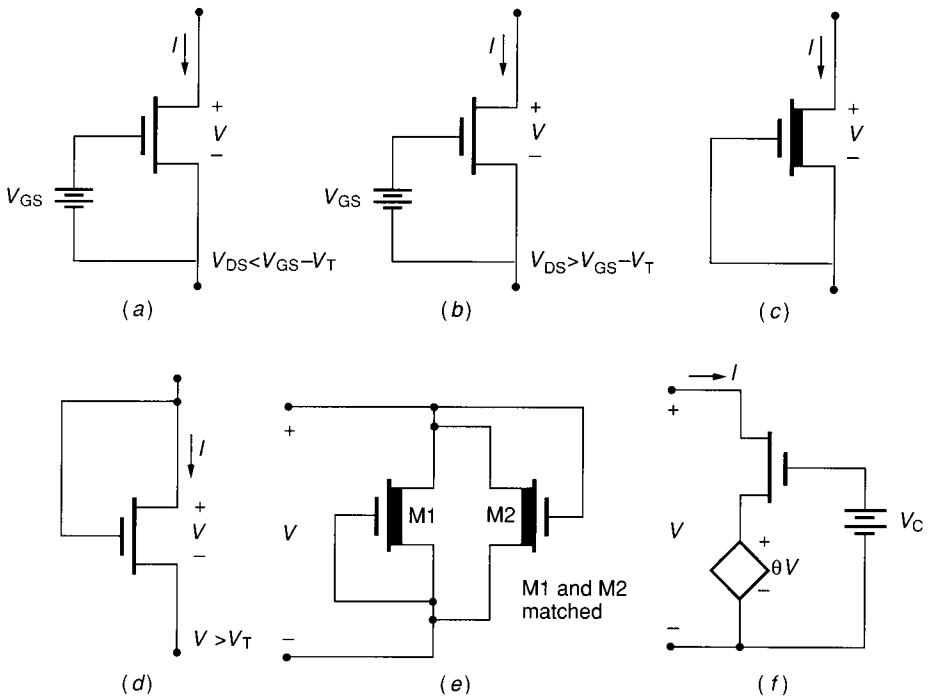


FIGURE 3.4-2
Active MOS resistors.

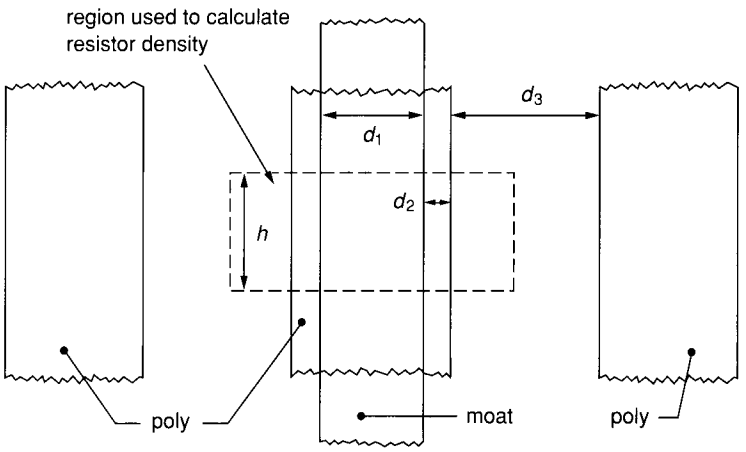


FIGURE 3.4-3
Calculation of resistance density of MOS resistor in ohmic region.

Example 3.4-1. Compare the area required to make a 1 MΩ resistor using a minimum size POLY I string with that using a MOS depletion resistor operating in the saturation region with $V_{GS} = 0$. Use the design rules and process parameters of the NMOS process discussed in Appendix 2A of Chapter 2. Assume the POLY I is uncovered and the feature size of the process is 3 μ (i.e., $\lambda = 1.5\ \mu$).

Solution. The resistance density of the POLY I string can be readily obtained (see Problem 3.55) and is given by

$$R_{dp} = \frac{R_\square}{d_4(d_3 + d_4)} \tag{3.4-7}$$

where d_3 is the minimum poly spacing, d_4 is the minimum poly width, and $R_\square$ is the sheet resistance of POLY I. From Tables 2A.2 and 2A.4 of Appendix A of Chapter 2, $d_3 = 3\ \mu, d_4 = 3\ \mu$, and $R_\square = 25\ \Omega/\square$. Substituting into (3.4-7), it follows that $R_{dp} = 1.39\ \Omega/\mu^2$.

If the MOSFET shown in Fig. 3.4-2*c* is biased to operate in the saturation region, then, from (4) of Table 3.1-1, the drain current is given by

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

The small signal impedance can be obtained by differentiation (assuming V_{GS} and V_{BS} constant) with respect to V_{DS} to obtain

$$R_{ss} = \frac{2L}{[\lambda K'W\,(V_{GS} - V_T)^2]} \tag{3.4-8}$$

Defining d_1–d_3 as in Fig. 3.4-3, it follows that the resistance density for a large serpentined structure is

$$R_{ds} = \frac{2}{[\lambda K' d_1(V_{GS} - V_T)^2(d_1 + 2d_2 + d_3)]} \tag{3.4-9}$$

From Tables 2A.2 and 2A.4 of Chapter 2, $\lambda = 0.01\ V^{-1}$, $K' = 25\ \mu A/V^2$, $V_T = -3$ V, $d_1 = 3\ \mu$, $d_2 = 3\ \mu$, and $d_3 = 3\ \mu$. Substituting into (3.4-9) and setting $V_{GS} = 0$, we obtain $R_{ds} = 74\ k\Omega/\mu^2$. It follows that the area ratio is the ratio of the resistance densities; that is, the ratio of R_{dp} to R_{ds}, which is about 67,000 to 1. The area required to make the 1 MΩ poly resistor is about $9 \times 10^5\ \mu^2$, whereas the active resistor requires an area of around 13 μ^2.

Note that for reasonable values of $V_{GS} - V_T$, the λ in the denominator of (3.4-9) makes the resistance density of the MOS resistor in the saturation region considerably higher than the resistance density of the same device biased to operate in the ohmic region. Small signal resistances in the 1 MΩ range become practical with the MOS resistor biased to operate in the saturation region.

Several other MOS active resistors are shown in Fig. 3.4-2. Those of Fig. 3.4-2*c* and *d* have proven the most popular in NMOS applications due to their simplicity. The structures of Fig. 3.4-2*e* and *f* offer improvements in linearity at the expense of increased area and/or complexity. The characteristics of these active loads are summarized in Table 3.4-2.

A popular bipolar active resistor is shown in Fig. 3.4-4. The equivalent resistance and resistance density will now be calculated.

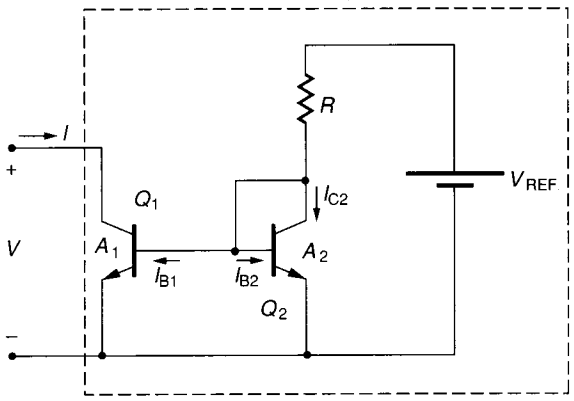


FIGURE 3.4-4
Active bipolar resistor.

Assuming Q_2 is operating in the active region and that β_F is large enough so that $(I_{B1} + I_{B2}) << I_{C2}$, it follows from (2) of Table 3.3-3 that

$$I_{C2} \simeq (V_{REF} - 0.6\text{ V})/R \tag{3.4-10}$$

and from (1) of Table 3.3-2 (neglecting V_{AF}, which is justifiable since $V_{CE2} \simeq 0.6\text{ V} << V_{AF}$),

$$I_{C2} \simeq J_S A_2 \exp\left(\frac{V_{BE2}}{V_t}\right) \tag{3.4-11}$$

Equating the two expressions for I_{C2}, it follows that

$$\exp\left(\frac{V_{BE2}}{V_t}\right) \simeq \frac{V_{REF} - 0.6\text{ V}}{RJ_S A_2} \tag{3.4-12}$$

Again, from (1) of Table 3.3-2, it follows that

$$I = J_S A_1\left(1 + \frac{V}{V_{AF}}\right)\exp\left(\frac{V_{BE1}}{V_t}\right) \tag{3.4-13}$$

Since $V_{BE1} = V_{BE2}$ it follows from (3.4-12) and (3.4-13) that

$$I = \frac{A_1\left(1 + \dfrac{V}{V_{AF}}\right)(V_{REF} - 0.6\text{ V})}{A_2 R} \tag{3.4-14}$$

The small signal impedance follows from differentiation with respect to V and is given by

$$R_{eq} = \frac{V_{AF} A_2 R}{A_1(V_{REF} - 0.6\text{ V})} \tag{3.4-15}$$

It can be shown that for large R, the area of R dominates that of Q_1 and Q_2; hence the resistance density is approximately m times that of R where

$$m = \left(\frac{V_{AF}}{V_{REF}}\right)\left(\frac{A_2}{A_1}\right) \tag{3.4-16}$$

It can be seen that this active resistor can easily result in an area savings of from 10 to 1000 over that required for the resistor R. The high output impedance of the circuit of Fig. 3.4-4 will be exploited in the discussion of current mirrors in Chapter 5.

Both active and passive resistors are used in IC designs. When area required for passive resistors becomes excessive, the designer should consider the active resistor alternative but must bear in mind that the active resistors are typically nonlinear and often require special biasing considerations.

3.5 SUMMARY

In this chapter, models for MOSFETs, diodes, BJTs, and passive components have been developed. Included are large signal dc models, small signal models, and high-frequency models of varying degrees of complexity. Small signal models were obtained by differentiation of the large signal dc models, and high-frequency models were obtained by identifying the relevant parasitic capacitances inherent in the processes in which the devices were fabricated. This multiple-model approach allows the user to select the simplest model acceptable for a given application. The most notable differences between the MOSFET and the BJT are (1) square law contrasted to exponential dc transfer characteristics, and (2) different input impedances, characterized by a nearly infinite input impedance for the MOSFET contrasted to a small input impedance for the BJT. The models developed here will be used for analysis and design throughout later chapters and will be expanded for use in computer simulations in Chapter 4.

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PROBLEMS

Section 3.0

3.1. A linear three-terminal network can be characterized in terms of the y-parameters by the equations

$$i_1 = y_{11}v_1 + y_{12}v_2$$
$$i_2 = y_{21}v_1 + y_{22}v_2$$

Obtain the corresponding small signal equivalent circuit.

3.2. Show that the small signal Thevenin equivalent circuits of both of the circuits in Fig. P3.2 are resistors of value R using the definitions of Section 3.0-3.

3.3. Develop a small signal model for a device characterized by the following equations:

$$I_1 = 5(V_1 - 4)$$
$$I_2 = -25(V_1 - 2)^3\left(1 + \frac{V_2}{5}\right)$$

Section 3.1

3.4. Verify that if a MOSFET is modeled by Eq. (3.1-1), the designation of "source" and "drain" is arbitrary (i.e., the same I–V characteristics are obtained if the node initially labeled "drain" is called the "source" and the node initially labeled "source" is called the "drain").

3.5. Derive an expression for the MOSFET for the locus of points in the I_D–V_{DS} plane where

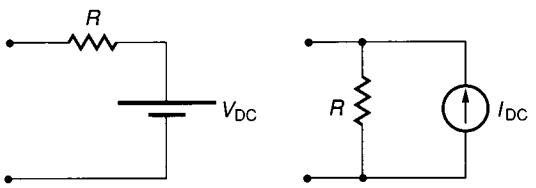

FIGURE P3.2
Circuits for Problem 3.2.

$$\frac{\partial I_D}{\partial V_{DS}} = 0$$

Assume the device is modeled by Eq. 3.1-1.

3.6. Assume a MOS device is to be modeled in the saturation region by the equation

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2 \tag{P1}$$

but that the device is actually characterized by the equation

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2\left(1 + \frac{V_{DS}}{20}\right) \tag{P2}$$

where V_T is assumed constant in both equations. Also assume that the unknown parameters K' and V_T are to be experimentally obtained from (P1) by measuring I_D at $V_{GS} = 2.0$ V and again at $V_{GS} = 2.2$ V with $V_{DS} = 2$ V and then solving simultaneously the two versions of (P1) to obtain the two unknowns. Further assume that $W = 5\ \mu, L = 15\ \mu$, and the measured values of I_D are 6.336 μA and 8.624 μA at 2.0 and 2.2 V respectively.

(*a*) What values will be obtained for the parameters K' and V_T?

(*b*) What percentage error between experimental and theoretical results will be obtained in using Eq. P1 and the parameters obtained in (*a*) to predict I_D if the device is to operate at $V_{GS} = 2.1$ V and $V_{DS} = 2.5$ V?

(*c*) What percentage error between experimental and theoretical results will be obtained in using Eq. P1 and the parameters obtained in (*a*) to predict I_D if the device is to operate at $V_{GS} = 6$ V and $V_{DS} = 15$ V?

(*d*) How can correlation between theoretical and experimental results be improved?

3.7. The transfer characteristics for the CMOS inverter shown in Fig. P3.7 are plotted parametrically in Fig. 3.1-13*b* for the case that $V_{DD} > V_{TON} - V_{TOP}$. Plot parametrically the transfer characteristics of this circuit if $V_{DD} < V_{TON} - V_{TOP}$ and identify the mode of operation of each transistor in each region.

3.8. The small signal model of the MOSFET is used most often for the analysis of MOS circuits in which the transistors are operating in the saturation region.

(*a*) Derive the small signal low frequency model for the MOS transistor operating in the ohmic region with Q-point I_{DQ}, V_{GSQ}, V_{DSQ}, and V_{BSQ}.

(*b*) What does this reduce to if $V_{DSQ} = 0$ V?

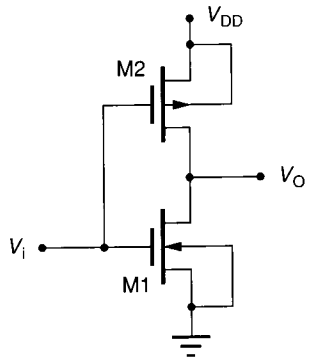

FIGURE P3.7
Circuit for Problem 3.7.

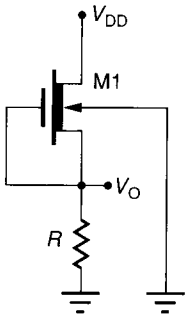

FIGURE P3.9
Circuit for Problem 3.9.

3.9. One easy way to include λ and γ effects in the calculation of V_O for the circuit shown in Fig. P3.9 is to set up an iteration defined for $N = 1$ by

$$V_{T1} = V_{T0}$$

$$I_{D1} = \frac{K'W}{2L}(V_{T1})^2$$

$$V_{O1} = I_{D1}R$$

and for $N > 1$,

$$V_{TN} = V_{T0} + \gamma\left(\sqrt{\phi + V_{O,N-1}} - \sqrt{\phi}\right)$$

$$I_{DN} = \frac{K'W}{2L}(V_{TN})^2[1 + \lambda(V_{DD} - V_{O,N-1})]$$

$$V_{ON} = I_{DN}R$$

How many iterations are required for I_{DN} to converge to within 0.01% of its actual value if M1 is fabricated in the NMOS process of Table 3.1-2 and if $W = 3\,\mu$, $L = 12\,\mu$, $R = 20\,\text{k}\Omega$, and $V_{DD} = 6$ V?

3.10. Obtain an expression for and plot the maximum deviation over the ohmic region, in percentage, from the current as predicted by (3.1-1) from that obtained if (3.1-1) is multiplied by $(1 + \lambda V_{DS})$ to maintain continuity at the ohmic region–saturation region interface.

3.11. Assume the MOSFET in Fig. P3.11 is characterized by the CMOS model parameters of Table 3.1-2.

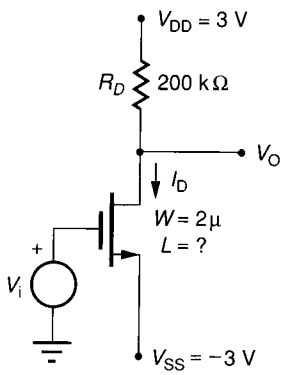

FIGURE P3.11
MOSFET for Problem 3.11.

(*a*) Determine L so that $A_V = v_o/v_i = -25$. What is the Q-point (V_{OQ}, I_{DQ}) with this value of L?

(*b*) Determine L so that $V_{OQ} = OV$. What is $A_V = v_o/v_i$ with this value of L?

3.12. Obtain the dc model for the devices shown in Fig. P3.12. Make a qualitative comparison of the performance of these structures.

3.13. The output characteristics for a MOSFET with $V_{BS} = 0$ are shown in Fig. P3.13.

(*a*) Determine as many parameters as possible from the set

$$\{K', V_{T0}, \gamma, \lambda, W, L, K'W/L, \phi, C_{ox}\}$$

(*b*) If the device is biased to operate at the point Q, determine as many parameters as possible of the set $\{g_m, g_{ds}, g_{mb}\}$.

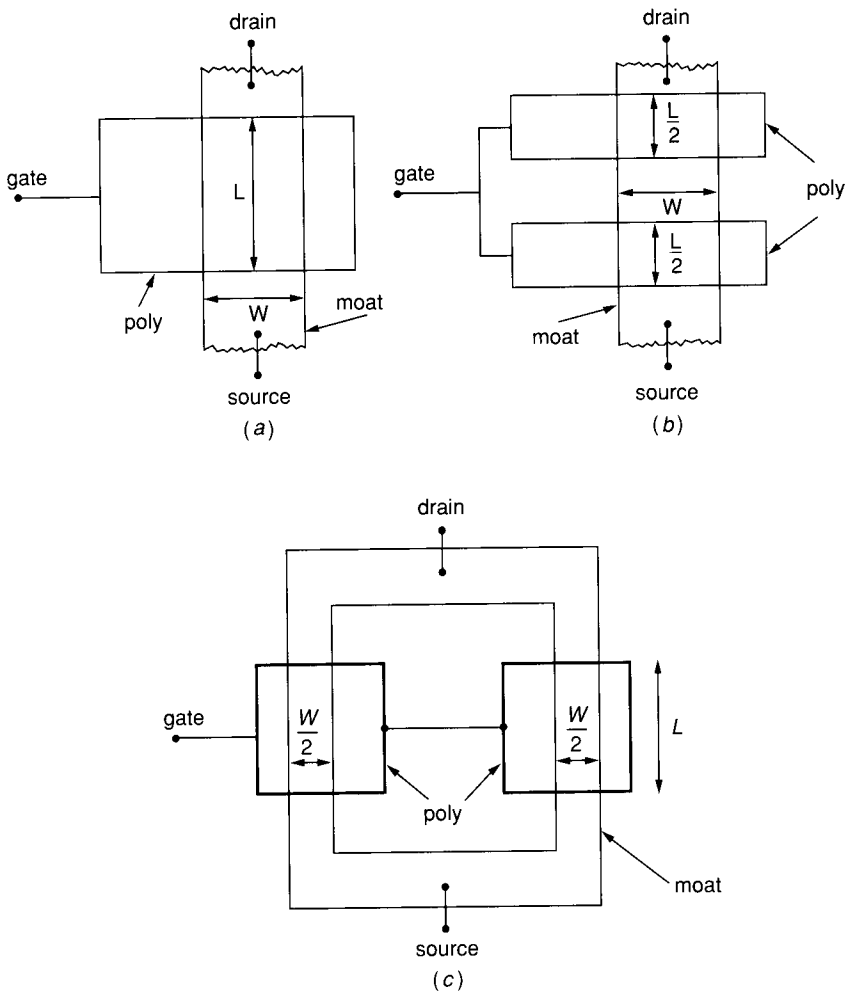

FIGURE P3.12
Devices for Problem 3.12.

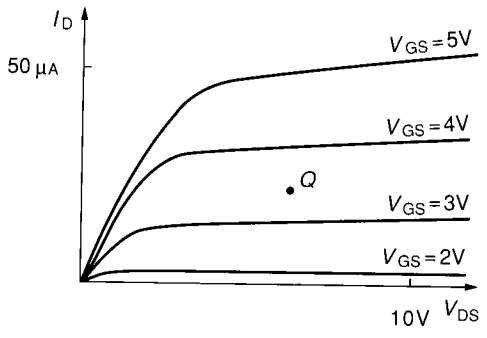

FIGURE P3.13
Graph for Problem 3.13.

3.14. Plot g_m, g_{ds}, and g_{mb} versus I_{DQ} on the same axis for I_{DQ} in the interval [100 nA, 10 mA] for a MOSFET with $W = L = 5\ \mu$ designed in the CMOS process characterized in Table 3.1-2.

3.15. Determine the small signal model of the MOSFET operating in weak inversion saturation. Compare this model to that of the same device if it operates in strong inversion.

3.16. A simple single transistor amplifier is shown in Fig. P3.16.

(*a*) Using the typical CMOS process parameters of Table 3.1-2, determine W/L of M so that $I_{DQ} = I_{BIAS} = 20\ \mu$A, if $V_{SS} = -2$ V and $V_i = 0$ V.

(*b*) Determine the small signal voltage gain $A_V = v_o/v_i$ for the value of W/L obtained in (*a*).

(*c*) If the subthreshold parameters I_{DO} and n of (3.1-32) are $I_{DO} = 20$ nA and $n = 2$, determine W/L of M so that $I_{DQ} = I_{BIAS} = 20\ \mu$A at room temperature if $V_{SS} = -0.1$ V and $V_i = 0$ V.

(*d*) Determine the small signal voltage gain $A_V = v_o/v_i$ for the value of W/L obtained in (*c*) and compare these results with that obtained for operation in strong inversion.

3.17. Obtain an expression for and plot I versus V for the enhancement load circuit of Fig. P3.17 based upon the MOSFET model of Table 3.1-1, and compare these transfer characteristics with those used for the simple model of Eq. 3.1-45.

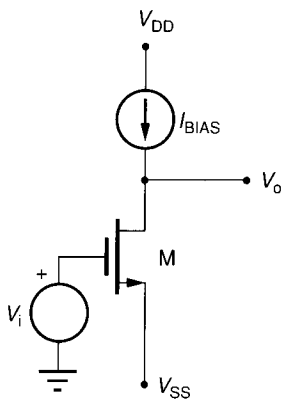

FIGURE P3.16
Problem 3.16.

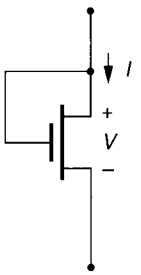

FIGURE P3.17
Circuit for Problem 3.17.

3.18. Derive the small signal model for the MOSFET operating in the saturation region from the dc model of the MOSFET given by Eq. 3.1-5. Verify that these results are equivalent to those given in Table 3.1-3.

3.19. If $I_B = 50\ \mu A$, then M1 in Fig. P3.19 is operating in strong inversion for $V_i = 0$. If I_B remains constant, how much must the W/L ratio of M1 be increased to force M1 into subthreshold? Assume $I_{DO} = 20$ nA, $n = 2$, $K' = 24\ \mu A/V^2$, and $V_T = 0.75$ V.

3.20. Consider a single MOS transistor. If $V_{BS} = 0$ and $V_{DS} > 3V_t$, determine the value of V_{GS} at the intersection of the strong inversion drain saturation current of (4) in Table 3.1-1 with the weak inversion current. How does this relate to the transition region of Eq. 3.1-31? Assume $I_{DO} = 20$ nA, $n = 2$ in Eq. 3.1-32, $K' = 24\ \mu A/V^2$, and $\lambda = 0$.

3.21. Obtain the output voltage for the circuit layout of Color Plate 10 if $V_{DD} = 5$ V and $V_I = 2$ V. Assume the devices were fabricated in the NMOS process summarized in Appendix 2A.

3.22. In the saturation region of operation, most of the channel region is characterized by an inversion layer, which is an extension of the source as depicted in Fig. 2.2-2*f*. This represents a series impedance in the source. Assuming the voltage drop is sufficiently small that Eq. 3.1-8 applies, calculate the series source–channel impedance, R_{sc}. *Note*: Due to a tapering of the channel near the drain, the source–channel impedance is actually about 50% larger than that predicted by (3.1-8).

3.23. If γ and λ effects are neglected, a MOSFET of width W and length L is equivalent to the series connection of the two devices as shown in Fig. P3.23 where ϵ is any real number which satisfies the expression $0 < \epsilon \leq L$.

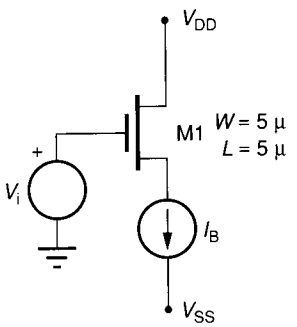

FIGURE P3.19
Circuit for Problem 3.19.

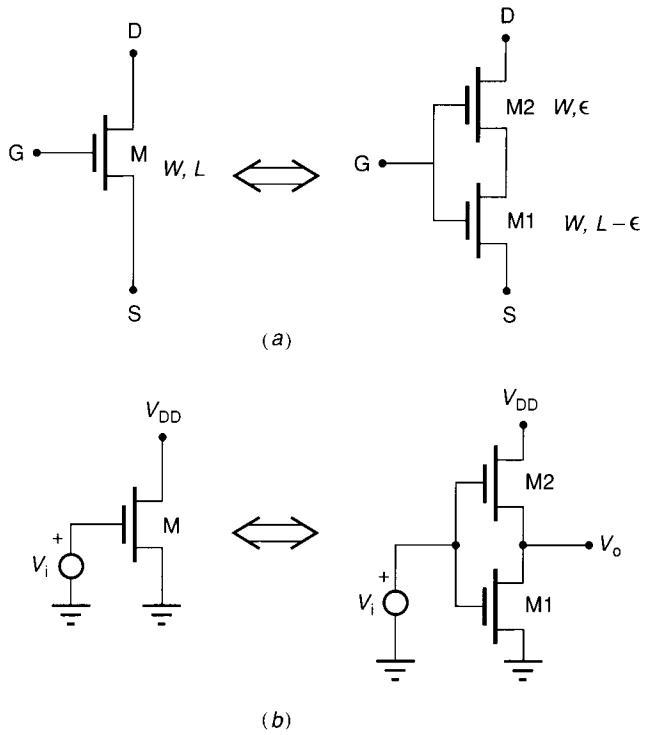

FIGURE P3.23
Circuits for Problem 3.23.

(*a*) If the MOSFET M is operating in the saturation region, show that in the equivalent circuit of Fig. P3.23*a*, M1 is operating in the ohmic region and M2 in the saturation region.

(*b*) If the equivalent MOSFET is connected as shown if Fig. P3.23*b* and M is operating in the saturation region, derive an expression for V_o in terms of V_i.

(*c*) Calculate the equivalent impedance of M1 in Fig. P3.23*b* assuming V_i is sufficiently small that (3.1-8) applies.

3.24. For the circuit of Fig. P3.24,

(*a*) Calculate parametrically the output thermal noise current in the frequency band 10 kHz $\leq f \leq$ 200 kHz and the output flicker noise current in the same

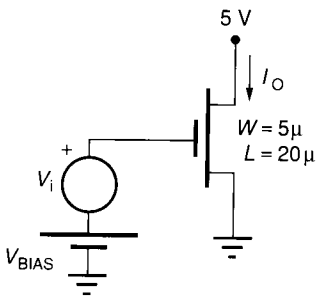

FIGURE P3.24
Circuit for Problem 3.24.

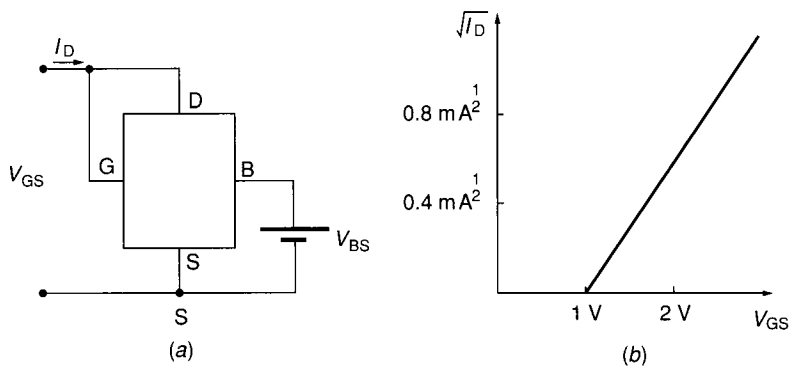

FIGURE P3.25
Circuit and graph for Problem 3.25.

band if $K_f = 3 \times 10^{-24}$ V^2·F at the dc operating point determined by $V_i = 0$.

(*b*) Calculate parametrically the equivalent input referred offset voltage.

(*c*) Calculate the signal to noise ratio of the output current if $V_{BIAS} = 2$ V and $V_i = 0.25 \sin 10^5 t$ over the frequency band given in (*a*). Neglect λ and γ effects and assume the remaining process parameters given in Appendix 2B.

3.25. A plot of V_{GS} versus $\sqrt{I_D}$ for an NMOS transistor is shown in Fig. P3.25. It has $\mu C_{ox} = 60\ \mu$A/V^2, $V_{BS} = 0$, and the remainder of the characterization parameters as indicated in the NMOS design rules discussed in Chapter 2.

(*a*) Is the device a depletion or enhancement transistor?

(*b*) What mode of operation is the device in?

(*c*) What is W/L?

(*d*) What is the threshold voltage?

(*e*) What will the horizontal axis intercept if V_{BS} is changed to -9 V?

3.26. The pn junction between an n^+ moat diffusion and substrate is used to form a capacitor. Determine the value of this capacitor with a reverse bias of 6 V if the area of the n^+ moat diffusion is 16 mil^2. Assume the process parameters of the NMOS process of Appendix 2A.

3.27. Compare the minimum area required to build a first-order lowpass filter with a 3 db cutoff frequency of 2 kHz using the two techniques shown in Fig. P3.27*a* and *b*

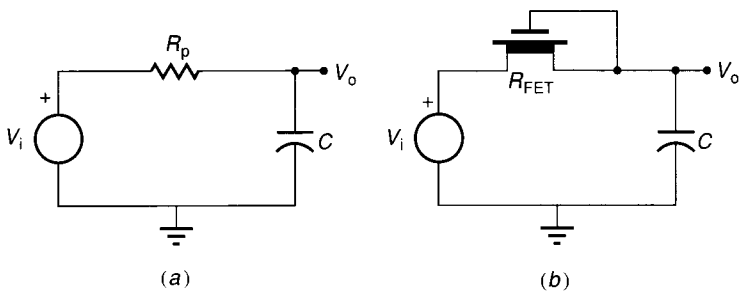

FIGURE P3.27
Circuits for Problem 3.27.

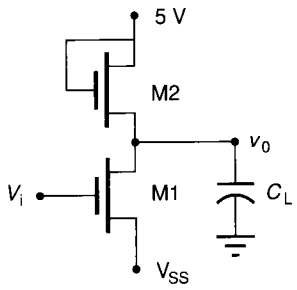

FIGURE P3.28
Circuit for Problem 3.28.

respectively. Assume R_p is made of a poly resistor with $R_\square = 30\ \Omega/\square$. R_{FET} is biased to operate in the ohmic region ($K' = 15\mu A/V^2$, $V_{T0} = -3.5V$, $\gamma = 0$, $\phi = 0$, $\lambda = 0$), the capacitance density is 0.2 pF/mil^2, and both R_p and R_{FET} are serpentined with minimum feature width of 5 μ, minimum feature spacing of 5 μ, and a gate–moat overlap of 2.5 μ. Derive all equations needed.

3.28. The voltage V_{SS} can be used to establish the quiescent drain currents with $V_i = 0$. Obtain an expression for the 3 db bandwidth of the circuit in Fig. P3.28 in terms of I_{DQ} and the model parameters of M1 and M2. Neglect all parasitic capacitors in M1 and M2.

3.29. Determine the small signal equivalent circuit for the circuit shown in Fig. P3.29.

3.30. Assume a MOSFET is characterized in strong and weak inversion by Eqs. (3.1-4) and (3.1-33) respectively.

(*a*) Show that if the transconductance gain is to be continuous at the strong inversion–weak inversion interface, then the transition must occur at $V_{GS} = V_T - 2nV_t$.

(*b*) Show that if I_D is to be continuous at the transition determined in (*a*), then I_{DO} and K' must be related by the equation

$$I_{DO} = \frac{K'2(nV_t)^2}{e^2}$$

Section 3.2

3.31. Show that the forward-biased pn junction capacitance model of Eq. 3.2-9 is a continuous and differentiable extension of the reverse-bias model of Eq. 3.2-8 at the transition $V = \phi_B/2$.

3.32. Assume a depletion region capacitor is characterized by $C_{ox} = 250$ fF/mil^2, $\phi = 0.6$ V, $n = 1/2$, and $A = 6$ mil^2. Determine the bias voltage required to reduce the capacitance to half of what it is at 0 V bias.

3.33. Accurately determine I in Fig. P3.33. Assume the diode is characterized by the BE diffusion of the bipolar process of Appendix 2C with a junction area of 500 μ^2. Assume operation at $T = 30°$ C.

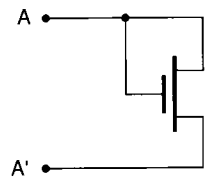

FIGURE P3.29
Circuit for Problem 3.29.

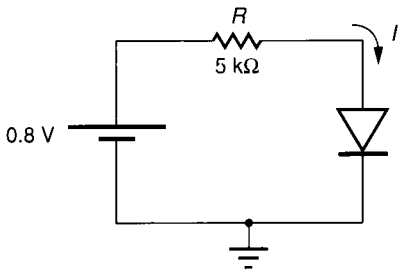

FIGURE P3.33
Circuit for Problem 3.33.

3.34. Assume the vertical npn base–collector junction of the process of Appendix 2C is to be used as a varactor diode.
(*a*) Determine the area of the base needed to generate a capacitance of 50 pF with a reverse bias of 3 V.
(*b*) Plot the capacitance of this diode versus reverse bias for $-5 \leq V_{BC} \leq 0$.
(*c*) Repeat part (*a*) if the BE junction is used instead of the BC junction in the same process.

3.35. A diode can be fabricated in the bipolar process of Appendix 2C in several ways. Give all ways that the diode can be fabricated and compare the performance characteristics from both dc and ac viewpoints. Include in your discussion a characterization of all relevant parasitics.

3.36. A "diode-connected transistor" is shown in Fig. P3.36*a*. Compare the performance of this to that of the BE and BC diodes (Figs. P3.36*b* and *c*) in the bipolar process of Appendix 2C.

3.37. The circuit shown in Fig. P3.37 is proposed as a rectifier. Compare the dc performance of this to that of the pn junction and that of the diode-connected transistor of Problem 3.36. How does the performance of this circuit as a rectifier change with W and L?

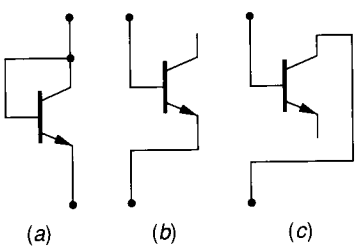

FIGURE P3.36
Diodes for Problem 3.36.

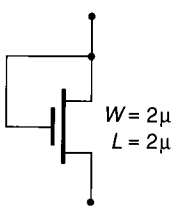

FIGURE P3.37
Circuit for Problem 3.37.

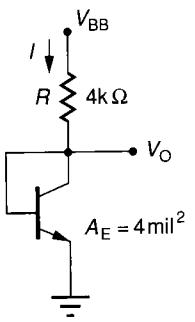

FIGURE P3.38
Circuit for Problem 3.38.

Section 3.3

3.38. Using Fig. P3.38, obtain V_O to within ±1% if (*a*) $V_{BB} = 12$ V and (*b*) $V_{BB} = 0.9$ V. Assume the BJT is characterized by the parameters of Table 3.3-1 and modeled by the Ebers-Moll Eqs. 3.3-1 and 3.3-2.

3.39. Determine the maximum error, in percentage, that results from using (3.3-10) and (3.3-11) instead of the more complicated Ebers-Moll equations of (3.3-1) and (3.3-2) in the region $V_{BE} > 0.5$ V, $V_{BC} < 0.3$ V. Assume the BJT is at room temperature and characterized by the parameters of Table 3.3-1.

3.40. Calculate the power that would be dissipated in a BJT if $A_E = 4$ mil^2 and the device is operating with (*a*) $V_{BE} = 0.6$ V and $V_{BC} = -5$ V, and (*b*) $V_{BE} = 1.6$ V and $V_{BC} = -5$ V. Assume the BJT is characterized by the process parameters of Table 3.3-1.

3.41. Plot the transconductance gain, g_m, versus bias current (collector or drain) for a MOSFET with $W = L = 10\ \mu$ and a BJT with $A_E = 100\ \mu^2$. Use the typical process parameters of Tables 3.1-2 and 3.3-1.

3.42. Rewrite the Ebers-Moll equations of (3.3-1) and (3.3-2) using V_{BE} and V_{CE} as the independent variables in terms of the parameters I_S, β_F, β_R, and V_T.

3.43. At high frequencies, a small signal gate current flows into the gate of the MOSFET. Compare the unity small signal–short circuit current gain frequency (of $A_I = i_o/i_i$)

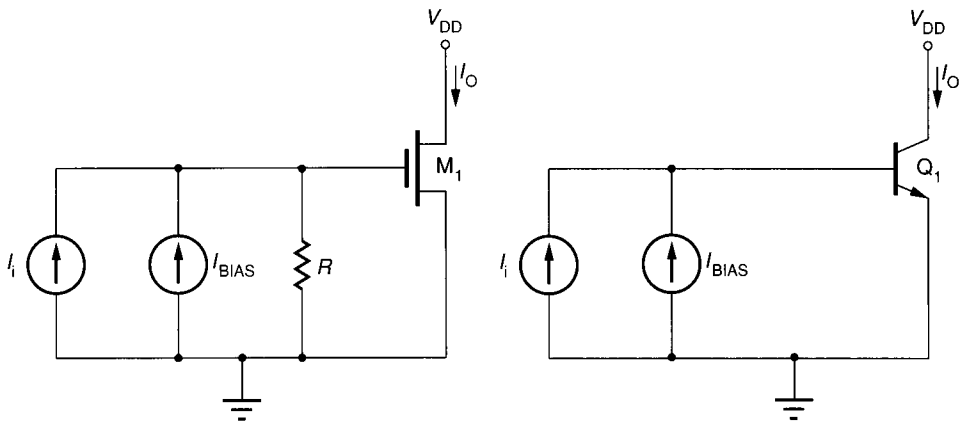

FIGURE P3.43
Circuit for Problem 3.43.

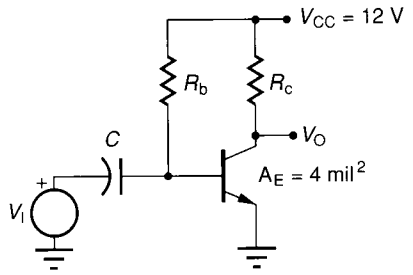

FIGURE P3.44
Circuit for Problem 3.44.

for the MOSFET to that of the BJT (see Fig. P3.43). Assume both devices are in their high-gain operating region, are of minimum size, are biased at $I_{OQ} = 200\,\mu A$, and are characterized by the process of Tables 2A and 2C of the Appendices of Chapter 2. Assume R is large.

3.44. (*a*) For the circuit shown in Fig. P3.44, bias the circuit (determine R_b) so that $V_{OQ} = 2$ V when $R_c = 500\ \Omega$. Determine the small signal voltage gain $A_v = v_o/v_i$ if it is assumed C is large. Use the typical process parameters of Table 3.3-1.
(*b*) Repeat part (*a*) if the parasitic emitter resistance is $R_E = 2\ \Omega$. Compare the results with those obtained in (*a*).
(*c*) Repeat parts (*a*) and (*b*) if $R_C = 10\ k\Omega$ and $V_{OQ} = 6$ V and compare with the results obtained in parts (*a*) and (*b*).

3.45. Assume the BJT of Fig. P3.45 is biased with R_b so that Q1 operates in the forward active region. What will be the tolerance in the value of V_{BE} due to processing? What will be the wafer-level tolerance in the value of V_{BE} due to wafer-level parameter variations? Assume the BJT process in which Q1 is fabricated is characterized by Table 2C.4 of Appendix 2C and that wafer-level variations (matching) are characterized by footnote 1 of that table.

3.46. The depletion region capacitance of the BE junction of an npn transistor with a rectangular emitter that is 0.3 mil × 6 mil is 0.63 pF at zero volts reverse bias. A circular transistor of the same test bar has the same emitter area. What is the depletion region capacitance of this device for a 6 V reverse bias at room temperature if the built-in potential, ϕ_B, is 0.70 V?

3.47. For the transistor shown in Fig. P3.47, $I_s = 2 \times 10^{-15}$ A and the emitter area is 1.5 mil^2. With $V = 1$ V, the current I is 52 μA, and with $V = 21$ V, I is 56 μA.
(*a*) Determine V_{AF}.
(*b*) Determine β_F.
(*c*) Determine V_{BE} at room temperature (300 °K).

3.48. If we plot ln I_C (vertical) versus V_{BE} (horizontal) for a bipolar transistor operating

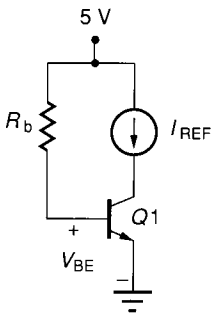

FIGURE P3.45
Circuit for Problem 3.45.

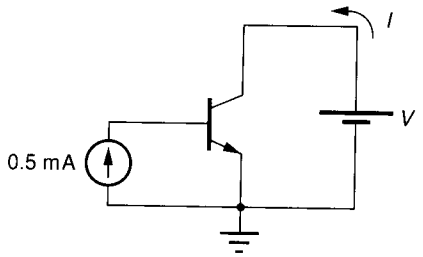

FIGURE P3.47
Transistor for Problem 3.47.

in the forward-active region, how can the area of the emitter be determined from the plot? What can be determined from the slope? Neglect Early voltage effects.

3.49. For the circuit shown in Fig. P3.49, assume the collector current is 10 mA, the emitter is a square with sides of 1 mil, the base is a square with sides of 3 mil, and the collector area is defined by a square with sides of 6 mil. For the following, assume that no changes are made in the circuit schematic.
(*a*) What will be the collector current if the sides of the base are increased to 4 mil?
(*b*) What will be the collector current if the emitter sides are decreased to 0.5 mil?
(*c*) What will be the collector current if the collector sides are increased to 7 mil?

3.50. A plot of ln I_C versus V_{BE} for a BJT transistor, with emitter area 4 mil^2, and a base area of 10 mil^2, operating in the forward active region is shown by the solid line in Fig. P3.50. Determine as many of the following model parameters as possible: J_S, T, V_T, β_F, β_R, α_F.

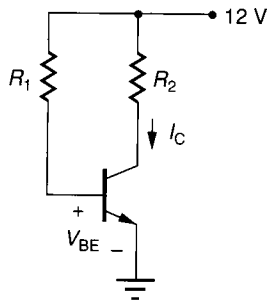

FIGURE P3.49
Circuit for Problem 3.49.

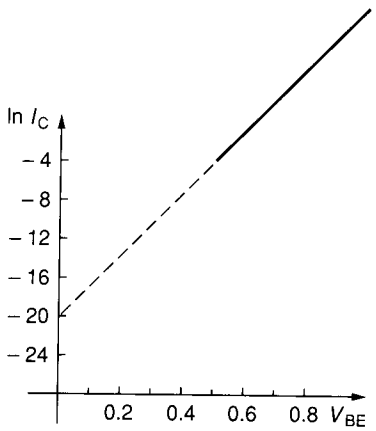

FIGURE P3.50
Graph for Problem 3.50.

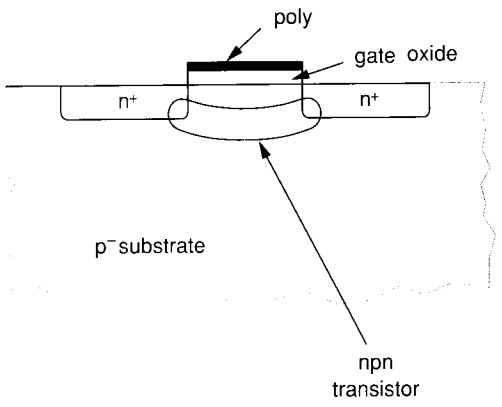

FIGURE P3.51
NMOS structure for Problem 3.51.

3.51. The NMOS structure shown in Fig. P3.51 is proposed as an npn transistor to be used with n-channel MOSFET devices. Give two good reasons why this device may not be practical.

3.52. Assume the two circuits shown in Fig. P3.52 are biased (with V_{B1} and V_{B2} respectively) so that $V_{OQ} = 5$ V. Compare the small signal voltage gains of the two circuits.

3.53. Calculate the value of C_{JE} and C_{JC} for the npn vertical transistor characterized by the process of Table 2C.4 in Appendix 2C. Assume the emitter is square with dimensions 20 $\mu \times 20$ μ, the base is square with sides of 50 μ, and the collector is square with sides of 100 μ. Compare these results to the values listed in Table 2C.5.

3.54. Calculate the value of C_{JE}, C_{JC}, and the base–substrate capacitance for a lateral pnp transistor with $30\,\mu \times 30\,\mu$ square collector and emitter areas separated by a distance of 15 μ if they lie symmetrically inside an isolated square epitaxial region that is 110 μ on a side. Assume the process parameters of Table 2C.4 of the Appendix 2C.

3.55. From the equivalent circuit of Fig. 3.3-8, rigorously define the h parameters and derive an expression for the h parameters in the small-signal BJT model (*a*) in terms of the y parameters g_m, g_π, and g_o, and (*b*) in terms of the operating point and parameters used in the Ebers-Moll model.

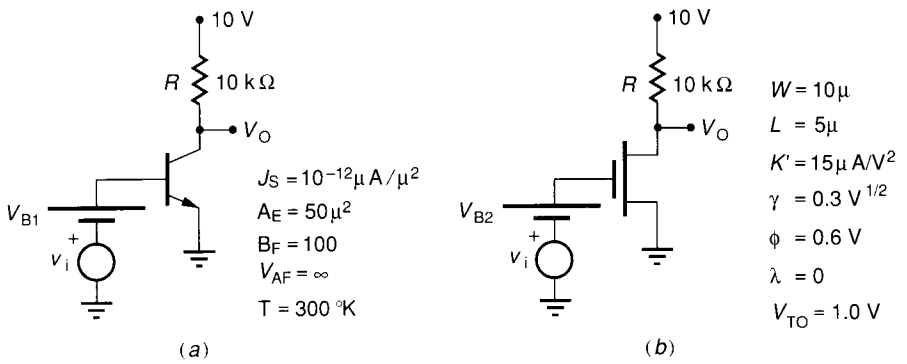

FIGURE P3.52
Circuits for Problem 3.52.

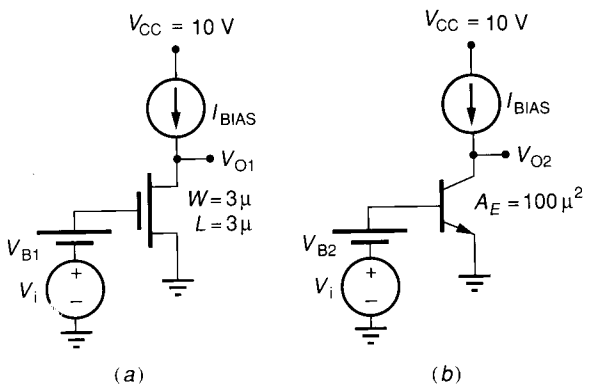

FIGURE P3.56
Amplifiers for Problem 3.56.

3.56. Plot the small signal voltage gains, v_{O1}/v_i and v_{O2}/v_i, versus bias current for the two amplifiers shown in Fig. P3.56. Assume that V_{B1} and V_{B2} are adjusted so that $V_{O1Q} = V_{O2Q} = 5$ V. Use the typical process parameters of Tables 3.1-2 and 3.3-1.

3.57. Two different schemes for biasing the BJT are shown in Fig. P3.57. Assume the BJT is characterized by the process parameters of Table 3.3-1.

(*a*) Determine the value of R_B and V_B necessary to bias the outputs at 5 V.

(*b*) Determine the change in V_{O1} and V_{O2} that will be expected for each circuit if V_{CC} varies around 10 V by ±0.1 V.

(*c*) Determine the change in V_{O2} that will be expected if V_B varies about the value obtained in part (*a*) by ±0.1 V.

(*d*) What can be said about the sensitivity of the quiescent output voltage to the biasing voltages V_{CC} and V_B for the two circuits?

Section 3.4

3.58. If the sheet resistance of polysilicon is $R_\square$, the minimum poly width is d_4, and the minimum poly spacing is d_3, determine the resistance density of a large, minimum-feature-size, serpentined poly resistor in terms of d_3, d_4, and $R_\square$. Neglect any area associated with corners and contacts.

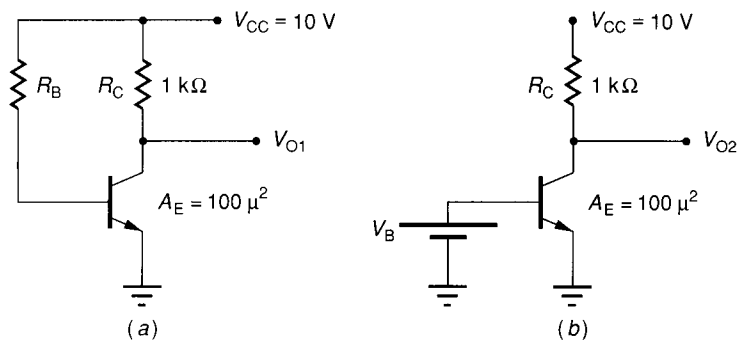

FIGURE P3.57
Circuits for Problem 3.57.