CHAPTER 4

CIRCUIT SIMULATION

4.0 INTRODUCTION

Computer simulation of a circuit entails using a computer to predict, or simulate, the performance of a circuit or system. The circuit which is simulated may include anywhere from a few components to several hundred thousand. Many different types of computer programs are used for simulations of integrated circuits, depending on the type of analysis required and the size of circuit involved.

The major emphasis in this chapter is on the use of the SPICE simulation program for circuit simulation, and, in particular, on a discussion of the active device models used in SPICE and the interrelationship between these models and the device models discussed in Chapter 3. The simulation program SPICE was selected because of its long-term acceptance and use, as well as its widespread availability to both industrial and academic groups. The reader should have access to and be familiar with the SPICE User's Guide[1] and the basic use of SPICE.

In the design of state-of-the-art integrated circuits; circuit simulations comprise only a small portion of the overall use of the computer. The discussion of a circuit simulation program is included in this chapter because of the challenging nature of circuit simulation. Many students and even practicing engineers experience more problems with circuit simulation than with most of the other sophisticated CAD tools used for VLSI design. These problems largely result from unfamiliarity with the capabilities, limitations, and uses of the simulators.

4.1 CIRCUIT SIMULATION USING SPICE

The circuit simulation program called SPICE is the result of a continuing effort, which has spanned nearly 20 years, by a large group of individuals at the University of California at Berkeley. It was initially written in FORTRAN; later

versions in that language are nearly 18,000 lines long. A C–Language version of SPICE was practically introduced in 1987, and now both the FORTRAN and C versions are widely used. SPICE has been adapted to a large number of different hardware configurations and is used in both industry and academia. Although there are several competing programs, some of which may offer advantages in some respects, none are as universally accepted as SPICE.

SPICE utilizes a modified nodal analysis approach. It can be used for nonlinear-dc, nonlinear-transient, and linear-ac analysis problems. It also includes modules for more specialized analysis such as noise analysis, temperature analysis, etc. The inputs can be constant or time varying. For the nonlinear-dc and nonlinear-transient analyses, the program includes the nonlinear effects of all devices specified by the user. For the ac analysis, the dc operating point is internally determined. From the dc operating point, the small signal equivalent circuit of each device is obtained. The resulting linear network is analyzed using the appropriate matrix manipulations. The small signal analysis *includes no nonlinear effects* of the devices.

A block diagram showing the fundamental operation of SPICE appears in Fig. 4.1-1. The subroutine READIN reads the SPICE input file. ERRCHK verifies that the input syntax is correct. Temperature effects are handled in SPICE by repeating the entire analysis for each temperature. The subroutines DCTRAN, DCOP and ACAN perform the bulk of the manipulations. DCTRAN and DCOP are used for dc transfer characteristics, dc operating point calculations, and transient analysis. ACAN performs the small signal ac analysis.

Documentation about the program SPICE is required for utilizing the program. At a minimum, the IC designer needs the following two documents available from Berkeley to effectively use SPICE for MOS IC design.

1. "SPICE User's Guide"[1]
2. "The Simulation of MOS Integrated Circuits Using SPICE"[2]

These publications, along with other relevant documentation[3–12,22,23] are listed in the references. The SPICE source code[6] contains good comments and serves as the ultimate reference document on the program.

One of the strong points of SPICE is its inclusion of respectable models for the basic active devices, specifically, the diode, BJT, JFET, and MOSFET. The user can create generic models for the active devices that correspond to, and are consistent with, the process parameters and design rules of the process used for a specific design. This model library may actually contain numerous generic device models for a given process, each of which contains as little or as much information as needed for the desired emphasis in the simulation. The designer can then use geometric parameters and specific model name references to specify the complete model for each active device in the circuit being analyzed.

To run SPICE[1], the user must first create a file, sometimes referred to as a SPICE deck, which contains a complete description of the circuit (including device models) along with a description of the excitation and the type of analysis desired. This file is accessed when the SPICE program runs.

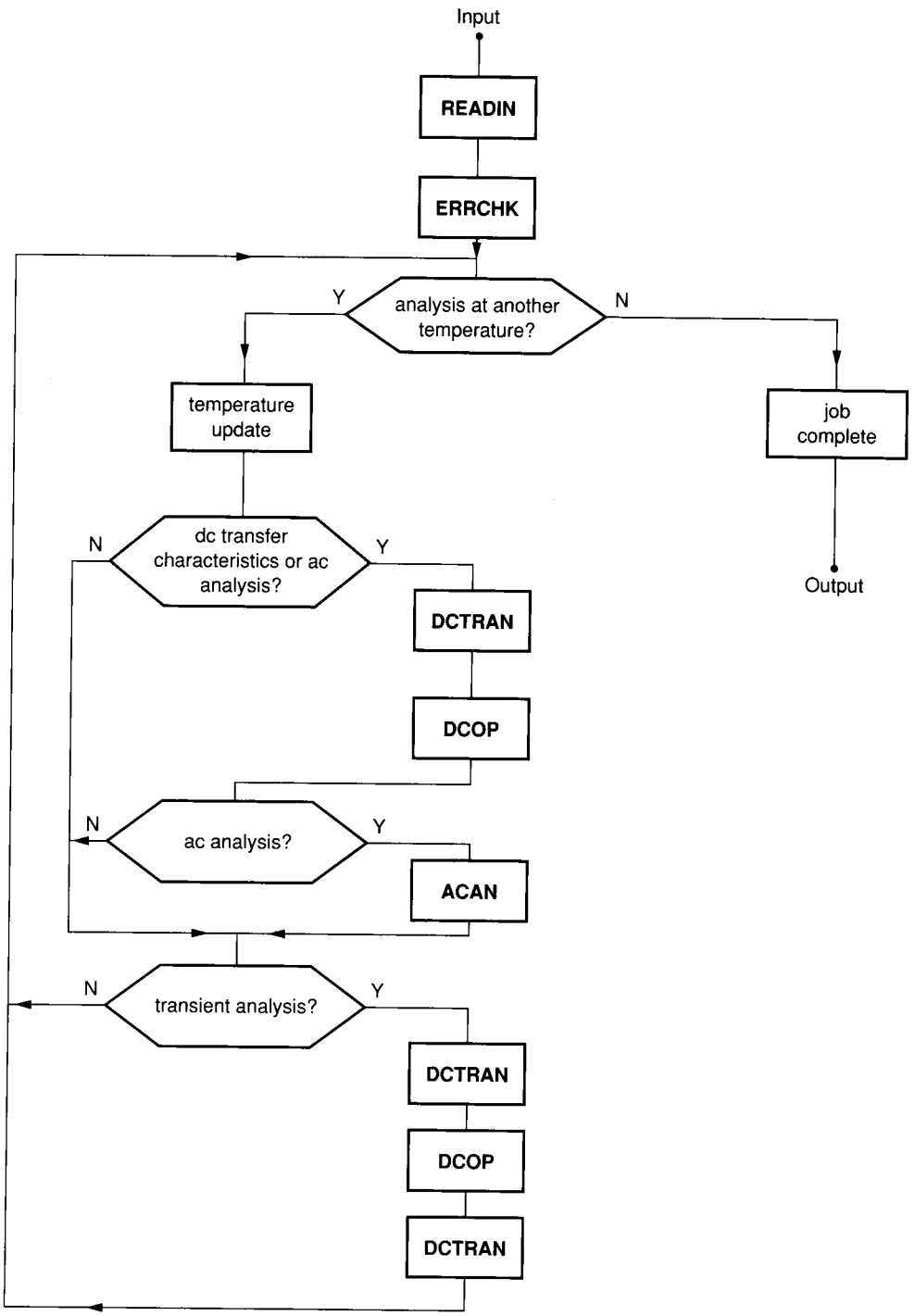


FIGURE 4.1-1
Simplified SPICE functional flowchart (boldface mnemonics indicate names of major subroutines).

The designer must be familiar with the device models used in any computer simulation. In the following sections the device models of the active devices used in SPICE are discussed. These models are related to those used for hand calculations that were introduced in Chapter 3. Each section is self-contained.

4.2 MOSFET MODEL

SPICE Version 2G has three different MOSFET models, designated as Level 1, Level 2, and Level 3. Version 3 of SPICE also contains a fourth MOSFET model, the BSIM model[7–12]. The BSIM model is a process-oriented model which places a major emphasis on short channel devices. The discussion here will be restricted to the Level 1, Level 2, and Level 3 models. The Level 1 model is basically the same as introduced in Chapter 3 and is termed the Shichman–Hodges model; it closely follows the work of Sah[13]. The Level 1 model is the simplest model and is useful for verifying that no errors occurred in the hand calculations. In some applications the Level 1 model may be adequate for computer simulations.

The Level 2 model differs from the Level 1 model both in its method of calculating the effective channel length (λ effects) and the transition between the saturation and ohmic regions. A time-consuming polynomial rooting routine is required for the Level 2 model to determine the transition point between the linear and saturation regions. The Level 2 model offers improvements in performance which are particularly significant for short channel devices.

The Level 3 model is termed a semi-empirical model. Several empirical parameters (parameters not obviously related to or motivated by the device physics of the MOSFET) are introduced in the Level 3 model. These parameters may offer improvements in fit of the model. The Level 3 model also offers a reduction in time required to calculate the transition point between the linear and saturation regions of operation.

The Level 1, Level 2, and Level 3 device models can be found respectively in subroutines MOSEQ1, MOSEQ2, and MOSEQ3 of the SPICE source code. Subroutine MODCHK is used for some of the hierarchical parameter definitions. The terminal voltages of the MOSFET are passed to these subroutines, and the nodal currents are returned along with the small signal model parameters at the operating point. In each interval of time in a transient analysis, nodal currents are comprised of two parts. The first is the dc current obtainable from the large signal device model. The second is the charge current associated with the parasitic capacitances in the devices. This latter current plays a major role in high-frequency transient analyses.

Temperature effects can also be modeled in SPICE. The functional form of the temperature-dependent device parameters will be discussed later.

Individual MOSFETS are modeled by a two-step process in SPICE. The device element line (card) in the SPICE deck contains information about the nodal location of the device in the circuit as well as geometrical information about the device and optional initial condition variables. In the device element line, reference is made to a specific device *model*. The .MODEL line (card) in the SPICE deck contains generic information about the electrical characteristics

of devices formed in a process based upon the characterizing process parameters. Each device has a separate device element line. Typically, many devices will reference a single .MODEL line.

A simplified flowchart of MOSEQ1, MOSEQ2 and MOSEQ3 is shown in Figure 4.2-1. The large signal currents in Quadrant 1 of the $I_D - V_{DS}$ plane are calculated from the expression:

$$I_G = I_B = 0 \tag{4.2-1}$$

$$I_D = \begin{cases} I_{CUTOFF} & V_{GS} < V_{TH} \quad (4.2\text{-}2) \\ I_{OHMIC} & V_{GS} > V_{TH} \quad V_{DS} < V_{DSAT} \quad (4.2\text{-}3) \\ I_{SAT} & V_{GS} > V_{TH} \quad V_{DS} > V_{DSAT} \quad (4.2\text{-}4) \end{cases}$$

where it is assumed that the drain and source are designated so that $V_{DS} \geq 0$. The parameter V_{TH} denotes the threshold voltage which was denoted by V_T in Chapter 3. V_{DSAT} is a parameter that characterizes the transition between the ohmic and saturation regions. Operation in Quadrant 3 of the $I_D - V_{DS}$ plane is characterized by the same equations, where the drain and source designations are internally made so that $V_{DS} \geq 0$.

The small signal parameters are calculated from the derivatives of I_D with respect to V_{GS}, V_{DS}, and V_{BS} as explained in Sec. 3.1. In what follows, the expressions used for I_D for the Level 1 and Level 2 models are given along with a description of each of the parameters that appear in the model; the default values used in SPICE are given if the parameter is not specified. The parameters are summarized in Appendix 4A.

Some parameters in the model may be specified in more than one way. For example, the transconductance parameter K', introduced in Sec. 3.1, may be entered directly or calculated from the expression $K' = \mu_0 C_{ox}$. A hierarchical convention has been adopted in SPICE to avoid ambiguity. If a parameter is specified, that value will be used. If a parameter is not specified but can be calculated from other parameters that are specified (or have a nonzero default value), the calculated value will be used. If a parameter is not specified and at least one of the other parameters which can be used to calculate it is not specified and defaults to zero, the default value of the original parameter is adopted. A summary of the Level 1 and Level 2 large signal models follows. The parameters used in these models are defined in the Appendices of this chapter.

4.2.1 Level 1 Large Signal Model

$$I_{CUTOFF} = 0 \tag{4.2-5}$$

$$I_{OHMIC} = K' \frac{W}{L_{eff}} \left([V_{GS} - V_{TH}] - \frac{V_{DS}}{2} \right) V_{DS} \tag{4.2-6}$$

$$I_{SAT} = \frac{K'}{2} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \tag{4.2-7}$$

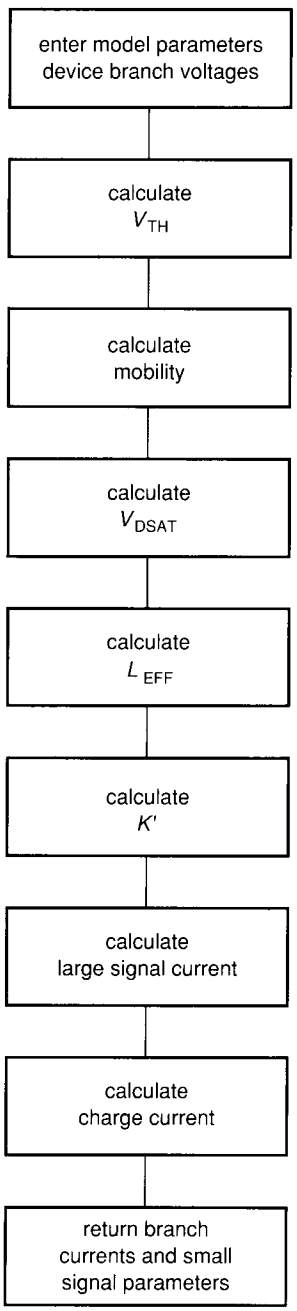


FIGURE 4.2-1
Simplified Flowchart of SPICE Subroutines MOSEQ1, MOSEQ2, and MOSEQ3.

where V_{DSAT} is given by

$$V_{DSAT} = V_{GS} - V_{TH} \tag{4.2-8}$$

and the regions of operation are as defined in Eqs. 4.2-1 – 4.2-4.
The parameters V_{TH} and L_{eff} represent the threshold voltage and effective length of the device, respectively, and are given by

$$V_{TH} = V_{T0} + \gamma\left[\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right] \tag{4.2-9}$$

and

$$L_{eff} = \frac{L_{adj}}{1 + \lambda V_{DS}} \tag{4.2-10}$$

where V_{T0} is the zero bias threshold voltage, γ is the bulk threshold parameter, ϕ is the surface potential, and λ is the channel length modulation parameter. λ is a SPICE input parameter. V_{T0}, γ, and ϕ can either be entered directly or be internally calculated, as discussed later. The parameter K', if not entered, can be calculated from the expression

$$K' = \mu_o C_{ox} \tag{4.2-11}$$

where μ_o is the nominal channel mobility (if μ_o is not entered, the default value will be used) and C_{ox} is the gate oxide capacitance density which can be calculated from the gate oxide thickness, T_{ox}, by the expression

$$C_{ox} = \epsilon_{ox}/T_{ox} \tag{4.2-12}$$

where ϵ_{ox} is the dielectric constant of SiO_2. The parameter L_{adj} represents the adjusted length which is the drawn length reduced by the lateral diffusion on the drain and source, LD.

$$L_{adj} = L - 2 \times \text{LD} \tag{4.2-13}$$

The parameters in V_{TH}, if not input, are calculated from

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{SUB}}}{C_{ox}} \tag{4.2-14}$$

$$\phi = \frac{2kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right) \tag{4.2-15}$$

and

$$V_{T0} = V_{FB} + \gamma\sqrt{\phi} + \phi \tag{4.2-16}$$

where ϵ_{si} is the dielectric constant of silicon, N_{SUB} is the substrate doping, q is the charge of an electron, and n_i is the intrinsic carrier concentration of silicon. N_{SUB} is a SPICE input parameter and n_i and ϵ_{si} are physical constants defined in Appendix 4A. The flatband voltage, V_{FB}, is given by

$$V_{FB} = \phi_{ms} - \frac{qN_{ss}}{C_{ox}} \tag{4.2-17}$$

where the input parameter, N_{ss}, is the effective surface state density and ϕ_{ms} is the semiconductor work function difference. ϕ_{ms} is calculated internally from

$$\phi_{ms} = W_{FN} - \frac{\phi}{2} \tag{4.2-18}$$

where the parameter W_{FN} is an internal function of physical constants characteristic of the materials involved, TPG (which specifies the types of materials used to construct the device), and temperature.

4.2.2 Level 2 Large Signal Model†

$$I_{CUTOFF} = \begin{cases} 0 & NFS = 0 \\ I_{\text{weak inversion}} & NFS \neq 0 \end{cases} \tag{4.2-19}$$

$$I_{OHMIC} = \frac{K_2' W}{L_{eff}} \left[\left(V_{GS} - V_{TH}^{*} - \eta \frac{V_{DS}}{2} \right) V_{DS} \right] + I_{BSO} \tag{4.2-20}$$

$$I_{SAT} = \frac{K_2' W}{2L_{eff}} \left[(V_{GS} - V_{TH}^{*})^2 (2 - \eta) \right] + I_{BSS} \tag{4.2-21}$$

where the cutoff transition region is determined by

$$V_{TH} = V_{T0} + \gamma \left[\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right] - \gamma\alpha \sqrt{\phi - V_{BS}} + (\phi - V_{BS}) \frac{\pi}{4} \frac{\epsilon_{si}}{C_{ox} L_{adj}} (\text{DELTA}) \tag{4.2-22}$$

The parameter L_{adj} is defined by (4.2-13). The parameters DELTA and α will be discussed later.

The parameter V_{MAX} is used to characterize the saturation/ohmic transition region as specified in (4.2-3) and (4.2-4); it denotes the maximum drift velocity of carriers in the channel. If the parameter V_{MAX} is not input, the saturation/ohmic transition region is determined by

$$V_{DSAT} = \frac{(V_{GS} - V_{TH}^{*})}{\eta} + \frac{1}{2} \left[\frac{\gamma_s}{\eta} \right]^2 \cdot \left\{ 1 - \left[1 + 4 \left(\frac{\gamma}{\eta} (1 - \alpha) \right)^{-2} \left(\frac{V_{GS} - V_{TH}^{*}}{\eta} + \phi - V_{BS} \right) \right]^{\frac{1}{2}} \right\} \tag{4.2-23}$$

If V_{MAX} is input, V_{DSAT} is obtained from solution of a complicated fourth-order polynomial. V_{MAX} essentially reduces the value of V_{DSAT} and hence the saturation current in a manner more consistent with experimental measurements. If

†See SPICE source code for the SPICE Model of the MOSFET in weak inversion. The accuracy of the weak inversion MOSFET Models has been questioned by some individuals. [14–15]

V_{MAX} is input, computational time for calculating V_{DSAT} does increase. Additional details about V_{MAX} can be found in the paper by Vladimerescu and Liu.[2]

The parameters η, V^*_{TH}, I_{BSO} and I_{BSS} are given by the following equations:

$$\eta = 1 + \frac{\pi}{4}\frac{\epsilon_{si}}{C_{ox}L_{adj}}(\text{DELTA}) \tag{4.2-24}$$

$$V^*_{TH} = V_{T0} - \gamma\sqrt{\phi} + (\phi - V_{BS})\frac{\pi}{4}\frac{\epsilon_{si}}{C_{ox}L_{adj}}(\text{DELTA}) \tag{4.2-25}$$

$$I_{BSO} = -\frac{2}{3}\frac{K'_2 W}{L_{eff}}\frac{\gamma_s}{\eta}\left[(\phi + V_{DS} - V_{BS})^{\frac{3}{2}} - (\phi - V_{BS})^{\frac{3}{2}}\right] \tag{4.2-26}$$

$$I_{BSS} = \frac{K'_2 W}{L_{eff}}\left[\left[(V_{GS} - V^*_{TH})(1-\eta) - \frac{\eta}{2}(V_{DSAT} - (V_{GS} - V^*_{TH}))\right]\right.$$
$$\left.(V_{DSAT} - (V_{GS} - V^*_{TH})) - \frac{2}{3}\frac{\gamma_s}{\eta}\left[(V_{DSAT} - V_{BS} + \phi)^{\frac{3}{2}} - (\phi - V_{BS})^{\frac{3}{2}}\right]\right] \tag{4.2-27}$$

The parameter K'_2 is obtained from the expression

$$K'_2 = K'\frac{\mu_s}{\mu_o} \tag{4.2-28}$$

where μ_s is the effective surface mobility. If not input, K' is determined from (4.2-11). The parameter DELTA is a SPICE input parameter and is used to characterize width reduction (see Problem 4.17) where the effective width, W_{eff}, is given by $W_{eff} = W(2 - \eta)$.

The parameters V_{T0}, L_{adj}, and ϕ are determined as for the Level 1 model. The parameter γ_s is given by

$$\gamma_s = \gamma(1 - \alpha) \tag{4.2-29}$$

The parameter α is given by:

$$\alpha = \frac{1}{2}\frac{XJ}{L_{adj}}\left[\sqrt{1 + \frac{2W_S}{XJ}} + \sqrt{1 + \frac{2W_D}{XJ}} - 2\right] \tag{4.2-30}$$

where

$$W_S = X_D\sqrt{\phi - V_{BS}} \tag{4.2-31}$$

$$W_D = X_D\sqrt{\phi - V_{BS} + V_{DS}} \tag{4.2-32}$$

and where XJ is a SPICE input parameter representing the metallurgical junction depth.

The parameter L_{eff} is defined by the expression

$$L_{eff} = L_{adj}(1 - \lambda V_{DS}) \tag{4.2-33}$$

If not specified as an input parameter, λ is calculated from the expression

$$\lambda = \frac{X_D}{L_{adj} V_{DS}} \left[\sqrt{\left(\frac{X_D V_{MAX}}{2\mu_s} \right)^2 + (V_{DS} - V_{DSAT})} - \frac{X_D V_{MAX}}{2\mu_s} \right] \quad (4.2\text{-}34)$$

The parameter X_D is given by the expression

$$X_D = \sqrt{\frac{2\epsilon_{si}}{qN_{SUB}}} \quad (4.2\text{-}35)$$

The effective surface mobility, μ_s, is given by

$$\mu_s = \begin{cases} \mu_o \left[\dfrac{\text{UCRIT} \cdot \epsilon_{si}}{C_{ox}(V_{GS} - V_{TH})} \right]^{\text{UEXP}} & \text{for Level 2} \\ \mu_o \left[\dfrac{\text{UCRIT} \cdot \epsilon_{si}}{C_{ox}(V_{GS} - V_{TH} - \text{UTRA} \cdot V_{DS})} \right]^{\text{UEXP}} & \text{for Level 3} \end{cases} \quad (4.2\text{-}36)$$

The parameters UCRIT, UTRA and UEXP are SPICE input parameters used to characterize mobility degradation.

4.2.3 High-Frequency MOSFET Model

The high-frequency MOSFET model is obtained from the dc model by adding the identifiable parasitic capacitances to the dc model previously discussed. Parasitic device capacitors in SPICE are essentially modeled as in Section 3.1.3 of Chapter 3. Those capacitors that are voltage independent are modeled by

$$C = \frac{\epsilon A}{t} \quad (4.2\text{-}37)$$

where ϵ is the dielectric constant (permittivity), A is the area of the intersection of the two plates and t is the dielectric thickness. The voltage independent capacitors are comprised of those that are operation-region dependent and those that are not.

The operation-region independent capacitors are comprised of those overlap capacitors that appear on the periphery of the MOSFET. A top view of these parasitic capacitors appears in Fig. 4.2-2. All are essentially rectangular in shape.

The effective area of the overlap component of the gate–source capacitance is $W \cdot \text{LD}$ where W is the channel width and LD is the lateral diffusion of the source. From (4.2-37) the gate–source overlap capacitor, C_{GSOL}, can be expressed as

$$C_{GSOL} = \frac{\epsilon \, \text{LD} \cdot W}{t} \quad (4.2\text{-}38)$$

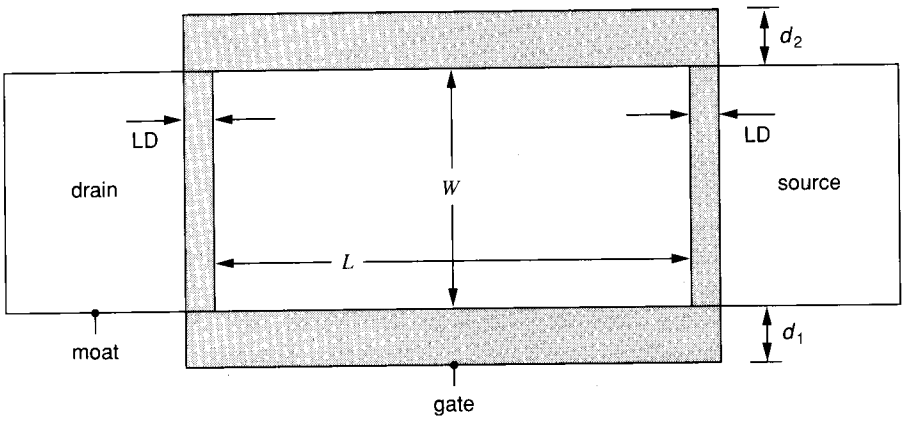


FIGURE 4.2-2
Top view of operation-region independent, or overlap (shaded) capacitors, in MOS transistors.

or

$$C_{GSOL} = C_{GSO}W \tag{4.2-39}$$

where $C_{GSO} = \epsilon LD/t$ represents the overlap capacitance per unit width of the gate. C_{GSO} serves as an input parameter in SPICE to model the overlap capacitance. Since the dielectric thickness is the same as the gate oxide thickness, this parasitic has an area capacitance density of C_{ox}. If C_{GSO} is not entered in SPICE, C_{GSOL} is calculated from

$$C_{GSOL} = (C_{ox})(LD)W \tag{4.2-40}$$

where C_{ox} is calculated via either the entered or defaulted value of the gate oxide thickness, T_{ox}. The gate-drain overlap capacitance is modeled in the same manner.

From Fig. 4.2-2, it follows that the gate–bulk overlap capacitance is linearly proportional to L and dependent upon d_1 and d_2. The dielectric thickness, however, is not constant for this parasitic. The dielectric thickness of the gate–bulk overlap is essentially equal to the gate oxide thickness on the sides adjacent to the channel and equal to the height of the field oxide on the sides farthest from the channel. Although it cannot be modeled by (4.2-37), it is voltage independent. Since it is proportional to L, it is modeled by

$$C_{GBOL} = C_{GBO}L \tag{4.2-41}$$

where C_{GBO} represents the total gate–bulk capacitance per unit length of the device. C_{GBO} serves as an input parameter in SPICE to characterize the gate–bulk overlap. Since field oxide thickness is not considered in the MOSFET model, and since d_1 and d_2 are layout dependent, the C_{GB0} parameter must be entered if the effects of gate–bulk overlap are to be included in the model. It is common practice to assume that $d_1 = d_2 = d$ where d is the minimum overlap of the poly over the moat. With this assumption, any bulk-substrate capacitance associated with a larger gate polysilicon region is accounted for by adding an additional parasitic capacitance to the circuit schematic from gate to substrate.

Those capacitors that are voltage dependent are the pn junction capacitors. They occur between bulk and source, bulk and drain, and bulk and channel. They are modeled as in Chapter 3 by

$$C = \frac{C_{j0}A}{(1 - V_F/\phi_B)^n} \qquad \text{for } V_F < \text{FC} \cdot \phi_B \tag{4.2-42}$$

where C_{j0} is the zero-bias junction capacitance density. FC is called the forward bias capacitance coefficient (FC $\simeq$ .5) which defines the region where (4.2-42) is valid, ϕ_B is the barrier potential, n is a constant that characterizes the junction type, A is the junction cross-sectional area, and V_F is the forward bias on the junction (which is usually negative for MOS devices). The modeling of the junction capacitors is complicated somewhat by the actual geometry of the pn junction. A cross section of a pn diffused junction is shown in Fig. 4.2-3. The junction is not planar. The impurity concentrations in the p and n type materials at the bottom of the junctions are different than the concentrations along the sidewalls causing the grading coefficient, n, to vary as a function of position. Although the sidewall capacitances become negligible for large structures, they may actually dominate for small or narrow junctions. The total junction capacitance associated with the "reverse biased" (actually for $V_F < \text{FC} \cdot \phi_B$) junction of either the source or drain is thus

$$C_{\text{RB, TOTAL}} = \frac{\text{CJ} \cdot A}{[1 - (V_F/\phi_B)]^{\text{MJ}}} + \frac{\text{CJSW} \cdot P}{[1 - (V_F/\phi_B)]^{\text{MJSW}}} \tag{4.2-43}$$

where CJ is the zero-bias bottom capacitance area density, CJSW is the zero-bias sidewall capacitance per unit length of the perimeter, MJ is the bottom junction

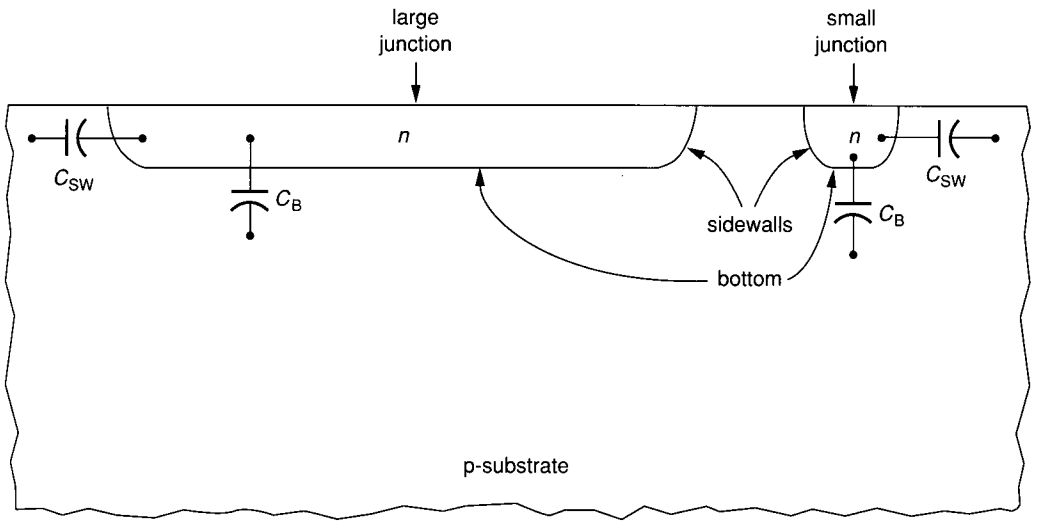


FIGURE 4.2-3
Cross section of diffused region showing parasitic junction capacitors.

grading coefficient, FC is the forward bias coefficient (which defines the region where (4.2–43) remains valid), and MJSW is the sidewall grading coefficient. A is the junction bottom area and P is the junction sidewall perimeter. The parameters FC, CJ, CJSW, MJ, MJSW and ϕ_B can be entered in SPICE on the .MODEL card (line). The parameters A and P for the drain and source junctions must be entered on the device card (line). If not input, CJ is calculated internally from N_{SUB} (if input), under the assumption of a step graded junction, from the expression

$$\mathrm{CJ} = \sqrt{\frac{\epsilon_{si} q N_{SUB}}{2\phi_B}} \tag{4.2-44}$$

As an alternative to specifying the drain and source geometries and the junction capacitance density, the user can specify the overriding parameters C_{BD} and C_{BS} which represent the total zero-bias bottom capacitance of the bulk-drain and bulk-source junctions, respectively. These are then used in place of CJ · A in (4.2-43).

Under forward bias ($V_F > \mathrm{FC}\cdot\phi_B$), the total junction capacitances are modeled by

$$C_{FB.\,TOTAL} = \frac{\mathrm{CJ}\cdot A}{(1-\mathrm{FC})^{(1+\mathrm{MJ})}}\left[1 - \mathrm{FC}(1+\mathrm{MJ}) + \frac{V_{BS}}{\phi_B}\mathrm{MJ}\right] + \frac{\mathrm{CJSW}\cdot P}{(1-\mathrm{FC})^{(1+\mathrm{MJSW})}}\left[1 - \mathrm{FC}(1+\mathrm{MJSW}) + \frac{V_{BS}}{\phi_B}\mathrm{MJSW}\right] \tag{4.2-46}$$

This approximation represents a linear continuation of the reverse-bias capacitance which agrees functionally and in the first derivative at the transition point, $V_F = \mathrm{FC}\cdot\phi_B$ (see Problem 3.31 of Chapter 3).

Finally, the operation-region dependent capacitances associated with the channel region itself must be considered. These are essentially distributed capacitances; as such they are more difficult to model. Furthermore, to ease calculations these parasitics are subsequently lumped internally and added to the operation-region independent components of the gate–source, gate–drain, gate–bulk, source–bulk, and drain–bulk capacitors discussed previously. Depending on the operating region, some of the channel capacitances are voltage independent and are modeled by (4.2-37), while others are actually junction capacitances modeled by (4.2-42). The user need not enter any additional parameters; the parasitic channel capacitances are calculated internally from the parameters that characterize the operation-region independent capacitors discussed above. The user is, however, at the mercy of the approximations employed in SPICE to model the channel capacitances. Some industrial groups are not satisfied with the channel capacitance modeling in SPICE and have made modifications which they believe offer some improvements. The exact formulation of the channel capacitances is quite involved and beyond the scope of this text. Details can be found in references 16 and 17, as well as in the SPICE source code itself [6]. The total parasitic capacitances (fixed plus voltage dependent) associated with the lumped approximation used in SPICE are basically as indicated in Fig. 4.2-4.

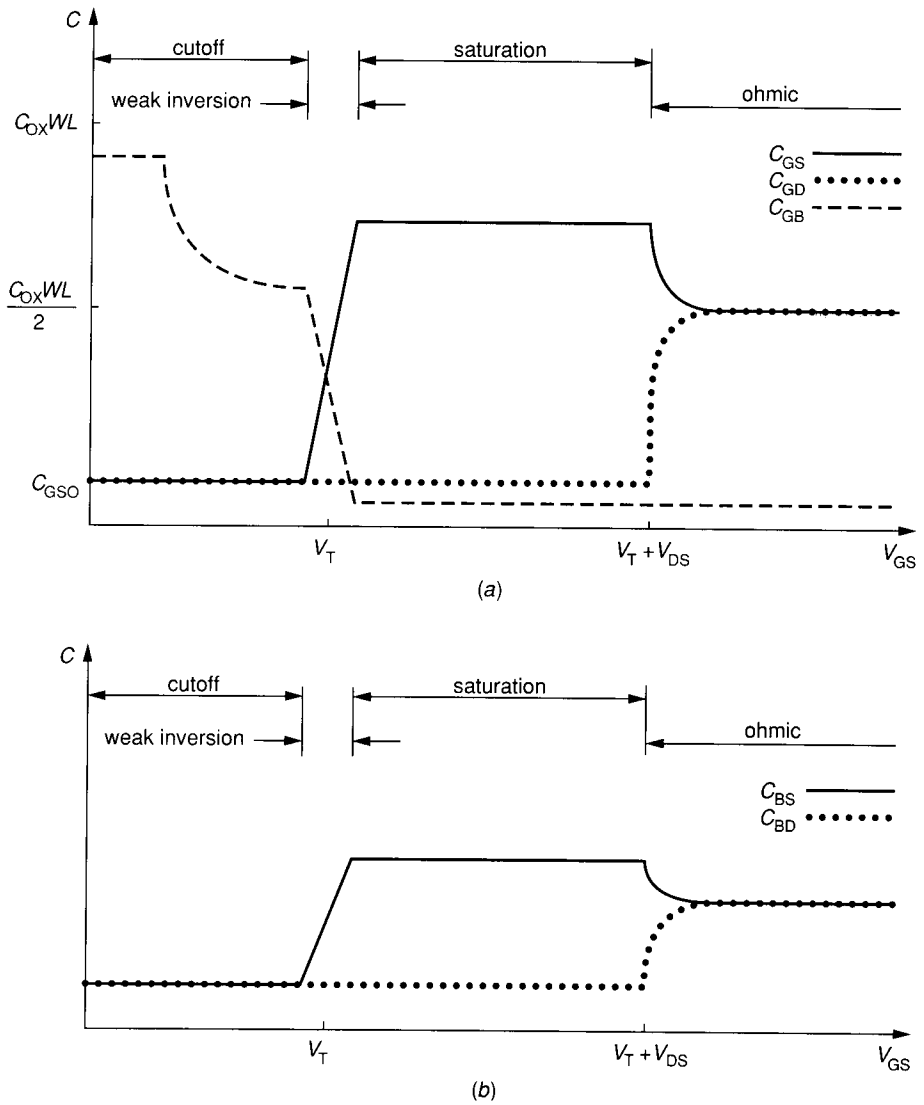


FIGURE 4.2-4
Lumped parasitic capacitances for MOSFET as a function of operating point: (*a*) Associated with gate charge, (*b*) Associated with bulk charge.

4.2.4 Noise Model of the MOSFET

There are four noise-current generators modeled in the MOSFET device model in SPICE.[18] Two of these represent thermal noise associated with the parasitic series resistances in the drain and source. These are modeled by spectral densities of

$$S_{\mathrm{IRD}} = \frac{4kT}{\mathrm{RD}} \tag{4.2-47}$$

and

$$S_{\mathrm{IRS}} = \frac{4kT}{\mathrm{RS}} \tag{4.2-48}$$

respectively, where k is Boltzmann's constant, T is the temperature in °K, and RD and RS represent the drain and source parasitic resistances.

The other two noise-current generators are modeled as current sources from drain to source. One represents white shot noise and the other flicker ($1/f$) noise. These are characterized in the saturation region by spectral densities of[1]

$$S_{\mathrm{W}} = \frac{8kTg_{\mathrm{m}}}{3} \tag{4.2-49}$$

and

$$S_f = \frac{(K_{\mathrm{F}})I_{\mathrm{DQ}}^{A_{\mathrm{F}}}}{fC_{\mathrm{ox}}WL_{\mathrm{eff}}} \tag{4.2-50}$$

where K_{F} and A_{F} are user enterable parameters, g_{m} is the small signal transconductance gain at the Q-point, I_{DQ} is the quiescent drain current, L_{eff} is the effective channel length and f is frequency in Hz. All noise sources are assumed to be uncorrelated. S_{W} and S_f add to obtain the overall noise spectral density as discussed in Sec. 3.1.8.

4.2.5 Temperature Dependence of the MOSFET

Several of the parameters that characterize the MOSFET are temperature dependent. Specifically, SPICE models the temperature dependence of the parameters K', V_{T0}, μ_{o}, ϕ, ϕ_{B}, I_{S}, J_{S}, C_{BD}, C_{BS}, CJ, CJSW, $\mathrm{K_F}$ and $\mathrm{A_F}$. The basic equations used to characterize the temperature dependence in most situations are given below. See Reference 9 and subroutine TMPUPD of the SPICE source code for additional details.

$$K'(T) = \left(\frac{T}{T_1}\right)^{\frac{3}{2}} K'(T_1) \tag{4.2-51}$$

$$\mu_{\mathrm{o}}(T) = \left(\frac{T}{T_1}\right)^{\frac{3}{2}} \mu_{\mathrm{o}}(T_1) \tag{4.2-52}$$

$$I_S(T) = I_S(T_1)e^{\left[\frac{EG(T)}{V_t(T)} - \frac{EG(T_1)}{V_t(T_1)}\right]} \quad (4.2\text{-}53)$$

$$J_S(T) = J_S(T_1)e^{\left[\frac{EG(T)}{V_t(T)} - \frac{EG(T_1)}{V_t(T_1)}\right]} \quad (4.2\text{-}54)$$

$$\phi(T) = \phi(T_1) \cdot (T/T_1) + \phi_{BF}(T) \quad (4.2\text{-}55)$$

$$\phi_B(T) = \phi_B(T_1) \cdot (T/T_1) + \phi_{BF}(T) \quad (4.2\text{-}56)$$

$$C_{BD}(T) = C_{BD}(T_1) \cdot [1 + \theta_C(T)] \quad (4.2\text{-}57)$$

$$C_{BS}(T) = C_{BS}(T_1) \cdot [1 + \theta_C(T)] \quad (4.2\text{-}58)$$

$$CJ(T) = CJ(T_1) \cdot [1 + \theta_C(T)] \quad (4.2\text{-}59)$$

$$CJSW(T) = CJSW(T_1) \cdot [1 + \theta_C(T)] \quad (4.2\text{-}60)$$

$$K_F(T) = K_F(T_1) \cdot [\phi_B(T)/\phi_B(T_1)] \quad (4.2\text{-}61)$$

$$A_F(T) = A_F(T_1) \cdot [\phi_B(T)/\phi_B(T_1)] \quad (4.2\text{-}62)$$

where T_1 is any reference temperature in °K , $V_t = kT/q$, and the parameters EG, ϕ_{BF}, and θ_C are defined respectively by the equations

$$EG(T) = [1.16 - (.000702T^2)/(T + 1108)]\text{volts} \quad (4.2\text{-}63)$$

$$\phi_{BF}(T) = -3V_t \ln (T/T_1) - EG(T) + [EG(T_1)] \cdot (T/T_1) \quad (4.2\text{-}64)$$

and

$$\theta_C(T) = MJ \cdot \{0.0004(T - T_1) + 1 - [\phi_B(T)/\phi_B(T_1)]\} \quad (4.2\text{-}65)$$

4.3 DIODE MODEL

Individual diodes are modeled by a two-step process in SPICE.[1,3,5] The device element line (card) contains information about the nodal location of the device in the circuit as well as geometrical information (relative junction cross-sectional area) and optional initial condition variables useful in transient analyses. In the device element line, reference is made to a specific device model. The .MODEL line (card) contains generic information about the electrical characteristics of devices formed in the process based upon the characterizing process parameters. Each diode has a separate device element line. Typically many devices will reference a single .MODEL line. Most of the diode modeling information can be found in subroutines DIODE and MODCHK in the SPICE source code. As is the case for all device models in SPICE, the small signal parameters which characterize the small signal operation of the diode are calculated from the appropriate derivatives. A philosophy distinctly different from that used for characterizing MOS processes has been adopted for characterizing the process used to fabricate diodes. This difference lies in that the characteristics of a specific

"reference diode" are specified in the .MODEL line. The size of the reference diode is conceptually arbitrary although it is advised to select a reference that is geometrically similar in size and shape to those devices that will be modeled. In the device element line (card) the *relative area* of the reference diode used to characterize the model is specified.

The diode is modeled as the series combination of a resistor, r_S, and a non-ideal diode, D2, shunted by a parasitic capacitor C_D, as indicated in Fig. 4.3-1. The resistor, r_S, accounts for both the series resistance of the diode as well as high-level injection effects.[3.19] It is assumed to be an ideal resistor. In this section, emphasis will be placed upon the model of the series diode, D2, of Fig. 4.3-1*b*. As indicated in Fig. 4.3-1*b*, the current of diode D2 is modeled as the sum of a dc (large signal) current, denoted by I_{DC}, and a current that flows through a parasitic shunting capacitance associated with the pn junction. The large signal current and parasitic capacitance current will be considered separately in the following sections.

4.3.1 Large Signal Diode Current

The large signal diode current, I_{DC} in Fig. 4.3-1*b*, is modeled by that given in the standard diode equation

$$I_{DC} = I_S A_n [e^{V_D/(nV_t)} - 1] \tag{4.3-1}$$

where, as discussed in Chapter 3,

$$V_t = \frac{kT}{q} \tag{4.3-2}$$

I_S = saturation current

and

n = emission coefficient.

The parameter A_n represents the *normalized* cross-sectional area of the junction. It is a dimensionless parameter that is entered on the device element line; it represents the ratio of the cross-sectional area of the device on the device element

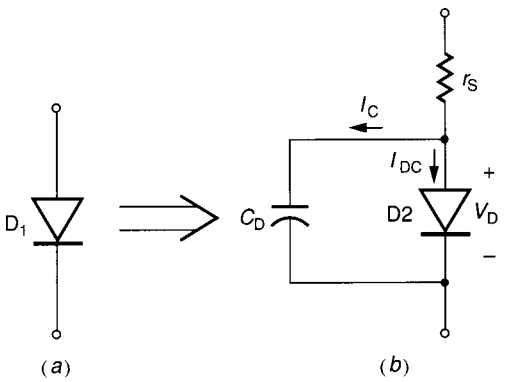


FIGURE 4.3-1
Diode model in SPICE: (*a*) Physical two-terminal device, (*b*) Equivalent circuit.

line to the reference model which is characterized on the .MODEL line. If not specified, SPICE adopts a default value of $A_n = 1$. The reverse breakdown voltage, BV, is not of major concern in VLSI design since BV generally exceeds the maximum voltages which will be permitted in VLSI circuits.

4.3.2 High-Frequency Diode Model

At high frequencies the parasitic junction capacitance of the diode plays a major role in the performance of the diode. The junction capacitance also affects the transient response. In the following the capacitance is defined by the expression

$$C_D = \frac{dQ}{dV_D} \tag{4.3-3}$$

C_D thus represents the small signal parasitic capacitance. In general, C_D is strongly a function of the instantaneous dc operating point of the diode. Although the model for C_D will be given here, the charge Q is regularly used internally in SPICE for transient analysis.

As discussed in Chapter 3 and Section 4.2, the characterization of a junction capacitor under reverse bias is different from the characterization under forward bias. Under reverse bias (actually for $V_D < \text{FC} \cdot \phi_B$), the capacitance is modeled by the equation

$$C_D = \frac{C_{jo}A_n}{[1 - (V_D/\phi_B)]^m} + \frac{\tau I_S A_n}{n V_t} e^{V_D/(nV_t)} \tag{4.3-4}$$

where I_S, A_n, n, and V_t are as previously defined, and the remaining parameters are defined by

C_{jo} = zero-bias junction capacitance
ϕ_B = capacitance barrier potential
m = grading coefficient
τ = transit time
FC = coefficient for forward/reverse bias transition

As was the case for I_S, it should be noted that C_{jo} is the zero-bias junction capacitance of the specific area device referred to by the .MODEL line. Although the first term on the right-hand side of (4.3-4) is essentially functionally equivalent to that used in the model of the junction capacitance for the MOSFET, (4.2-42) of Section 4.2, it should be emphasized that in SPICE C_{jo} represents the capacitance density in (4.2-42), whereas C_{jo} represents the capacitance of the reference diode itself in (4.3-4).

The second term on the right-hand side of (4.3-4) arises from the charge stored in the junction due to minority carrier injection. The transit time, τ, characterizes this capacitance.

For $V_D > \text{FC} \cdot \phi_B$, SPICE models the capacitance, C_D, with the equation

$$C_D = \frac{C_{jo}A_n}{(1 - \text{FC})^{(1+m)}}\left[1 - \text{FC}[1 + m] + \frac{mV_D}{\phi_B}\right] + \frac{\tau I_S A_n}{n V_t} e^{V_D/(nV_t)} \tag{4.3-5}$$

The first term on the right-hand side of (4.3-5) represents a continuous and differentiable linear extension of the first term on the right-hand side of (4.3-4) across the boundary V_D = FC $\cdot\phi_B$. The second terms on the right-hand side, of Eqs. 4.3-4 and 4.3-5 are identical.

4.4 BJT MODEL

The SPICE model of the BJT is based upon a modified Gummel–Poon model. [20,21] Simulations based upon the simpler Gummel–Poon model discussed in Chapter 3 can also be readily made by setting the appropriate Ebers–Moll parameters to zero as will be discussed later in this section. Use of the Ebers–Moll model in the early stages of a simulation may be useful for verifying theoretical hand calculations.

The bipolar junction transistor is modeled by two input lines (cards) in SPICE. The device line (card) is used for indicating the nodal connections of the BJT in a circuit. It is also used to reference a specific model, by name, which contains process information. An optional normalized parameter on the device line, A_n, is used to indicate the ratio of the area of the emitter to the emitter area of the device of the referenced model. An optional initial condition parameter can also be included on the device line if desired.

The second input line (card) that is used to model the BJT is the .MODEL line. SPICE version 2G.6 provides for user entry of up to 40 parameters on the .MODEL line for characterizing the device. As was the case with the diode, a user-selected reference transistor is used to characterize the bipolar process. The BJT model information is contained primarily in subroutines MODCHK and BJT in the SPICE source code. MODCHK does preprocessing of some of the input parameters (e.g., the reciprocals of some parameters are actually used as variables in the source code rather than the parameters themselves). The model itself basically appears in subroutine BJT.

As is the case for the other semiconductor models in SPICE, the BJT model is characterized by four types of input parameters. These are 1) large signal or dc parameters, 2) charge storage or capacitance parameters, 3) noise parameters, and 4) temperature characterization parameters.

The small signal low-frequency model used in SPICE is obtained from a symbolic differentiation of the large signal current equations evaluated at the dc operation point. As is the case for all small signal analyses in SPICE, the small signal model of the BJT is linear and thus the small signal simulation gives no distortion information. (Distortion information at a specific frequency can be obtained from a much more time consuming transient response with a sinusoidal excitation of fixed frequency and amplitude.) To obtain reliable distortion information, it is crucial that the transient analysis interval is long enough to guarantee essentially steady state operation.

A series resistance is modeled in series with each lead of the BJT as indicated in Fig. 4.4-1. These resistances are input parameters in SPICE. In the model discussion that follows, all formulation is relative to transistor T2 (denoted by nodes C, B, and E) in this figure; specifically, V_{BE} and V_{CE} represent the base–emitter and collector–emitter voltages of T2 rather than the actual base–emitter and collector–emitter voltages of the device (denoted by nodes C_A, B_A, and E_A)

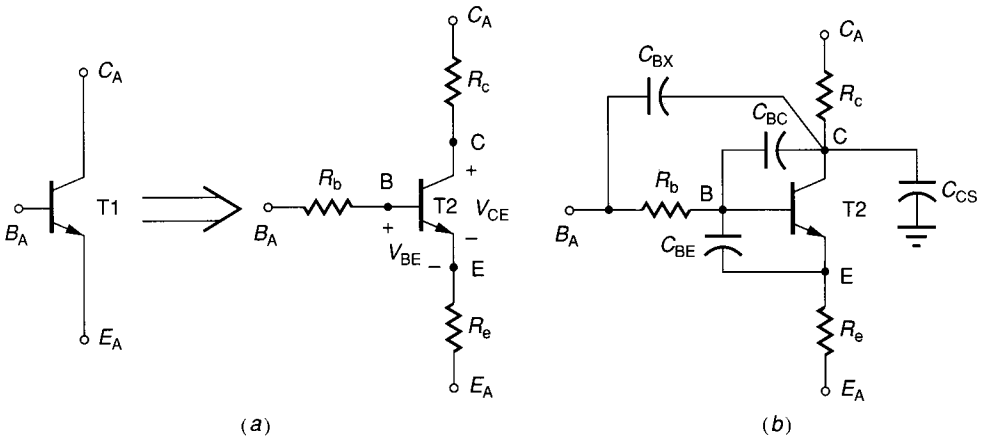


FIGURE 4.4-1
Modeling of the BJT in SPICE: (*a*) dc modeling, (*b*) High-frequency modeling.

which is to be modeled, T1. In the model that follows, junction breakdown voltages will not be discussed in detail since, with the exception of the reverse base-emitter breakdown, voltage levels in bipolar integrated circuits are usually considerably below the breakdown voltages of the BJT.

4.4.1 Large Signal BJT Model

The collector current and base current are characterized by the equations

$$I_C = \frac{I_S A_n}{Q_B}\left(e^{V_{BE}/(NF\cdot V_t)} - 1\right) - I_S A_n\left(\frac{1}{Q_B} + \frac{1}{BR}\right)\left(e^{V_{BC}/(NR\cdot V_t)} - 1\right) - I_{SC}A_n\left(e^{V_{BC}/(NC\cdot V_t)} - 1\right) \quad (4.4\text{-}1)$$

$$I_B = \frac{I_S A_n}{BF}\left(e^{V_{BE}/(NF\cdot V_t)} - 1\right) + \frac{I_S A_n}{BR}\left(e^{V_{BC}/(NR\cdot V_t)} - 1\right) + I_{SE}A_n\left(e^{V_{BE}/(NE\cdot V_t)} - 1\right) + I_{SC}A_n\left(e^{V_{BC}/(NC\cdot V_t)} - 1\right) \quad (4.4\text{-}2)$$

where $V_t = kT/q$
A_n = normalized emitter area ratio
I_S = saturation current
I_{SE} = B-E leakage saturation current
I_{SC} = B-C leakage saturation current
NF = forward current emission coefficient
NR = reverse current emission coefficient
NE = B-E leakage current emission coefficient
NC = B-C leakage current emission coefficient
BF = ideal maximum forward β
BR = ideal maximum reverse β

and

$$Q_B = \left[\frac{1}{1 - (V_{BC}/V_{AF}) - (V_{BE}/V_{AR})}\right] \cdot \left[\frac{1 + \sqrt{1 + 4\left[(I_S/I_{KF})(e^{V_{BE}/(NF \cdot V_t)} - 1) + (I_S/I_{KR})(e^{V_{BC}/(NR \cdot V_t)} - 1)\right]}}{2}\right] \quad (4.4\text{-}3)$$

The parameters in (4.4-3) are defined as

V_{AF} = Forward Early Voltage
V_{AR} = Reverse Early Voltage
I_{KF} = Corner for forward current gain roll-off
I_{KR} = Corner for reverse current gain roll-off

This completes the large signal model of the BJT. A discussion of the characterizing parameters in the BJT model follows. In addition to providing insight into how these parameters impact performance of the BJT, this discussion should provide a mechanism for obtaining SPICE parameters from measured device data.

Although it may appear that all dependence of I_C and I_B on V_{BE} and V_{BC} is exponential, it can be seen from (4.4-3) that Q_B is a complicated function of V_{BC} and V_{BE}. If I_{KF} and I_{KR} are neglected (i.e., $I_{KF} = I_{KR} = \infty$), then Q_B reduces to

$$Q_B = \left(1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}}\right)^{-1} \quad (4.4\text{-}4)$$

so that the $\frac{1}{Q_B}$ term in (4.4-1) becomes

$$Q_B^{-1} = 1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}} = 1 + \frac{V_{CE}}{V_{AF}} - V_{BE}\left(\frac{1}{V_{AF}} + \frac{1}{V_{AR}}\right) \quad (4.4\text{-}5)$$

which is approximately equal to the multiplying factor used to model Early Voltage effects in the extended Ebers-Moll model of Chapter 3. Even if I_{KF} and I_{KR} effects are included, Q_B can be approximated by (4.4-4) until V_{BE} or V_{BC} becomes quite large, since I_{KF} is typically about ten orders of magnitude larger than I_S. For large V_{BE} or V_{BC}, however, I_C varies essentially linearly with $e^{V_{BE}/2NF \cdot V_t}$ or $e^{V_{BC}/2NR \cdot V_t}$.

Considerable insight into how the parameters affect device performance can be obtained by plotting I_C and I_B versus one device branch voltage, V_{BE} or V_{BC}, with the other branch voltage set to zero. For brevity, only the $V_{BC} = 0$ case will be considered here. The analysis for the $V_{BE} = 0$ case is essentially a mirror image of the $V_{BC} = 0$ analysis.

Under the assumption that $V_{BC} = 0$, (4.4-1), (4.4-2) and (4.4-3) simplify to

$$I_C = \frac{I_S A_n}{Q_B}(e^{V_{BE}/(NF \cdot V_t)} - 1) \quad (4.4\text{-}6)$$

$$I_B = \frac{I_S A_n}{BF}\left(e^{V_{BE}/(NF \cdot V_t)} - 1\right) + I_{SE} A_n \left(e^{V_{BE}/(NE \cdot V_t)} - 1\right) \tag{4.4-7}$$

$$Q_B = \left[\frac{1}{1 - (V_{BE}/V_{AR})}\right]\left[\frac{1 + \sqrt{1 + 4(I_S/I_{KF})\left(e^{V_{BE}/(NF \cdot V_t)} - 1\right)}}{2}\right] \tag{4.4-8}$$

A plot of I_C and I_B versus V_{BE} for $V_{BE} < 0$ is shown in Fig. 4.4-2. The parameter A_n, which denotes the relative emitter area, is obtained from geometrical information. The projection of the linear portion of the I_C curve intercepts the I axis at $-I_S A_n$. The slope of the linear portion of the I_C curve can subsequently be used to determine V_{AR}. The vertical axis intercept of the projection of the linear portion of the I_B curve can be used to determine I_{SE} since I_{SE} is typically about four orders of magnitude larger than I_S/BF . Although the $V_{BE} < 0$ curves can be used to determine I_S, I_{SE} and V_{AR}, they are most useful for the V_{AR} determination. The parameters I_S and I_{SE} are typically determined from the $V_{BE} > 0$ plots.

A plot of I_C and I_B versus V_{BE} for $V_{BE} > 0$ is shown in Fig. 4.4-3 on a graph with a logarithmic scale for the vertical axis. Also shown are four straight lines which essentially represent asymptotic behavior of the BJT over a fairly wide range of V_{BE} values. The equations of these asymptotic lines are easily derived from (4.4-6)–(4.4-8). Several of the dc parameters that characterize the BJT can be readily determined from the curves shown in Fig. 4.4–3. A sequence of calculations follows for determining some of the dc parameters after V_{AR} has been determined from Fig. 4.4-2.

First, I_S and I_{SE} can be determined from the y-intercepts of Line 3 and Line 2, respectively. With I_S known, BF can be determined from the y-intercept of Line 4. I_{KF} can be determined from either the vertical axis intercept of Line 1 or the y-coordinate of the intersection of Lines 1 and 3. NF can be obtained

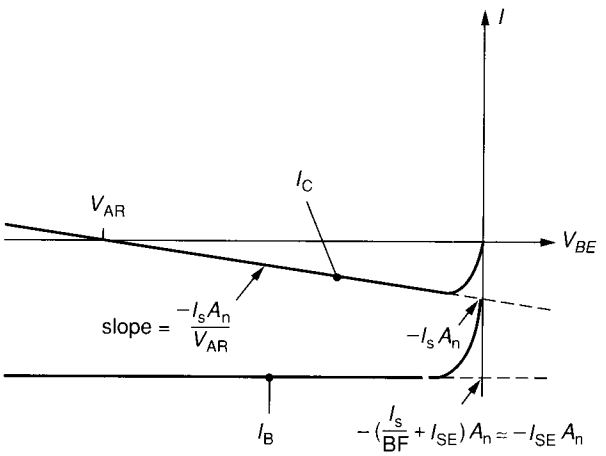
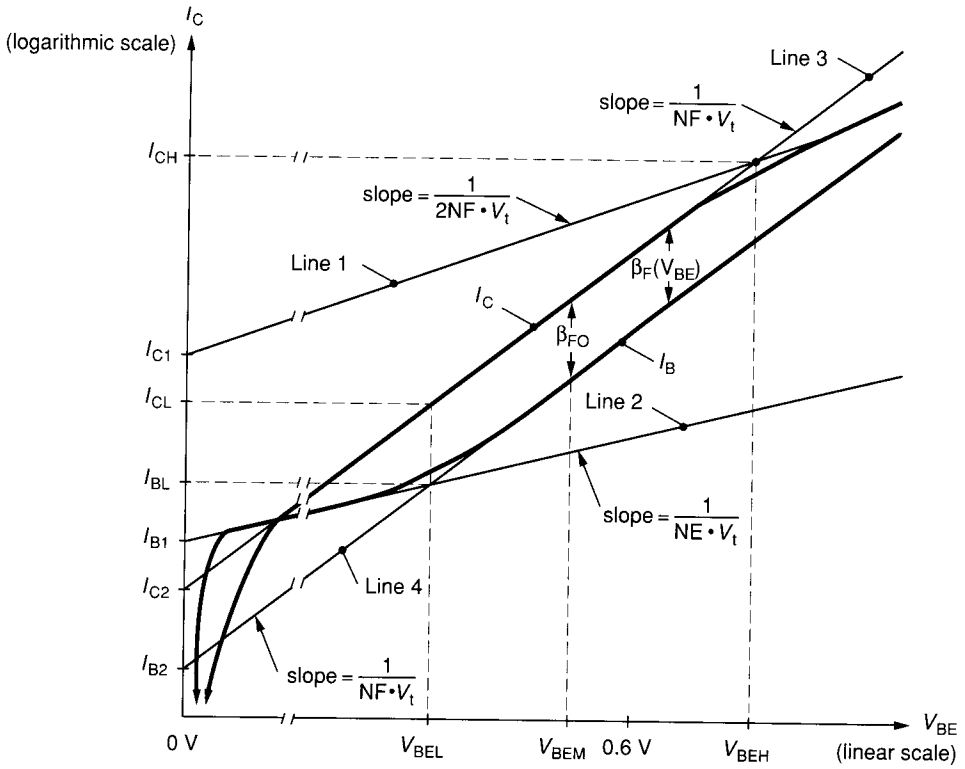


FIGURE 4.4-2
Plot of collector and base current vs. V_{BE} for $V_{BC} = 0, V_{BE} < 0$.



$$V_{BEL} = \frac{V_t \cdot NE \cdot NF}{NE - NF} \ln\left(\frac{I_{SE} \cdot BF}{I_S}\right)$$

$$V_{BEH} = V_t \cdot NF \cdot \ln\left(\frac{I_{KF}}{I_S}\right)$$

$$\text{Line 1: } I = \left(1 + \frac{0.6\text{ V}}{V_{AR}}\right) A_n \sqrt{I_S I_{KF}}\, e^{\frac{V_{BE}}{2NF \cdot V_t}}$$

$$\text{Line 2: } I = I_{SE} A_n\, e^{\frac{V_{BE}}{NE \cdot V_t}}$$

$$\text{Line 3: } I = \left(1 + \frac{0.6\text{ V}}{V_{AR}}\right) I_S A_n\, e^{\frac{V_{BE}}{NF \cdot V_t}}$$

$$\text{Line 4: } I = \frac{I_S A_n}{BF}\, e^{\frac{V_{BE}}{NF \cdot V_t}}$$

$$I_{CH} = I_{KF} A_n \left(1 + \frac{0.6\text{ V}}{V_{AR}}\right)$$

$$I_{C1} = A_n \sqrt{I_S I_{KF}} \left(1 + \frac{0.6\text{ V}}{V_{AR}}\right)$$

$$I_{CL} = I_{SE}\, A_n \left(\frac{I_{SE} \cdot BF}{I_S}\right)^{\frac{NF}{NE - NF}}$$

$$I_{BL} = A_n\, I_{SE}^{\frac{NE}{NE - NF}} \left(\frac{I_S}{BF}\right)^{\frac{NF}{NF - NE}}$$

$$I_{B1} = I_{SE}\, A_n$$

$$I_{C2} = I_S\, A_n \left(1 + \frac{0.6\text{ V}}{V_{AR}}\right)$$

$$I_{B2} = \frac{I_S\, A_n}{BF}$$

FIGURE 4.4-3
Plot of collector current and base current vs. V_{BE} for $V_{BC} = 0$, $V_{BE} > 0$ (logarithmic scale on vertical axis).

from the slope of Lines 1, 3, or 4, while NE can be determined from the slope of Line 2. At this point, it is easy to verify that *all* parameters in the dc model of (4.4-1)–(4.4-3) can be determined from the plots in Fig. 4.4-2 and Fig. 4.4-3 and the corresponding plots for $V_{BE} = 0$, $V_{BC} > 0$.

The current gain of the BJT is often of interest. Defining the forward current gain (a similar procedure can be used for the reverse current gain) by the expression

$$\beta_F = \left.\frac{I_C}{I_B}\right|_{V_{BC}=0} \tag{4.4-9}$$

it follows from the curves in Fig. 4.4-3 that β_F is V_{BE} dependent. For a rather large range of V_{BE}, however, it is essentially constant and (neglecting V_{AR} effects) approximately equal to

$$\beta_F = BF \simeq \beta_{FO} \tag{4.4-10}$$

where β_{FO} represents the maximum value of β_F for $V_{BEL} < V_{BE} < V_{BEH}$ and where V_{BEL} and V_{BEH} are as defined in Fig. 4.4-3. V_{BEM} denotes value of V_{BE} where β_F is maximum. At lower V_{BE}, β_F decreases due to changes in the characteristics of I_B; for higher V_{BE}, β_F decreases due to changes in the characteristics of I_C. A plot of β_F versus V_{BE} as defined by Eq. 4.4-9 appears in Fig. 4.4-4. It can be seen from Figs. 4.4-3 and 4.4-4 that the parameter I_{KF} is approximately equal to the value of collector current where high-current roll-off in β_F occurs, which explains the name for I_{KF}, "corner for forward current gain roll-off." The corresponding low-frequency roll-off, which occurs at $V_{BE} = V_{BEL}$, is not characterized by a single parameter but is strongly dependent upon the B–E leakage saturation current, I_{SE}.

This section concludes with a discussion of how the SPICE model parameters can be specified to do simulations based upon the simplified Ebers–Moll model of Chapter 3, characterized by Eqs. 3.3-1 and 3.3-2.

It follows from Eqs. 4.4-1–4.4-3 that if $I_{SE} = I_{SC} = 0$, $I_{KF} = I_{KR} = \infty$, $V_{AF} = V_{AR} = \infty$ and NF = NR = 1, the model will agree with this Ebers–Moll model. Since these variable assignments are the default values, the user only needs to specify IS, BF, and BR to use the simplified dc Ebers–Moll model.

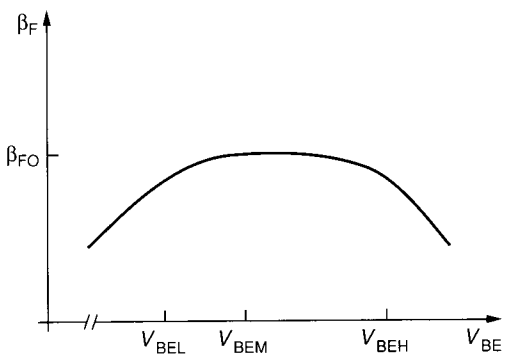


FIGURE 4.4-4
Forward current gain of BJT vs. $V_{BE}(V_{BC} = 0)$.

4.4.2 High-Frequency BJT Model

The high-frequency model of the BJT used in SPICE is obtained by adding three parasitic capacitors to the transistor T2 in Fig. 4.4-1 and one capacitor, CBX, between the base of T1 (node B_A) and the collector of T2 (node C). The parasitic capacitors are, in general, voltage dependent. The capacitor values used in SPICE are defined by the derivative

$$C = \frac{dQ}{dV} \tag{4.4-11}$$

where Q is the charge on the capacitor and V is the corresponding port voltage. Seventeen parameters are used to characterize the four parasitic capacitors in SPICE.

The parasitic capacitors are, in general, modeled by the parallel combination (sum) of a depletion region capacitor and a capacitor which occurs due to charge accumulation in the depletion region. The depletion region capacitor is voltage dependent and is modeled by Eqs. 3.2-8 and 3.2-9 of Chapter 3. The capacitor attributed to the charge accumulation is current dependent. Finally, under forward bias the model for the parasitic capacitors has a different parametric form, than under reverse bias. The voltage where transition must be made from the reverse bias parametric capacitance model to the forward bias parametric model is termed the transition voltage. A summary of the parasitic capacitors used in SPICE 2G.6 is shown in Table 4.4-1.

The depletion region reverse-biased junction capacitors are defined by the expressions

$$C_{BEDR} = A_n C_{JE}\left(1 - \frac{V_{BE}}{\phi_B}\right)^{-M_{JE}} \tag{4.4-12}$$

$$C_{BCDR} = \theta A_n C_{JC}\left(1 - \frac{V_{BC}}{\phi_C}\right)^{-M_{JC}} \tag{4.4-13}$$

$$C_{CSDR} = A_n C_{JS}\left(1 - \frac{V_{CS}}{\phi_S}\right)^{-M_{JS}} \tag{4.4-14}$$

$$C_{XSDR} = (1 - \theta) A_n C_{JC}\left(1 - \frac{V_{B'C}}{\phi_C}\right)^{-M_{JC}} \tag{4.4-15}$$

where $M_{JE}, M_{JS}, M_{JC}, C_{JE}, C_{JS}$ and C_{JC} are input parameters. ϕ_B, ϕ_S, ϕ_C, and θ are also SPICE input parameters, denoted by PB, PS, PC and XCJC, respectively. The parameter θ represents the percentage of the B–C capacitance which is to be associated with the internal base node (base of T2 in Fig. 4.4-1). $V_{B'C}$ is the voltage from the base of T1 to the collector of T2 in Fig. 4.4-1.

The transition voltages $V_{BET}, V_{BCT}, V_{CST}$ and V_{XST} are FC · ϕ_B, FC · ϕ_C, 0 V, and FC · ϕ_C respectively where FC is a SPICE input parameter used to characterize the transition.

The forward biased depletion junction capacitors $C_{BEDF}, C_{BCDF}, C_{CSDF}$, and C_{XSDF} are the continuous and differentiable linear extensions of Eqs. 4.4-12–

TABLE 4.4–1
Parasitic capacitors in BJT model

	Operating region				
	Reverse bias			Forward bias	
	Depletion junction	Accumulation charge	Transition voltage	Depletion junction	Accumulation charge
C_{BE}	C_{BEDR}	C_{BEAR}	V_{BET}	C_{BEDF}	C_{BEAF}
C_{BC}	C_{BCDR}	C_{BCAR}	V_{BCT}	C_{BCDF}	C_{BCAF}
C_{CS}	C_{CSDR}	$C_{CSAR} = 0$	$V_{CST} = 0$ V	C_{CSDF}	$C_{CSAF} = 0$
C_{XS}	C_{XSDR}	$C_{XSAR} = 0$	V_{XST}	C_{XSDF}	$C_{XSAF} = 0$

4.4-15, respectively, at the transition voltage. These capacitances are functionally of the form of the corresponding extension used for characterizing the diode capacitance under forward bias as given by (3.2-9).

The accumulated charge capacitors C_{CSAR}, C_{CSAF}, C_{XSAR}, and C_{XSAF} are all zero. The forward and reverse bias accumulation charge capacitors are assumed equal (i.e., $C_{BEAR} = C_{BEDF}$ and $C_{BCAR} = C_{BCDF}$). It remains to characterize C_{BEAR} and C_{BCAR}. The functional form of these capacitors is given in (3.1-29) of Chapter 3. Unfortunately, the transit time is affected by the operating conditions (V_{BE} and V_{BC}) of the BJT. The parameters TF, XTF, VTF, ITF, PTF, and TR are used to characterize the transit times. The expression for the effective transit times is quite unwieldly, so it will not be given here. The interested reader should examine subroutine BJT (especially the expressions for CAPBE and CAPBC) in the SPICE source code for details.[6]

4.4.3 BJT Noise Model

Five noise sources are used to model the noise characteristics of the BJT. Thermal resistance noise sources are characterized by current sources with a spectral density of

$$S_{NR} = \frac{4kT}{R_x} \qquad \text{for } x \in \{\text{b, e, c}\} \tag{4.4-16}$$

These are modeled in parallel with the three resistors R_b, R_e, and R_c of Fig. 4.4-1. Parameters in this equation are defined in Appendix 4C. Shot and flicker noise are modeled by two current sources, the first with a spectral density of

$$S_{NB} = 2qI_{CQ} \tag{4.4-17}$$

is connected from the base to the emitter of T2 in Fig. 4.4-1. The second current source has a spectral density of

$$S_{NC} = 2qI_{BQ} + \frac{K_F I_{BQ}^{AF}}{f} \tag{4.4-18}$$

and is connected from the collector to the emitter of T2 in the same figure. The parameters q, k, and T have been defined previously and are included in Appendix 4C. K_F and AF are SPICE input parameters and f is frequency in Hz. I_{BQ} and I_{CQ} represent the quiescent values of I_B and I_C, respectively. All noise sources in the BJT are assumed to be uncorrelated.

4.4.4 Temperature Dependence of the BJT

Several of the parameters that characterize the BJT are temperature dependent. SPICE models the temperature dependence of the saturation currents (I_S, I_{SE}, and I_{SC}), betas (BF and BR), the junction capacitance parameters ($C_{JE}, C_{JC}, C_{JS}, \phi_B, \phi_C$ and ϕ_S), and the noise coefficients K_F and A_F. The saturation currents at a temperature T are characterized by the equations

$$I_S(T) = I_S(T_1)\left(\frac{T}{T_1}\right)^{XTI} \exp\left[\left(\frac{T}{T_1} - 1\right)\frac{EG(T) \cdot q}{kT}\right] \tag{4.4-19}$$

$$I_{SE}(T) = I_{SE}(T_1)\left(\frac{T}{T_1}\right)^{[(XTI/NE)-XTB]} \exp\left[\left(\frac{T}{T_1} - 1\right)\left(\frac{EG(T) \cdot q}{NE \cdot kT}\right)\right] \tag{4.4-20}$$

$$I_{SC}(T) = I_{SC}(T_1)\left(\frac{T}{T_1}\right)^{[(XTI/NC)-XTB]} \exp\left[\left(\frac{T}{T_1} - 1\right)\left(\frac{EG(T) \cdot q}{NC \cdot kT}\right)\right] \tag{4.4-21}$$

where T_1 is any reference temperature, EG(T) is given in Eq. (4.2-63) and the remaining parameters are SPICE input parameters.

The parameters BF and BR are given by the expressions

$$BF(T) = BF(T_1)\left(\frac{T}{T_1}\right)^{XTB} \tag{4.4-22}$$

$$BR(T) = BR(T_1)\left(\frac{T}{T_1}\right)^{XTB} \tag{4.4-23}$$

The temperature dependence of $C_{JC}, C_{JE}, C_{JS}, \phi_B, \phi_C$, and ϕ_S is given for $Y \in \{C, E, S\}$ by

$$C_{JY}(T) = C_{JY}(T_1) \cdot [1 + \theta_Y(T)] \tag{4.4-24}$$

where

$$\theta_Y(T) = MJY \cdot \{0.0004(T - T_1) + 1 - [\phi_Y(T)/\phi_Y(T_1)]\} \tag{4.4-25}$$

and

$$\phi_Y(T) = \phi_Y(T_1) \cdot (T/T_1) + \phi_{BF}(T) \tag{4.4-26}$$

and where $\phi_{BF}(T)$ is given by Eq. (4.2-64).

The temperature dependence of K_F and A_F is modeled by (4.2-61) and (4.2-62) where $\phi_B(T)$ is replaced with $\phi_E(T)$. Additional details can be found in subroutine TMPUPD of the SPICE source code.

4.5 SUMMARY

Models for the MOSFET, diode, and BJT which are used in the program SPICE have been presented. The similarity between these more detailed models and the simpler models discussed in Chapter 3 should be apparent. Although these models have been presented in the context of SPICE, they should be viewed, in their own right, as a more complete analytical characterization of the three basic devices, which form the nucleus of most integrated circuits. Many parts of these models were not developed specifically for SPICE but rather evolved over the years in the technical literature as researchers attempted to understand the fundamental operation of the basic devices. In many demanding situations, the designers should find the relevant analytical model equations presented in this chapter directly useful for design, insight, and optimization.

The authors have repeatedly observed confusion and uncertainty by both students and practicing engineers about the validity of simulations. This is often attributable to either lack of knowledge of the model used in their simulator or lack of understanding of how specific model parameters impact performance. A firm understanding of the models used in a simulator is essential for utilization of these powerful tools. The glossaries and tables which appear in the appendices of this chapter should prove to be a useful reference for SPICE users.

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PROBLEMS

4.1. Assume the transistor in Figure P4.1 is fabricated in the CMOS process characterized in Appendix 2B.
(*a*) Determine V_{SS} so that $V_{OQ} = 1$ V (when $V_i = 0$). Use the Level 1 SPICE MOSFET model.
(*b*) Compare the small signal voltage gain using the Level 1 and Level 2 models with V_{SS} as determined in (*a*).
(*c*) Compare the small signal 3 dB bandwidth using the Level 1 and Level 2 models at the same Q-point as used in (*a*) and (*b*).

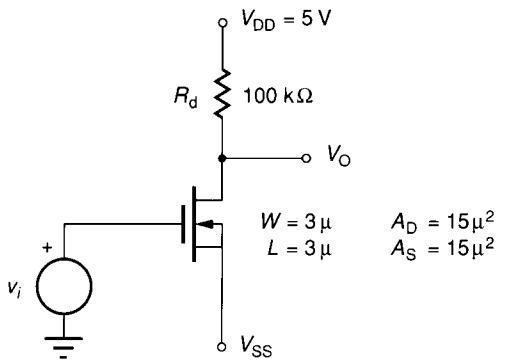

FIGURE P4.1
Problem 4.1.

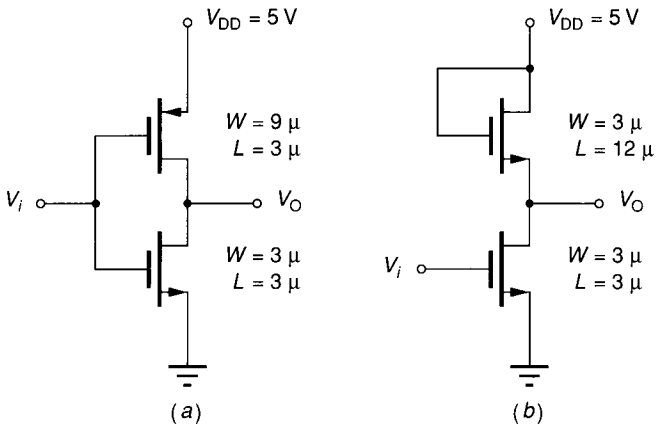

FIGURE P4.2
Problem 4.2.

4.2. (*a*) Use SPICE to obtain the dc transfer characteristics for the two circuits shown in Fig. P4.2, using first the Level 1 model and then the Level 2 model. Assume the transistors are characterized by the CMOS process of Appendix 2B.
(*b*) Obtain the low frequency small signal voltage gain for both circuits and plot as the quiescent input voltage is varied between 0 V and 5 V.
(*c*) If these circuits are loaded by a 50 fF capacitor, determine the response to a 5 V pulse input that lasts 100 μsec.
(*d*) If these circuits are biased at V_{OQ} = 2.5 V, determine the small signal 3 dB bandwidth of the voltage gain $A_v = v_o/v_i$.

4.3. Compare the dc transfer characteristics (I_D vs. V_{DS} as a function of V_{GS}) for a MOSFET using the Level 1 and Level 2 SPICE models. Use the SPICE process model parameters of Appendix 2B.

4.4. Compare the small signal output conductance when λ is an input parameter in the Level 2 model to that obtained if λ is calculated by Eq. 4.2-34. Assume the process parameters of the CMOS process discussed in the Appendices of Chapter 2 when making this comparison.

4.5. Plot I_D vs. V_{GS} for .3 V < V_{GS} < 5 V for the circuit in Fig. P4.5 using a logarithmic I_D axis. Use the process of Appendix 2B and include any subthreshold currents.

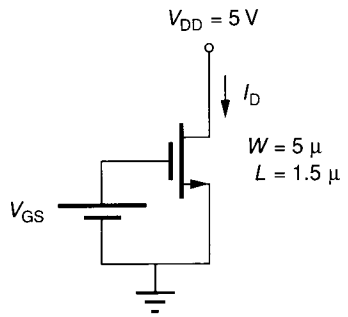

FIGURE P4.5
Problem 4.5.

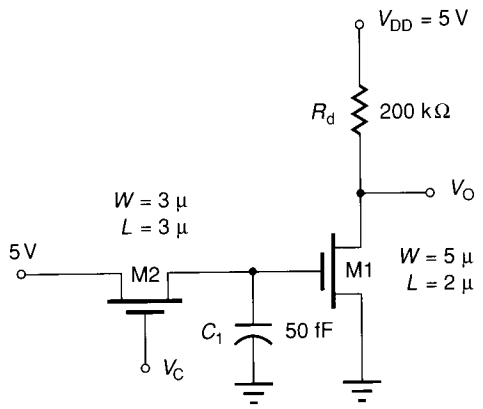

FIGURE P4.6
Problem 4.6.

4.6. In Fig. P4.6, at time $t = 0$ the control voltage V_C is taken from 5 V to 0 V and maintained at 0 V.
(*a*) If M2 serves as an ideal switch (short between drain and source when $V_C = 5$ V and open when $V_C = 0$ V), what is $V_O(t)$?
(*b*) Leakage current through the drain or source diffusion of M2 will discharge C. Use the process of Appendix 2B to find how M2 should be laid out to minimize the output voltage droop.
(*c*) Plot $V_O(t)$ if the source diffusion of M2 contacting the gate of M1 is $3\ \mu \times 12\ \mu$.

4.7. Practically determine and illustrate the effect of the mobility degradation parameters UCRIT, ULTRA, and UEXP on the I_D–V_{DS} characteristics of the MOSFET.

4.8. Plot C_{GS}, C_{GD}, C_{BD}, C_{BS}, and C_{BG} in the following two cases for the MOSFET shown in Fig. P4.8.
(*a*) vs. V_{GS} for $0 \le V_{GS} \le 5$ V if $V_{DS} = 5$ V and $V_{BS} = -5$ V.
(*b*) vs. V_{GS} for $0 \le V_{GS} \le 5$ V if $V_{DS} = 5$ V and $V_{BS} = 0$.

4.9. Plot C_{BE}, C_{BC}, and C_{CS} vs. I_B for 1 nA $\le I_B \le$ 100 μA for the BJT shown in Fig. P4.9. Assume $V_{CE} = 5$ V.

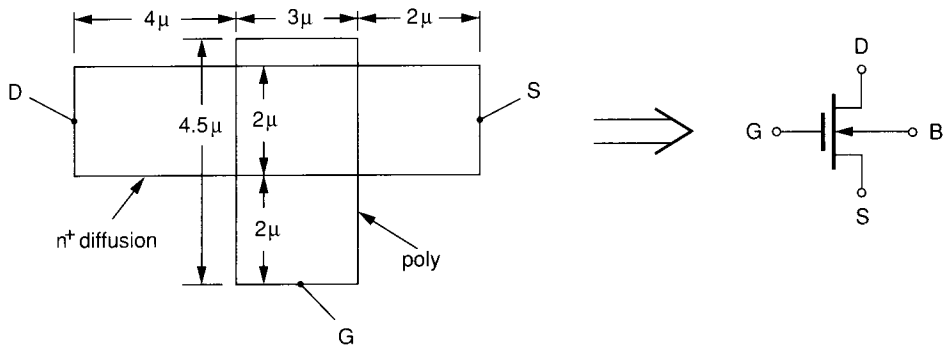

FIGURE P4.8
Problem 4.8.

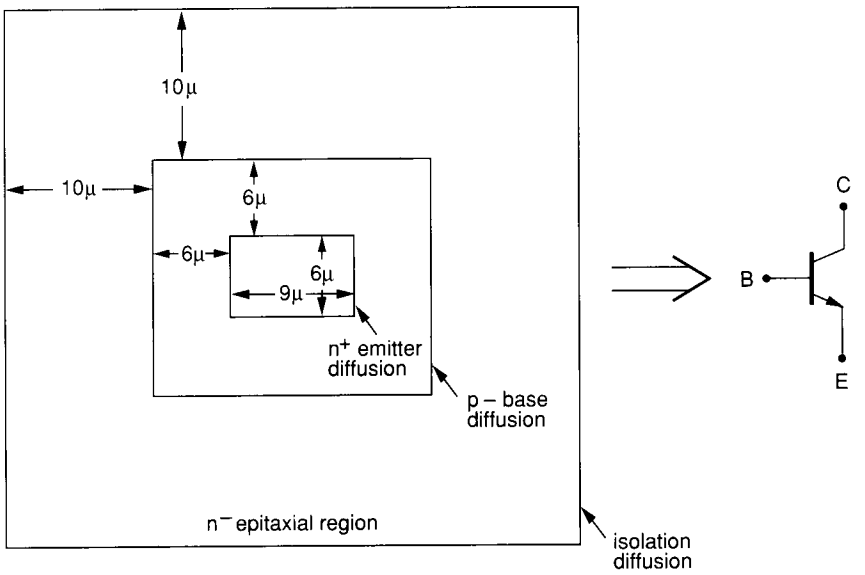

FIGURE P4.9
Problem 4.9.

4.10. A CMOS digital inverter loaded by an identical device is shown in Fig. P4.10. Assume the device is fabricated in the CMOS process of Appendix 2B.

(*a*) If a pulse of height 5 V is applied to the input (V_i) at $t = 0$, what is the minimum pulse width that can be applied if V_{O1} must swing down to at least 0.5 V? Assume $C_L = 0$.

(*b*) How does the minimum pulse width change if 40 identical inverters load the node V_{O1}? Assume $C_L = 0$.

(*c*) If the digital inverter is loaded by only a 2pF load, how does the response time of this circuit compare to that obtained in (*a*)?

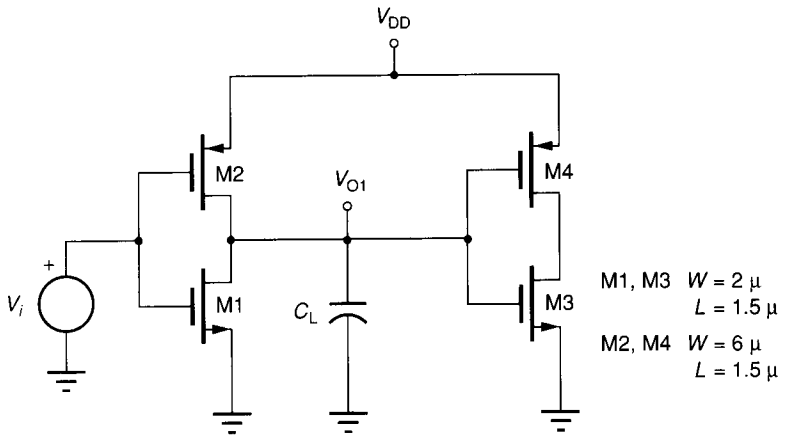

FIGURE P4.10
Problem 4.10.

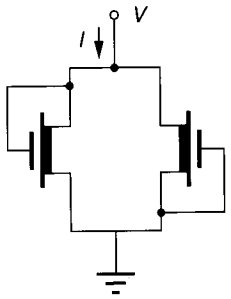

FIGURE P4.11
Problem 4.11.

4.11. Plot I vs. V for the circuit shown in Fig. P4.11 for $-3\text{V} \leq V \leq 3$ V. Assume M1 and M2 matched with $W = 3\ \mu$ and $L = 30\ \mu$. Use the NMOS process parameters of Appendix 2A.

4.12. If I_{BIAS} in Fig. P4.12 is set to 100 μA and V_{B1} and V_{B2} are adjusted so that $V_{O1Q} = V_{O2Q} = 5$ V, obtain from SPICE the small signal voltage gain and the 3 dB bandwidth of each circuit for a small signal excitation. Use the SPICE process model parameters of Appendices 2B and 2C and include realistic parasitics for M1 and Q1.

4.13. Assume that V_{B1} and V_{B2} in Problem 4.12 are fixed at the value needed to make $V_{O1Q} = V_{O2Q} = 5$ V at room temperature (30°C). What will happen to the Q-point, voltage gain and 3 dB bandwidth for the two circuits of Fig. P4.12 if the temperature is increased to 200°C? Decreased to −50°C?

4.14. The circuit shown in Fig. P4.14 has been proposed as a linear temperature transducer (output voltage linearly proportional to temperature). Plot V_O vs. temperature for $-50°\text{C} \leq T \leq 200°\text{C}$, and comment on the suitability of this device as a temperature transducer. Use the model parameters of Appendix 2C in your simulations. Assume $I_{REF} = 1\ \mu A$.

4.15. Examine the MOSFET shown in Fig. P4.15.
(*a*) Adjust V_{BB} so that $V_{OQ} = 3$ V.

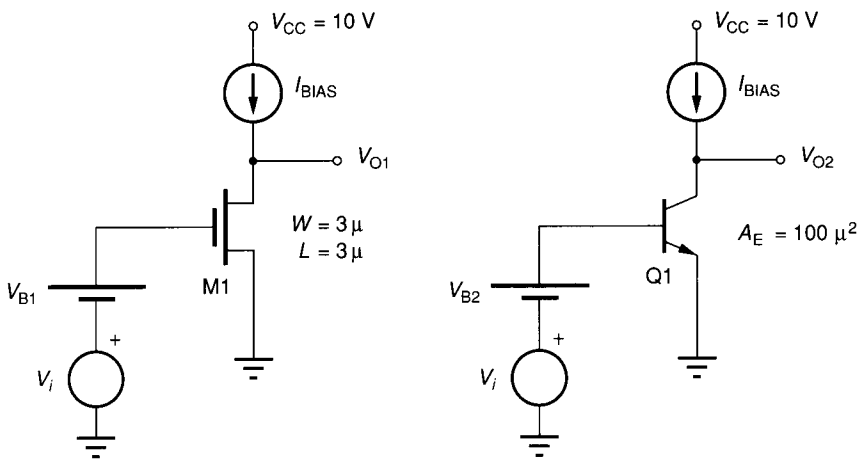

FIGURE P4.12
Problem 4.12.

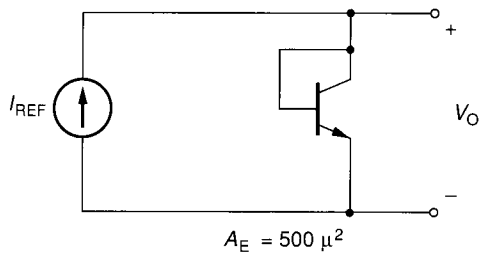

FIGURE P4.14
Problem 4.14.

(*b*) Determine V_m so that the peak to peak output swing is about 2 V around the Q-point established in (*a*).

(*c*) If the time varying output voltage is 2 V p–p, determine the signal to noise ratio of the output voltage in the frequency band [100 Hz, 20 KHz]. Use the MOS process of Appendix 2B and typical noise parameters.

(*d*) Repeat parts (*a*), (*b*) and (*c*) if the MOSFET is replaced with a BJT with an emitter area of 500 μ^2 that is characterized by the process of Appendix 2C and compare with the results obtained for the MOSFET.

4.16. Use SPICE and the process description of Appendix 2C to find the following quantities in the circuit of Fig. P4.16.

(*a*) Determine the quiescent output voltage and the small signal model parameters of Q_1 at the Q-point.

(*b*) Determine the small signal voltage gain using the ac analysis in SPICE.

(*c*) Determine the steady state output voltage using a transient analysis if the input $v_i(t)$ is defined by

$$v_i(t) = \begin{cases} 0 & t < 0 \\ .005 \sin 1000t & t \geq 0 \end{cases}$$

(*d*) In calculating a steady state response due to a sinusoidal excitation with SPICE, how does the effort and computation time required for a transient analysis compare to that required for a small signal ac analysis?

4.17. (*a*) From Eqs. 4.2-21 and 4.2-24, obtain an expression for the effective width reduction, WR = $W - W_{eff}$, where $W_{eff} = W(2 - \eta)$ in terms of the parameter

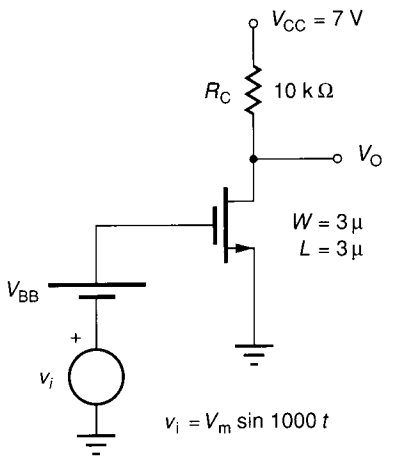

FIGURE P4.15
Problem 4.15.

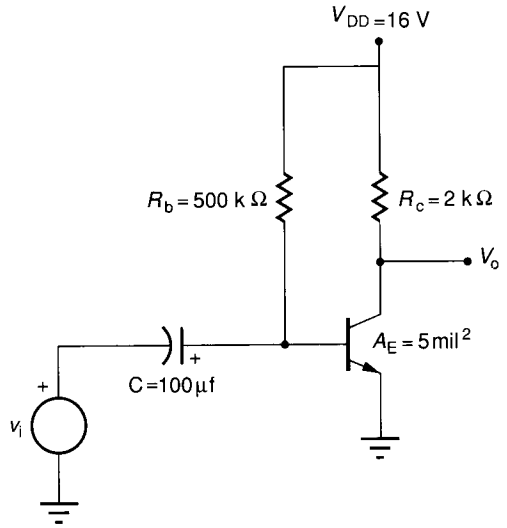

FIGURE P4.16
Problem 4.16.

DELTA when the MOSFET is operating in the saturation region.

(*b*) For drawn widths of $W = 5\ \mu$, $2\ \mu$, and $1\ \mu$ plot the effective length, L_{eff}, of a MOSFET as the drawn length is reduced from $10\ \mu$ to $0.5\ \mu$. Assume the SPICE model parameters of Appendix 2B remain valid as the drawn length is varied.

(*c*) Using the same model, plot the effective device width as the drawn width is varied between $10\ \mu$ and $0.5\ \mu$ for drawn lengths of $L = 5\ \mu, 2\ \mu$, and $1\ \mu$.

APPENDIX 4A
MOSFET PARAMETER DEFINITIONS

A brief alphabetical listing of the major parameters used in the MOS device models follows. Those parameters that serve specifically as SPICE input parameters are summarized in Table 4A. For more details about these parameters, the reader is referred to the SPICE User's Guide[1] or the SPICE source code[6].

AD represents the area of the drain diffusion. This serves as a SPICE input parameter which is entered on the device element card.

AF denotes the flicker noise exponent. This, along with the parameter KF, is used to characterize a noise current source that goes from drain to source in the MOSFET model. The RMS noise current density is given by

$$I_N = \sqrt{\frac{8kTg_m}{3} + \frac{\text{KF} \cdot I_{dq}^{\text{AF}}}{fC_{OX}L^2}} \tag{4A-1}$$

where g_m is the saturation region transconductance gain at the operating point and I_{dq} is the quiescent drain current. The first term under the radical represents

TABLE 4A
SPICE input parameter summary for MOSFET

Parameter	Symbol	Name	Default if non-zero	How entered directly†	Levels valid	Characterizing eqs. if not entered	
						Level 1	Level 2
LEVEL		Model level (1,2, or 3)	1	.MOD (1)			
VTO	V_{T0}	Zero-bias threshold voltage		.MOD (2)	all	4.2-16	4.2-16
KP	K'	Transconductance parameter	$2 \times 10^{-5} A/V^2$	.MOD (3)	all	4.2-11	4.2-11
GAMMA	γ	Bulk threshold parameter		.MOD (4)	all	4.2-14	4.2-14
PHI	ϕ	Surface potential	.6 V	.MOD (5)	all	4.2-15	4.2-15
LAMBDA	λ	Channel-length modulation		.MOD (6)	2	4.2-34	4.2-34
RD		Drain ohmic resistance		.MOD (7)	all		
RS		Source ohmic resistance		.MOD (8)	all		
CBD	C_{BD}	Zero-bias bulk–drain junction capacitance		.MOD (9)	all		
CBS	C_{BS}	Zero-bias bulk–source junction capacitance		.MOD (10)	all		
IS		Bulk junction saturation current	10^{-14} A	.MOD (11)	all		
PB	ϕ_B	Bulk junction potential	.5 V	.MOD (12)	all		
CGSO	C_{GSO}	Gate–source overlap capacitance per meter of channel width of source		.MOD (13)	all		
CGDO	C_{GDO}	Gate–drain overlap capacitance per meter of channel width of drain		.MOD (14)	all		
CGBO	C_{GBO}	Gate–bulk overlap capacitance per meter of channel length		.MOD (15)	all		
RSH		Sheet resistance of drain & source diffusions		.MOD (16)	all		
CJ		Zero-bias bulk junction bottom capacitance area density	in pf/u^2	.MOD (17)	all		
MJ		Bulk junction bottom grading coefficient	.5	.MOD (18)	all		

TABLE 4A
(Continued)

Parameter	Symbol	Name	Default if non-zero	How entered directly†	Levels valid	Characterizing eqs. if not entered	
						Level 1	Level 2
CJSW		Zero-bias bulk junction sidewall capacitance per meter of junction perimeter		.MOD (19)	all		
MJSW		Bulk junction sidewall grading coefficient		.MOD (20)	all		
JS		Bulk junction saturation current area density		.MOD (21)	all		
TOX	T_{OX}	Gate oxide thickness	10^{-7}m	.MOD (22)	2,3		
NSUB	N_{SUB}	Substrate doping		.MOD (23)	all		
NSS	N_{SS}	Surface state density		.MOD (24)	all		
NFS		Fast surface state density		.MOD (25)	all		
TPG		Type of gate material	1	.MOD (26)	all		
XJ		Metallurgical junction depth		.MOD (27)	all		
LD	L_D	Lateral diffusion		.MOD (28)	all		
UO	μ_O	Nominal surface mobility	600 $cm^2/V \cdot A$	.MOD (29)	all		
UCRIT		Critical field for mobility degradation	10^4	.MOD (30)	2		
UEXP		Critical field exponent in mobility degradation		.MOD (31)	2		
UTRA		Mobility transverse field coefficient		.MOD (32)	2		
VMAX	V_{MAX}	Maximum carrier drift velocity		.MOD (33)	all		
NEFF	N_{EFF}	Total channel charge	1.0	.MOD (34)	2		
XQC		Thin-oxide capacitance model flag and coefficient of channel charge	1.0	.MOD (35)	all		
KF	K_F	Flicker noise coefficient		.MOD (36)	all		
AF	A_F	Flicker noise exponent	1.0	.MOD (37)	all		
FC		Coefficient for forward-bias depletion capacitance	0.5	.MOD (38)	all		

TABLE 4A
(Continued)

Parameter	Symbol	Name	Default if non-zero	How entered directly†	Levels valid	Characterizing eqs. if not entered	
						Level 1	Level 2
DELTA		Width effect on threshold voltage		.MOD (39)	2,3		
THETA		Mobility degradation		.MOD (40)	3		
ETA		Static feedback		.MOD (41)	3		
KAPPA		Saturation field factor	0.2	.MOD (42)	3		
L		Drawn channel length		DE	all		
W		Drawn channel width		DE	all		
AD		Drain area		DE	all		
AS		Source area		DE	all		
PD		Drain perimeter		DE	all		
PS		Source perimeter		DE	all		
NRD		Drain sheet resistance		DE	all		
NRS		Source sheet resistance		DE	all		

†.MOD (x) denotes the entry is via the .MODEL card (line) at the x^{th} parameter location in Reference 1, DE notes entry from the device element card (line). Since the input parser in SPICE looks for each parameter by name, the ordering as denoted by the parameter x is arbitrary but was included for convenient reference to Reference 1.

shot noise and the second term $1/f$ noise. The corresponding spectral densities appear in Eqs. 4.2-49 and 4.2-50.

α is used to correct γ for short channel effects. It is not an input parameter to SPICE and is defined by (4.2-30); it provides linear correction of γ as indicated in (4.2-29).

AS represents the area of the source diffusion. This serves as a SPICE input parameter which is entered on the device element card.

β is not used as a SPICE input parameter, but it is often used to reduce notational complexity in the dc MOSFET model. It is defined by the expression

$$\beta = \frac{\mu_0 C_{OX} W}{L} \tag{4A-2}$$

CBD and **CBS** (C_{BD} and C_{BS}) are SPICE input parameters which represent the zero-bias diffusion bottom capacitance of the bulk–drain and bulk–source junction capacitors, respectively. If not input, C_{BD} and C_{BS} are calculated from CJ, AD, and AS by the expressions

$$C_{BD} = \text{CJ} \cdot \text{AD}$$
$$C_{BS} = \text{CJ} \cdot \text{AS} \tag{4A-3}$$

CGBO, CGDO, and **CGSO** (C_{GBO}, C_{GDO}, and C_{GSO}) are SPICE input parameters that represent the *linear* capacitance density of the gate–bulk, gate–drain and gate–source overlap capacitors respectively. They are expressed in terms of capacitance per unit length. These capacitors are discussed in more detail in Sec. 4.2.3.

CJ is the SPICE input parameter which represents the zero-bias junction bottom capacitance density of the moat–bulk diffusions. It is expressed in terms of capacitance per unit area of the junction. The zero-bias junction bottom capacitance of the drain–bulk and source–bulk junctions can be obtained internally in SPICE from CJ by multiplying CJ by AD and AS, respectively. The total junction capacitances are then calculated from Eq. 4.2-43 for junctions under reverse bias and from Eq. 4.2-46 for junctions under forward bias. If not input, CJ is calculated internally from Eq. 4.2-44.

CJSW is the SPICE input parameter which represents the zero-bias sidewall capacitance density of the moat–bulk diffusions. It is expressed in terms of capacitance per unit length of the junction permitter. The zero-bias junction sidewall capacitances of the drain–bulk and source–bulk junctions are obtained internally in SPICE from CJSW by multiplying by PD and PS, respectively. The total junction capacitances are then obtained from Eq. 4.2-43 for junctions under reverse bias and from Eq. 4.2-46 for junctions under forward bias. If CJSW is not entered, the sidewall capacitances are assumed to be zero.

C_{ox} represents the capacitance density of the gate–channel junction. It is expressed in terms of capacitance per unit area. Although not input directly in SPICE, it is calculated internally from the expression

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} \tag{4A-4}$$

where ϵ_{ox} is the dielectric constant (more precisely, the real permittivity) of the gate oxide and T_{ox} is the gate oxide thickness. C_{ox} is a key parameter in the MOS device models. It appears in the defining expression of several major parameters including K' (4.2-11), γ (4.2-14), V_{TO} (4.2-16), V_{FB} (4.2-17) and V_{TH}.

DELTA is a SPICE input parameter that characterizes the effective width reduction in the Level 2 and Level 3 models. It appears in the expression for η given in (4.2-24). With DELTA equal to its ideal value of 0, η assumes the ideal value of 1. DELTA also appears in the expressions for V_{TH} and V_{TH}^{*} as given in (4.2-22) and (4.2-25), respectively.

ϵ_0 is the permittivity of free space. It is a physical constant equal to 8.86×10^{-14} F/cm.

ϵ_{ox} is the dielectric constant (more precisely, the real permittivity) of SiO_2. It is a physical constant and is equal to $3.9\epsilon_0$.

ϵ_{si} is the dielectric constant (more precisely, the real permittivity) of Si. It is a physical constant and is equal to $11.7\epsilon_0$.

ETA is a SPICE input parameter termed the static feedback effect parameter. It is an empirical constant and is used only in the Level 3 model. It should not be confused with the parameter η listed below.

η is not a SPICE input parameter; it is used to characterize width reduction in the Level 2 and Level 3 models. It is primarily dependent upon the SPICE input parameter DELTA as can be seen from (4.2-24). This should not be confused with the SPICE input parameter ETA discussed above.

FC is the SPICE input parameter which denotes the forward bias coefficient in the parasitic junction capacitance model. The junction is assumed "reverse biased" for a forward bias less than FC $\cdot \phi_B$, and its capacitance is characterized by (4.2-43). For a forward bias greater than FC $\cdot \phi_B$, the junction is assumed "forward biased" and the junction capacitance is characterized by (4.2-46).

GAMMA (γ) is a SPICE input parameter called the bulk threshold. It plays a major role in the expression for the threshold voltage (Eqs. 4.2-9 and 4.2-16 for the Level 1 model, and 4.2-25 and 4.2-16 for the Level 2 model). If not input, it is calculated internally from N_{SUB} and T_{ox} by Eq. 4.2-14.

γ_s The parameter γ effectively decreases for short channel devices. The parameter $\gamma_s = \gamma(1 - \alpha)$, as defined by (4.2-29), is used in place of γ in the drain current expressions for the Level 2 and Level 3 models.

IS (I_S) is the bulk junction saturation current; it is a SPICE input parameter. The current flowing through the bulk junction is characterized by the standard diode equation

$$I = I_S\left(e^{\frac{V_{FB}}{V_t}} - 1\right) \tag{4A-5}$$

where V_{FB} represents the forward bias on the junction. This parameter is of particular concern in such circuits as the basic DRAM cell where the charge loss on switched storage capacitors is primarily due to current flow into the bulk

through the reverse biased moat junction formed between either the drain or source diffusion of the switch and the bulk. Either IS or JS can be used to characterize the bulk junction current characteristics.

JS (J_S) is a SPICE input parameter that denotes the bulk junction current density; it is expressed in terms of current per unit area of junction area. If the parameter IS is not input, it is calculated from JS by multiplying JS by the junction area.

k is Boltzmann's constant. It is a physical constant equal to 1.381×10^{-23} J/°K.

$\mathbf{K_2'}$ is the transconductance parameter that appears in the expression for the drain current in the Level 2 model as indicated by (4.2-20) and (4.2-21). It differs from K′ in that the effective mobility, μ_s, is used in place of μ_o in the defining equation (4.2-28).

KF is a SPICE input parameter called the flicker noise coefficient. It appears in the expression for the noise current as indicated by (4.2-47).

KP (K') is a key SPICE input parameter termed the transconductance parameter. It appears in the expression for the drain current of the Level 1 model as indicated in (4.2-6) and (4.2-7). If not input, K' is calculated from the mobility and C_{ox} by (4.2-11).

KAPPA is the saturation field factor. This SPICE input parameter is an empirical constant used only in the Level 3 model.

L denotes the drawn length of the MOS transistor. It is entered on the device element card. The out diffusion of the drain and source regions geometrically reduces the length of the device by twice the lateral diffusion, LD, to the adjusted geometrical length, L_{adj}.

$\boldsymbol{L_{adj}}$ is the adjusted geometrical length and is internally calculated by the expression

$$L_{adj} = L - 2LD \tag{4A-6}$$

$\boldsymbol{L_{eff}}$ is the effective device length. In addition to the geometrical length reduction, additional reductions in the effective length occur due to the applied drain–source voltage. The expression for L_{eff} is given by (4.2-10) for the Level 1 model and by (4.2-33) and (4.2-34) for the Level 2 model.

LD is the SPICE input parameter denoting the lateral (out) diffusion of the drain and source regions under the gate. Since the out diffusion on the source side is generally equal to that on the drain side of the gate, the geometrical length is effectively reduced by 2LD as indicated by (4.2-52).

LEVEL indicates which model is to be used for analysis. If not entered on the MODEL card, Level 1 is assumed.

LAMBDA (λ) is a SPICE input parameter called the channel-length modulation parameter. It arises from the V_{DS} dependence of the effective channel length. The output conductance of the small signal model is also proportional to $1/\lambda$. If this parameter is forced by specifying it on the .MODEL input card, the robustness of the Level 2 model is seriously restricted. Specifically, λ as

determined by (4.2-34) is not used in the calculation of L_{eff} by (4.2-33) if λ is an input parameter. If not input, the parameter defaults to 0 in the Level 1 model or is calculated from (4.2-35) in the Level 2 MOSFET model.

MJ and **MJSW** are SPICE input parameters for the bulk junction bottom grading coefficient and the bulk junction sidewall grading coefficient, respectively. They appear only in equations (4.2-43) and (4.2-46), which characterize the parasitic bulk–moat junction capacitances.

NEFF (N_{eff}) is an input parameter for the total channel charge coefficient. It is used only in the Level 2 model and only when V_{MAX} is specified. In this case, N_{eff} serves as an empirical constant that modifies (4.2-32) to read

$$\text{XD} = \sqrt{\frac{2\epsilon_{\text{si}}}{qN_{\text{eff}}N_{\text{SUB}}}} \tag{4A-7}$$

NFS is a SPICE input parameter called the effective fast surface state density. It is used only in the Level 2 and Level 3 models. NFS has two purposes. First, it serves as a flag to determine whether SPICE will assume the current in cutoff to be zero or $I_{\text{weak inversion}}$ as indicated in (4.2-19). Its second purpose is to characterize $I_{\text{weak inversion}}$ as shown in References 1 and 6.

n_{i} is the intrinsic carrier concentration of silicon and is equal to 1.45×10^{10} cm $^{-3}$ at room temperature.

NRD and **NRS** are the number of squares of moat in the drain and source respectively. They can be entered on the device element card. If RD and RS are entered, these parameters are ignored. If RD and RS are not entered, the drain and source resistances are calculated from the expressions

$$\begin{aligned} \text{RD} &= \text{RSH} \cdot \text{NRD} \\ \text{RS} &= \text{RSH} \cdot \text{NRS} \end{aligned} \tag{4A-8}$$

respectively, provided the sheet resistance of the moat, RSH, has been entered on the .MODEL card.

NSUB (N_{SUB}) is a SPICE input parameter indicating the substrate doping. It plays a key role in calculations of parameters used to define the threshold voltage.

NSS (N_{SS}) is a SPICE input parameter called the effective surface charge density. Although it can be used to define the flatband voltage (4.2-17), which subsequently determines V_{TO}, it is usually better to enter V_{TO} directly.

PB (ϕ_{B}) is a SPICE input parameter called the bulk junction potential (alternately, built-in potential). ϕ_B is used to characterize the bulk junction capacitors as indicated in (4.2-43) and (4.2-46).

PHI (ϕ) is a SPICE input parameter called the surface potential. If not input, this parameter is calculated from (4.2-15) provided N_{SUB} is input.

ϕ_{MS} is the metal-semiconductor work function difference. It is calculated internally in SPICE from (4.2-18) and is used to define the flatband voltage.

PS and **PD** can be entered on the device element card. They represent the perimeter of the source and drain, respectively. They are used for calculating the sidewall capacitance of the drain and source regions as indicated in (4.2-43) and (4.2-46).

q is the charge of an electron. It is a physical constant equal to 1.602×10^{-19} coulomb.

RD and **RS** are SPICE input parameters representing the series drain and source resistances, respectively. If not input, they are calculated from (4A-8), provided that the sheet resistance of the moat, RSH, is specified.

RSH is a SPICE input parameter representing the sheet resistance of the moat. To allow for geometrical device variations, it is often more convenient to specify RSH, NRD, and NRS, and then let SPICE calculate RD and RS from (4A-8), rather than to enter RD and RS directly.

T is a SPICE input parameter indicating the operating temperature of the circuit.

THETA is a SPICE input parameter. It is an empirical parameter used only in the Level 3 model.

TPG is a SPICE input parameter indicating the type of gate. It is a flag that assumes a value of $+1$ for poly gates with the same flavor (both n or both p doping) as the substrate, -1 for poly gates with the flavor opposite to that of the substrate, and 0 for aluminum gates.

TOX (T_{OX}) is the thickness of the gate oxide. It is a SPICE input parameter used to determine the key parameter C_{OX}.

UO (μ_o) is the surface mobility of the channel. It is a SPICE input parameter used to calculate K' (or K_2') if T_{OX} is entered and K' is not entered.

μ_s represents the degraded surface mobility. It is an internal parameter and used only in the Level 2 model. SPICE uses the parameters UCRIT, UTRA, and UEXP to characterize μ_s as indicated by (4.2-36); the μ_s is used to define the transconductance parameter for the Level 2 model, K_2', as shown in (4.2-28).

UCRIT, UEXP, and **UTRA** are SPICE input parameters used to characterize the degraded surface mobility, μ_s, as indicated by (4.2-36).

V_{FB} is the flatband voltage. It is an internal SPICE parameter characterized by (4.2-17).

VMAX (V_{MAX}) is the maximum drift velocity of carriers in the channel. It is a SPICE input parameter which partially defines the transition region between ohmic and saturation in the Level 2 model. See Reference 2 for a more complete discussion of V_{MAX}. It is ignored in the Level 1 model.

V_t is an internal parameter calculated from the expression

$$V_t = \frac{kT}{q} \tag{4A-9}$$

where k is Boltzmann's constant, T is temperature in °K, and q is the charge of an electron. It is used for calculating the bulk–moat reverse saturation current as

indicated by (4A-5) and the drain current when operating in weak inversion. V_t should not be confused with V_T, the notation used for threshold voltage in Chapter 3.

VTO (V_{T0}) is a SPICE input parameter. It is the zero-bias ($V_{BS} = 0$) threshold voltage. If not input, it is calculated from (4.2-16).

V_T (See V_{TH} definition.)

V_{TH} is the threshold voltage of the device. It is used to characterize the cutoff transition region. It is an internal parameter determined by (4.2-9) for the Level 1 model and (4.2-25) for the Level 2 model. In Chapter 3, the variable V_T was used to denote the threshold voltage. V_T should not be confused with $V_t = kT/q$.

V^*_{TH} is nearly equal to V_{TH} in the Level 2 model. It is an internal parameter used to characterize the drain currents as indicated by (4.2-20) and (4.2-21). V^*_{TH} is determined from (4.2-25). V_{BIN} is used for V^*_{TH} in the SPICE source code and some of the other SPICE documentation.

W denotes the drawn width of the MOS transistor. It is entered on the device element card.

W_S and W_D are defined in equations (4.2-31) and (4.2-32), respectively.

XJ is the metallurgical junction depth. It is a SPICE input parameter which is used to characterize the effective bulk threshold parameter, γ_s, as indicated by (4.2-30).

XQC is a SPICE input parameter used to denote the percent of channel charge that is associated with the drain. It is used in the approximation which converts distributed channel charge to lumped drain and source charge when the device is operating in the saturation region. The reader is referred to Reference 2 and the SPICE source code[6] for additional details.

APPENDIX 4B
DIODE PARAMETER DEFINITIONS

A brief alphabetical listing of the major parameters used in the DIODE device models follows. Those parameters that serve specifically as SPICE input parameters are summarized in Table 4B. For more details about these parameters, the reader is referred to Reference 1 or to the SPICE source code [6].

AF (A_F) denotes the flicker noise exponent. This, along with the parameter KF, is used to characterize the flicker noise in the diode. A noise current source in shunt with diode D2 in Fig. 4.3-1 is used to characterize the shot and flicker noise in the diode. This RMS current source is modeled by the density equation

$$I_{N1} = \sqrt{2qI + \frac{KF \cdot I^{AF}}{f}} \qquad \text{(4B-1)}$$

where I is the diode current, f is the frequency in Hz, and q is the charge of an electron. The noise model of the diode in SPICE is completed by adding a second noise current source, which represents thermal noise in R_s, in shunt with the series resistor R_s in Fig. 4.3-1. The density of this RMS current is given by

TABLE 4B
SPICE input parameter summary for diode

Parameter	Symbol	Name	Default if non-zero	How entered†
IS		Saturation current	10^{-14}A	.MOD (1)
RS	r_s	Ohmic resistance		.MOD (2)
N	n	Emission coefficient	1	.MOD (3)
TT	τ	Transit time		.MOD (4)
CJO	C_{j0}	Zero-bias junction capacitance		.MOD (5)
VJ	ϕ_B	Junction potential	1 V	.MOD (6)
M	m	Junction grading coefficient	0.5	.MOD (7)
EG		Activation energy	1.11 V	.MOD (8)
XTI		Saturation current temp.exp.	3.0	.MOD (9)
KF	K_F	Flicker noise coefficient		.MOD (10)
AF	A_F	Flicker noise exponent	1	.MOD (11)
FC		Coefficient for forward-reverse bias transition	0.5	.MOD (12)
BV		Reverse breakdown voltage	∞	.MOD (13)
IBV		Current at breakdown voltage	1 mA	.MOD (14)
AREA	A_n	Normalized junction area	1	DE

†.MOD (x) denotes the entry is via the .MODEL card (line) at the x^{th} parameter location in Reference 1. DE notes entry from the device element card (line). Since the input parser in SPICE looks for each parameter by name, the ordering as denoted by the parameter x is arbitrary but was included for convenient reference to Reference 1.

$$I_{N2} = \sqrt{\frac{4kT}{R_s}} \tag{4B-2}$$

where k is Boltzmann's constant and T is temperature in degrees Kelvin.

AREA (A_n) denotes the ratio of the cross-sectional area of the pn junction on the device input line to the cross-sectional area of the device modeled in the referenced .MODEL line. A_n is thus a normalized area and is dimensionless.

BV is the reverse breakdown voltage of the diode.

CJO (C_{jo}) is the junction capacitance at zero bias on the pn junction of the device modeled on the .MODEL line. Note that this differs from the closely related parameter CJ, which was used to model the junction capacitance in the MOSFET; CJO represents the capacitance while CJ represents the capacitance density.

EG denotes the activation energy. It is used along with the parameter XTI to characterize the temperature dependence of the saturation current[3]. The temperature dependence of IS is characterized by the expression

$$\mathrm{IS}(T) = \mathrm{IS}(T_1) \cdot \left(\frac{T}{T_1}\right)^{\mathrm{XTI}} \exp\left[\left(\frac{q(\mathrm{EG})}{kT}\right)\left(\frac{T}{T_1} - 1\right)\right] \tag{4B-3}$$

where T is temperature in degrees Kelvin, T_1 is any reference temperature, $\mathrm{IS}(T_1)$ is the saturation current at T_1, k is Boltzmann's constant, and q is the charge of an electron.

FC is the forward bias coefficient in the parasitic junction capacitance model which characterizes the transition voltage between the "reverse bias" and "forward bias" capacitance models. The junction is assumed "reverse biased" for a forward bias less than FC · ϕ_B.

IBV is the current in the diode at breakdown. It represents the nearly constant current that flows in the diode prior to breakdown. There is a fixed relationship between IBV, BV, and IS. If this relationship is not established with the specified parameters, SPICE adjusts either IBV or BV to attain the required relationship. See subroutines MODCHK and DIODE in the SPICE source code for details.

IS (I_S) denotes the saturation current in a diode. This SPICE input parameter is a key parameter in the diode equation.

k is Boltzmann's constant. It is a physical constant equal to 1.381×10^{-23} J/°K.

KF is called the flicker noise coefficient. It is used, along with AF, to characterize the flicker noise in the diode as indicated by equation (4B-1).

M (m) is called the junction grading coefficient. It characterizes, along with ϕ_B and C_{jo}, the junction capacitance as indicated by (4.3-4).

N (n) is the emission coefficient that appears in the diode equation (4.3-1). It is typically near unity.

RS denotes the series resistance in the diode. It is assumed to be an ideal resistor in SPICE.

TT (τ) is called the transient time. It is used to characterize the effects of stored change in the junction due to minority carrier injection as indicated by (4.3-4) and (4.3-5).

VJ (ϕ_B) is called the junction potential. It characterizes, along with C_{jo} and m, the junction capacitance as indicated by (4.3-4). The FC · ϕ_B product also determines the transition between "reverse bias" and "forward bias" on the junction.

XTI denotes the saturation current temperature exponent. It is used along with EG to characterize the temperature dependence of IS as indicated by (4B-3).

APPENDIX 4C
BJT PARAMETER DEFINITIONS

A brief alphabetical listing of the major parameters used in the BJT device models follows. Those parameters that serve specifically as SPICE input parameters are summarized in Table 4C. For more details about these parameters, the reader is referred to Reference 1 or to the SPICE source code[6].

TABLE 4C
SPICE input parameter summary for the BJT

Parameter	Symbol	Name	Default if non-zero	How entered directly†
IS	I_S	Transport saturation current	1.0E-16 A	.MOD (1)
BF		Ideal maximum forward beta	100	.MOD (2)
NF		Forward current emission coefficient	1	.MOD (3)
VAF	V_{AF}	Forward Early voltage	∞	.MOD (4)
IKF	I_{KF}	Forward beta high-current roll-off	∞	.MOD (5)
ISE	I_{SE}	B-E leakage saturation current		.MOD (6)
NE		B-E leakage emission coefficient	1.5	.MOD (7)
BR		Ideal maximum reverse beta	1	.MOD (8)
NR		Reverse current emission coefficient	1	.MOD (9)
VAR	V_{AR}	Reverse Early voltage	∞	.MOD (10)
IKR	I_{KR}	Reverse beta high-current roll-off	∞	.MOD (11)
ISC	I_{SC}	B-C leakage saturation current		.MOD (12)
NC		B-C leakage emission coefficient	2	.MOD (13)
RB	R_B	Zero bias base resistance		.MOD (14)
IRB		Current where base resistance falls halfway to its minimum value	∞	.MOD (15)
RBM		Minumum base resistance at high currents	RB	.MOD (16)
RE		Emitter resistance		.MOD (17)
RC		Collector resistance		.MOD (18)
CJE	C_{JE}	Zero-bias B–E depletion region capacitance		.MOD (19)
VJE	ϕ_B	B–E built–in potential	.75	.MOD (20)
MJE	M_{JE}	B–E junction exponential factor	.33	.MOD (21)
TF		Ideal forward transit time		.MOD (22)
XTF		Coefficient for bias dependence of TF		.MOD (22)
VTF		Voltage describing B–C voltage dependence of TF	∞	.MOD (23)
ITF		High-current effect on TF		.MOD (24)
PTF		Excess phase at $f = \frac{1}{2\pi \cdot TF}$		.MOD (25)
CJC	C_{JC}	Zero-bias B-C depletion region capacitance		.MOD (26)
VJC	ϕ_C	B–C built–in potential	.75	.MOD (27)
MJC	M_{JC}	B–C junction exponential factor	.33	.MOD (28)
XCJC	θ	Fraction of B–C depletion capacitance connected to internal base node	1	.MOD (29)
TR		Ideal reverse transit time		.MOD (30)
CJS	C_{JS}	Zero-bias collector–substrate capacitance		.MOD (31)
VJS	ϕ_S	Substrate junction built–in potential	.75	.MOD (32)
MJS	M_{JS}	Substrate junction exponential factor		.MOD (33)
XTB		Temperature exponent for BF and BR		.MOD (34)
EG		Activation energy for temperature dependence of IS	1.11ev	.MOD (35)
XTI		Saturation current temperature exponent	3	.MOD (36)
KF	K_F	Flicker noise coefficient		.MOD (37)
AF	A_F	Flicker noise exponent	1	.MOD (39)
FC		Forward bias capacitor transition coefficient	0.5	.MOD (40)
AREA	A_n	Emitter area ratio	1	DE

†.MOD (x) denotes the entry is via the .MODEL card (line) at the x^{th} parameter location in Reference 1. DE notes entry from the device element card (line). Since the input parser in SPICE looks for each parameter by name, the ordering as denoted by the parameter x is arbitrary but was included for convenient reference to Reference 1.

AF denotes the flicker noise exponent. This input parameter, along with the parameter KF, is used to characterize the flicker noise in the C–E noise source as indicated by (4.4-18).

AREA (A_n) denotes the ratio of the emitter area of the BJT on the device input line to the emitter area of the BJT modeled in the referenced .MODEL line. A_n is thus a normalized area and is dimensionless.

BF is the ideal maximum forward beta. It is one of the key input parameters used to characterize the BJT and is approximately equal to the current gain from the base to collector. It appears in the characterizing equation (4.4-2) and in Fig. 4.4-3.

β_F is by definition the ratio of the total collector current to the total base current under forward BE bias as indicated by (4.4-9); it is not a SPICE input parameter. It is shown pictorially in Fig. 4.4-3. β_F is operating point dependent but nearly equal to BF for midrange V_{BE} values.

BR is the ideal maximum reverse beta. This SPICE input parameter is most useful for characterizing the BJT in the reverse active region. It appears in the characterizing equation (4.4-1) and the plot corresponding to that of Fig. 4.4-3 obtained by forward biasing the BC junction and reverse biasing the BE junction.

β_R is by definition the ratio of the total emitter current to the total base current under forward BC bias evaluated at the Q-point; it is not a SPICE input parameter. It is the reverse active equivalent of β_F.

C2 and **C4** are parameters which were used to denote ISE and ISC in some earlier versions of SPICE. They are still used for this purpose in some SPICE documentation.

CJC, CJE, and **CJS** (C_{JC}, C_{JE}, and C_{JS}) are the zero-bias depletion region capacitances of the base–collector, base–emitter and collector–substrate junctions. They are useful for characterizing the parasitic capacitances in vertical transistors. These SPICE input parameters appear in (4.4-12)–(4.4-15).

EG denotes the activation energy. It is used along with the parameter XTI to characterize the temperature dependence of the saturation current.[3] The temperature dependence of IS is characterized by the expression

$$\mathrm{IS}(T) = \mathrm{IS}(T_1) \cdot \left(\frac{T}{T_1}\right)^{\mathrm{XTI}} \exp\left[\left(\frac{qEG}{kT}\right)\left(\frac{T}{T_1} - 1\right)\right] \tag{4C-1}$$

where T is temperature in degrees Kelvin, T_1 is any reference temperature, $\mathrm{IS}(T_1)$ is the saturation current at T_1, k is Boltzmann's constant, and q is the charge of an electron.

FC is the SPICE input parameter which denotes the forward bias coefficient in the parasitic junction capacitance (B–C, B–E, and C–S). All junction capacitors are assumed "reverse biased" and characterized by (4.4-12)–(4.4-15) for a forward bias less than or equal to FC $\cdot$ ϕ_X, for $X \in \{B, C, S\}$. For a forward bias greater than FC $\cdot$ ϕ_X the junction capacitors are assumed "forward biased" and are characterized by the continuous and differentiable linear extension of the reverse-bias region at the transition voltage.

IKR is the corner for the reverse beta high-current roll-off. This SPICE input parameter is a dual of the parameter IKF for the reverse active mode of operation.

IKF is the corner for the forward beta high-current roll-off. This SPICE input parameter appears in (4.4-3) and Fig. 4.4-3.

IRB is the current where the base resistance falls half way to its minimum value. The base resistance is assumed to be current dependent and is characterized by the three parameters RB, IRB, and RBM.

IS is the transport saturation current of the BJT. This SPICE input parameter is a key parameter in the dc model as indicated by (4.4-1) and (4.4-2).

ISC and **ISE** (I_{SE} and I_{SC}) represent the B–C and B–E leakage saturation currents. They appear in the dc model as indicated by (4.4-1) and (4.4-2).

ITF is a SPICE input parameter which characterizes the forward transit time at high current levels. The reader should consult the SPICE source code in subroutine BJT for details.

k is Boltzmann's constant. It is a physical constant equal to 1.381×10^{-23}J/°K.

KF is the flicker noise coefficient used to characterize noise in the collector–emitter noise source as indicated by (4.4-18).

MJC, MJE and **MJS** (M_{JC}, M_{JE} and M_{JS}) are the junction grading coefficients of the B–C, B–E, and C–S junctions, respectively. These SPICE input parameters appear as exponents in the voltage dependent depletion junction capacitances as indicated by (4.4-12)–(4.4-15).

NC, NE, NF, and **NR** are leakage emission coefficients and appear in the exponents of the dc characterizing equations, (4.4-1) and (4.4-2).

ϕ_C, ϕ_B, and ϕ_S (See VJC, VJE, and VJS.)

PTF is the excess phase at $f = \text{TF}/(2\pi)$ and is used to characterize the actual transit time. It is used in determining the accumulated charge on parasitic capacitors. The interested reader should refer to subroutine BJT in the SPICE source code for the specific formulation.

q is the charge of an electron. It is a physical constant equal to 1.602×10^{-19} coulomb.

RB is the zero-bias base resistance. The actual zero-bias base resistance used in SPICE, R_b of Fig. 4.4–1, is a function of RB, RBM, and IRB. If IRB is not specified, R_b is calculated from the expression

$$R_b = \frac{\text{RB}}{A_n Q_B} + \frac{\text{RBM}}{A_n}\left(1 - \frac{1}{Q_B}\right) \qquad \text{(4C-2)}$$

where Q_B is as defined in (4.4-8). If IRB is specified, the expression for R_b is quite unwieldy. For details, see subroutine BJT of the SPICE source code.

RBM is the minimum base resistance at high currents. The parameters RB, RBM, and IRB are used to characterize the base resistance.

RC and **RE** are the collector and emitter series resistances respectively. SPICE obtains the actual collector and emitter resistances by dividing these parameters by the area normalization factor, A_n.

θ (See XCJC.)

T is temperature in degrees Kelvin.

TF and **TR** are the forward and reverse transit times. These are key parameters in determining the accumulated charge parasitic capacitors. The reader should consult subroutine BJT in the SPICE source code for details.

VAF and **VAR** (V_{AF} and V_{AR}) are the forward and reverse Early voltages, respectively. These SPICE input parameters contribute considerably to the non-infinite output impedance at the collector of the BJT. The effects of the Early voltages on the dc *I-V* characteristics of the BJT are apparent from (4.4-1)–(4.4-3).

VJC, VJE, and **VJS** (ϕ_C, ϕ_B, ϕ_S) represent the built-in potential of the C–B, E–B, and C–S junctions. They are used to characterize the depletion region capacitances as indicated in (4.4-12)–(4.4-15).

V_t is an internal parameter calculated from the expression

$$V_t = \frac{kT}{q} \tag{4C-3}$$

The parameters k, T, and q have been previously defined.

VTF is a SPICE input parameter characterizing the B-C voltage dependence of the forward transit time. The interested reader should consult subroutine BJT in the SPICE source code for details.

XCJC is the fraction of the B–C depletion capacitance that is to be assigned to the internal base node. This SPICE input parameter appears as the parameter θ in equations (4.4-13) and (4.4-15).

XTB is the temperature exponent for both the forward and reverse beta as indicated by (4.4-22) and (4.4-23). XTB is a SPICE input parameter.

XTF is a SPICE input parameter which characterizes the bias dependence of TF. The reader should check subroutine BJT in the SPICE source code for details.

XTI denotes the saturation current temperature exponent. It is used along with EG to characterize the temperature dependence of IS as indicated by (4.4-19). XTI is a SPICE input parameter.