TABLE 4.4-1
Parasitic capacitors in BJT model

	Operating region				
	Reverse bias			Forward bias	
	Depletion junction	Accumulation charge	Transition voltage	Depletion junction	Accumulation charge
C_{BE}	C_{BEDR}	C_{BEAR}	V_{BET}	C_{BEDF}	C_{BEAF}
C_{BC}	C_{BCDR}	C_{BCAR}	V_{BCT}	C_{BCDF}	C_{BCAF}
C_{CS}	C_{CSDR}	$C_{CSAR} = 0$	$V_{CST} = 0$ V	C_{CSDF}	$C_{CSAF} = 0$
C_{XS}	C_{XSDR}	$C_{XSAR} = 0$	V_{XST}	C_{XSDF}	$C_{XSAF} = 0$

4.4-15, respectively, at the transition voltage. These capacitances are functionally of the form of the corresponding extension used for characterizing the diode capacitance under forward bias as given by (3.2-9).

The accumulated charge capacitors C_{CSAR}, C_{CSAF}, C_{XSAR}, and C_{XSAF} are all zero. The forward and reverse bias accumulation charge capacitors are assumed equal (i.e., $C_{BEAR} = C_{BEDF}$ and $C_{BCAR} = C_{BCDF}$). It remains to characterize C_{BEAR} and C_{BCAR}. The functional form of these capacitors is given in (3.1-29) of Chapter 3. Unfortunately, the transit time is affected by the operating conditions (V_{BE} and V_{BC}) of the BJT. The parameters TF, XTF, VTF, ITF, PTF, and TR are used to characterize the transit times. The expression for the effective transit times is quite unwieldly, so it will not be given here. The interested reader should examine subroutine BJT (especially the expressions for CAPBE and CAPBC) in the SPICE source code for details.[6]

4.4.3 BJT Noise Model

Five noise sources are used to model the noise characteristics of the BJT. Thermal resistance noise sources are characterized by current sources with a spectral density of

$$S_{NR} = \frac{4kT}{R_x} \qquad \text{for } x \in \{b, e, c\} \tag{4.4-16}$$

These are modeled in parallel with the three resistors R_b, R_e, and R_c of Fig. 4.4-1. Parameters in this equation are defined in Appendix 4C. Shot and flicker noise are modeled by two current sources, the first with a spectral density of

$$S_{NB} = 2qI_{CQ} \tag{4.4-17}$$

is connected from the base to the emitter of T2 in Fig. 4.4-1. The second current source has a spectral density of

$$S_{NC} = 2qI_{BQ} + \frac{K_F I_{BQ}^{AF}}{f} \tag{4.4-18}$$

and is connected from the collector to the emitter of T2 in the same figure. The parameters q, k, and T have been defined previously and are included in Appendix 4C. K_F and AF are SPICE input parameters and f is frequency in Hz. I_{BQ} and I_{CQ} represent the quiescent values of I_B and I_C, respectively. All noise sources in the BJT are assumed to be uncorrelated.

4.4.4 Temperature Dependence of the BJT

Several of the parameters that characterize the BJT are temperature dependent. SPICE models the temperature dependence of the saturation currents (I_S, I_{SE}, and I_{SC}), betas (BF and BR), the junction capacitance parameters ($C_{JE}, C_{JC}, C_{JS}, \phi_B, \phi_C$ and ϕ_S), and the noise coefficients K_F and A_F. The saturation currents at a temperature T are characterized by the equations

$$I_S(T) = I_S(T_1)\left(\frac{T}{T_1}\right)^{\mathrm{XTI}} \exp\left[\left(\frac{T}{T_1} - 1\right)\frac{\mathrm{EG}(T) \cdot q}{kT}\right] \tag{4.4-19}$$

$$I_{SE}(T) = I_{SE}(T_1)\left(\frac{T}{T_1}\right)^{[(\mathrm{XTI/NE}) - \mathrm{XTB}]} \exp\left[\left(\frac{T}{T_1} - 1\right)\left(\frac{\mathrm{EG}(T) \cdot q}{\mathrm{NE} \cdot kT}\right)\right] \tag{4.4-20}$$

$$I_{SC}(T) = I_{SC}(T_1)\left(\frac{T}{T_1}\right)^{[(\mathrm{XTI/NC}) - \mathrm{XTB}]} \exp\left[\left(\frac{T}{T_1} - 1\right)\left(\frac{\mathrm{EG}(T) \cdot q}{\mathrm{NC} \cdot kT}\right)\right] \tag{4.4-21}$$

where T_1 is any reference temperature, EG(T) is given in Eq. (4.2-63) and the remaining parameters are SPICE input parameters.

The parameters BF and BR are given by the expressions

$$\mathrm{BF}(T) = \mathrm{BF}(T_1)\left(\frac{T}{T_1}\right)^{\mathrm{XTB}} \tag{4.4-22}$$

$$\mathrm{BR}(T) = \mathrm{BR}(T_1)\left(\frac{T}{T_1}\right)^{\mathrm{XTB}} \tag{4.4-23}$$

The temperature dependence of $C_{JC}, C_{JE}, C_{JS}, \phi_B, \phi_C$, and ϕ_S is given for $Y \in \{C, E, S\}$ by

$$C_{JY}(T) = C_{JY}(T_1) \cdot [1 + \theta_Y(T)] \tag{4.4-24}$$

where

$$\theta_Y(T) = \mathrm{MJ}Y \cdot \{0.0004(T - T_1) + 1 - [\phi_Y(T)/\phi_Y(T_1)]\} \tag{4.4-25}$$

and

$$\phi_Y(T) = \phi_Y(T_1) \cdot (T/T_1) + \phi_{\mathrm{BF}}(T) \tag{4.4-26}$$

and where $\phi_{\mathrm{BF}}(T)$ is given by Eq. (4.2-64).

The temperature dependence of K_F and A_F is modeled by (4.2-61) and (4.2-62) where $\phi_B(T)$ is replaced with $\phi_E(T)$. Additional details can be found in subroutine TMPUPD of the SPICE source code.

4.5 SUMMARY

Models for the MOSFET, diode, and BJT which are used in the program SPICE have been presented. The similarity between these more detailed models and the simpler models discussed in Chapter 3 should be apparent. Although these models have been presented in the context of SPICE, they should be viewed, in their own right, as a more complete analytical characterization of the three basic devices, which form the nucleus of most integrated circuits. Many parts of these models were not developed specifically for SPICE but rather evolved over the years in the technical literature as researchers attempted to understand the fundamental operation of the basic devices. In many demanding situations, the designers should find the relevant analytical model equations presented in this chapter directly useful for design, insight, and optimization.

The authors have repeatedly observed confusion and uncertainty by both students and practicing engineers about the validity of simulations. This is often attributable to either lack of knowledge of the model used in their simulator or lack of understanding of how specific model parameters impact performance. A firm understanding of the models used in a simulator is essential for utilization of these powerful tools. The glossaries and tables which appear in the appendices of this chapter should prove to be a useful reference for SPICE users.

REFERENCES

1. A. Vladimirescu, K. Ahang, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, "SPICE Version 2G User's Guide," Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, 1981.
2. A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE 2," UCB/ERL M80/7, University of California, Berkeley, Engineering Research Laboratory, Feb. 1980 (Revised Oct. 1980).
3. L. W. Nagel, "SPICE 2: A Computer Program to Simulate Semiconductor Circuits," UBC/ERL M520, University of California, Berkeley, Engineering Research Laboratory, May 1975.
4. S. Liu, "A Unified CAD Model for MOSFETS," UCB/ERL M 81/31, University of California, Berkeley, Engineering Research Laboratory, May 1981.
5. G. D. Anderson, "Evaluation and Optimization of MOS Device Drain Conductance Modeling in the SPICE Level 2 Model," UCB/ERL M84/3, University of California, Berkeley, Engineering Research Laboratory, Jan. 1984.
6. SPICE Source Code, Version 2G.6, Electronics Research Laboratory, University of California, Berkeley, March 1983.
7. B. J. Sheu, D. L. Scharfetter, and P. K. Ko, "SPICE 2 Implementation of BSIM," UCB/ERL M85/42, University of California, Berkeley, Engineering Research Laboratory, May 1985.
8. W. Christopher, "SPICE 3A7 User's Manual," Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, 1986.
9. T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni–Vincentelli, "SPICE 3A7 User's Manual," Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, 1986.

10. P. M. Lee, "BSIM—Substrate Current Modeling," UCB/ERL M86/49 University of California, Berkeley, Engineering Research Laboratory, June, 1986.
11. J. Pierret, "A MOS Parameter Extraction Program for the BSIM Model," UCB/ERL M84/99, University of California, Berkeley, Engineering Research Laboratory, November 1984.
12. M.-C. Jeng, B. J. Sheu, and P. K. Ko, "BSIM Parameter Extraction—Algorithms and User's Guide," UCB/ERL M85/79, University of California, Berkeley, Engineering Research Laboratory, October 1985.
13. C. T. Sah, "Characteristics of the Metal-Oxide-Semiconductor Transistor," *IEEE Trans. Electron Devices, vol. ED-11, pp. 324–345, July 1964.*
14. P. Antonetti, D. D. Cariglia, and E. Profumo, "CAD Model for Threshold and Subthreshold Conduction in MOSFETs," *IEEE J. Solid State Circuits*, vol. SC-17, pp. 454–458, June 1982.
15. T. Grotjon and B. Hoefflinger, "A Parametric Short-Channel MOS Transistor Model for Subthreshold and Strong Inversion Current," *IEEE J. Solid State Circuits,* vol. SC–19, pp. 100–112, Feb. 1984.
16. P. Yang, B. Epler, and P. K. Chatterjee, "An Investigation of Charge Conservation Problem for MOSFET Circuit Simulation," *IEEE J. Solid State Circuits,* vol. SC–18, pp. 128–133, Feb. 1983.
17. D. E. Ward and R. W. Dutton, "A Charge-Oriented Model for MOS Transient Capacitances," *IEEE J. Solid State Circuits*, vol. SC–13, pp. 703–708, October 1978.
18. "PSPICE Documentation," Micro Sim Corporation, Laguna Hills, CA, 1986.
19. R. N. Hall, "Power Rectifiers and Transistors," *Proc. IRE*, vol. 40, pp. 1512–1519, Nov. 1952.
20. H. K. Gummel and H. C. Poon, "An Integral Charge Control Model of Bipolar Transistors," *Bell Syst. Tech. Journal*, vol. 49, pp. 827–852, May 1970.
21. I. Getreu, "Modeling the Bipolar Transistor," Tektronix Inc., Beaverton, Oregon, 1976.
22. P. W. Tuinenga, "*SPICE: A Guide to Circuit Simulation and Analysis Using PSPICE*," Prentice-Hall, Englewood Cliffs, NJ, 1988.
23. P. Antognetti and Massobrio, "*Semiconductor Device Modeling with SPICE*," McGraw-Hill, New York, 1988.

PROBLEMS

4.1. Assume the transistor in Figure P4.1 is fabricated in the CMOS process characterized in Appendix 2B.

(*a*) Determine V_{SS} so that $V_{OQ} = 1$ V (when $V_i = 0$). Use the Level 1 SPICE MOSFET model.

(*b*) Compare the small signal voltage gain using the Level 1 and Level 2 models with V_{SS} as determined in (*a*).

(*c*) Compare the small signal 3 dB bandwidth using the Level 1 and Level 2 models at the same Q-point as used in (*a*) and (*b*).

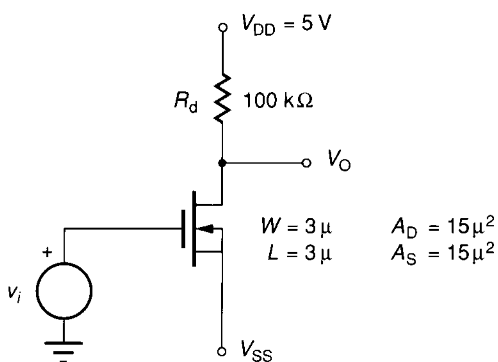

FIGURE P4.1
Problem 4.1.

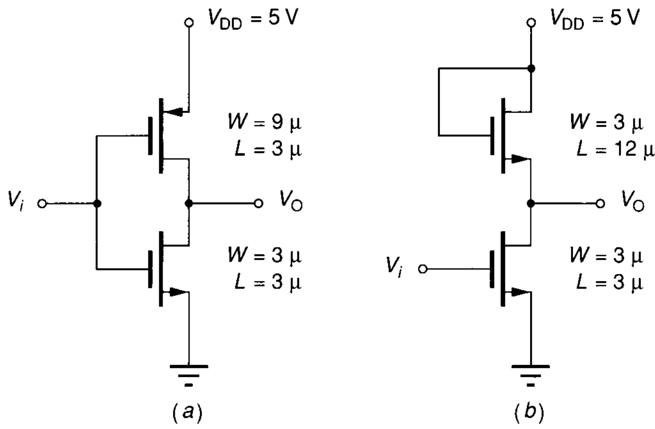

FIGURE P4.2
Problem 4.2.

4.2. (*a*) Use SPICE to obtain the dc transfer characteristics for the two circuits shown in Fig. P4.2, using first the Level 1 model and then the Level 2 model. Assume the transistors are characterized by the CMOS process of Appendix 2B.

(*b*) Obtain the low frequency small signal voltage gain for both circuits and plot as the quiescent input voltage is varied between 0 V and 5 V.

(*c*) If these circuits are loaded by a 50 fF capacitor, determine the response to a 5 V pulse input that lasts 100 μsec.

(*d*) If these circuits are biased at $V_{OQ} = 2.5$ V, determine the small signal 3 dB bandwidth of the voltage gain $A_v = v_o/v_i$.

4.3. Compare the dc transfer characteristics (I_D vs. V_{DS} as a function of V_{GS}) for a MOSFET using the Level 1 and Level 2 SPICE models. Use the SPICE process model parameters of Appendix 2B.

4.4. Compare the small signal output conductance when λ is an input parameter in the Level 2 model to that obtained if λ is calculated by Eq. 4.2-34. Assume the process parameters of the CMOS process discussed in the Appendices of Chapter 2 when making this comparison.

4.5. Plot I_D vs. V_{GS} for .3 V < V_{GS} < 5 V for the circuit in Fig. P4.5 using a logarithmic I_D axis. Use the process of Appendix 2B and include any subthreshold currents.

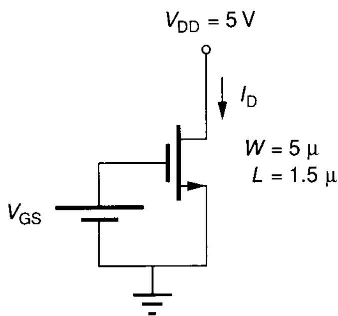

FIGURE P4.5
Problem 4.5.

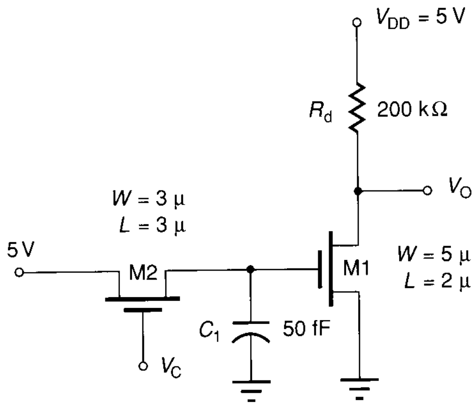

FIGURE P4.6
Problem 4.6.

4.6. In Fig. P4.6, at time $t = 0$ the control voltage V_C is taken from 5 V to 0 V and maintained at 0 V.

(*a*) If M2 serves as an ideal switch (short between drain and source when $V_C = 5$ V and open when $V_C = 0$ V), what is $V_O(t)$?

(*b*) Leakage current through the drain or source diffusion of M2 will discharge C. Use the process of Appendix 2B to find how M2 should be laid out to minimize the output voltage droop.

(*c*) Plot $V_O(t)$ if the source diffusion of M2 contacting the gate of M1 is $3\ \mu \times 12\ \mu$.

4.7. Practically determine and illustrate the effect of the mobility degradation parameters UCRIT, ULTRA, and UEXP on the I_D–V_{DS} characteristics of the MOSFET.

4.8. Plot C_{GS}, C_{GD}, C_{BD}, C_{BS}, and C_{BG} in the following two cases for the MOSFET shown in Fig. P4.8.

(*a*) vs. V_{GS} for $0 \leq V_{GS} \leq 5$ V if $V_{DS} = 5$ V and $V_{BS} = -5$ V.

(*b*) vs. V_{GS} for $0 \leq V_{GS} \leq 5$ V if $V_{DS} = 5$ V and $V_{BS} = 0$.

4.9. Plot C_{BE}, C_{BC}, and C_{CS} vs. I_B for 1 nA $\leq I_B \leq 100\ \mu$A for the BJT shown in Fig. P4.9. Assume $V_{CE} = 5$ V.

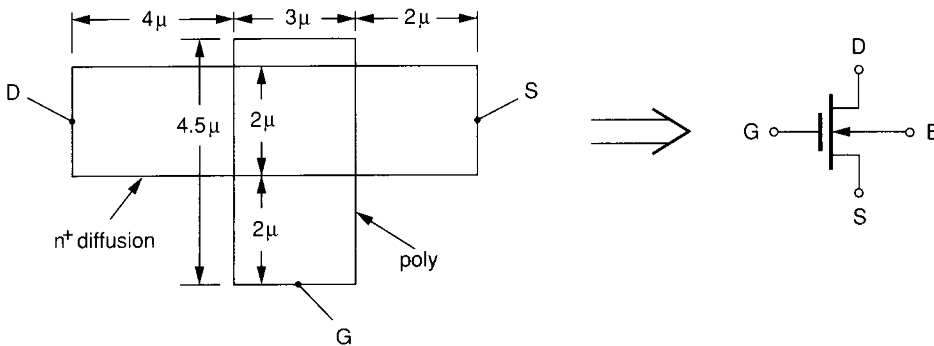

FIGURE P4.8
Problem 4.8.

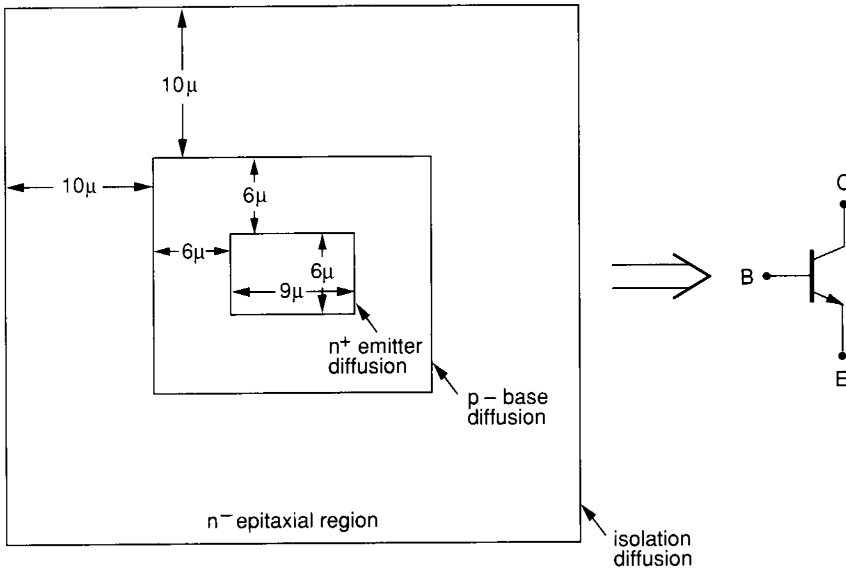

FIGURE P4.9
Problem 4.9.

4.10. A CMOS digital inverter loaded by an identical device is shown in Fig. P4.10. Assume the device is fabricated in the CMOS process of Appendix 2B.

(*a*) If a pulse of height 5 V is applied to the input (V_i) at $t = 0$, what is the minimum pulse width that can be applied if V_{O1} must swing down to at least 0.5 V? Assume $C_L = 0$.

(*b*) How does the minimum pulse width change if 40 identical inverters load the node V_{O1}? Assume $C_L = 0$.

(*c*) If the digital inverter is loaded by only a 2pF load, how does the response time of this circuit compare to that obtained in (*a*)?

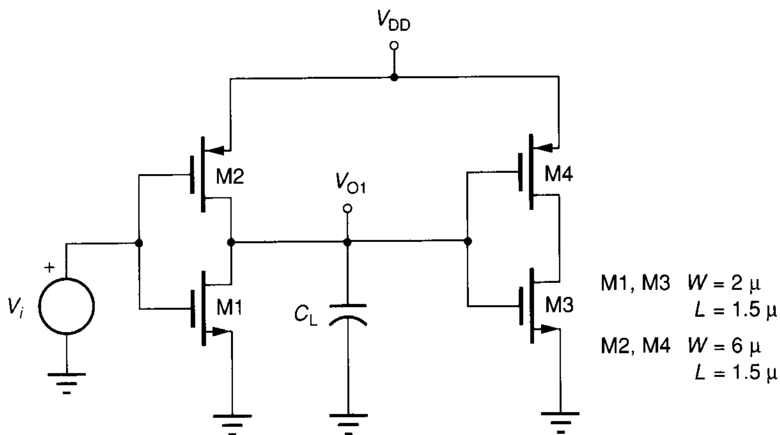

FIGURE P4.10
Problem 4.10.

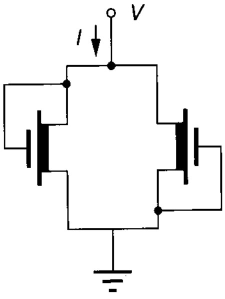

FIGURE P4.11
Problem 4.11.

4.11. Plot I vs. V for the circuit shown in Fig. P4.11 for $-3\text{V} \le V \le 3$ V. Assume M1 and M2 matched with $W = 3\ \mu$ and $L = 30\ \mu$. Use the NMOS process parameters of Appendix 2A.

4.12. If I_{BIAS} in Fig. P4.12 is set to 100 μA and V_{B1} and V_{B2} are adjusted so that $V_{\text{O1Q}} = V_{\text{O2Q}} = 5$ V, obtain from SPICE the small signal voltage gain and the 3 dB bandwidth of each circuit for a small signal excitation. Use the SPICE process model parameters of Appendices 2B and 2C and include realistic parasitics for M1 and Q1.

4.13. Assume that V_{B1} and V_{B2} in Problem 4.12 are fixed at the value needed to make $V_{\text{O1Q}} = V_{\text{O2Q}} = 5$ V at room temperature (30°C). What will happen to the Q-point, voltage gain and 3 dB bandwidth for the two circuits of Fig. P4.12 if the temperature is increased to 200°C? Decreased to −50°C?

4.14. The circuit shown in Fig. P4.14 has been proposed as a linear temperature transducer (output voltage linearly proportional to temperature). Plot V_{O} vs. temperature for $-50°\text{C} \le T \le 200°\text{C}$, and comment on the suitability of this device as a temperature transducer. Use the model parameters of Appendix 2C in your simulations. Assume $I_{\text{REF}} = 1\ \mu A$.

4.15. Examine the MOSFET shown in Fig. P4.15.
(*a*) Adjust V_{BB} so that $V_{\text{OQ}} = 3$ V.

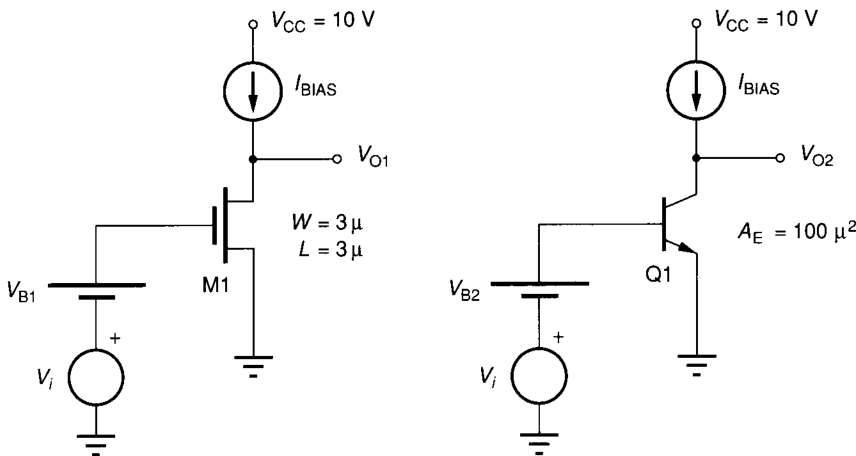

FIGURE P4.12
Problem 4.12.

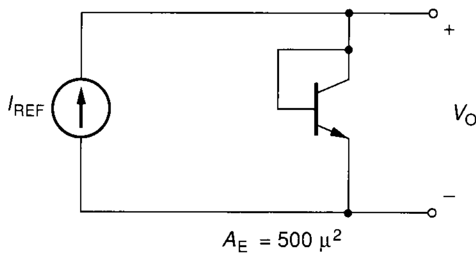

FIGURE P4.14
Problem 4.14.

(*b*) Determine V_m so that the peak to peak output swing is about 2 V around the Q-point established in (*a*).

(*c*) If the time varying output voltage is 2 V p–p, determine the signal to noise ratio of the output voltage in the frequency band [100 Hz, 20 KHz]. Use the MOS process of Appendix 2B and typical noise parameters.

(*d*) Repeat parts (*a*), (*b*) and (*c*) if the MOSFET is replaced with a BJT with an emitter area of 500 μ^2 that is characterized by the process of Appendix 2C and compare with the results obtained for the MOSFET.

4.16. Use SPICE and the process description of Appendix 2C to find the following quantities in the circuit of Fig. P4.16.

(*a*) Determine the quiescent output voltage and the small signal model parameters of Q_1 at the Q-point.

(*b*) Determine the small signal voltage gain using the ac analysis in SPICE.

(*c*) Determine the steady state output voltage using a transient analysis if the input $v_i(t)$ is defined by

$$v_i(t) = \begin{cases} 0 & t < 0 \\ .005 \sin 1000t & t \geq 0 \end{cases}$$

(*d*) In calculating a steady state response due to a sinusoidal excitation with SPICE, how does the effort and computation time required for a transient analysis compare to that required for a small signal ac analysis?

4.17. (*a*) From Eqs. 4.2-21 and 4.2-24, obtain an expression for the effective width reduction, WR = $W - W_{eff}$, where $W_{\text{eff}} = W(2 - \eta)$ in terms of the parameter

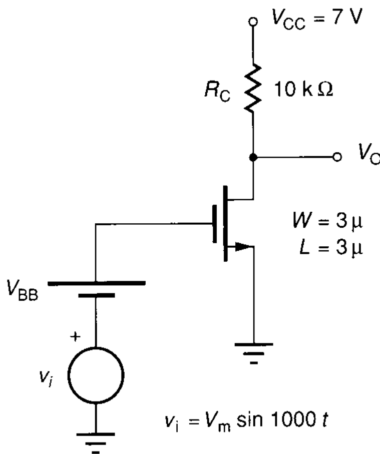

FIGURE P4.15
Problem 4.15.

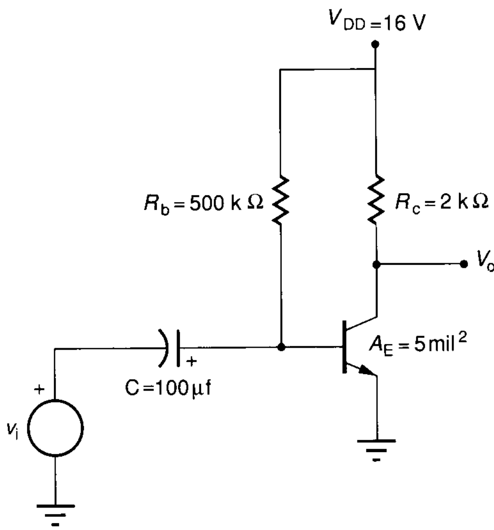

FIGURE P4.16
Problem 4.16.

DELTA when the MOSFET is operating in the saturation region.

(*b*) For drawn widths of $W = 5\ \mu$, $2\ \mu$, and $1\ \mu$ plot the effective length, L_{eff}, of a MOSFET as the drawn length is reduced from $10\ \mu$ to $0.5\ \mu$. Assume the SPICE model parameters of Appendix 2B remain valid as the drawn length is varied.

(*c*) Using the same model, plot the effective device width as the drawn width is varied between $10\ \mu$ and $0.5\ \mu$ for drawn lengths of $L = 5\ \mu, 2\ \mu$, and $1\ \mu$.

APPENDIX 4A MOSFET PARAMETER DEFINITIONS

A brief alphabetical listing of the major parameters used in the MOS device models follows. Those parameters that serve specifically as SPICE input parameters are summarized in Table 4A. For more details about these parameters, the reader is referred to the SPICE User's Guide[1] or the SPICE source code[6].

AD represents the area of the drain diffusion. This serves as a SPICE input parameter which is entered on the device element card.

AF denotes the flicker noise exponent. This, along with the parameter KF, is used to characterize a noise current source that goes from drain to source in the MOSFET model. The RMS noise current density is given by

$$I_{\mathrm{N}} = \sqrt{\frac{8kTg_{\mathrm{m}}}{3} + \frac{\mathrm{KF} \cdot I_{\mathrm{dq}}^{\mathrm{AF}}}{fC_{\mathrm{OX}}L^2}} \tag{4A-1}$$

where g_{m} is the saturation region transconductance gain at the operating point and I_{dq} is the quiescent drain current. The first term under the radical represents

TABLE 4A
SPICE input parameter summary for MOSFET

Parameter	Symbol	Name	Default if non-zero	How entered directly†	Levels valid	Characterizing eqs. if not entered	
						Level 1	Level 2
LEVEL		Model level (1,2, or 3)	1	.MOD (1)			
VTO	V_{T0}	Zero-bias threshold voltage		.MOD (2)	all	4.2-16	4.2-16
KP	K'	Transconductance parameter	$2 \times 10^{-5} A/V^2$	.MOD (3)	all	4.2-11	4.2-11
GAMMA	γ	Bulk threshold parameter		.MOD (4)	all	4.2-14	4.2-14
PHI	ϕ	Surface potential	.6 V	.MOD (5)	all	4.2-15	4.2-15
LAMBDA	λ	Channel-length modulation		.MOD (6)	2	4.2-34	4.2-34
RD		Drain ohmic resistance		.MOD (7)	all		
RS		Source ohmic resistance		.MOD (8)	all		
CBD	C_{BD}	Zero-bias bulk–drain junction capacitance		.MOD (9)	all		
CBS	C_{BS}	Zero-bias bulk–source junction capacitance		.MOD (10)	all		
IS		Bulk junction saturation current	10^{-14} A	.MOD (11)	all		
PB	ϕ_B	Bulk junction potential	.5 V	.MOD (12)	all		
CGSO	C_{GSO}	Gate–source overlap capacitance per meter of channel width of source		.MOD (13)	all		
CGDO	C_{GDO}	Gate–drain overlap capacitance per meter of channel width of drain		.MOD (14)	all		
CGBO	C_{GBO}	Gate–bulk overlap capacitance per meter of channel length		.MOD (15)	all		
RSH		Sheet resistance of drain & source diffusions		.MOD (16)	all		
CJ		Zero-bias bulk junction bottom capacitance area density		.MOD (17)	all		
MJ		Bulk junction bottom grading coefficient	.5	.MOD (18)	all		

TABLE 4A
(Continued)

Parameter	Symbol	Name	Default if non-zero	How entered directly†	Levels valid	Characterizing eqs. if not entered: Level 1	Level 2
CJSW		Zero-bias bulk junction sidewall capacitance per meter of junction perimeter		.MOD (19)	all		
MJSW		Bulk junction sidewall grading coefficient		.MOD (20)	all		
JS		Bulk junction saturation current area density		.MOD (21)	all		
TOX	T_{OX}	Gate oxide thickness	10^{-7}m	.MOD (22)	2,3		
NSUB	N_{SUB}	Substrate doping		.MOD (23)	all		
NSS	N_{SS}	Surface state density		.MOD (24)	all		
NFS		Fast surface state density		.MOD (25)	all		
TPG		Type of gate material	1	.MOD (26)	all		
XJ		Metallurgical junction depth		.MOD (27)	all		
LD	L_D	Lateral diffusion		.MOD (28)	all		
UO	μ_O	Nominal surface mobility	600 $cm^2/V \cdot A$	.MOD (29)	all		
UCRIT		Critical field for mobility degradation	10^4	.MOD (30)	2		
UEXP		Critical field exponent in mobility degradation		.MOD (31)	2		
UTRA		Mobility transverse field coefficient		.MOD (32)	2		
VMAX	V_{MAX}	Maximum carrier drift velocity		.MOD (33)	all		
NEFF	N_{EFF}	Total channel charge	1.0	.MOD (34)	2		
XQC		Thin-oxide capacitance model flag and coefficient of channel charge	1.0	.MOD (35)	all		
KF	K_F	Flicker noise coefficient		.MOD (36)	all		
AF	A_F	Flicker noise exponent	1.0	.MOD (37)	all		
FC		Coefficient for forward-bias depletion capacitance	0.5	.MOD (38)	all		

TABLE 4A
(Continued)

Parameter	Symbol	Name	Default if non-zero	How entered directly†	Levels valid	Characterizing eqs. if not entered	
						Level 1	Level 2
DELTA		Width effect on threshold voltage		.MOD (39)	2,3		
THETA		Mobility degradation		.MOD (40)	3		
ETA		Static feedback		.MOD (41)	3		
KAPPA		Saturation field factor	0.2	.MOD (42)	3		
L		Drawn channel length		DE	all		
W		Drawn channel width		DE	all		
AD		Drain area		DE	all		
AS		Source area		DE	all		
PD		Drain perimeter		DE	all		
PS		Source perimeter		DE	all		
NRD		Drain sheet resistance		DE	all		
NRS		Source sheet resistance		DE	all		

†.MOD (x) denotes the entry is via the .MODEL card (line) at the xth parameter location in Reference 1, DE notes entry from the device element card (line). Since the input parser in SPICE looks for each parameter by name, the ordering as denoted by the parameter x is arbitrary but was included for convenient reference to Reference 1.

shot noise and the second term $1/f$ noise. The corresponding spectral densities appear in Eqs. 4.2-49 and 4.2-50.

$\boldsymbol{\alpha}$ is used to correct γ for short channel effects. It is not an input parameter to SPICE and is defined by (4.2-30); it provides linear correction of γ as indicated in (4.2-29).

AS represents the area of the source diffusion. This serves as a SPICE input parameter which is entered on the device element card.

$\boldsymbol{\beta}$ is not used as a SPICE input parameter, but it is often used to reduce notational complexity in the dc MOSFET model. It is defined by the expression

$$\beta = \frac{\mu_0 C_{OX} W}{L} \tag{4A-2}$$

CBD and **CBS** (C_{BD} and C_{BS}) are SPICE input parameters which represent the zero-bias diffusion bottom capacitance of the bulk–drain and bulk–source junction capacitors, respectively. If not input, C_{BD} and C_{BS} are calculated from CJ, AD, and AS by the expressions

$$C_{BD} = \text{CJ} \cdot \text{AD}$$
$$C_{BS} = \text{CJ} \cdot \text{AS} \tag{4A-3}$$

CGBO, CGDO, and **CGSO** (C_{GBO}, C_{GDO}, and C_{GSO}) are SPICE input parameters that represent the *linear* capacitance density of the gate–bulk, gate–drain and gate–source overlap capacitors respectively. They are expressed in terms of capacitance per unit length. These capacitors are discussed in more detail in Sec. 4.2.3.

CJ is the SPICE input parameter which represents the zero-bias junction bottom capacitance density of the moat–bulk diffusions. It is expressed in terms of capacitance per unit area of the junction. The zero-bias junction bottom capacitance of the drain–bulk and source–bulk junctions can be obtained internally in SPICE from CJ by multiplying CJ by AD and AS, respectively. The total junction capacitances are then calculated from Eq. 4.2-43 for junctions under reverse bias and from Eq. 4.2-46 for junctions under forward bias. If not input, CJ is calculated internally from Eq. 4.2-44.

CJSW is the SPICE input parameter which represents the zero-bias sidewall capacitance density of the moat–bulk diffusions. It is expressed in terms of capacitance per unit length of the junction permitter. The zero-bias junction sidewall capacitances of the drain–bulk and source–bulk junctions are obtained internally in SPICE from CJSW by multiplying by PD and PS, respectively. The total junction capacitances are then obtained from Eq. 4.2-43 for junctions under reverse bias and from Eq. 4.2-46 for junctions under forward bias. If CJSW is not entered, the sidewall capacitances are assumed to be zero.

$\boldsymbol{C_{ox}}$ represents the capacitance density of the gate–channel junction. It is expressed in terms of capacitance per unit area. Although not input directly in SPICE, it is calculated internally from the expression

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} \tag{4A-4}$$

where ϵ_{ox} is the dielectric constant (more precisely, the real permittivity) of the gate oxide and T_{ox} is the gate oxide thickness. C_{ox} is a key parameter in the MOS device models. It appears in the defining expression of several major parameters including K' (4.2-11), γ (4.2-14), V_{TO} (4.2-16), V_{FB} (4.2-17) and V_{TH}.

DELTA is a SPICE input parameter that characterizes the effective width reduction in the Level 2 and Level 3 models. It appears in the expression for η given in (4.2-24). With DELTA equal to its ideal value of 0, η assumes the ideal value of 1. DELTA also appears in the expressions for V_{TH} and V^*_{TH} as given in (4.2-22) and (4.2-25), respectively.

$\boldsymbol{\epsilon_0}$ is the permittivity of free space. It is a physical constant equal to 8.86 $\times 10^{-14}$ F/cm.

$\boldsymbol{\epsilon_{ox}}$ is the dielectric constant (more precisely, the real permittivity) of SiO_2. It is a physical constant and is equal to $3.9\epsilon_0$.

$\boldsymbol{\epsilon_{si}}$ is the dielectric constant (more precisely, the real permittivity) of Si. It is a physical constant and is equal to $11.7\epsilon_0$.

ETA is a SPICE input parameter termed the static feedback effect parameter. It is an empirical constant and is used only in the Level 3 model. It should not be confused with the parameter η listed below.

$\boldsymbol{\eta}$ is not a SPICE input parameter; it is used to characterize width reduction in the Level 2 and Level 3 models. It is primarily dependent upon the SPICE input parameter DELTA as can be seen from (4.2-24). This should not be confused with the SPICE input parameter ETA discussed above.

FC is the SPICE input parameter which denotes the forward bias coefficient in the parasitic junction capacitance model. The junction is assumed "reverse biased" for a forward bias less than FC $\cdot\ \phi_B$, and its capacitance is characterized by (4.2-43). For a forward bias greater than FC $\cdot\ \phi_B$, the junction is assumed "forward biased" and the junction capacitance is characterized by (4.2-46).

GAMMA ($\boldsymbol{\gamma}$) is a SPICE input parameter called the bulk threshold. It plays a major role in the expression for the threshold voltage (Eqs. 4.2-9 and 4.2-16 for the Level 1 model, and 4.2-25 and 4.2-16 for the Level 2 model). If not input, it is calculated internally from N_{SUB} and T_{ox} by Eq. 4.2-14.

$\boldsymbol{\gamma_s}$ The parameter γ effectively decreases for short channel devices. The parameter $\gamma_s = \gamma(1 - \alpha)$, as defined by (4.2-29), is used in place of γ in the drain current expressions for the Level 2 and Level 3 models.

IS ($\boldsymbol{I_S}$) is the bulk junction saturation current; it is a SPICE input parameter. The current flowing through the bulk junction is characterized by the standard diode equation

$$I = I_S\left(e^{\frac{V_{FB}}{V_t}} - 1\right) \tag{4A-5}$$

where V_{FB} represents the forward bias on the junction. This parameter is of particular concern in such circuits as the basic DRAM cell where the charge loss on switched storage capacitors is primarily due to current flow into the bulk

through the reverse biased moat junction formed between either the drain or source diffusion of the switch and the bulk. Either IS or JS can be used to characterize the bulk junction current characteristics.

JS (J_S) is a SPICE input parameter that denotes the bulk junction current density; it is expressed in terms of current per unit area of junction area. If the parameter IS is not input, it is calculated from JS by multiplying JS by the junction area.

k is Boltzmann's constant. It is a physical constant equal to 1.381×10^{-23} J/°K.

$\mathbf{K}_2'$ is the transconductance parameter that appears in the expression for the drain current in the Level 2 model as indicated by (4.2-20) and (4.2-21). It differs from K′ in that the effective mobility, μ_s, is used in place of μ_o in the defining equation (4.2-28).

KF is a SPICE input parameter called the flicker noise coefficient. It appears in the expression for the noise current as indicated by (4.2-47).

KP (K') is a key SPICE input parameter termed the transconductance parameter. It appears in the expression for the drain current of the Level 1 model as indicated in (4.2-6) and (4.2-7). If not input, K' is calculated from the mobility and C_{ox} by (4.2-11).

KAPPA is the saturation field factor. This SPICE input parameter is an empirical constant used only in the Level 3 model.

L denotes the drawn length of the MOS transistor. It is entered on the device element card. The out diffusion of the drain and source regions geometrically reduces the length of the device by twice the lateral diffusion, LD, to the adjusted geometrical length, L_{adj}.

L_{adj} is the adjusted geometrical length and is internally calculated by the expression

$$L_{adj} = L - 2\text{LD} \tag{4A-6}$$

L_{eff} is the effective device length. In addition to the geometrical length reduction, additional reductions in the effective length occur due to the applied drain–source voltage. The expression for L_{eff} is given by (4.2-10) for the Level 1 model and by (4.2-33) and (4.2-34) for the Level 2 model.

LD is the SPICE input parameter denoting the lateral (out) diffusion of the drain and source regions under the gate. Since the out diffusion on the source side is generally equal to that on the drain side of the gate, the geometrical length is effectively reduced by 2LD as indicated by (4.2-52).

LEVEL indicates which model is to be used for analysis. If not entered on the MODEL card, Level 1 is assumed.

LAMBDA (λ) is a SPICE input parameter called the channel-length modulation parameter. It arises from the V_{DS} dependence of the effective channel length. The output conductance of the small signal model is also proportional to $1/\lambda$. If this parameter is forced by specifying it on the .MODEL input card, the robustness of the Level 2 model is seriously restricted. Specifically, λ as

determined by (4.2-34) is not used in the calculation of L_{eff} by (4.2-33) if λ is an input parameter. If not input, the parameter defaults to 0 in the Level 1 model or is calculated from (4.2-35) in the Level 2 MOSFET model.

MJ and **MJSW** are SPICE input parameters for the bulk junction bottom grading coefficient and the bulk junction sidewall grading coefficient, respectively. They appear only in equations (4.2-43) and (4.2-46), which characterize the parasitic bulk–moat junction capacitances.

NEFF (**N_{eff}**) is an input parameter for the total channel charge coefficient. It is used only in the Level 2 model and only when V_{MAX} is specified. In this case, N_{eff} serves as an empirical constant that modifies (4.2-32) to read

$$\text{XD} = \sqrt{\frac{2\epsilon_{si}}{qN_{eff}N_{SUB}}} \tag{4A-7}$$

NFS is a SPICE input parameter called the effective fast surface state density. It is used only in the Level 2 and Level 3 models. NFS has two purposes. First, it serves as a flag to determine whether SPICE will assume the current in cutoff to be zero or $I_{\text{weak inversion}}$ as indicated in (4.2-19). Its second purpose is to characterize $I_{\text{weak inversion}}$ as shown in References 1 and 6.

n_i is the intrinsic carrier concentration of silicon and is equal to 1.45×10^{10} cm $^{-3}$ at room temperature.

NRD and **NRS** are the number of squares of moat in the drain and source respectively. They can be entered on the device element card. If RD and RS are entered, these parameters are ignored. If RD and RS are not entered, the drain and source resistances are calculated from the expressions

$$\text{RD} = \text{RSH} \cdot \text{NRD}$$
$$\text{RS} = \text{RSH} \cdot \text{NRS} \tag{4A-8}$$

respectively, provided the sheet resistance of the moat, RSH, has been entered on the .MODEL card.

NSUB (**N_{SUB}**) is a SPICE input parameter indicating the substrate doping. It plays a key role in calculations of parameters used to define the threshold voltage.

NSS (N_{SS}) is a SPICE input parameter called the effective surface charge density. Although it can be used to define the flatband voltage (4.2-17), which subsequently determines V_{TO}, it is usually better to enter V_{TO} directly.

PB (**ϕ_B**) is a SPICE input parameter called the bulk junction potential (alternately, built-in potential). ϕ_B is used to characterize the bulk junction capacitors as indicated in (4.2-43) and (4.2-46).

PHI (**ϕ**) is a SPICE input parameter called the surface potential. If not input, this parameter is calculated from (4.2-15) provided N_{SUB} is input.

ϕ_{MS} is the metal-semiconductor work function difference. It is calculated internally in SPICE from (4.2-18) and is used to define the flatband voltage.

PS and **PD** can be entered on the device element card. They represent the perimeter of the source and drain, respectively. They are used for calculating the sidewall capacitance of the drain and source regions as indicated in (4.2-43) and (4.2-46).

q is the charge of an electron. It is a physical constant equal to 1.602×10^{-19} coulomb.

RD and **RS** are SPICE input parameters representing the series drain and source resistances, respectively. If not input, they are calculated from (4A-8), provided that the sheet resistance of the moat, RSH, is specified.

RSH is a SPICE input parameter representing the sheet resistance of the moat. To allow for geometrical device variations, it is often more convenient to specify RSH, NRD, and NRS, and then let SPICE calculate RD and RS from (4A-8), rather than to enter RD and RS directly.

T is a SPICE input parameter indicating the operating temperature of the circuit.

THETA is a SPICE input parameter. It is an empirical parameter used only in the Level 3 model.

TPG is a SPICE input parameter indicating the type of gate. It is a flag that assumes a value of +1 for poly gates with the same flavor (both n or both p doping) as the substrate, −1 for poly gates with the flavor opposite to that of the substrate, and 0 for aluminum gates.

TOX (T_{OX}) is the thickness of the gate oxide. It is a SPICE input parameter used to determine the key parameter C_{OX}.

UO (μ_o) is the surface mobility of the channel. It is a SPICE input parameter used to calculate K' (or K_2') if T_{OX} is entered and K' is not entered.

μ_s represents the degraded surface mobility. It is an internal parameter and used only in the Level 2 model. SPICE uses the parameters UCRIT, UTRA, and UEXP to characterize μ_s as indicated by (4.2-36); the μ_s is used to define the transconductance parameter for the Level 2 model, K_2', as shown in (4.2-28).

UCRIT, UEXP, and **UTRA** are SPICE input parameters used to characterize the degraded surface mobility, μ_s, as indicated by (4.2-36).

V_{FB} is the flatband voltage. It is an internal SPICE parameter characterized by (4.2-17).

VMAX (V_{MAX}) is the maximum drift velocity of carriers in the channel. It is a SPICE input parameter which partially defines the transition region between ohmic and saturation in the Level 2 model. See Reference 2 for a more complete discussion of V_{MAX}. It is ignored in the Level 1 model.

V_t is an internal parameter calculated from the expression

$$V_t = \frac{kT}{q} \tag{4A-9}$$

where k is Boltzmann's constant, T is temperature in °K, and q is the charge of an electron. It is used for calculating the bulk–moat reverse saturation current as

indicated by (4A-5) and the drain current when operating in weak inversion. V_t should not be confused with V_T, the notation used for threshold voltage in Chapter 3.

VTO (V_{T0}) is a SPICE input parameter. It is the zero-bias ($V_{BS} = 0$) threshold voltage. If not input, it is calculated from (4.2-16).

V_T (See V_{TH} definition.)

V_{TH} is the threshold voltage of the device. It is used to characterize the cutoff transition region. It is an internal parameter determined by (4.2-9) for the Level 1 model and (4.2-25) for the Level 2 model. In Chapter 3, the variable V_T was used to denote the threshold voltage. V_T should not be confused with $V_t = kT/q$.

V^*_{TH} is nearly equal to V_{TH} in the Level 2 model. It is an internal parameter used to characterize the drain currents as indicated by (4.2-20) and (4.2-21). V^*_{TH} is determined from (4.2-25). V_{BIN} is used for V^*_{TH} in the SPICE source code and some of the other SPICE documentation.

W denotes the drawn width of the MOS transistor. It is entered on the device element card.

W_S and W_D are defined in equations (4.2-31) and (4.2-32), respectively.

XJ is the metallurgical junction depth. It is a SPICE input parameter which is used to characterize the effective bulk threshold parameter, γ_s, as indicated by (4.2-30).

XQC is a SPICE input parameter used to denote the percent of channel charge that is associated with the drain. It is used in the approximation which converts distributed channel charge to lumped drain and source charge when the device is operating in the saturation region. The reader is referred to Reference 2 and the SPICE source code[6] for additional details.

APPENDIX 4B DIODE PARAMETER DEFINITIONS

A brief alphabetical listing of the major parameters used in the DIODE device models follows. Those parameters that serve specifically as SPICE input parameters are summarized in Table 4B. For more details about these parameters, the reader is referred to Reference 1 or to the SPICE source code [6].

AF (A_F) denotes the flicker noise exponent. This, along with the parameter KF, is used to characterize the flicker noise in the diode. A noise current source in shunt with diode D2 in Fig. 4.3-1 is used to characterize the shot and flicker noise in the diode. This RMS current source is modeled by the density equation

$$I_{NI} = \sqrt{2qI + \frac{\mathrm{KF} \cdot I^{\mathrm{AF}}}{f}} \tag{4B-1}$$

where I is the diode current, f is the frequency in Hz, and q is the charge of an electron. The noise model of the diode in SPICE is completed by adding a second noise current source, which represents thermal noise in R_s, in shunt with the series resistor R_s in Fig. 4.3-1. The density of this RMS current is given by

TABLE 4B
SPICE input parameter summary for diode

Parameter	Symbol	Name	Default if non-zero	How entered†
IS		Saturation current	10^{-14}A	.MOD (1)
RS	r_s	Ohmic resistance		.MOD (2)
N	n	Emission coefficient	1	.MOD (3)
TT	τ	Transit time		.MOD (4)
CJO	C_{jo}	Zero-bias junction capacitance		.MOD (5)
VJ	ϕ_B	Junction potential	1 V	.MOD (6)
M	m	Junction grading coefficient	0.5	.MOD (7)
EG		Activation energy	1.11 V	.MOD (8)
XTI		Saturation current temp.exp.	3.0	.MOD (9)
KF	K_F	Flicker noise coefficient		.MOD (10)
AF	A_F	Flicker noise exponent	1	.MOD (11)
FC		Coefficient for forward-reverse bias transition	0.5	.MOD (12)
BV		Reverse breakdown voltage	∞	.MOD (13)
IBV		Current at breakdown voltage	1 mA	.MOD (14)
AREA	A_n	Normalized junction area	1	DE

†.MOD (x) denotes the entry is via the .MODEL card (line) at the xth parameter location in Reference 1. DE notes entry from the device element card (line). Since the input parser in SPICE looks for each parameter by name, the ordering as denoted by the parameter x is arbitrary but was included for convenient reference to Reference 1.

$$I_{N2} = \sqrt{\frac{4kT}{R_s}} \tag{4B-2}$$

where k is Boltzmann's constant and T is temperature in degrees Kelvin.

AREA (A_n) denotes the ratio of the cross-sectional area of the pn junction on the device input line to the cross-sectional area of the device modeled in the referenced .MODEL line. A_n is thus a normalized area and is dimensionless.

BV is the reverse breakdown voltage of the diode.

CJO (C_{jo}) is the junction capacitance at zero bias on the pn junction of the device modeled on the .MODEL line. Note that this differs from the closely related parameter CJ, which was used to model the junction capacitance in the MOSFET; CJO represents the capacitance while CJ represents the capacitance density.

EG denotes the activation energy. It is used along with the parameter XTI to characterize the temperature dependence of the saturation current[3]. The temperature dependence of IS is characterized by the expression

$$\text{IS}(T) = \text{IS}(T_1) \cdot \left(\frac{T}{T_1}\right)^{\text{XTI}} \exp\left[\left(\frac{q(\text{EG})}{kT}\right)\left(\frac{T}{T_1} - 1\right)\right] \tag{4B-3}$$

where T is temperature in degrees Kelvin, T_1 is any reference temperature, IS(T_1) is the saturation current at T_1, k is Boltzmann's constant, and q is the charge of an electron.

FC is the forward bias coefficient in the parasitic junction capacitance model which characterizes the transition voltage between the "reverse bias" and "forward bias" capacitance models. The junction is assumed "reverse biased" for a forward bias less than FC · ϕ_B.

IBV is the current in the diode at breakdown. It represents the nearly constant current that flows in the diode prior to breakdown. There is a fixed relationship between IBV, BV, and IS. If this relationship is not established with the specified parameters, SPICE adjusts either IBV or BV to attain the required relationship. See subroutines MODCHK and DIODE in the SPICE source code for details.

IS (I_S) denotes the saturation current in a diode. This SPICE input parameter is a key parameter in the diode equation.

k is Boltzmann's constant. It is a physical constant equal to 1.381×10^{-23} J/°K.

KF is called the flicker noise coefficient. It is used, along with AF, to characterize the flicker noise in the diode as indicated by equation (4B-1).

M (m) is called the junction grading coefficient. It characterizes, along with ϕ_B and C_{jo}, the junction capacitance as indicated by (4.3-4).

N (n) is the emission coefficient that appears in the diode equation (4.3-1). It is typically near unity.

RS denotes the series resistance in the diode. It is assumed to be an ideal resistor in SPICE.

TT (τ) is called the transient time. It is used to characterize the effects of stored change in the junction due to minority carrier injection as indicated by (4.3-4) and (4.3-5).

VJ (ϕ_B) is called the junction potential. It characterizes, along with C_{jo} and m, the junction capacitance as indicated by (4.3-4). The FC · ϕ_B product also determines the transition between "reverse bias" and "forward bias" on the junction.

XTI denotes the saturation current temperature exponent. It is used along with EG to characterize the temperature dependence of IS as indicated by (4B-3).

APPENDIX 4C
BJT PARAMETER DEFINITIONS

A brief alphabetical listing of the major parameters used in the BJT device models follows. Those parameters that serve specifically as SPICE input parameters are summarized in Table 4C. For more details about these parameters, the reader is referred to Reference 1 or to the SPICE source code[6].

TABLE 4C
SPICE input parameter summary for the BJT

Parameter	Symbol	Name	Default if non-zero	How entered directly†
IS	I_S	Transport saturation current	1.0E-16 A	.MOD (1)
BF		Ideal maximum forward beta	100	.MOD (2)
NF		Forward current emission coefficient	1	.MOD (3)
VAF	V_{AF}	Forward Early voltage	∞	.MOD (4)
IKF	I_{KF}	Forward beta high-current roll-off	∞	.MOD (5)
ISE	I_{SE}	B-E leakage saturation current		.MOD (6)
NE		B-E leakage emission coefficient	1.5	.MOD (7)
BR		Ideal maximum reverse beta	1	.MOD (8)
NR		Reverse current emission coefficient	1	.MOD (9)
VAR	V_{AR}	Reverse Early voltage	∞	.MOD (10)
IKR	I_{KR}	Reverse beta high-current roll-off	∞	.MOD (11)
ISC	I_{SC}	B-C leakage saturation current		.MOD (12)
NC		B-C leakage emission coefficient	2	.MOD (13)
RB	R_B	Zero bias base resistance		.MOD (14)
IRB		Current where base resistance falls halfway to its minimum value	∞	.MOD (15)
RBM		Minumum base resistance at high currents	RB	.MOD (16)
RE		Emitter resistance		.MOD (17)
RC		Collector resistance		.MOD (18)
CJE	C_{JE}	Zero-bias B–E depletion region capacitance		.MOD (19)
VJE	ϕ_B	B–E built–in potential	.75	.MOD (20)
MJE	M_{JE}	B–E junction exponential factor	.33	.MOD (21)
TF		Ideal forward transit time		.MOD (22)
XTF		Coefficient for bias dependence of TF		.MOD (22)
VTF		Voltage describing B–C voltage dependence of TF	∞	.MOD (23)
ITF		High-current effect on TF		.MOD (24)
PTF		Excess phase at $f = \frac{1}{2\pi \cdot TF}$		.MOD (25)
CJC	C_{JC}	Zero-bias B-C depletion region capacitance		.MOD (26)
VJC	ϕ_C	B–C built–in potential	.75	.MOD (27)
MJC	M_{JC}	B–C junction exponential factor	.33	.MOD (28)
XCJC	θ	Fraction of B–C depletion capacitance connected to internal base node	1	.MOD (29)
TR		Ideal reverse transit time		.MOD (30)
CJS	C_{JS}	Zero-bias collector–substrate capacitance		.MOD (31)
VJS	ϕ_S	Substrate junction built–in potential	.75	.MOD (32)
MJS	M_{JS}	Substrate junction exponential factor		.MOD (33)
XTB		Temperature exponent for BF and BR		.MOD (34)
EG		Activation energy for temperature dependence of IS	1.11ev	.MOD (35)
XTI		Saturation current temperature exponent	3	.MOD (36)
KF	K_F	Flicker noise coefficient		.MOD (37)
AF	A_F	Flicker noise exponent	1	.MOD (39)
FC		Forward bias capacitor transition coefficient	0.5	.MOD (40)
AREA	A_n	Emitter area ratio	1	DE

†.MOD (x) denotes the entry is via the .MODEL card (line) at the xth parameter location in Reference 1. DE notes entry from the device element card (line). Since the input parser in SPICE looks for each parameter by name, the ordering as denoted by the parameter x is arbitrary but was included for convenient reference to Reference 1.

AF denotes the flicker noise exponent. This input parameter, along with the parameter KF, is used to characterize the flicker noise in the C–E noise source as indicated by (4.4-18).

AREA (A_n) denotes the ratio of the emitter area of the BJT on the device input line to the emitter area of the BJT modeled in the referenced .MODEL line. A_n is thus a normalized area and is dimensionless.

BF is the ideal maximum forward beta. It is one of the key input parameters used to characterize the BJT and is approximately equal to the current gain from the base to collector. It appears in the characterizing equation (4.4-2) and in Fig. 4.4-3.

β_F is by definition the ratio of the total collector current to the total base current under forward BE bias as indicated by (4.4-9); it is not a SPICE input parameter. It is shown pictorially in Fig. 4.4-3. β_F is operating point dependent but nearly equal to BF for midrange V_{BE} values.

BR is the ideal maximum reverse beta. This SPICE input parameter is most useful for characterizing the BJT in the reverse active region. It appears in the characterizing equation (4.4-1) and the plot corresponding to that of Fig. 4.4-3 obtained by forward biasing the BC junction and reverse biasing the BE junction.

β_R is by definition the ratio of the total emitter current to the total base current under forward BC bias evaluated at the Q-point; it is not a SPICE input parameter. It is the reverse active equivalent of β_F.

C2 and **C4** are parameters which were used to denote ISE and ISC in some earlier versions of SPICE. They are still used for this purpose in some SPICE documentation.

CJC, CJE, and **CJS** (C_{JC}, C_{JE}, and C_{JS}) are the zero-bias depletion region capacitances of the base–collector, base–emitter and collector–substrate junctions. They are useful for characterizing the parasitic capacitances in vertical transistors. These SPICE input parameters appear in (4.4-12)–(4.4-15).

EG denotes the activation energy. It is used along with the parameter XTI to characterize the temperature dependence of the saturation current.[3] The temperature dependence of IS is characterized by the expression

$$\mathrm{IS}(T) = \mathrm{IS}(T_1) \cdot \left(\frac{T}{T_1}\right)^{\mathrm{XTI}} \exp\left[\left(\frac{q\mathrm{EG}}{kT}\right)\left(\frac{T}{T_1} - 1\right)\right] \tag{4C-1}$$

where T is temperature in degrees Kelvin, T_1 is any reference temperature, $\mathrm{IS}(T_1)$ is the saturation current at T_1, k is Boltzmann's constant, and q is the charge of an electron.

FC is the SPICE input parameter which denotes the forward bias coefficient in the parasitic junction capacitance (B–C, B–E, and C–S). All junction capacitors are assumed "reverse biased" and characterized by (4.4-12)–(4.4-15) for a forward bias less than or equal to FC $\cdot$ ϕ_X, for $X \in \{B, C, S\}$. For a forward bias greater than FC $\cdot$ ϕ_X the junction capacitors are assumed "forward biased" and are characterized by the continuous and differentiable linear extension of the reverse-bias region at the transition voltage.

IKR is the corner for the reverse beta high-current roll-off. This SPICE input parameter is a dual of the parameter IKF for the reverse active mode of operation.

IKF is the corner for the forward beta high-current roll-off. This SPICE input parameter appears in (4.4-3) and Fig. 4.4-3.

IRB is the current where the base resistance falls half way to its minimum value. The base resistance is assumed to be current dependent and is characterized by the three parameters RB, IRB, and RBM.

IS is the transport saturation current of the BJT. This SPICE input parameter is a key parameter in the dc model as indicated by (4.4-1) and (4.4-2).

ISC and **ISE** (I_{SE} and I_{SC}) represent the B–C and B–E leakage saturation currents. They appear in the dc model as indicated by (4.4-1) and (4.4-2).

ITF is a SPICE input parameter which characterizes the forward transit time at high current levels. The reader should consult the SPICE source code in subroutine BJT for details.

k is Boltzmann's constant. It is a physical constant equal to 1.381×10^{-23}J/°K.

KF is the flicker noise coefficient used to characterize noise in the collector–emitter noise source as indicated by (4.4-18).

MJC, MJE and **MJS** (M_{JC}, M_{JE} and M_{JS}) are the junction grading coefficients of the B–C, B–E, and C–S junctions, respectively. These SPICE input parameters appear as exponents in the voltage dependent depletion junction capacitances as indicated by (4.4-12)–(4.4-15).

NC, NE, NF, and **NR** are leakage emission coefficients and appear in the exponents of the dc characterizing equations, (4.4-1) and (4.4-2).

ϕ_C, ϕ_B, and ϕ_S (See VJC, VJE, and VJS.)

PTF is the excess phase at $f = \mathrm{TF}/(2\pi)$ and is used to characterize the actual transit time. It is used in determining the accumulated charge on parasitic capacitors. The interested reader should refer to subroutine BJT in the SPICE source code for the specific formulation.

q is the charge of an electron. It is a physical constant equal to 1.602×10^{-19} coulomb.

RB is the zero-bias base resistance. The actual zero-bias base resistance used in SPICE, R_b of Fig. 4.4–1, is a function of RB, RBM, and IRB. If IRB is not specified, R_b is calculated from the expression

$$R_b = \frac{\mathrm{RB}}{A_n Q_B} + \frac{\mathrm{RBM}}{A_n}\left(1 - \frac{1}{Q_B}\right) \tag{4C-2}$$

where Q_B is as defined in (4.4-8). If IRB is specified, the expression for R_b is quite unwieldy. For details, see subroutine BJT of the SPICE source code.

RBM is the minimum base resistance at high currents. The parameters RB, RBM, and IRB are used to characterize the base resistance.

RC and **RE** are the collector and emitter series resistances respectively. SPICE obtains the actual collector and emitter resistances by dividing these parameters by the area normalization factor, A_n.

θ (See XCJC.)

T is temperature in degrees Kelvin.

TF and **TR** are the forward and reverse transit times. These are key parameters in determining the accumulated charge parasitic capacitors. The reader should consult subroutine BJT in the SPICE source code for details.

VAF and **VAR** (V_{AF} and V_{AR}) are the forward and reverse Early voltages, respectively. These SPICE input parameters contribute considerably to the non-infinite output impedance at the collector of the BJT. The effects of the Early voltages on the dc *I-V* characteristics of the BJT are apparent from (4.4-1)–(4.4-3).

VJC, VJE, and **VJS** (ϕ_C, ϕ_B, ϕ_S) represent the built-in potential of the C–B, E–B, and C–S junctions. They are used to characterize the depletion region capacitances as indicated in (4.4-12)–(4.4-15).

V_t is an internal parameter calculated from the expression

$$V_t = \frac{kT}{q} \tag{4C-3}$$

The parameters k, T, and q have been previously defined.

VTF is a SPICE input parameter characterizing the B-C voltage dependence of the forward transit time. The interested reader should consult subroutine BJT in the SPICE source code for details.

XCJC is the fraction of the B–C depletion capacitance that is to be assigned to the internal base node. This SPICE input parameter appears as the parameter θ in equations (4.4-13) and (4.4-15).

XTB is the temperature exponent for both the forward and reverse beta as indicated by (4.4-22) and (4.4-23). XTB is a SPICE input parameter.

XTF is a SPICE input parameter which characterizes the bias dependence of TF. The reader should check subroutine BJT in the SPICE source code for details.

XTI denotes the saturation current temperature exponent. It is used along with EG to characterize the temperature dependence of IS as indicated by (4.4-19). XTI is a SPICE input parameter.