
CHAPTER 5

BASIC INTEGRATED CIRCUIT BUILDING BLOCKS

5.0 INTRODUCTION

This chapter introduces various integrated circuit building blocks, which form the first step in integrated circuit design. Figures 5.0-1 and 5.0-2 illustrate the circuit diagrams of a BJT op amp and a CMOS op amp. Although such circuits will not be covered until Chapter 6, they are useful in illustrating how the various building blocks are combined to form more complex circuits. There are two important observations to make concerning these two figures. The first is that circuit design is remarkably similar for different technologies. The architecture of both op amps is identical although the performance may not be identical. This fact will permit circuit design ideas developed in one technology to be applicable to a new technology. The second observation is that some components in each op amp perform more than one function. For example, Q3 (M3) serves as an active resistor load but also serves as part of a current mirror. This characteristic of circuits makes it difficult to distinguish the function of a component in a circuit.

In this chapter, some of the building blocks of Figs. 5.0-1 and 5.0-2 will be discussed. These blocks include switches (not shown on Figs. 5.0-1 or 5.0-2), active resistors, current sinks and sources, current mirrors, and voltage and current references. These blocks, along with passive resistors and capacitors, will form the lowest level of the design hierarchy. The next level of hierarchy takes the blocks of this chapter and implements more complex circuits such as amplifiers or comparators. Chapters 6 and 7 address analog and digital circuits, respectively, implemented from the building blocks of this chapter. Chapters 8 and 9 address

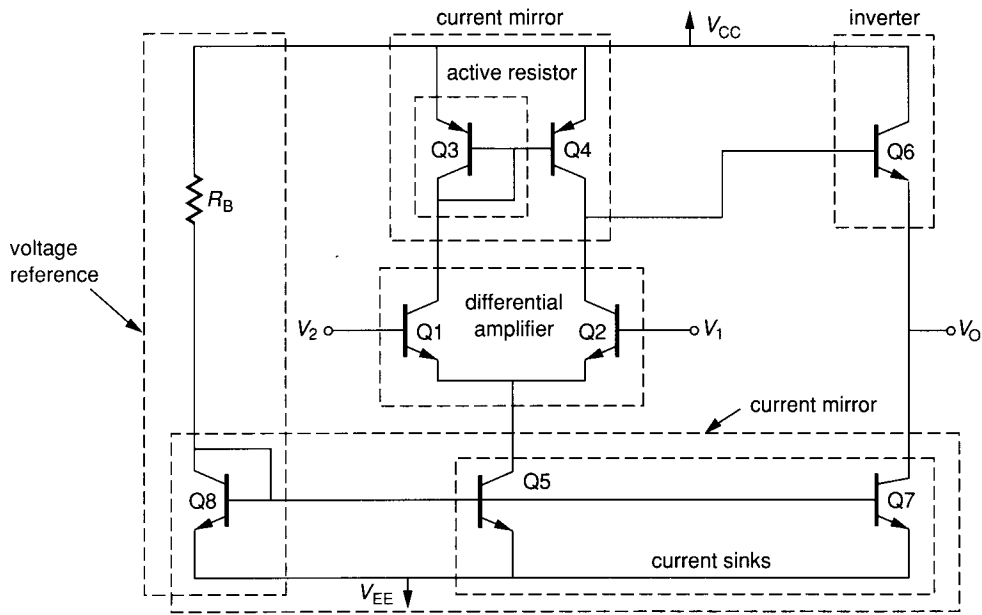


FIGURE 5.0-1 BJT op amp illustrating the various components.

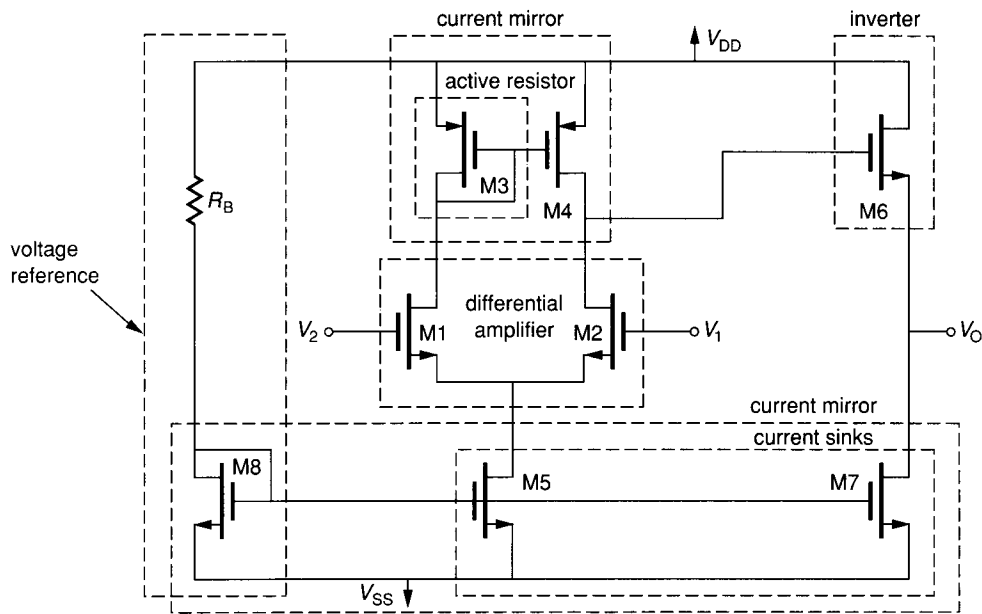


FIGURE 5.0-2 CMOS op amp illustrating the various components.

TABLE 5.0-1
Design hierarchy of Chapters 5 through 9

Design hierarchy	Analog design	Digital design
Systems	Chapter 8	Chapter 9
Basic circuits	Chapter 6	Chapter 7
Building blocks	Chapter 5	—

the use of these analog and digital circuits to perform analog and digital signal processing functions, respectively. The hierarchical relationships of this material are illustrated in Table 5.0-1.

Throughout this chapter, several key concepts are introduced. These concepts include both techniques and principles. How to use both positive and negative feedback in order to improve some aspect of the performance of the building blocks will be shown. The important principle of matched devices that is key to integrated circuit design will be presented and illustrated. Techniques such as how to make a mismatch analysis or how to attain the zero sensitivity of a circuit to some parameter will be described. These principles and techniques should be understood by the reader since they are invariant and applicable regardless of the technology. The summary will include a review of these important principles and techniques.

5.1 SWITCHES

Although the switch is not one of the components illustrated in Fig. 5.0-1 or Fig. 5.0-2, it will be considered first because of its simplicity and importance. The switch finds many applications in integrated circuit design. In analog circuits, the switch is used to implement such useful functions as the switched simulation of a resistor in Sec. 5.2. The switch is also useful for multiplexing, modulation, autozeroing and a number of other applications. The switch is used as a transmission gate in digital circuits and adds a dimension of flexibility not found in standard logic circuits. The objective of this section is to study the characteristics of switches that are compatible with integrated circuits.

Figure 5.1-1*a* illustrates a model of the ideal voltage-controlled switch. Terminals **A** and **B** represent the switch terminals, and terminal **C** is the controlling terminal. Ideally, the voltage at V_C has two states. In one state, the switch is open (off) and in the other state the switch is closed (on). In the on state, the ideal switch presents a short circuit between terminals **A** and **B**. In the off state, the ideal switch presents an open circuit between terminals **A** and **B**.

Unfortunately, practical switch implementations only approximate the model given in Fig. 5.1-1*a*. Figure 5.1-1*b* is a model of the switch that includes some of the more important nonideal characteristics. R_{ON} is a resistance that represents the small but finite resistance between terminals **A** and **B** when the switch is on. R_{OFF} represents the large but not infinite resistance between terminals **A** and **B** when the switch is off. In many applications it will be desirable to have R_{ON} as small as possible and R_{OFF} as large as possible.

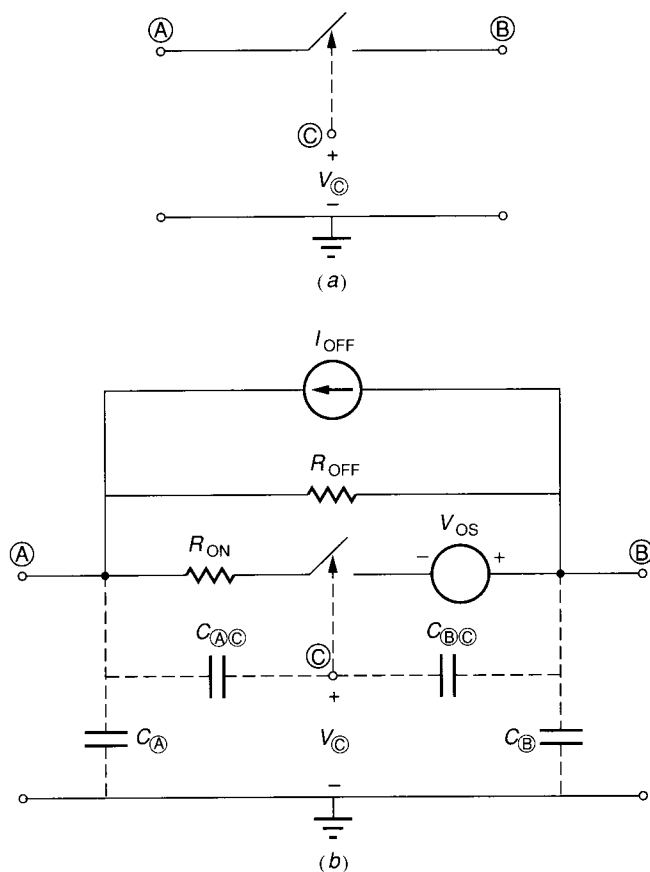


FIGURE 5.1-1
Models of the switch: (a) Ideal, (b) Nonideal.

Another practical characteristic of the switch is given by V_{OS} and I_{OFF} shown in Fig. 5.1-1b. The voltage that exists between terminals A and B when the switch is on but the current through it is zero is approximately the offset voltage and is modeled by an independent voltage source of V_{OS} . Similarly, the current that flows between terminals A and B when the switch is off but the voltage across the switch terminals is zero is approximately the offset current and is modeled by an independent current source of I_{OFF} . The polarities of the offset current and voltage are not known and have arbitrarily been assigned in Fig. 5.1-1b.

Figure 5.1-1b also shows some of the parasitic capacitances that exist between the various switch terminals and to ground. C_{AC} and C_{BC} will be particularly important when considering the influence of the controlling voltage on the switch performance. There are many other nonideal characteristics of the switch such as linearity, commutation time, noise, etc. that are not modeled by Fig. 5.1-1b.

The graphical characterization of a switch shown in Fig. 5.1-2 is useful in determining how well the switch can be implemented by a bipolar or MOS

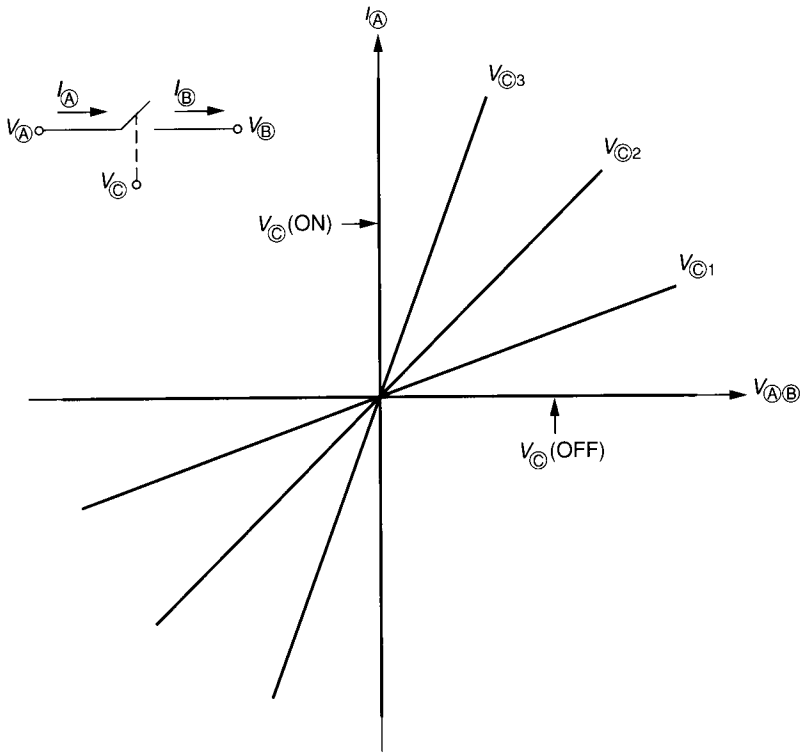


FIGURE 5.1-2
Graphical characteristics of a controlled switch.

transistor. $V_{A\oplus B} = V_A - V_B$ is the voltage across the switch, and I_A is the current into the terminal **A** and I_B the current out of terminal **B** of the switch. When $V_C = V_C(\text{ON})$, ideally $V_{A\oplus B} = 0$ and $I_A(I_B)$ can have any value. In the on state, the ideal switch is a short circuit. When $V_C = V_C(\text{OFF})$, $I_A = I_B = 0$ and $V_{A\oplus B}$ can have any value and is identical to an open circuit. V_{C1} , V_{C2} , and V_{C3} are values of V_C that cause the switch to be between its on and off states. Normally $V_{C(\text{OFF})} < V_{C1} < V_{C2} < V_{C3} < V_C(\text{ON})$.

Now consider the bipolar transistor as an implementation of the switch as shown in Fig. 5.1-3a, where $V_{A\oplus B} = V_{CE}$, $I_A = I_C$, and $V_C = V_B$. The right-hand side of these equalities refers to the transistor, whereas the left-hand side refers to the switch in Fig. 5.1-1 or 5.1-2. Typical BJT characteristics are shown in Fig. 5.1-3b with $V_B = 0 (V_E = 0)$. Several shortcomings of the BJT switch realization are immediately apparent in Fig. 5.1-3b. The first is that the origin of the characteristics for $I_A = 0$ is not zero. Thus V_{OS} of Fig. 5.1-1 is approximately 16 mV. The second is the nonlinearity of the various curves for a constant V_C . This would severely limit the dynamic range of the switch. Lastly, the switch characteristics are not symmetrical in the first and third quadrants. Another problem, which is not apparent from Fig. 5.1-3b, is that the BJT requires

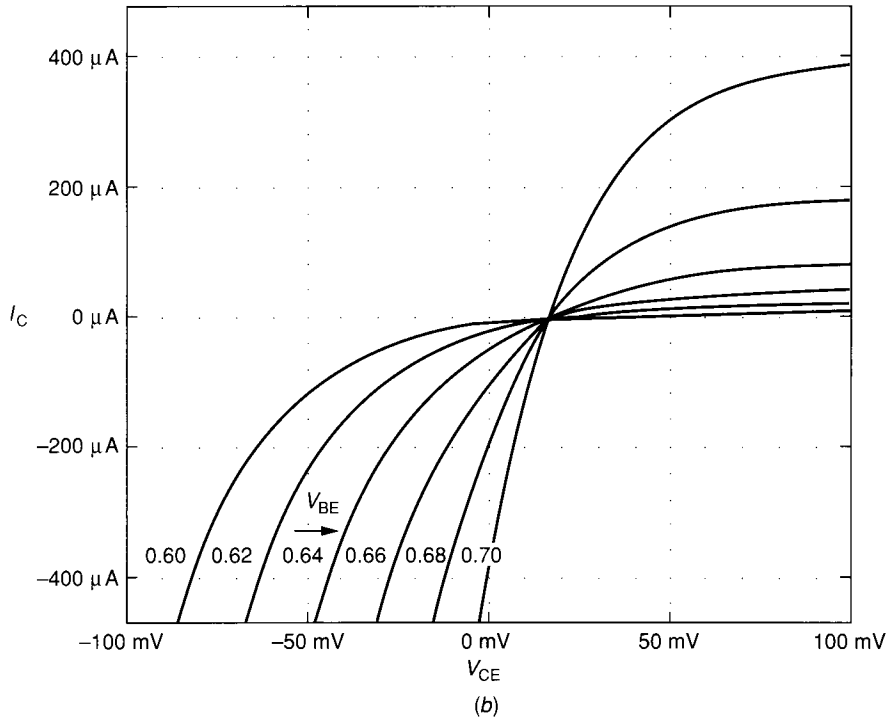
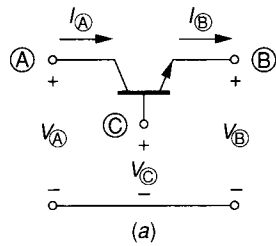


FIGURE 5.1-3
 (a) Bipolar transistor as a switch, (b) Graphical characteristics of a where $V_{A\oplus B} = V_{CE}$, $I_A = I_C$, and $V_C = V_B$. Note that $V_E = 0$.

a small current flowing in the controlling terminal, causing the current flowing in terminal A to be different from that flowing out of terminal B.

Figure 5.1-4b shows the graphical characteristics of the MOS transistor of Fig. 5.1-4a, where $V_{A\oplus B} = V_{DS}$, $I_A = I_D$, and $V_C = V_G$. Again, the right-hand side of these inequalities refers to the MOS transistor while the left-hand side refers to the switch in Fig. 5.1-1 or 5.1-2. Comparison of Figs. 5.1-2, 5.1-3b, and 5.1-4b strongly suggests that the MOS transistor is a much better switch realization.

Figure 5.1-5 shows a MOS transistor that will be used as a switch. It will be important to consider the influence of the bulk voltage on the switch operation. The performance of this realization can be determined by comparing

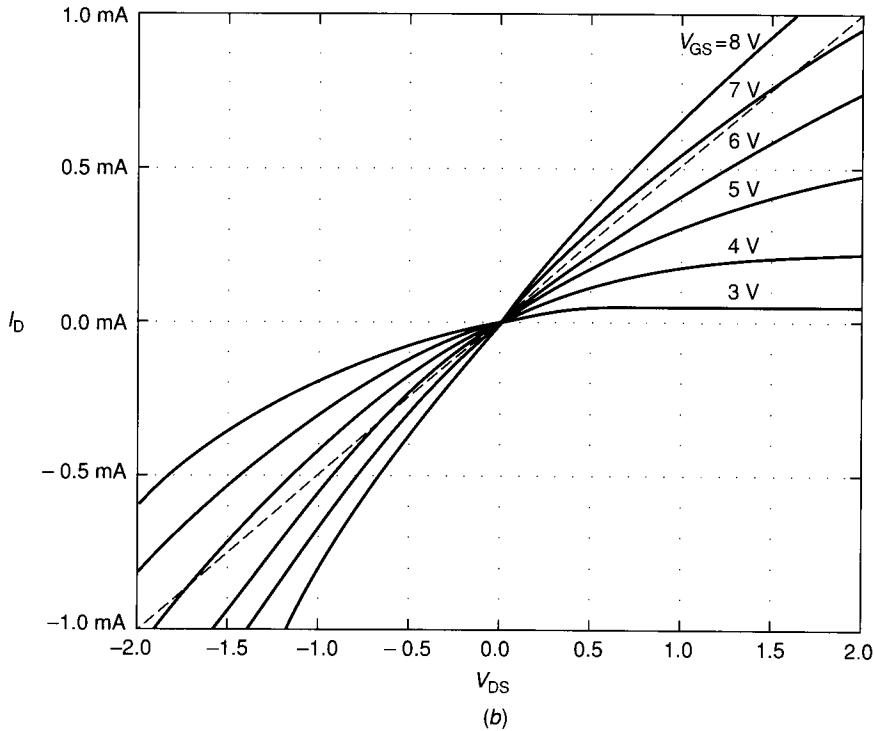
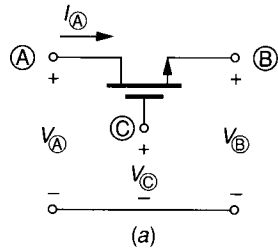


FIGURE 5.1-4

(a) MOS transistor as a switch, (b) Graphical characteristics of a where $V_{\text{A}\text{B}} = V_{\text{DS}}$, $I_{\text{A}} = I_{\text{D}}$, and $V_{\text{C}} = V_{\text{G}}$. Note that $V_{\text{S}} = 0$.

Fig. 5.1-1b with the large signal model for the MOS transistor. We see that terminals A or B can either be the drain or source of the MOS transistor. The on resistance is seen to consist of the series combination of R_{D} , R_{S} , and whatever channel resistance exists. An expression for the on channel resistance can be found as follows. In the on state of the switch, the voltage across the switch should be small, and V_{GS} should be large. Therefore, the MOS device is assumed to be in the ohmic region. Furthermore, let us assume that the channel length modulation effects can be ignored. From Sec. 3.1, the drain current is given by

$$I_{\text{D}} = \frac{K'W}{2L} [2(V_{\text{GS}} - V_{\text{T}})V_{\text{DS}} - V_{\text{DS}}^2] \quad (5.1-1)$$

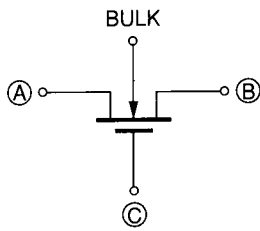


FIGURE 5.1-5
MOS transistor used as a switch.

if V_{DS} is less than $V_{GS} - V_T$ but greater than zero. (V_{GS} becomes V_{GD} if V_{DS} is negative.) Assuming that there is no offset voltage, the large signal channel resistance when $V_{GS} > V_T$ is

$$R_{ON} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{(K'W/L)(V_{GS} - V_T - V_{DS})} \quad (5.1-2)$$

Figure 5.1-6 illustrates Eq. 5.1-2 for very small values of V_{DS} . When $V_{GS} < V_T$ and $V_{DS} = 0$, R_{ON} is infinite. For large V_{DS} , the curves of Fig. 5.1-6 will start to decrease in slope (see Fig. 3.1-2) for increasing V_{DS} . A plot of R_{ON} as a function of V_{GS}/V_T is shown in Fig. 5.1-7 for small V_{DS} using the parameters indicated for various values of W/L . A lower value of R_{ON} is achieved for larger values of W/L .

When the switch is off, V_{GS} is less than or equal to V_T and the transistor is always in the cutoff region. R_{OFF} is ideally infinite. A typical value is in the range of $10^{12} \Omega$. Because of this large value, the leakage current from drain and source to substrate is a more important parameter than R_{OFF} . This leakage current is a combination of the subthreshold current, the surface leakage current, and the package leakage current. Typically this leakage current is in the 10 pA range at room temperature and doubles for every 10°C increase. The resistances

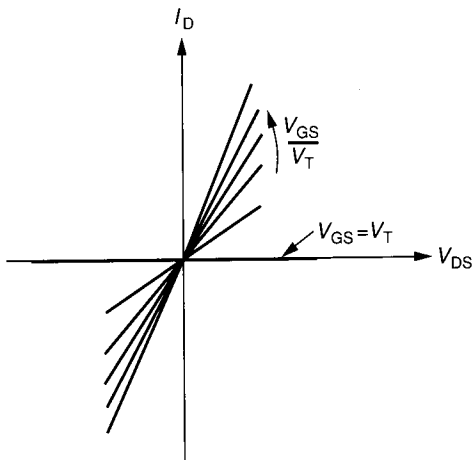


FIGURE 5.1-6
Illustration of the on state of a switch. V_{GS}/V_T is increasing in equal increments.

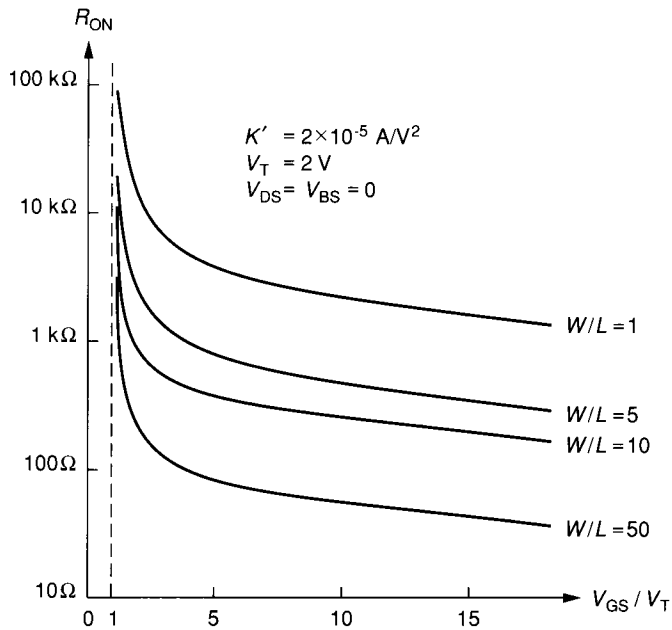


FIGURE 5.1-7
Illustration of the R_{ON} characteristics of an MOS transistor with W/L as a parameter.

representing this leakage current are called R_{A} and R_{B} and are connected from A and B to ground in Fig. 5.1-1 and are on the order of $10^{10} \Omega$. Unfortunately, R_{A} and R_{B} prevent the designer from achieving R_{OFF} of $10^{12} \Omega$.

The offset voltage of the MOS device is zero and does not influence the switch performance. The capacitors C_{A} , C_{B} , C_{AC} , and C_{BC} of Fig. 5.1-1b correspond directly to the capacitors C_{BD} , C_{BS} , C_{GD} , and C_{GS} of the MOS transistor of Fig. 5.1-4a. The maximum commutation rate of the MOS switch is determined primarily by the capacitors of Fig. 5.1-1b and the external resistances. Commutation rates for CMOS switches of 20 MHz are typical depending upon the load capacitance.

One important aspect of the switch is the range of voltages on the switch terminals compared to the control voltage. In the n-channel MOS transistor we see that the gate voltage must be considerably larger than either the drain or source voltage to insure that the MOS transistor is on. Typically the bulk is taken to the most negative potential for the n-channel MOS switch. The problem can be illustrated as follows. Suppose that the on voltage of the gate is the positive power supply V_{DD} . With the bulk connected to ground this should keep the MOS switch on until the signal on the switch terminals (which should be approximately identical at the source and drain) approaches $V_{\text{DD}} - V_T$. As the signal approaches $V_{\text{DD}} - V_T$, the switch begins to turn off. This often introduces an undesired nonlinear distortion in the transmission of analog signals. Typical voltages used for an n-channel MOS switch are shown in Fig. 5.1-8, where the switch is connected between two circuits and the power supplies are $\pm 5 \text{ V}$.

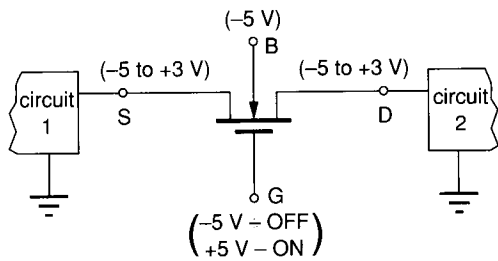


FIGURE 5.1-8
Application of an n-channel MOS transistor as a switch with typical terminal voltages indicated.

To illustrate the influence of the switches on the circuit, consider the use of a switch to charge an integrated capacitor, as shown in Fig. 5.1-9. M1 is a MOS transistor used as a switch, and ϕ_1 is called the clock. The on resistance of the switches can become important during the charge transfer phase of this circuit. For example, when ϕ_1 goes high, M1 connects C_1 to the voltage source V_{in} . The equivalent circuit at this time is shown in Fig. 5.1-10. It is seen that C_1 will charge to V_{in} with the time constant of $R_{ON}C_1$. For successful operation $R_{ON}C_1 \ll T$, where T is the time ϕ_1 is high. The value of R_{ON} is not constant during the charging of C_1 because the value of V_{GS} decreases as the capacitor charges. The assumption that R_{ON} is constant avoids the solution of nonlinear differential equations necessary for the exact solution.

The maximum acceptable value of R_{ON} will determine required values for W and L of M1. Typical values of C_1 are less than 20 pF because the area required to implement larger capacitors would be too large to be practical. If the time ϕ_1 is high is $T = 10 \mu s$ and $C_1 = 20$ pF, then R_{ON} must be less than 0.5 M Ω . Since small capacitors are used, switches with a large R_{ON} can still perform satisfactorily. As a result, the MOS devices used for switching typically use minimum geometries. For a clock of 10 V, the MOS device of Fig. 5.1-7 with $W = L$ and $V_{in} = 5$ V gives R_{ON} of approximately 6 k Ω , which is sufficiently small to transfer the charge in the desired time. The minimum size switches will also help to reduce parasitic capacitances.

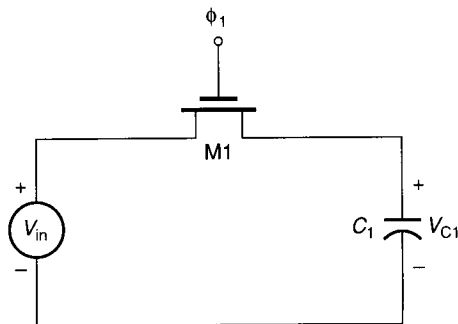


FIGURE 5.1-9
An application of a MOS switch.

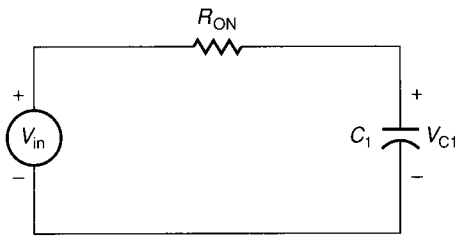


FIGURE 5.1-10
Model for the on state of the switch in Fig. 5.1-9.

The off state of the switch has little influence upon the performance of the circuit in Fig. 5.1-9 except for the leakage current. Figure 5.1-11 shows two cases where the leakage current can create serious problems. Figure 5.1-11a is a sample-and-hold circuit. If C_H is not large enough, then in the hold mode, where the MOS switch is off, the leakage current can charge or discharge C_H by a significant amount. Figure 5.1-11b shows an integrator. The leakage current can cause the circuit to integrate in a continuous mode, which can lead to large values of dc offset unless there is an external feedback path from V_{OUT} back to the inverting input of the operational amplifier. This feedback must contain resistors and may go through other dc circuits before returning to the input. If the

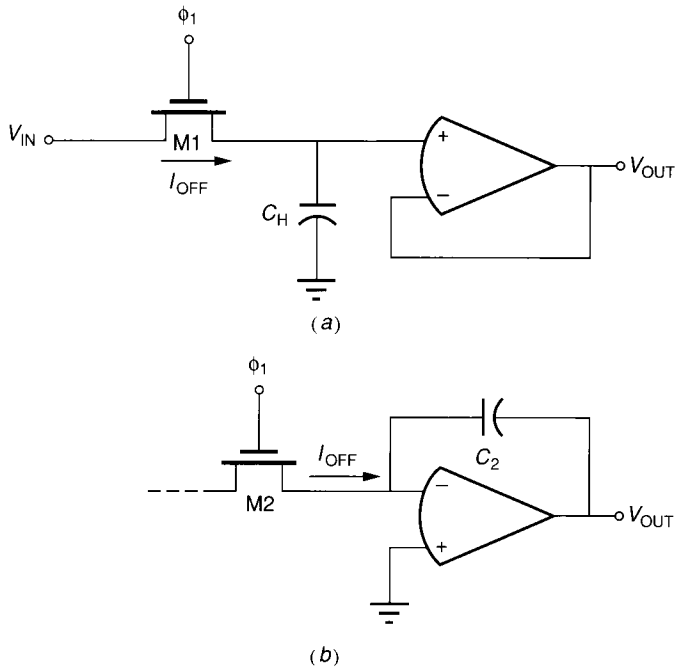


FIGURE 5.1-11
Examples of the influence of I_{OFF} : (a) Sample-and-hold circuit, (b) Integrator. Switch is off in both cases.

gate voltage of an MOS switch is equal to or less than the lowest source/drain potential, I_{OFF} is negligible.

One of the most serious limitations of switches is the clock feedthrough that can occur between the switch control signal and the switch terminals. This coupling occurs through the parasitic capacitors of the switch, namely C_{AC} and C_{BC} of Fig. 5.1-1*b*. Figure 5.1-12 shows the parasitic capacitances associated with the MOS switch of Fig. 5.1-9. Since the clock (gate) signal must make very large transitions, this signal can easily couple to the source and drain through C_{GS} or C_{GD} , respectively. The effects of clock feedthrough can be observed in Fig. 5.1-13 by following the sequence of events occurring when ϕ_1 is high. Assume that C_{GS} and C_{GD} are 2 fF, $C_1 = 1$ pF, $V_{in} = 5$ V and V_{C1} is initially zero. The clock waveform is shown in Fig. 5.1-13 and has finite rise and fall times for purposes of explanation. Following the convention that the lowest potential determines the source of an MOS transistor, the source will be the side connected to the capacitor. During the time t_0 to t_1 the switch is off and the clock feeds through C_{GD} and C_{GS} . The feedthrough via C_{GD} has no effect because of the voltage source V_{in} . However, the feedthrough via C_{GS} will change the voltage across C_1 . Assuming the switch turns on at t_1 and connects C_1 to V_{in} , any further feedthrough has no effect, again because the voltage source V_{in} is connected to C_1 . The problem occurs when the switch turns off. From t_3 to t_4 the switch is still on so that any feedthrough is unimportant. However, from t_4 to t_5 the switch is off, and feedthrough occurs from the clock to C_1 . As a result, the voltage across V_{C1} is decreased below V_{in} by an amount ΔV_{C1} , given as

$$\Delta V_{C1} = \left(\frac{C_{GS}}{C_1 + C_{GS}} \right) (V_{in} + V_T) \approx 0.002 V_{in} \quad (5.1-3)$$

If V_{in} is 5 V, then a feedthrough of -10 mV to C_1 occurs during the ϕ_1 phase period. This feedthrough results in an offset, which can be a very serious problem. Furthermore, the offset is dependent upon the signal level, which will cause a non-linear offset. In general, the feedthrough will be dependent upon the switch configuration, the size of the switch, and the size of the capacitors in the circuit.

The situation concerning feedthrough is often not as bad as implied. For example, once C_1 has been charged to V_{in} (minus ΔV_{C1}) it will typically be

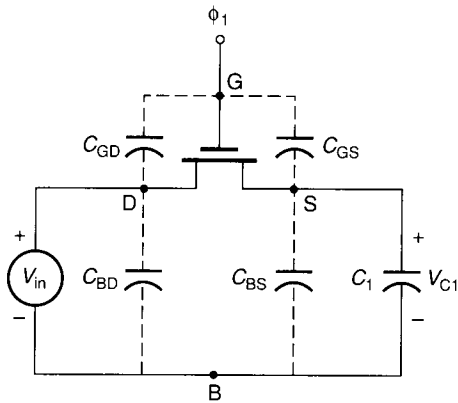


FIGURE 5.1-12
Illustration of the parasitics associated with the switch of Fig. 5.1-9.

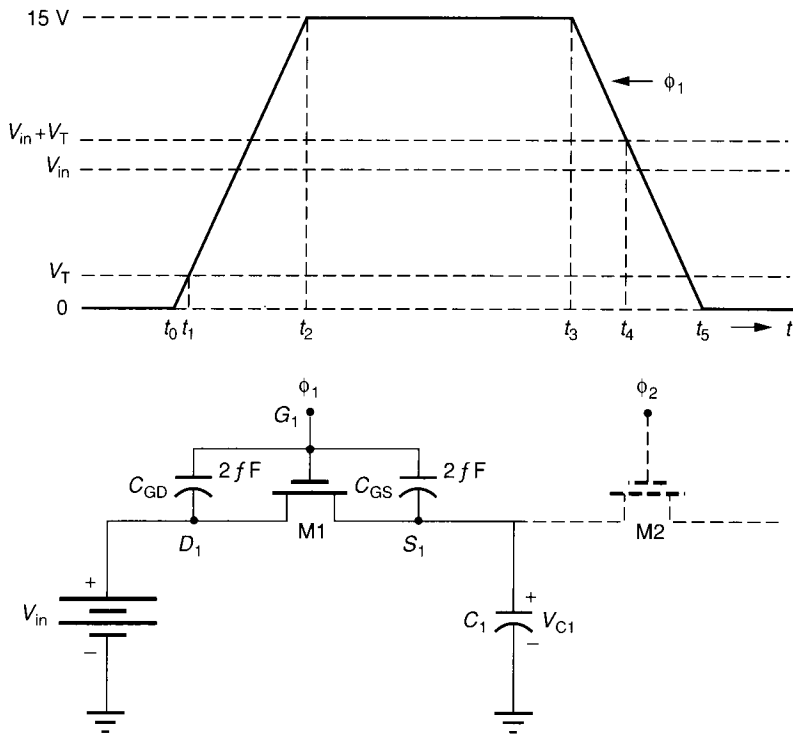


FIGURE 5.1-13
Illustration of switch feedthrough and the ϕ_1 waveform.

connected by some other switch (M2 in Fig. 5.1-13) to some other circuit. As M2 turns from off to on, there will be a positive feedthrough from ϕ_2 on to C_1 via the parasitic capacitance of M2. If the source of M2 is the terminal connected to C_1 , then the net feedthrough should approximately cancel if M1 and M2 are identical. The problem is that the potential of the right-hand side of M2 is usually ground, making that side the drain and causing the positive feedthrough to be

$$\Delta V_{C1}(\text{due to M2}) = \left(\frac{C_{GD}}{C_{GD} + C_1} \right) V_T \quad (5.1-4)$$

which is less than that of Eq. 5.1-3 if $V_{in} \neq 0$.

It is possible to partially cancel some of the feedthrough effects using the technique illustrated in Fig. 5.1-14. Here a dummy MOS transistor, MD, with source and drain both attached to the signal line and the gate attached to the

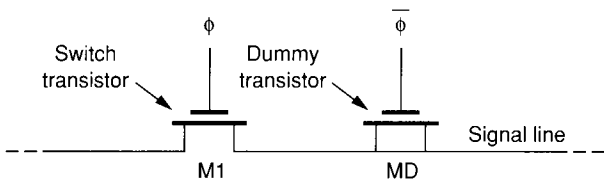


FIGURE 5.1-14
The use of a dummy transistor to cancel clock feedthrough.

inverse clock, is used to apply an opposing clock feedthrough due to M1. The area of MD can be designed to provide minimum clock feedthrough. Unfortunately, this method never completely removes the feedthrough, and in some cases may worsen it. Also, it is necessary to generate an inverted clock, which is applied to the dummy switch. In some cases, the dummy switch is a transistor with the gate attached to the source of M1, and the source and drain of the dummy switch connected to the inverse clock. This avoids charge pumping of the substrate, which can defeat the purpose of the dummy switch. Clock feedthrough can be reduced by using the largest circuit capacitors possible, using minimum geometry switches, and keeping the clock swings as small as possible. Typically, these solutions will create problems in other areas, requiring a compromise to be made.

Some of the problems associated with single-channel MOS switches can be avoided with the CMOS switch shown in Fig. 5.1-15. Using CMOS technology, a switch is usually constructed by paralleling p-channel and n-channel enhancement transistors; therefore, when ϕ is low ($\bar{\phi}$ is high) both transistors are off, creating an effective open circuit. When ϕ is high ($\bar{\phi}$ is low) both transistors are on, giving a low-impedance state. The on resistance of the CMOS switch can be lower than $1\text{ k}\Omega$ while the off leakage current is in the 1 pA range. The bulk potentials of the p-channel (V_{BP}) and the n-channel devices (V_{BN}) are taken to the highest and lowest potentials, respectively. It is also possible to apply the clocks to the bulks of the MOS devices to improve their switching characteristics.

The CMOS switch has two advantages over the single-channel MOS switch. The first advantage is that the dynamic analog signal range in the on state is greatly increased. The second is that since the n-channel and p-channel devices are in parallel and require opposing clock signals, the feedthrough due to the clock will be diminished through cancellation.

The increased signal amplitude of the analog signal can be seen to be a direct result of using complementary devices. When one of the transistors is being turned off because of a large analog signal on the drain and source, this large analog signal will be causing the other transistor to be fully on. As a consequence, both transistors of Fig. 5.1-15 are on for analog signal amplitudes less than the clock

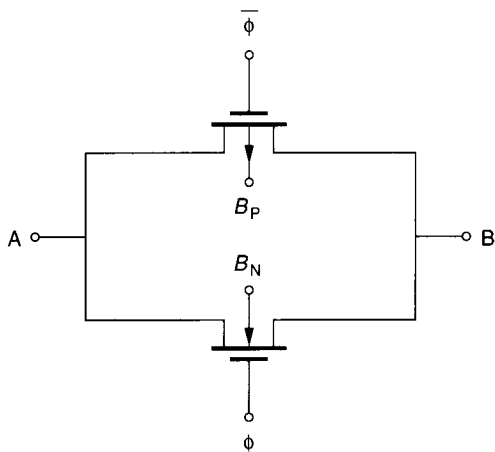


FIGURE 5.1-15
A CMOS switch.

magnitude, and at least one of the transistors is on for analog signal amplitudes equal to the magnitude of the clock signal.

The feedthrough cancellation of the CMOS switch in Fig. 5.1-15 is not complete for two reasons. One is that the feedthrough capacitances of the n-channel device are not necessarily equal to the feedthrough capacitances of the p-channel device. The second reason is that the turn-on delay of each type of transistor is not equal, and so the channel conductances do not necessarily track each other during turn-on and turn-off.

CMOS switches are generally used in place of single-channel switches when the technology permits. Although the CMOS switches have larger parasitics than single-channel switches, these parasitics can be minimized through the use of circuit techniques that will be illustrated in Chapter 8. The clock circuitry for CMOS switches is more complex because of the requirement for a complementary clock. The configuration of Fig. 5.1-15 is often called a transmission gate.

One must be careful in using switches where the power supply voltages are small. If $|V_{DD} - V_{SS}|$ is less than 5 V, it will become necessary to use a CMOS technology with twin wells so that the bulk potentials can be switched as shown in Fig. 5.1-16 in order to achieve low values of on resistance. It is

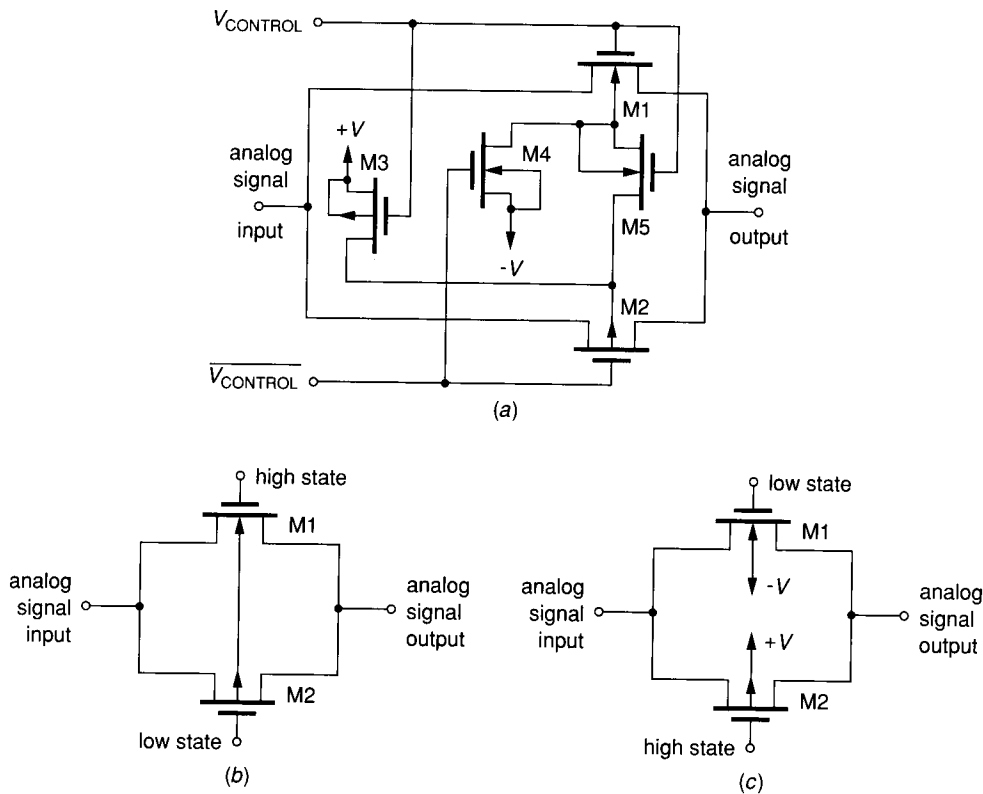


FIGURE 5.1-16
A twin-well CMOS switch with control circuitry: (a) Circuit, (b) On state, (c) Off state.

assumed that V_{CONTROL} and $\overline{V_{\text{CONTROL}}}$ are generated from the clock waveform. When V_{CONTROL} is high, the transmission gate is on. The equivalent circuit in this condition is shown in Fig. 5.1-16b. Here we see that the n-channel gate is taken to the high state and the p-channel gate is in the low state. Also the substrates have been connected together by means of the switches M3, M4, and M5. M3 and M4 are off while M5 is on. This helps to keep the switch on resistance from being a function of the analog signal potential. When V_{CONTROL} is low, the transmission gate is off and has the equivalent circuit shown in Fig. 5.1-16c. The bulks of the n- and p-channel device terminals have been taken to $-V$ and $+V$, respectively, since M3 and M4 are on and M5 is off. This insures that the off state will be maintained since V_{BS} is strongly reverse-biased and causes a large V_{T} .

If $|V_{\text{DD}} - V_{\text{SS}}|$ is less than 4 V, switches can only be used if a clock signal of 5 V or higher can be obtained. One can either apply external clocks or use a voltage doubler to provide an on-chip voltage which is higher than $|V_{\text{DD}} - V_{\text{SS}}|$.

In this section we have seen that the MOS transistor makes a good switch realization for integrated circuits. They require small area, dissipate very little power, and provide reasonable values of R_{ON} and R_{OFF} for most applications. This section has also illustrated the importance of the terminal voltages on the behavior of the MOS transistor. The incorporation of a good realization of a switch into the basic building blocks will produce some interesting and useful circuits and systems which will be studied in the following material.

5.2 ACTIVE RESISTORS

In Chapters 2 and 3, the implementation of a resistance and a capacitance by IC technologies was discussed. The passive components including resistors and capacitors are very important in analog signal processing. Typically the gain of an amplifier is determined by ratios of resistors or capacitors while the time constant of a filter is determined by the product of resistors and capacitors. Thus, the performance of many analog systems can be directly related to their resistive and capacitive passive components.

The capacitor can be implemented as a parallel plate configuration of a conductor-insulator-conductor sandwich. The MOS capacitance uses the thin oxide of the MOS process as the insulator while the conductors (plates) can be metal, polysilicon, or a heavily doped semiconductor. The conductor-insulator-conductor capacitor was found to be a near ideal component, having only the problems of size and parasitics. For reasonable area usage the value of the conductor-insulator-conductor capacitor is limited to the 10–20 pF range. Fortunately, in many applications the influence of the parasitics can be eliminated. Another possible implementation of the capacitor is the pn junction capacitance. This capacitance exhibits a strong voltage dependence, which limits its usefulness.

Compared to capacitors, the resistors implemented by IC technologies were found to be lacking in several areas of performance. The typical sheet resistance was sufficiently small that large values of resistors required large areas. The higher value of resistance attained with pinched resistors suffered nonlinearity. In

addition, the tolerance of the resistors, their temperature coefficient, and their voltage coefficient were all poorer than those of the capacitor. Of course, modifications to the standard IC technology can result in better resistor implementation. However, the objective of this section is to investigate ways of emulating a resistor without having the inherent disadvantages using standard IC technologies.

We shall discuss two ways of implementing resistors that have found use in integrated circuit design. The first method is to use active devices, such as those introduced in Sec. 3.4, and the second method is to use switched capacitors. The first method has the advantage of minimizing the area required for resistors, and the second has the advantage of a resistor whose accuracy is dependent upon the frequency of a clock and a capacitor. It will be shown that the RC time constant accuracy of circuits using a switched capacitor resistor simulation is equivalent to the relative accuracy of the capacitor, which is quite good.

There are two distinct applications of resistors that are important. These applications are dc resistors and ac resistors. The dc resistor is typically used to provide a dc voltage drop given a dc current. The ac resistor provides an ac voltage drop given an ac current. Figure 5.2-1 illustrates the difference, although in many cases the resistor is used simultaneously as both an ac and dc resistor. As a dc resistor, Fig. 5.2-1 shows that a dc voltage drop of V_Q is produced for a dc current of I_Q . As an ac resistor, Fig. 5.2-1 shows that an ac voltage of ΔV_Q is produced for an ac current of ΔI_Q . The use of an active element to implement a dc resistor will be considered first.

Ignoring the substrate terminal for the moment, the MOS and BJT transistors are three-terminal devices. Through proper connection of these three terminals,

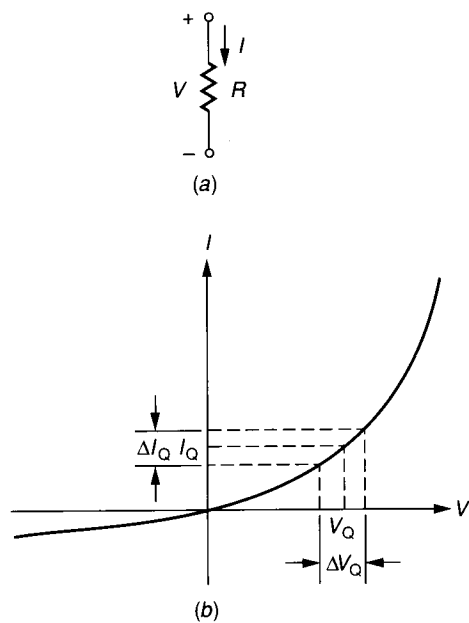


FIGURE 5.2-1

The distinction between a dc and an ac resistor. (a) Resistor, (b) I - V characteristics.

the active device becomes a two-terminal resistor called an *active resistor*. The active resistor can be used in place of a polysilicon or diffused resistor to produce a dc voltage drop and/or provide a small signal resistance that is linear over a small range. There are many cases where the area required to obtain a small signal resistance is more important than the linearity. A small MOS or BJT device can simulate a resistor in much less area than is required with an equivalent polysilicon or diffused resistor.

The active resistor can be implemented by simply connecting the gate of an n- or p-channel enhancement MOS device to the drain, as shown in Fig. 5.2-2a and b. For the n-channel device, the source should be placed at the most negative power supply voltage, V_{SS} , if possible, to eliminate the bulk effect. The source of the p-channel device should be taken to the most positive voltage for the same reason. Since V_{GS} is now equal to V_{DS} , the transconductance curve (I_D vs. V_{GS}) of the MOS transistor shown in Fig. 5.2-2c characterizes the large signal behavior of the active resistor. This curve is valid for both the n- and p-channel enhancement transistors for the polarities shown. It is seen that the resistance is not linear, which was anticipated. In many circumstances, the signal swing is very small, and in these cases the active resistor works very well. Since the connection of the gate to the drain guarantees operation in the saturation region for $V > V_T$, the I - V characteristics can be written as

$$I = I_D = \frac{K'W}{2L} [(V_{GS} - V_T)^2] \tag{5.2-1}$$

or

$$V = V_{GS} = V_{DS} = V_T + \left(\frac{2I_D L}{K'W} \right)^{1/2} \tag{5.2-2}$$

where

$$K' = \mu_0 C_{ox} \tag{5.2-3}$$

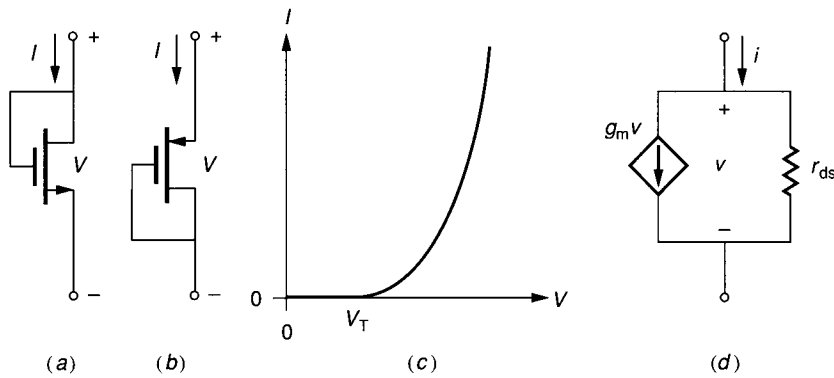


FIGURE 5.2-2 (a) n-channel enhancement active resistor, (b) p-channel enhancement active resistor, (c) Voltage-current characteristics of the MOS active resistor, (d) Small signal model of a or b.

If either V or I is defined, then the other variable can be found by using Eq. 5.2-1 or Eq. 5.2-2.

Connecting the gate to the drain means that V_{DS} controls I_D , and therefore the channel transconductance becomes a channel conductance. The small signal conductance can be found by differentiating Eq. 5.2-1 with respect to V , resulting in

$$g = \frac{\partial I}{\partial V} \cong \left(\frac{2IK'W}{L} \right)^{1/2} = \frac{K'W}{L}(V - V_T) \quad (5.2-4)$$

Another method of finding the small signal conductance is to use the small signal model of the MOS transistor of Fig. 3.1-14. The small signal model of the active resistor valid for either the n- or the p-channel active resistor is shown in Fig. 5.2-2d where $r_{ds} = 1/g_{ds}$. Assuming $v_{bs} = 0$, it is easily seen that the small signal conductance of these circuits is

$$g = \frac{1 + g_m r_{ds}}{r_{ds}} \cong g_m \quad (5.2-5)$$

where $g_m r_{ds}$ is greater than unity. The influence of an ac bulk voltage can be incorporated into Eq. 5.2-5 using the same model (see Prob. 5.8). In either case, we note how the value of g depends upon the dc values of V and I (refer back to Table 3.1-3 in Chapter 3 for the dependence of g_m and r_{ds} upon V and I).

The bipolar junction transistor can be used to form an active resistor in the same manner as for the MOS transistor. The circuit of Fig. 5.2-3 is topologically identical to the MOS circuit of Fig. 5.2-2. When operating in the forward active region, it follows from Eq. 3.3-10 that the I - V characteristics of the BJT active resistor can be expressed as

$$I \cong I_S \exp(V/V_T) \quad (5.2-6)$$

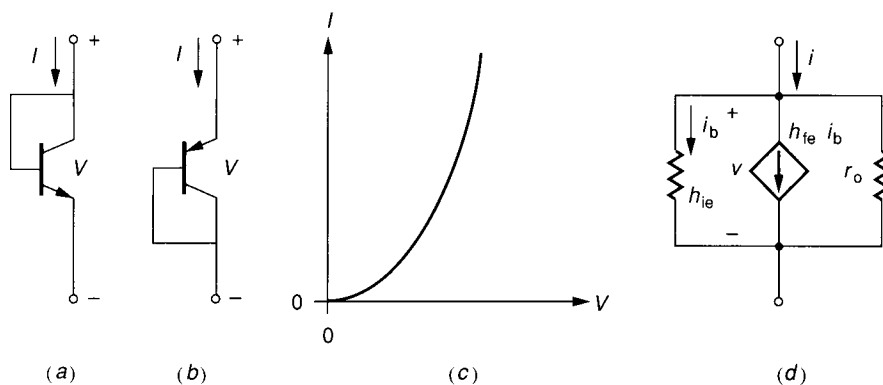


FIGURE 5.2-3

(a) npn BJT active resistor, (b) pnp BJT active resistor, (c) Voltage-current characteristics of the BJT active resistor, (d) Small signal model for the BJT active resistor.

or

$$V = V_t \ln \left[\frac{I}{I_s} \right] \tag{5.2-7}$$

where

I_s = reverse saturation current of the emitter base junction
 $V_t = (kT)/q = 0.026$ V at room temperature

The small signal conductance of the BJT active resistor can be found by differentiating Eq. 5.2-6 with respect to $V (= V_{BE})$ to get

$$g = \frac{\partial I}{\partial V} = \frac{|I|}{V_t} \tag{5.2-8}$$

The small signal model of Fig. 5.2-3d, derived from Fig. 3.3-8, can also be used to more accurately calculate the small signal conductance and gives

$$g = h_{oe} + \frac{1 + h_{fe}}{h_{ie}} \tag{5.2-9}$$

These small signal model parameters have been defined in Table 3.3-4 of Chapter 3. The dependence of g upon the dc values of the BJT active resistor are indicated by Table 3.3-4.

Active resistors can be used to produce a dc voltage or to provide a small signal resistance. An example illustrating the application of the active resistor to provide a dc voltage follows.

Example 5.2-1. Voltage division using active resistors. Figure 5.2-4 shows the use of an n-channel MOS active resistor and a p-channel MOS active resistor to provide a dc voltage, V_{out} . Find a W/L ratio for M1 and M2 that give V_{out} of 1 V if $V_{DD} = 5$ V, $V_{SS} = -5$ V and $I = 50 \mu\text{A}$. Assume that $V_{TN} = +0.75$ V, $V_{TP} = -0.75$ V, $K'_N = 2.4 \times 10^{-5}$ A/V² and $K'_P = 0.8 \times 10^{-5}$ A/V².

Solutions. Both bulks are connected to their respective sources so that the body effect has no influence. Also since $V_{DG} = 0$, both transistors are saturated. Since the currents through both transistors must be the same and V_{DS1} and V_{DS2} are defined, we can solve for the W/L ratios of M1 and M2 using Eq. 5.2-1 as 0.15 and 1.18, respectively.

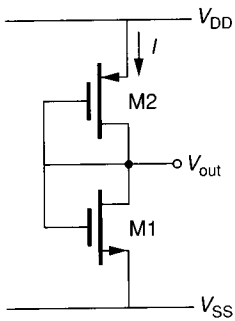


FIGURE 5.2-4 Use of active resistors to achieve voltage division.

BJT active resistors can be used to divide voltages in the same manner as illustrated in the example; however, the voltages across the BJT are limited to less than 1 V.

The use of active resistors to develop large dc voltages requires large currents or W/L ratios that are much less than unity. This can be circumvented by cascading devices as shown in Fig. 5.2-5. The voltages V_1 , V_2 and V_3 are given by Eq. 5.2-2, where I is from a known current source. If the voltages are specified, then the W/L ratio of each device can be determined from Eq. 5.2-2 if the bulk-source voltage is taken into consideration. If the W/L ratios are given, then the voltages V_1 through V_3 can be calculated starting with V_1 . Using more than one device to drop the voltage will result in W/L ratios closer to unity and smaller dc currents.

Example 5.2-2. Replacement of one active resistor by two. An n-channel MOS active resistor is used to produce a dc voltage drop of 5 V from a 25 μA current. Assuming that the bulk-source effects can be neglected, (a) find the W/L ratio of a single active resistor, and (b) find the W/L ratio of two identical n-channel active resistors in series replacing the single active resistor of (a). Assume that the MOS parameters of Example 5.2-1 are valid in this example. Compare the gate area required for both cases.

Solution. For case (a) we get $W/L = 1/8.7$. If we assume that W has a unit length, then the gate area required is 8.7 square units. For case (b) we find that the W/L of one of the transistors is $1/1.47$. If $W = 1$, then $L = 1.47$ with a gate area of 1.47, two identical active resistors would require 2.94 square units. A savings in gate area of almost 3 to 1 results in case (b) compared to case (a). The source and drain area would reduce this ratio.

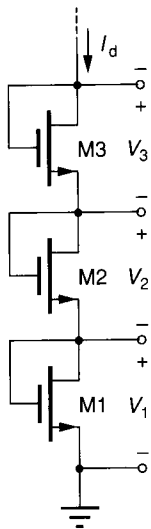


FIGURE 5.2-5

Use of cascaded devices to create large voltage drops.

The second application of a resistor is to provide an ac voltage (or current) for a given ac current (or voltage). In this presentation, the dc current will be zero. For a zero dc current, the active resistors of Figs. 5.2-2 and 5.2-3 are not satisfactory because the value of resistance approaches infinity. The switches of Figs. 5.1-3 and 5.1-4 make a much better realization of an ac resistor with the MOS switch being nearly linear and having no dc offset. By controlling the value of voltage between the gate and source, one can get a linear ac resistance for values ΔV up to 1 V.

Example 5.2-3. A MOS switch as an ac resistor. Assume that the circuit of Fig. 5.1-4a is to be used to implement an ac resistor of 2000Ω and that the device parameters are $V_T = 0.75 \text{ V}$, $K'_N = 24 \mu\text{A}/\text{V}^2$, $\gamma_N = 0.8 \text{ V}^{1/2}$, $\lambda = 0.01 \text{ V}^{-1}$, and $\phi = 0.6 \text{ V}$. If $W = 50 \mu$, $L = 10 \mu$, $V_{DS} = 0$, and $V_{BS} = -5 \text{ V}$, find the value of $V_{GS} (= V_C)$.

Solution. The threshold voltage due to $V_{BS} = -5 \text{ V}$ is 2.023 V . Equating 2000Ω to Eq. 5.1-2 of Sec. 5.1 gives a value of $V_{GS} = 6.19 \text{ V}$. The dotted line in Fig. 5.1-4b corresponds to a resistance of 2000Ω . Figure 5.1-4b shows that the 2000Ω resistor is closely approximated by this value of V_{GS} .

The linearity of the ac resistor in the example is limited for negative values of V_{DS} by the effects of V_{BS} and for positive values of V_{DS} by V_{DS} itself. The bulk influences the linearity by causing V_T to change. The drain-source voltage influences the linearity by leaving the ohmic region and entering the saturation region. Techniques for eliminating both of these effects will now be considered.

Figure 5.2-6 shows how to eliminate the influence of V_{DS} upon the ac resistor realization.¹ The principle employed is to use two identical devices biased

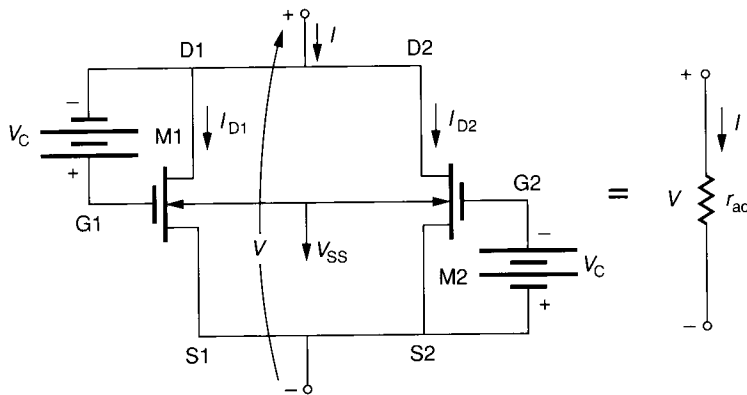


FIGURE 5.2-6 Configuration to eliminate the effects of V_{DS} in the ac resistor implementation of Figure 5.1-4a.

so that the influences of V_{DS} cancel. Using Eq. 3 of Table 3.1-1 to obtain expressions for I_{D1} and I_{D2} gives

$$\begin{aligned} I_{D1} &= K'_N \left(\frac{W_1}{L_1} \right) \left[(V_{GS1} - V_{T1}) V_{DS1} - \frac{V_{DS1}^2}{2} \right] \\ &= K'_N \left(\frac{W_1}{L_1} \right) \left[(V_{DS1} + V_C - V_{T1}) V_{DS1} - \frac{V_{DS1}^2}{2} \right] \\ &= K'_N \left(\frac{W_1}{L_1} \right) \left[\frac{V_{DS1}^2}{2} + (V_C - V_{T1}) V_{DS1} \right] \end{aligned} \quad (5.2-10)$$

and

$$\begin{aligned} I_{D2} &= K'_N \left(\frac{W_2}{L_2} \right) \left[(V_{GS2} - V_{T2}) V_{DS2} - \frac{V_{DS2}^2}{2} \right] \\ &= K'_N \left(\frac{W_2}{L_2} \right) \left[(V_C - V_{T2}) V_{DS2} - \frac{V_{DS2}^2}{2} \right] \end{aligned} \quad (5.2-11)$$

Noting that $V_{DS1} = V_{DS2} = V$ and assuming matched transistors allows the current I to be expressed as

$$I = I_{D1} + I_{D2} = \frac{2K'_N W}{L} (V_C - V_T) V_{DS} \quad (5.2-12)$$

Thus the value of ac resistance found by differentiating Eq. 5.2-12 with respect to I is

$$r_{ac} = \frac{\partial V_{DS}}{\partial I} = \frac{1}{2K'_N (W/L) (V_C - V_T)} \quad (5.2-13)$$

In the development of Eq. 5.2-13, it has been assumed that the transistors remain in the ohmic region or that V_{DS} is less than $V_{GS} - V_T$. This assumption places the following constraint on the value of V for Eq. 5.2-13 to be valid.

$$V < (V_C - V_T) \quad (5.2-14)$$

Therefore, a larger value of V_C will lead to a larger range of V . While the linearity range has been increased, the dependence upon V_{BS} through V_T is still present and must be eliminated to achieve a wide linearity range.

In many applications, resistors are used differentially in pairs. In these cases it is possible to achieve an increase in linearity and to eventually even cancel the bulk effects. A method of canceling the effects of V_{DS} will be discussed first. Figure 5.2-7a shows a pair of ac resistors used in a differential configuration.² Note that a differential signal (V_1) is applied to the left-hand side of the resistors

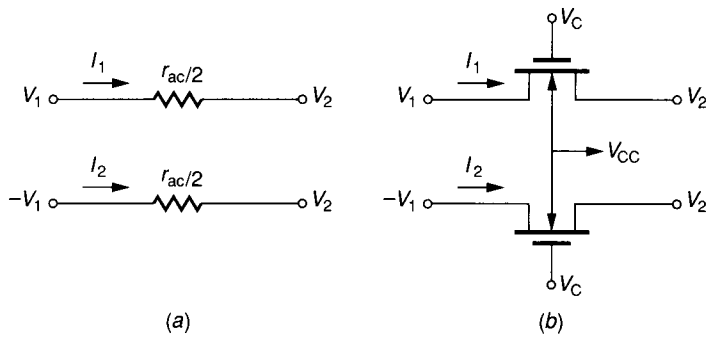


FIGURE 5.2-7
 (a) Differential ac resistor configuration, (b) Single-MOS implementation of *a*.

while the right-hand side is at the same potential (although not physically connected). Again Eq. 3 of Table 3.1-1 can be used to write

$$I_1 = \frac{K'_N W}{L} \left[(V_C - V_2 - V_T)(V_1 - V_2) - \frac{1}{2}(V_1 - V_2)^2 \right] \quad (5.2-15)$$

and

$$-I_2 = \frac{K'_N W}{L} \left[(V_C + V_1 - V_T)(V_2 + V_1) - \frac{1}{2}(V_2 + V_1)^2 \right] \quad (5.2-16)$$

Adding Eqs. 5.2-15 and 5.2-16 gives

$$I_1 - I_2 = \frac{K'_N W}{L} (V_C - V_T) 2V_1 \quad (5.2-17)$$

Defining r_{ac} as

$$r_{ac} = \frac{2V_1}{I_1 - I_2} \quad (5.2-18)$$

gives

$$r_{ac} = \frac{1}{(K'_N W/L)(V_C - V_T)} \quad (5.2-19)$$

Therefore, Fig. 5.2-7*a* simulates a resistor r_{ac} which is independent of V_1 or V_2 as long as

$$|V_1 - V_2| = V < V_C - V_T \quad (5.2-20)$$

Figures 5.2-8*a* and *b* show the I - V characteristics of the resistors of Figs. 5.2-6 and 5.2-7*b* using n-channel transistors having $W = 50 \mu$, $L = 10 \mu$ and model parameters of $V_T = 0.75$ V, $K'_N = 24 \mu\text{A}/\text{V}^2$, $\gamma_N = 0.8 \text{ V}^{1/2}$, $\lambda_N = 0.01 \text{ V}^{-1}$, and $\phi_N = 0.6$ V. The characteristics of Fig. 5.2-8*a* and *b* are almost identical and considerably more linear than Fig. 5.1-4*b*. For large values of V_C , the linearity range increases, as predicted by Eq. 5.2-20.

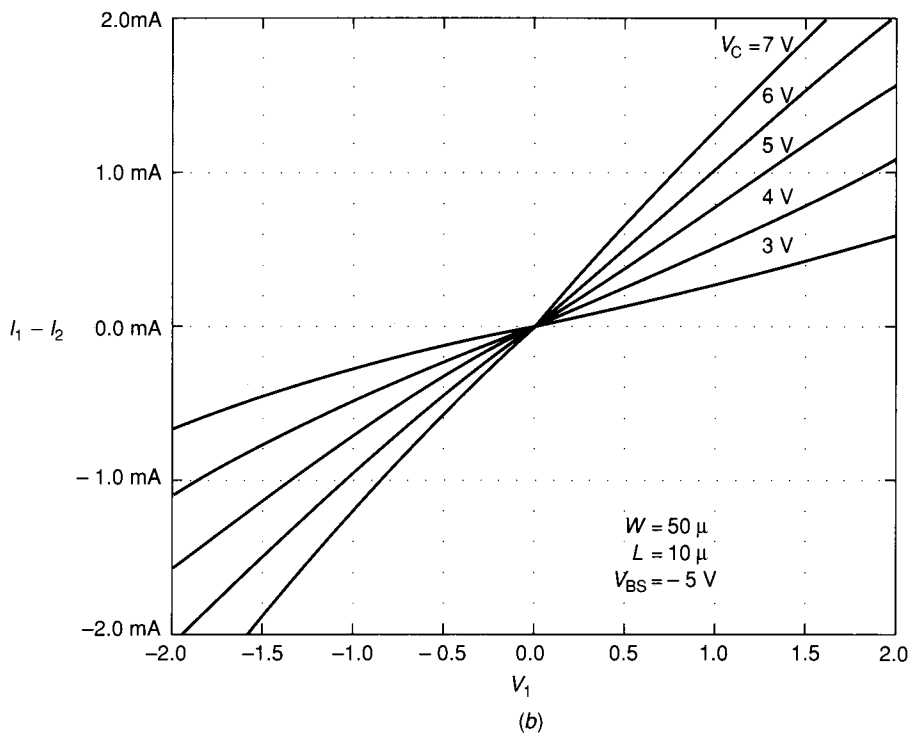
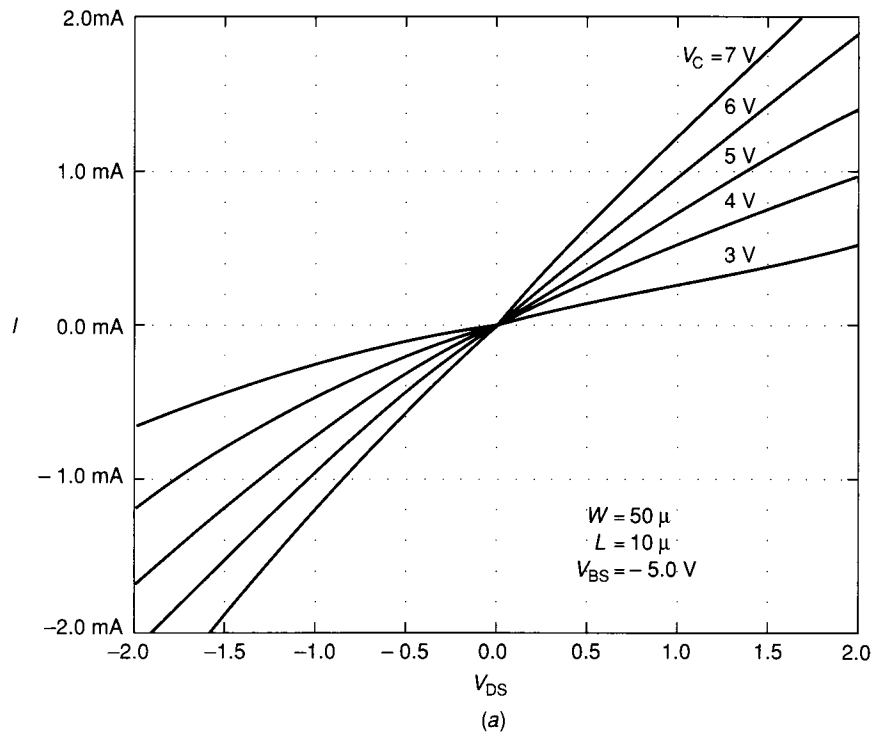


FIGURE 5.2-8
 I - V characteristics of: (a) Parallel MOS resistor, (b) A single-MOS differential resistor. (Note that the actual voltage across Fig. 5.2-7 is $2V_1$.)

A double-MOS, differential configuration, shown in Fig. 5.2-9a, not only linearizes the ac resistor but removes the influence of the bulk-source voltage.² The relationship for the ac resistance can be obtained by assuming all of the devices are matched and in the ohmic region. Using Eq. 3 of Table 3.1-1 to solve for I_1 and I_2 results in the following.

$$I_1 = I_{D1} + I_{D3} = \frac{K'_N W}{L} \left[(V_{C1} - V_3 - V_T)(V_1 - V_3) - \frac{1}{2}(V_1 - V_3)^2 \right] + \frac{K'_N W}{L} \left[(V_{C2} - V_3 - V_T)(V_2 - V_3) - \frac{1}{2}(V_2 - V_3)^2 \right] \tag{5.2-21}$$

and

$$I_2 = I_{D2} + I_{D4} = \frac{K'_N W}{L} \left[(V_{C2} - V_3 - V_T)(V_1 - V_3) - \frac{1}{2}(V_1 - V_3)^2 \right] + \frac{K'_N W}{L} \left[(V_{C1} - V_3 - V_T)(V_2 - V_3) - \frac{1}{2}(V_2 - V_3)^2 \right] \tag{5.2-22}$$

Using Eqs. 5.2-21 and 5.2-22 to find $I_1 - I_2$ gives

$$I_1 - I_2 = \frac{K'_N W}{L} (V_{C1} - V_{C2})(V_1 - V_2) \tag{5.2-23}$$

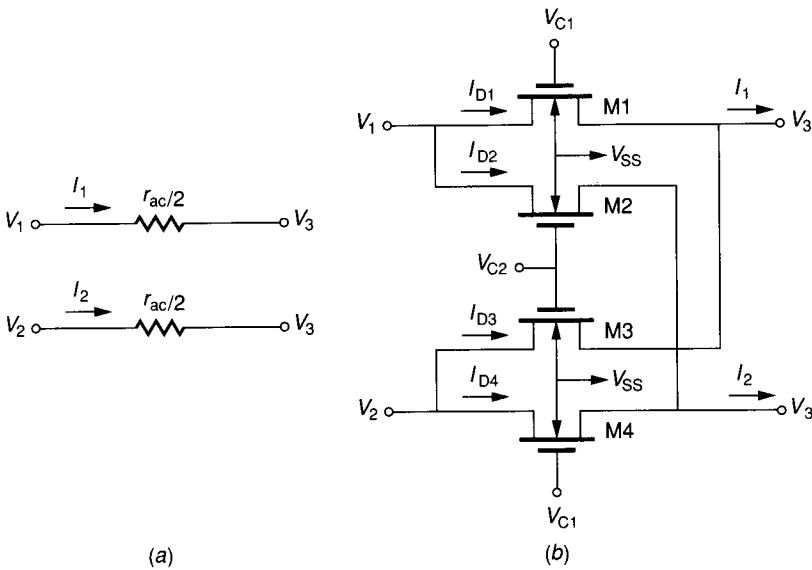


FIGURE 5.2-9 (a) Differential ac resistor configuration, (b) Double-MOS implementation of a.

r_{ac} can be found as

$$r_{ac} = \frac{V_1 - V_2}{I_1 - I_2} = \frac{1}{(K'_N W/L)(V_{C1} - V_{C2})} \quad (5.2-24)$$

Because all devices have been assumed to be in the ohmic region, Eq. 5.2-24 only holds when

$$V_1, V_2 \leq \min [V_{C1} - V_T, V_{C2} - V_T] \quad (5.2-25)$$

Figure 5.2-10 is a simulation of Fig. 5.2-9b when $V_{C1} = 7$ V, $V_3 = 0$, $V_{BS} = -5$ V and using the same device parameters as have been used for Figs. 5.1-4 and 5.2-7. It is of interest to compare the ac resistor realizations of Figs. 5.1-4, 5.2-6, 5.2-7b and 5.2-9b. Of all the realizations, the double-MOSFET differential resistor of Fig. 5.2-9b is superior in linearity. However, the double-MOSFET differential resistor is really a transresistance in that the voltages and currents are at different terminals. This restricts the double-MOSFET differential resistance to transresistance applications that are found in differential-in, differential-out op amps. The parallel MOS resistor of Fig. 5.2-6 and the single-MOSFET differential resistor of Fig. 5.2-7b are true resistor realizations that have approximately the same linearity. However, the parallel MOS resistor is a true floating resistor realization while the single MOSFET differential resistor must have a differential signal with reference

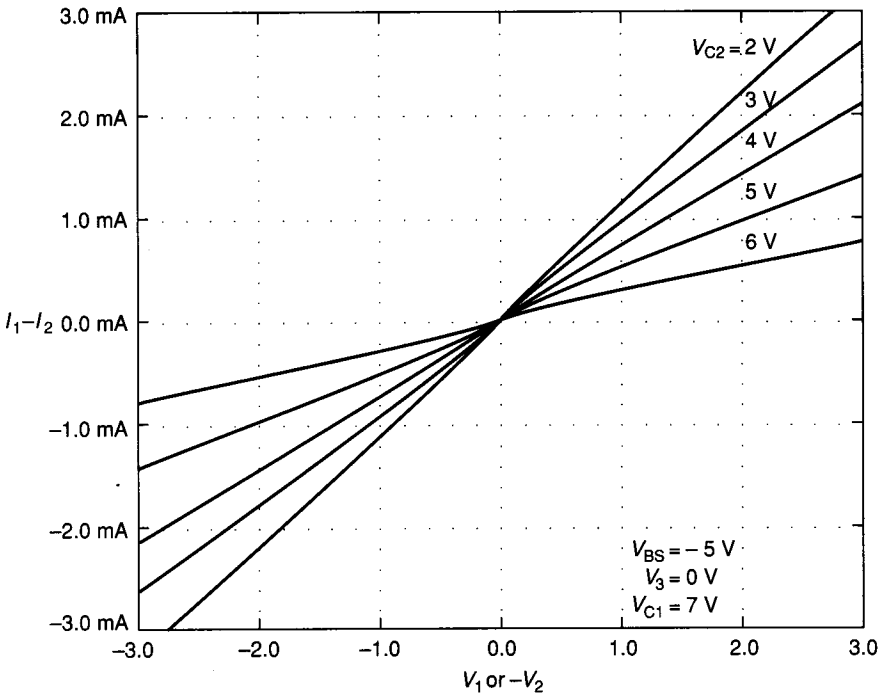


FIGURE 5.2-10
 I - V characteristics of a double-MOS differential resistor.

to V_2 of Fig. 5.2-7b. The performances of the ac resistor realizations that have been presented are summarized in Table 5.2-1.

A second approach to realizing ac resistors uses switches and capacitors. This approach is *discrete-time* and is often called the *switched capacitor* (SC) realization. If the clock rate is high enough, combinations of switches and capacitors can implement a resistor that is dependent only on the clock frequency and the capacitor. Four combinations of switches and capacitors will be considered.

The first approach to resistor simulation is called the parallel switched capacitor realization and is shown in Fig. 5.2-11a. It will be shown that under certain conditions, namely those found in a sampled data system, that the switched capacitor of Fig. 5.2-11a is an approximate realization of the resistor of Fig. 5.2-11b. Figure 5.2-11c shows the clock waveforms that control the opening and closing of the switches in Fig. 5.2-11a. Let us assume that V_1 and V_2 are two independent dc voltage sources. This assumption represents no loss of generality since the conditions for a sampled data system state that the "signals," V_1 and V_2 , are sampled at a rate that is sufficiently high that any change in V_1 or V_2 during a sampling period can be ignored.

Under steady state conditions, we can express the charge flow in the direction of I_1 over a time period from t_0 to $t_0 + T$ as

$$q_1(t_0 + T) = \int_{t_0}^{t_0+T} I_1(t) dt \tag{5.2-26}$$

However, this charge flow in the direction of I_1 during the time period from t_0 to $t_0 + T$ can be broken into two parts. The first part is the charge flowing from t_0 to $T/2$ and is given as

$$q_1\left(t_0 + \frac{T}{2}\right) = C \left[V_1\left(t_0 + \frac{T}{2}\right) - V_2(t_0) \right] \approx C(V_1 - V_2) \tag{5.2-27}$$

TABLE 5.2-1
Summary of R_{ac} realization characteristics

AC resistance realization	Figure	Linearity	How controlled	Restrictions
Single MOSFET	5.1-4	Poor	Gate voltage W/L	$V_{BULK} < \min(V_S, V_D)$
Parallel MOSFET	5.2-6	Good	V_C W/L	$V < V_C - V_T$ $V_{BULK} < \min(V_S, V_D)$
Single-MOSFET differential resistor	5.2-7a	Good	V_C W/L	$ V_1 - V_2 < V_C - V_T$ $V_{BULK} < -V_1$ Differential around V_2
Double-MOSFET differential resistor	5.2-9a	Good	$(V_{C1} - V_{C2})$ W/L	$V_1, V_2 < \min(V_{C1} - V_T, V_{C2} - V_T)$ $V_{BULK} < \min(V_1, V_2)$ Transresistance only

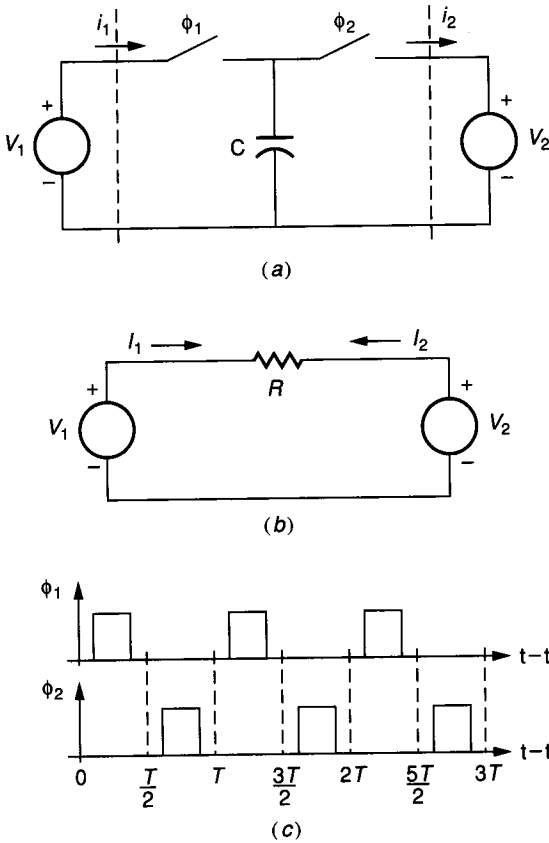


FIGURE 5.2-11
 (a) Parallel switched capacitor resistor realization, (b) A continuous resistor, (c) Clock waveforms for the switches of *a*.

The second part is the charge flowing from $T/2$ to T and is given as

$$q_1(t_0 + T) - q_1\left(t_0 + \frac{T}{2}\right) = 0$$

Therefore, Eq. 5.2-26 can be written as,

$$q_1(t_0 + T) = C(V_1 - V_2) = \int_{t_0}^{t_0+T} I_1(t) dt \quad (5.2-28)$$

Dividing both sides of Eq. 5.2-28 by T results in

$$\frac{C(V_1 - V_2)}{T} = \frac{1}{T} \int_{t_0}^{t_0+T} I_1(t) dt = I_1(\text{aver}) \quad (5.2-29)$$

Now let us find the average current, $I_1(\text{aver})$, flowing into the left-hand side of the continuous resistor of Fig. 5.2-11*b*. This value is given as

$$I_1(\text{aver}) = I_1 = \frac{V_1 - V_2}{R} \quad (5.2-30)$$

Equating Eqs. 5.2-29 and 5.2-30 results in

$$R = \frac{T}{C} = \frac{1}{Cf_{\text{clock}}} \quad (5.2-31)$$

where $f_{\text{clock}} = 1/T$ is the frequency of the clock signals ϕ_1 and ϕ_2 .

Therefore, we have shown that the switched capacitor circuit of Fig. 5.2-11a simulates the continuous resistor of Fig. 5.2-11b. We see that the switched capacitor resistor realization is dependent upon the capacitor C and the period or the frequency of the clock. The following example illustrates that very large resistors can be realized with a small amount of silicon area using switched capacitors.

Example 5.2-4. Switched capacitor resistor realization. If a $1 \text{ M}\Omega$ resistor is to be realized using the SC technique of Fig. 5.2-11 with a clock frequency of 100 kHz find the value of the capacitor and its area assuming that the capacitor is a polysilicon-to-polysilicon type. Compare this area to that required for a polysilicon resistor of the same value.

Solution. Equation 5.2-31 shows that the capacitance is 10 pF . Assuming a capacitance per unit area of 0.2 pF/mil^2 gives an area of 50 mils^2 . Using a polysilicon resistor with a sheet resistivity of $25 \text{ }\Omega/\text{square}$ requires an area of 3600 mils^2 using a minimum width of 0.3 mils . In addition to the capacitor area, the switched capacitor resistor realization requires two minimum-size MOS devices as the switches.

There are several other types of switched capacitor realizations of resistors. Figure 5.2-12 shows a realization called a series switched capacitor resistor, which results in a resistance given by Eq. 5.2-31. Figure 5.2-13 illustrates a series-parallel switched capacitor realization. It can be shown (see Prob. 5.15) that the equivalent resistance of the series-parallel switched capacitor resistor realization is

$$R = \frac{T}{C_1 + C_2} = \frac{1}{(C_1 + C_2)f_{\text{clock}}} \quad (5.2-32)$$

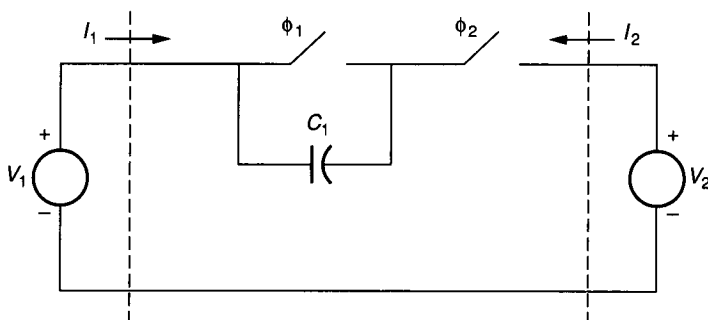


FIGURE 5.2-12
Series switched capacitor realization of a continuous resistor.

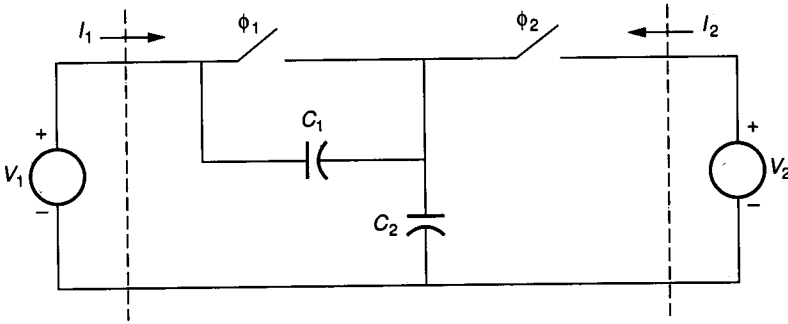


FIGURE 5.2-13
Series-parallel switched capacitor realization of a continuous resistance.

Figure 5.2-14 shows a switched capacitor resistor realization called the bilinear realization. The equivalent resistance of the bilinear switched capacitor resistance realization is (see Prob. 5.16)

$$R = \frac{T}{4C} = \frac{1}{4Cf_{\text{clock}}} \tag{5.2-33}$$

Table 5.2-2 summarizes the four switched capacitor resistor realizations discussed here.

This section has focused on the realization of dc and ac resistors using methods compatible with the standard IC technologies. It is discovered the MOS technology offers many more opportunities in this area. The reader will see all of these resistor realizations used along with other components in the following material. The most important concepts presented are the methods by which the dependence of drain current on the drain–source and bulk–source voltages can be reduced and the method by which resistors can be simulated by switches

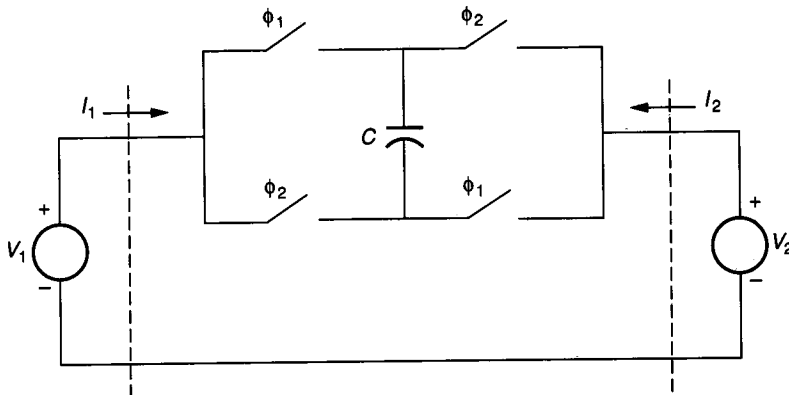


FIGURE 5.2-14
Bilinear switched capacitor realization of a continuous resistance.

TABLE 5.2-2
Summary of switched capacitor resistance realizations

SC resistor realization	Figure	Equivalent resistance	Type of resistance
Parallel	5.2-11a	T/C	Transresistance
Series	5.2-12	T/C	Resistance or transresistance
Series-parallel	5.2-13	$\frac{T}{C_1 + C_2}$	Transresistance
Bilinear	5.2-14	$\frac{T}{4C}$	Transresistance or resistance

and capacitors. Because the resistors realized by switched capacitor circuits are inversely proportional to capacitance, the effective RC time constants become proportional to capacitor ratios. The result is that time constants can be accurately realized using capacitors and switched capacitor resistor realizations.

5.3 CURRENT SOURCES AND SINKS

In this section we consider the realization of current sinks and sources that use standard bipolar or MOS devices. An ideal *current source* is a two-terminal element whose current is constant for any voltage across the source. The voltage across a current source depends upon the external circuitry. Figures 5.3-1a and b give the schematic symbol and the $I-V$ characteristics of a current source whose value is I_o . Most current source applications require one of their terminals to be common with the most positive or the most negative dc voltage in the circuit. This leads to the two possible configurations illustrated in Fig. 5.3-2. V_P and V_N are the most positive and most negative dc voltages, respectively. The configuration of Fig. 5.3-2a will be referred to as a *current sink*. The configuration of Fig. 5.3-2b will be called a *current source* even though we have used this notation for the general current source of Fig. 5.3-1. These two categories will become important in the practical considerations of implementing current sources/sinks. A third category is the *floating current source*, where neither terminal is connected to V_P or V_N .

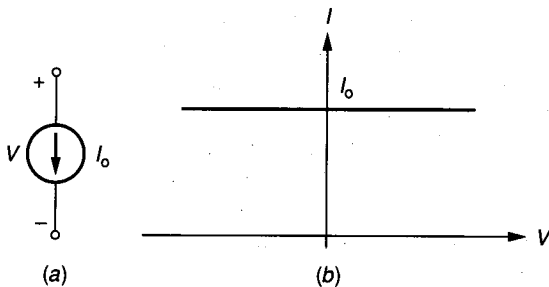


FIGURE 5.3-1
 (a) Schematic symbol for a current source, (b) $I-V$ characteristics of an ideal current source.

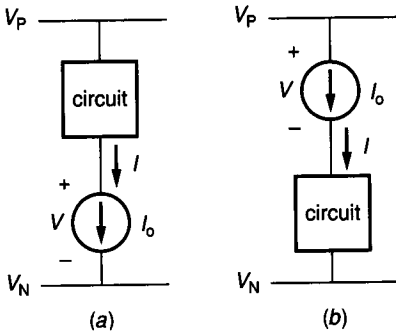


FIGURE 5.3-2
 (a) A current sink, (b) A current source.

In most current source/sink realizations, the ideal curve of Fig. 5.3-1b is only approximated over a limited range of the voltage V . Also the current is rarely bidirectional. The resulting I - V characteristics of a practical current source/sink realization are shown in Fig. 5.3-3. It is seen that there is a minimum voltage, V_{MIN} , below which the current source/sink will not be a good approximation to I_o . Further, it is seen that even in the region where the current source/sink is a reasonably good approximation to I_o , the actual source/sink deviates by a resistance R_o , which represents the parallel resistance of the current source/sink and ideally is infinite. Thus, the two major aspects by which a current source/sink is characterized are V_{MIN} and R_o .

Figure 5.3-4a shows a BJT realization of a current sink. V_{BB} is a battery used to bias Q1. It follows that for $V > V_{\text{CE}}(\text{sat})$ the current value is given by the following relation.

$$I_o = I_S \exp\left(\frac{V_{\text{BB}}}{V_t}\right) \quad (5.3-1)$$

$V_{\text{CE}}(\text{sat})$ is the collector-emitter voltage where Q1 enters the forward saturation region.

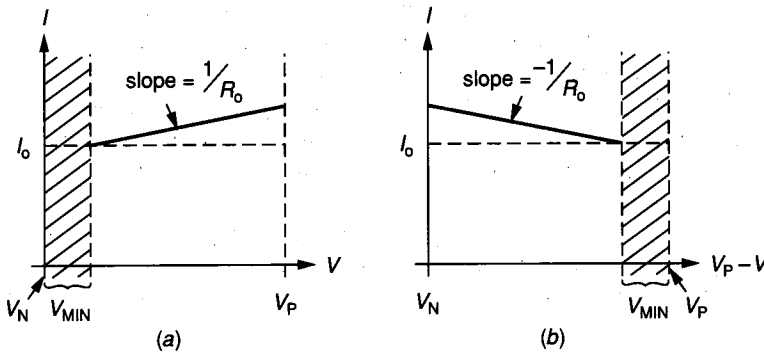
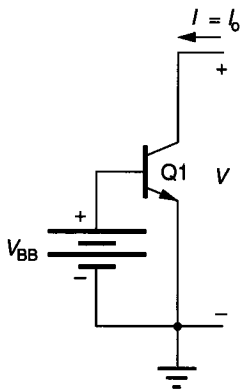
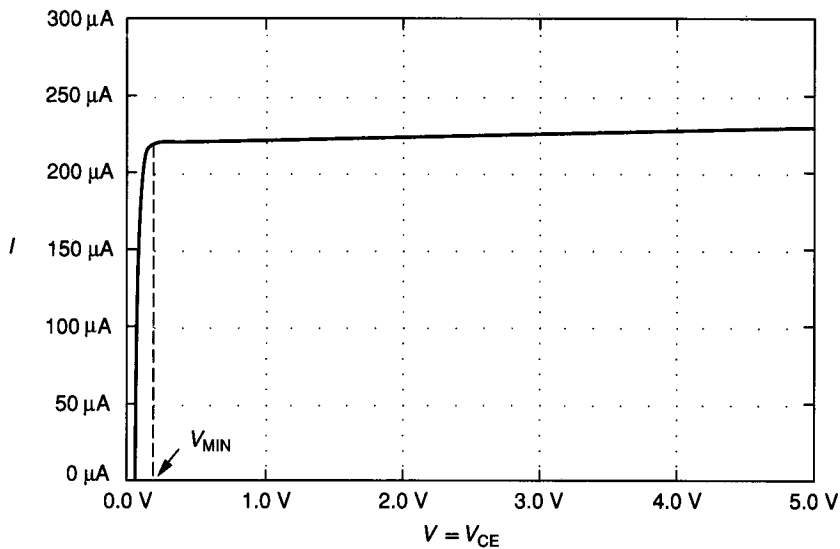


FIGURE 5.3-3
 Practical I - V characteristics for: (a) A current sink, (b) A current source.



(a)



(b)

FIGURE 5.3-4
(a) BJT current sink, (b) I - V characteristics of a.

The region from $V = 0$ to $V = V_{MIN}$ corresponds to the forward saturation region of Q1. As a result V_{MIN} is approximated by

$$V_{MIN} \approx V_{CE}(\text{sat}) \tag{5.3-2}$$

which is normally around 0.2 V (see Table 3.3-2). For $V > V_{MIN}$, the slope of the current is proportional to g_o , where the small signal output conductance is given in Table 3.3-4. Thus, the output resistance of the current sink, R_o , is

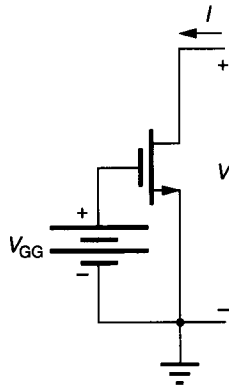
$$R_o \approx \frac{1}{g_o} = \frac{V_{AF}}{I_o} \tag{5.3-3}$$

Equations 5.3-1 through 5.3-3 also hold for the current source as characterized by Fig. 5.3-3b.

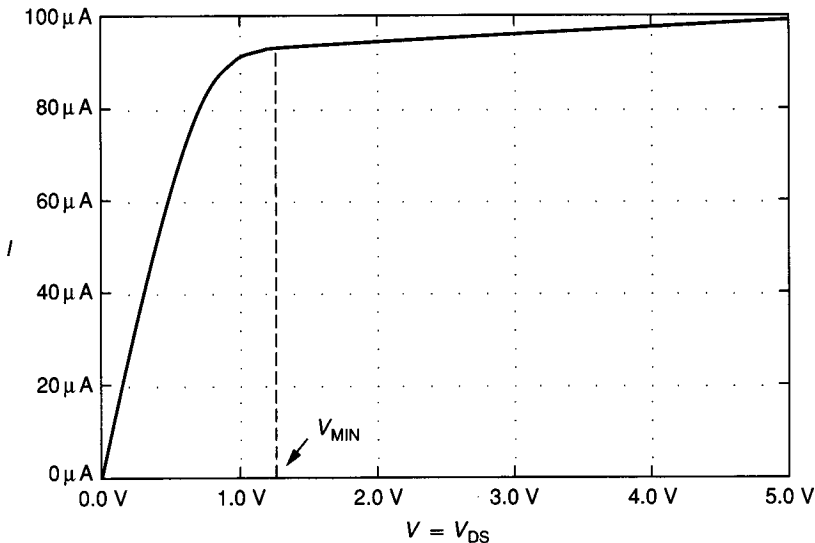
Figure 5.3-4b shows the I - V characteristics of the circuit of Fig. 5.3-4a with $V_{BE} = 0.7$ V, $I_S = 0.4$ fA, $\beta_F = 100$, and $V_{AF} = 200$ V. With these values V_{MIN} should be approximately 0.2 V, $I_o = 219$ μ A, and $R_o = 913$ k Ω for $V_t = 25.9$ mV. A SPICE simulation for the circuit of Fig. 5.3-4b gives $V_{MIN} = 0.2$ V, $I_o = 220$ μ A, and $R_o = 889$ k Ω .

Figure 5.3-5a shows a MOS realization of a current sink. From Eq. 3.1-5, if $\lambda = 0$, the value of I_o is given as

$$I_o = \frac{K'_N W}{2L} (V_{GG} - V_T)^2 \quad (5.3-4)$$



(a)



(b)

FIGURE 5.3-5

(a) MOS current sink, (b) I - V characteristics of a.