The value of V_{MIN} is equal to $V_{DS}(sat)$ and is given in Eq. 3.1-3 as

$$V_{MIN} = V_{GG} - V_T \tag{5.3-5}$$

The output resistance of the current sink for $V > V_{MIN}$ is equal to $1/g_{ds}$ of the small signal model parameters of the MOS (see Table 3.1-3) and is

$$R_o = \frac{1}{g_{ds}} = \frac{1}{\lambda |I_o|} \tag{5.3-6}$$

Equations 5.3-4 through 5.3-6 also hold for the MOS current source using the characterization of Fig. 5.3-3b.

Figure 5.3-5b shows the $I - V$ characteristics of the circuit of Fig. 5.3-5a with $V_{GG} = 2.0$ V, $W = 50 \mu$, $L = 10 \mu$, $V_T = 0.75$ V, $K'_N = 24 \mu$ A/V^2, $\gamma_N = 0.8 V^{1/2}$, $\lambda = 0.01 V^{-1}$ and $\phi = 0.6$ V. With these values, $V_{MIN} = 1.25$ V, $I_o = 94 \mu$A, and $R_o = 1.064$ MΩ. A SPICE simulation for Fig. 5.3-5b gives $V_{MIN} = 1.2$ V, $I_o = 97 \mu$A, and $R_o = 1.079$ MΩ.

The BJT and MOS current source/sinks are reasonable approximations of the ideal for limited values of voltage. While the output resistance of both are similar, the BJT has a much smaller value of V_{MIN}. In many cases, the output resistance of the simple BJT or MOS current source/sinks is not sufficiently large. Of course, R_o can be increased by decreasing I_o but other methods exist which allow R_o to be increased without decreasing I_o. Two methods will be investigated. The first uses negative feedback and the second uses positive feedback.

Consider the BJT current sink of Fig. 5.3-6a, which has a resistor R connected between the emitter and ground. The output resistance seen at the terminals across which V is defined will be called R_o. R_o is defined as a ratio of

(a)   (b)
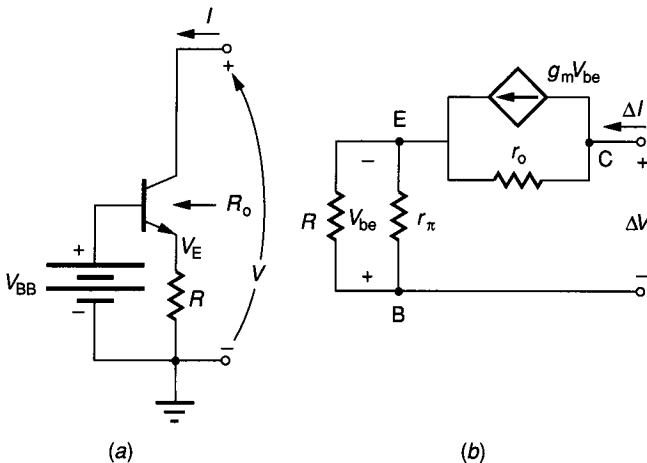
FIGURE 5.3-6
(a) Increasing the output resistance of the BJT current source/sink by negative feedback, (b) Small signal model of a.

ΔV over ΔI. Assume that an increase in ΔV causes an increase in ΔI. However, the ΔI increase causes a ΔV_E increase resulting in a ΔV_{BE} decrease. The ΔV_{BE} decrease will cause a decrease in I opposing the assumed increase in ΔI. The feedback is negative series, which will cause the value of R_o to be larger than R_o with $R = 0$ by approximately the value of the feedback loop gain.

The dc current I_0 can be found by iteratively solving the voltage loop equation consisting of V_{BB}, V_{BE}, and the drop across R. The small signal model of the circuit of Fig. 5.3-6a (see Fig. 3.3-8) is shown in Fig. 5.3-6b. ΔV and ΔI are the small signal values of V and I, respectively. Analysis of this circuit gives

$$R_o = \frac{\Delta V}{\Delta I} = r_o[1 + (g_m + g_o)(r_\pi \,\|\, R)] \qquad (5.3\text{-}7)$$

If $R = 0$, Eq. 5.3-7 reduces to r_o. The magnitude of the feedback loop gain is given by the second term in the brackets. As R becomes large, Eq. 5.3-7 approaches $r_o(1 + \beta_F)$, which means that the output resistance of the circuit of Fig. 5.3-6a with $R = 0$ can be increased by a factor of up to $1 + \beta_F$ for large values of R.

Figure 5.3-7a shows this principle applied to the MOS current sink. I_o can be found from the large signal model and letting $V_S = I_o R$. In the MOS case, the value of V_{BS} is not zero, so the small signal model is that shown in Fig. 5.3-7b. The output resistance of the circuit of Fig. 5.3-7b is
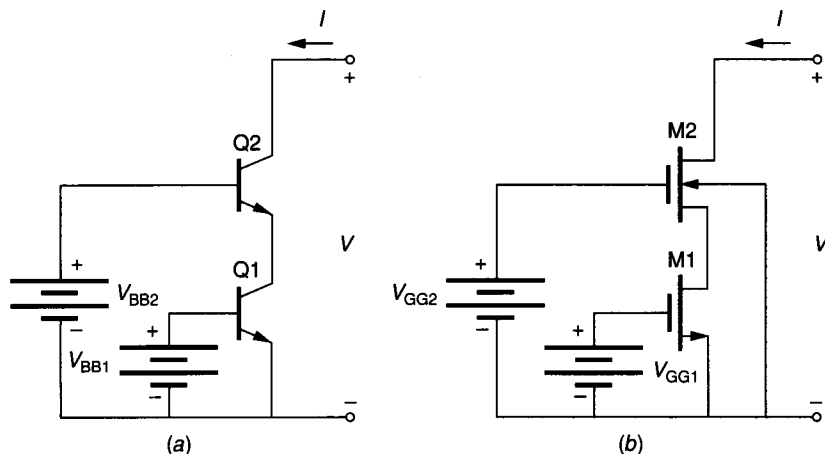
$$R_o = \frac{\Delta V}{\Delta I} = r_{ds}[1 + (g_m + g_{mb} + g_{ds})R] \approx r_{ds}(1 + g_m R) \qquad (5.3\text{-}8)$$

where $g_m > g_{mb} > g_{ds}$. In the MOS case, the magnitude of the feedback loop gain is $g_m R$ and continues to increase as R increases which helps to compensate for the fact that the g_m in Eq. 5.3-8 is typically less than the g_m in Eq. 5.3-7.
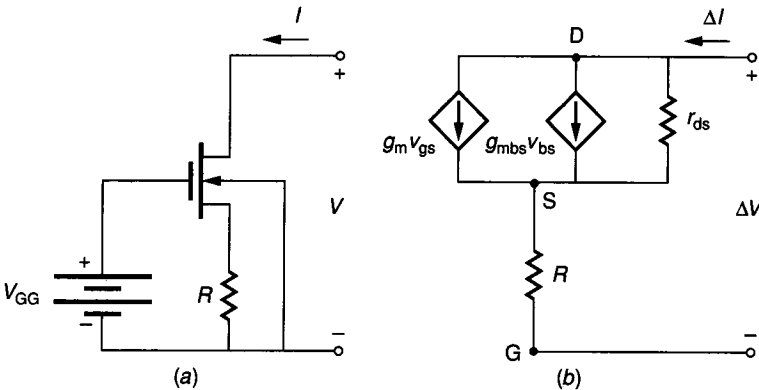
FIGURE 5.3-7
(a) Increasing the output resistance of the MOS current sink by negative feedback, (b) Small signal model of a.

FIGURE 5.3-8
Practical implementation of: (*a*) Fig. 5.3-6*a*, (*b*) Fig. 5.3–7*a*.

An implementation of the circuits of Figs. 5.3-6*a* and 5.3-7*a* is shown in the circuits of Figs. 5.3-8*a* and 5.3-8*b*, respectively. The output current is the same as given in Eqs. 5.3-1 and 5.3-4. The output resistance of the circuit of Fig. 5.3-8*a* can be found by replacing R in Eq. 5.3-7 by the output resistance of Q1, r_o to give

$$R_o = r_{o2}[1 + (g_{m2} + g_{o2})(r_{\pi 2} \| r_{o1})] \qquad (5.3\text{-}9)$$

Similarly, Eq. 5.3-8 can be used to find the output resistance of the circuit of Fig. 5.3-8*b* resulting in

$$R_o = r_{ds2}[1 + (g_{m2} + g_{mb2} + g_{ds2})r_{ds1}] \qquad (5.3\text{-}10)$$

Assuming that Q1 and Q2 of Fig. 5.3-8*a* are identical to the BJT used in Fig. 5.3-4*b*, we find that $g_{m2} = 8.456$ mS, $r_{o1} = r_{o2} = 913$ kΩ, and $r_{\pi 2} = 11.826$ kΩ. Substituting into Eq. 5.3-9 gives an output resistance of 91.05 MΩ. The increase of R_o from 0.913 MΩ to 91.05 MΩ is an increase of almost $1 + \beta_F$. Assuming that M1 and M2 of Fig. 5.3-8*b* are identical with the MOS device used in Fig. 5.3-5*a* gives a $g_{m2} = 152.6 \mu$S and $g_{ds1} = g_{ds2} = 0.97 \mu$S ignoring for the moment g_{mb2}. Substituting these values into Eq. 5.3-10 and neglecting g_{mb2} gives an output resistance of 171.9 MΩ.

While the values of R_o have been significantly increased for both the BJT and MOSFET current source/sinks, the value of V_{MIN} has also been increased. The design of V_{BB2} in Fig. 5.3-8*a* or V_{GG2} in Fig. 5.3-8*b* is crucial to achieving the minimum value of V_{MIN}. Fig. 5.3-9*a* shows the circuit of Fig. 5.3-8*a* biased for the minimum value of V_{MIN} which is equal to $2V_{CE}(\text{sat})$. Therefore, if both transistors are identical, then $V_{BE1} = V_{BE2}$ will give the same current assuming large β_F. Thus V_{BB2} should be designed to equal
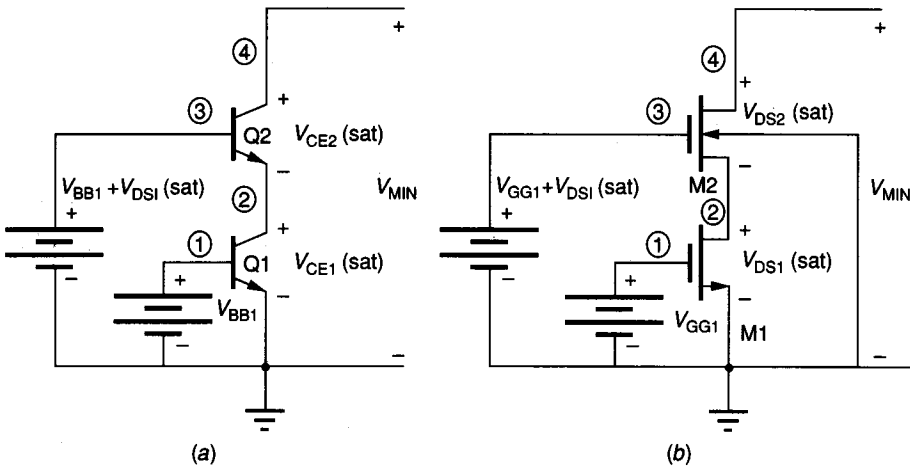
FIGURE 5.3-9
Minimum V_{MIN} design of: (a) Fig. 5.3-8a, (b) Fig. 5.3-8b.

$$V_{BB2} = V_{CE1}(\text{sat}) + V_{BB1} \qquad (5.3\text{-}11)$$

to achieve the minimum value of V_{MIN}. A similar consideration holds for the MOSFETs of Fig. 5.3-8b, which are redrawn in Fig. 5.3-9b. In this analysis we must include the effects of the bulk–source voltage on M2. To have the same current in both M2 and M1 implies that the following relationship must be true

$$V_{GS1} - V_{T1} = V_{GS2} - V_{T2} \qquad (5.3\text{-}12)$$

Therefore V_{GG2} of Fig. 5.3-8b is

$$V_{GG2} = V_{DS1}(\text{sat}) + V_{GS2} = V_{DS1}(\text{sat}) + V_{GG1} - V_{T1} + V_{T2} \qquad (5.3\text{-}13)$$

With this value of V_{GG2} the minimum value of V_{MIN} will be $2(V_{GG1} - V_{T1})$.

Figures 5.3-10a and b are the results of SPICE simulation of the circuits of Figs. 5.3-9a and b using the same model parameters as for the previous simulation and with $V_{BB2} = 0.4$ V and $V_{GG2} = (1.25 + 2.0 - 0.75 + 1.218) = 3.718$ V. It is seen that V_{MIN} for the BJT current sink of Fig. 5.3-9a is approximately 0.4 V. The output resistance is too large to be determined with any accuracy from the plots of Fig. 5.3-10a and b. Figure 5.3-10b shows that V_{MIN} for the MOS current sink of Fig. 5.3-9b is about 1.8 V. The advantage of BJTs over MOSFETs with regard to signal swing is very apparent in the circuits studied above.

The second method of increasing the value of R_o of a simple current source/sink uses positive feedback. Figure 5.3-11a shows the concept of this technique. I_o and R_o represent the current source or sink of Figs. 5.3-4a or 5.3-5a. The amplifier A of Fig. 5.3-11a is an ideal voltage-controlled, voltage source controlled by V. The battery V_o is used to permit a dc voltage drop across the

(a)

(b)
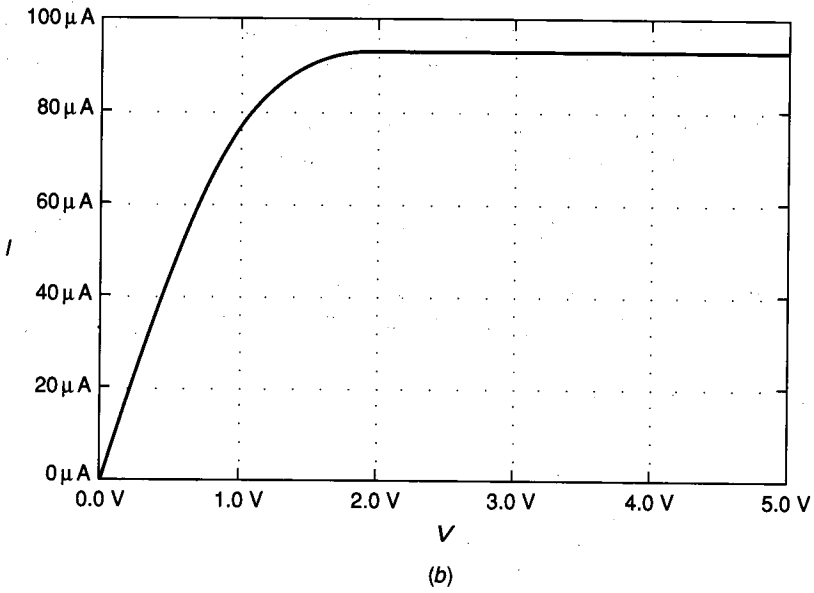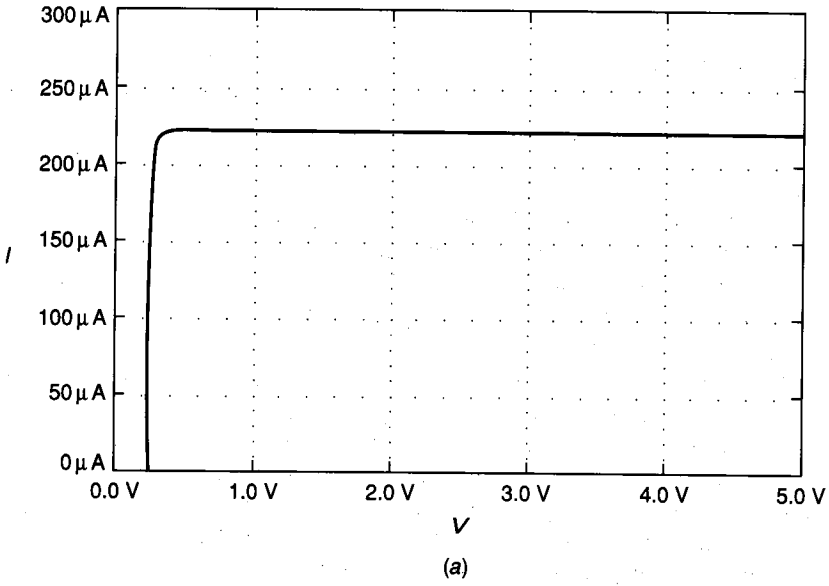
FIGURE 5.3-10
Simulation of: (a) Fig. 5.3-9a (b) Fig. 5.3-9b.
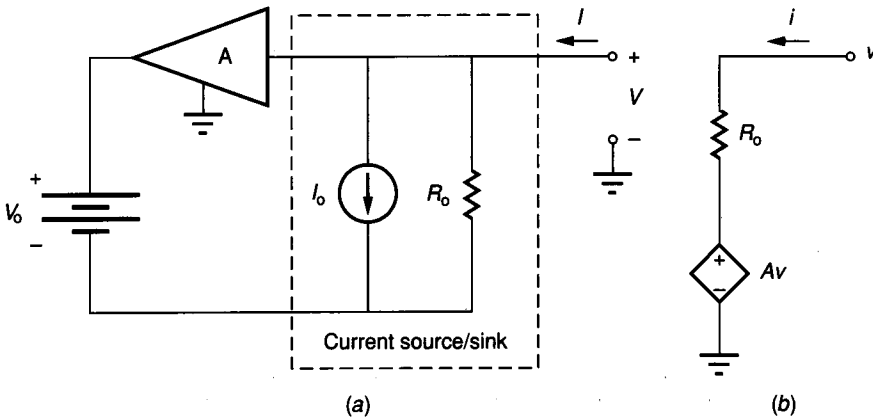
FIGURE 5.3-11
(a) Concept of using positive feedback to increase R_0, (b) ac model of a.

current sink/source. Figure 5.3-11b shows the ac model of the circuit of Fig. 5.3-11a. The output resistance can easily be found as

$$R_{out} = \frac{v}{i} = \frac{R_0}{1 - A} \qquad (5.3\text{-}14)$$

If A is slightly less than unity then $(1 - A)^{-1}$ is a large number causing R_{out} to be much greater than R_0. This technique is called *bootstrapping* and has many uses.

While this technique works better with depletion devices (e.g., can make V_0 in Fig. 5.3-11a with a depletion device), we shall first show how to apply bootstrapping to BJT and enhancement MOS transistors. Figure 5.3-12a shows how the current source of Fig. 5.3-4a can be bootstrapped by Q2. Because the ac voltage gain from the base of Q2 to the emitter of Q2 is always less than one, then the ac voltage at the emitter of Q1 follows the ac voltage at the collector of Q1. Consequently, there is very little ac change in voltage from the collector to emitter of Q1 thus boosting the output resistance value. The resistor R is necessary to allow the emitter of Q1 to follow its collector. Note that as the voltage V changes that all of this change is across R, and the current necessary to create this voltage comes from Q2. I_0 is approximately equal to I_1.

The value of V_{EE2} can be zero without influencing the circuit because Q1 is in the forward active region when $V_{CE1} = V_{BE2}$. Unfortunately, the resistance R keeps the bootstrapped current sink from having a low V_{MIN}. As V_{CE1} approaches V_{CE1} (sat), Q2 turns off. The voltage across R will be $I_1R = IR$ until Q1 goes into saturation. As a result

$$V_{MIN} = V_{CE}(\text{sat}) + I_0R \qquad (5.3\text{-}15)$$

If R is small and V_{EE2} negative ($V_{CE1}(\text{sat}) - V_{BE2}$), a very low value of V_{MIN} with high R_0 could be achieved.

Figure 5.3-12b gives the small signal model of Fig. 5.3-12a where the $g_{m2}v_{be2}$ has been simplified by source reduction. From this model the ac output resistance can be calculated as

$$R_o = \frac{v}{i} = \frac{r_{\pi2} \| r_{o1} + 1/g_{m2} \| R}{1 - g_{m2}R/(1 + g_{m2}R)} = \left[r_{\pi2} \| r_{o1} + \frac{1}{g_{m2}} \| R \right][1 + g_{m2}R]$$

(5.3-16)

Unfortunately, $r_{\pi2}$ tends to work against obtaining large values of ac output resistance using the BJT bootstrapped current sink.

Figure 5.3-13a shows a MOS implementation of the bootstrapped current sink. The MOS version does not suffer the $r_{\pi2}$ effects of the BJT version. The minimum value of V_{MIN} is given as

$$V_{MIN} = V_{DS1}(\text{sat.}) + I R \qquad (5.3\text{-}17)$$

and is achievable only when $V_{SS2} < V_{DS1}(\text{sat.}) - V_{T2}$. The bulk-source influence in M1 and M2 must also be considered in the design of Fig. 5.3-13a. The small signal model of the MOS bootstrapped current sink in Fig. 5.3-13b can be used to find the output resistance given as

$$R_o = \frac{v}{i} = \left[\frac{r_{ds1} + 1/g_m \| R}{1 - g_{m2}R/(1 + g_{m2}R)} \right] = \left(r_{ds1} + \frac{1}{g_{m2}} \| R \right)(1 + g_{m2}R) \quad (5.3\text{-}18)$$

It can be seen that the value of R_o of Fig. 5.3-5a can be increased by approximately $(1 + g_{m2}R)$.
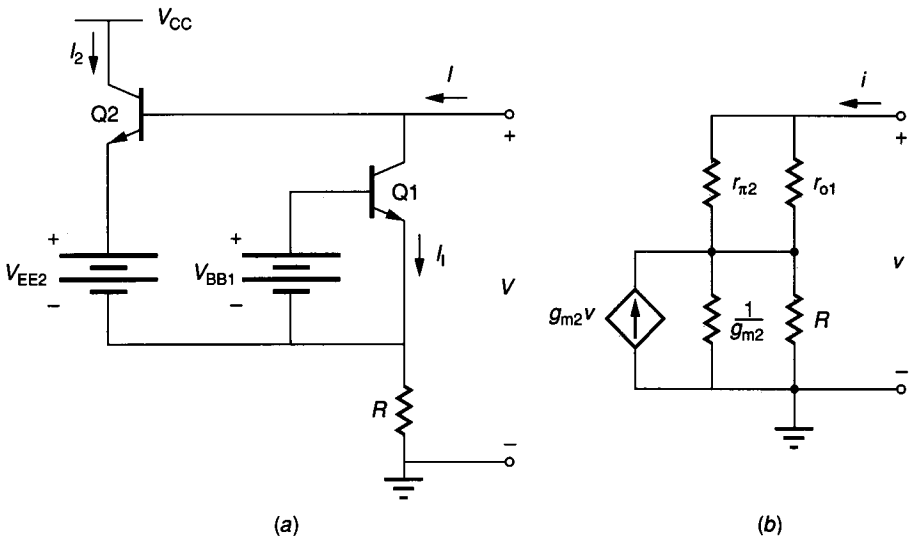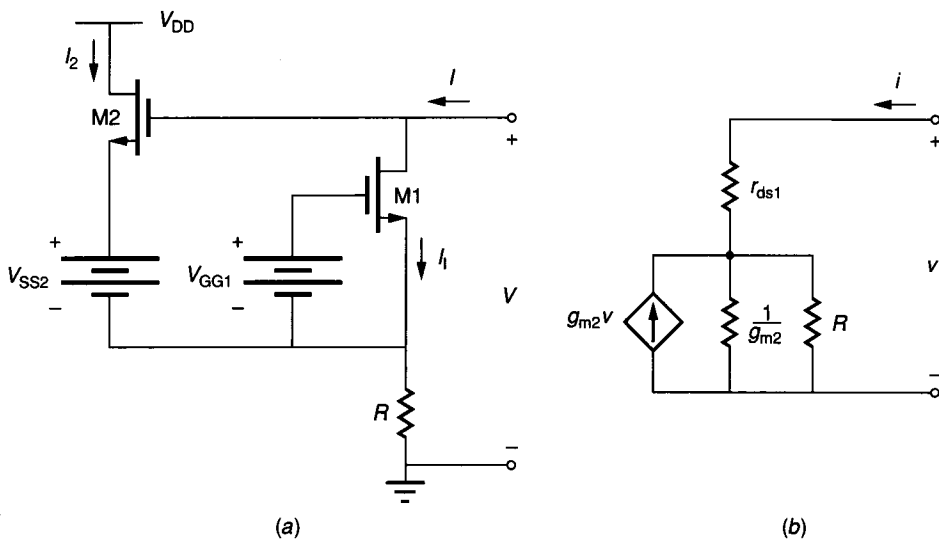

(a)

(b)

FIGURE 5.3-12
(a) BJT bootstrapped current sink, (b) ac model of a.

FIGURE 5.3-13
(a) MOS bootstrapped current sink, (b) ac model of a.

For depletion devices the dc polarity of V_{DS} and V_{GS} can be opposite. Examples are the depletion-mode MOSFET, the JFET, and the GaAs MESFET. Let us consider the n-channel depletion MOSFET as an example. Figure 5.3-14a shows that a depletion MOSFET current sink can be obtained by simply connecting the gate to the source. The I–V characteristics are shown in Fig. 5.3-14b, where V_T is the pinch-off voltage and I_o is the drain-source current with $V_{GS} = 0$. The bootstrapping principle can be applied to the depletion MOSFET very conveniently, as shown in Fig. 5.3-15a. In this circuit, M2 bootstraps the channel resistance r_{ds1} of M1, causing the output resistance
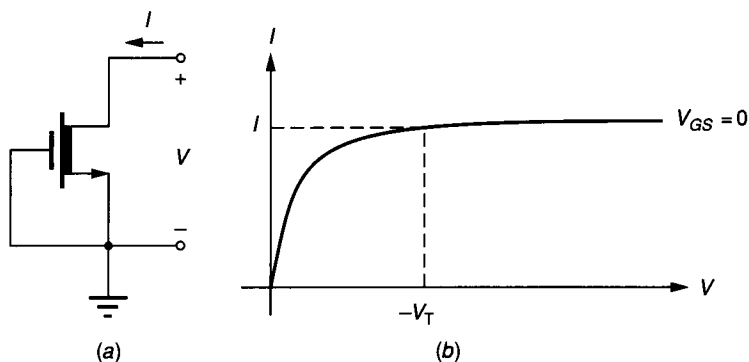
FIGURE 5.3-14
(a) n-channel, JFET current sink, (b) I–V characteristics of a.

of this current source to be increased. Fig. 5.3-15b gives the small signal model of Fig. 5.3-15a. The small signal output resistance is given as

$$R_o = \frac{v}{i} = \frac{r_{ds1} + (1/g_{m2}) \parallel r_{ds2}}{1 - (g_{m2}r_{ds2})/(1 + g_{m2}r_{ds2})} = \left(r_{ds1} + \frac{1}{g_{m2}} \parallel r_{ds2} \right)(1 + g_{m2}r_{ds2})$$

$$(5.3-19)$$

Unfortunately, the minimum value of V_{MIN} is not small and is at least equal to $| V_T |$. Without the flexibility of bias voltages, the geometries of M1 and M2 will have to be adjusted to account for the fact that $V_{GS1} \neq V_{GS2}$.

A MOS current source/sink that outperforms any of the previous current source/sinks considered so far in the area of high R_o and low V_{MIN} is shown in Fig. 5.3-16a[3] and is called a *regulated cascode current sink*. The output current is given by Eq. 5.3-4. The ac output resistance of M1 can be increased by stabilizing its drain-source voltage. In the regulated cascode current sink, the gate voltage of M2, which is the same as the drain–source voltage of M1, is regulated by a feedback loop consisting of M2 and M4 as an amplifier and M3 as a voltage follower. If all transistors operate in saturation and if the bulk effects are ignored, the ac output resistance can be found as

$$R_o \simeq r_{ds1} \left(\frac{g_{m2}g_{m3}}{g_{ds3}(g_{ds2} + g_4)} \right)$$

$$(5.3-20)$$

where g_4 is the output conductance of the I_4 current source. It is seen that the output resistance is higher than any MOS circuit considered so far. If $I_4 = 2$ μA, and $I = 94$ μA; then $g_1 = 0.02$ μS, $g_{d2} = 0.02$ μS, $g_{m2} = 21.9$ μS, r_{ds1}
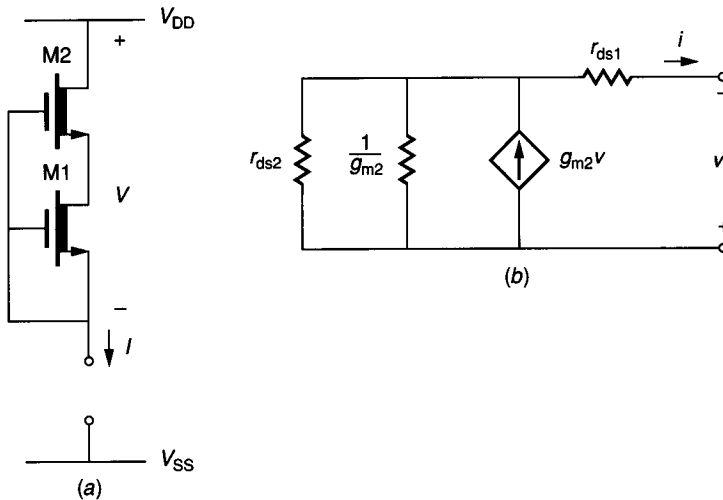
FIGURE 5.3-15
(a) Bootstrapped JFET current source, (b) Small signal model of a.
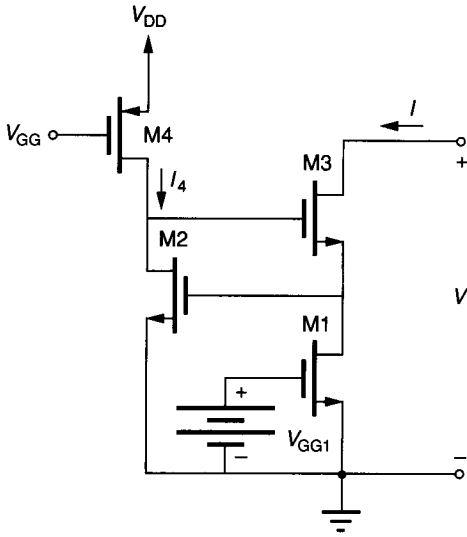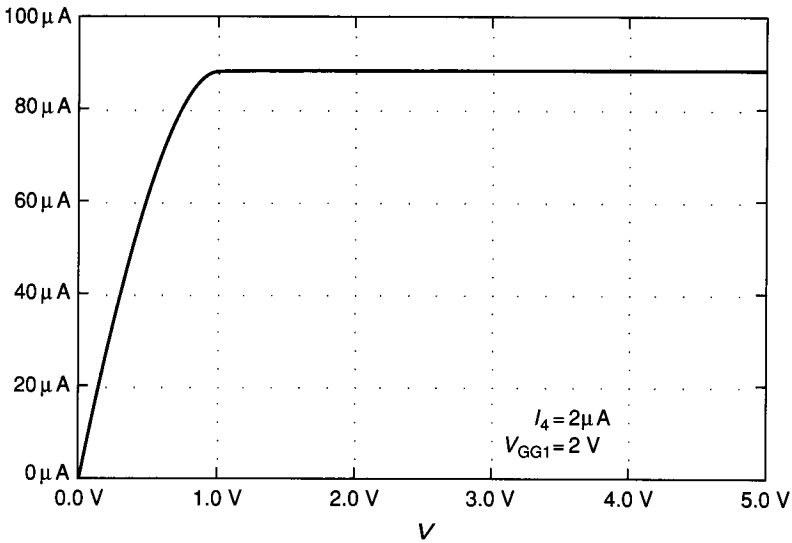
FIGURE 5.3-16
(a) Regulated cascode current sink, (b) Simulation results of Fig. 5.3-16a.

$= 1.064$ MΩ, $g_{m3} = 150.2$ μS, and $g_{ds3} = 0.94$ μS. Thus, the calculated value of R_o is 93.08 GΩ!

The circuit of Fig. 5.3-16a even works with a somewhat reduced R_o performance when the drain–source voltage across M3 is lowered to the point where it starts to operate in the ohmic region. The gate voltage of M3 may be driven by the feedback loop almost up to V_{DD}, causing the V_{DS} drop across M3 to stay

small. Thus, the minimum value of V_{MIN} is given approximately by V_{GS2} and is written as

$$V_{MIN} = V_{GS2} = \sqrt{\frac{2I_1 L_2}{K_N' W_2}} + V_{T2} \qquad (5.3\text{-}21)$$

Figure 5.3-16b is a simulated output of the circuit of Fig. 5.3-16a when $I_1 = 2$ μA and all transistors are identical with $W = 50$ μ and $L = 10$ μ using the model parameters previously employed. For the conditions stated above, the minimum value of V_{MIN} is 0.93 V. The current of Fig. 5.3-16b is slightly less than the anticipated 94 μA because the value of V_{GS2}, 0.93 V, is less than the 1.25 V required to keep M1 in saturation. Using Eq. 3 of Table 3.1-1 gives $I_o = 87.6 \mu$A, which matches well with Fig. 5.3-16b. Similar considerations could be used to develop a high-performance BJT current-sink.

In this section, we have examined methods of implementing current source/sinks. It was seen that a current source/sink can be characterized by its current, small signal output resistance, R_o, and its minimum voltage drop, V_{MIN}. It was shown how negative and positive feedback could be used to increase the value of R_o. Because these techniques increased V_{MIN} it was necessary to consider how to minimize this characteristic. Methods of implementing the bias supplies will be considered in the next several sections. A regulated cascode MOS current sink was introduced that had superior performance to all previous MOS current sink realizations. A comparison of the various current sinks considered in this section is given in Table 5.3-1. The current sources have similar characteristics.

TABLE 5.3-1
Comparison of current sinks

Current sink	Figure	R_O	Minimum V_{MIN}
Simple BJT	5.3-4a	$\dfrac{V_{AF}}{I_o}$	$V_{CE}(sat)$
Simple MOS	5.3-5a	$r_o = \dfrac{1}{\lambda I_o}$	$V_{GG1} - V_T$
Cascade BJT	5.3-9a	$r_{o2}[1 + g_{m2}(r_{\pi2} \| r_{o1})]$	$2V_{CE}(sat)$
Cascade MOS	5.3-9b	$r_{ds2}[1 + (g_{m2} + g_{mbs2})r_{ds1}]$	$2(V_{GG1} - V_{T1})$
Bootstrapped BJT	5.3-12a	$\left[(r_{\pi2} \| r_{o1}) + \left(\dfrac{1}{g_{m2}} \middle\| R\right)\right](1 + g_{m2}R)$	$V_{CE}(sat) + I_o R$
Bootstrapped MOS	5.3-13a	$\left(r_{ds1} + \dfrac{1}{g_{ms1}} \middle\| R\right)(1 + g_{m2}R)$	$V_{DS}(sat) + I_o R$
Regulated cascoded	5.3-16a	$r_{ds1}\left(\dfrac{g_{m2}g_{m3}}{g_{ds3}(g_{ds2} + g_4)}\right)$	$\sqrt{\dfrac{2I_1 L_2}{K_N' W_2}} + V_{T4}$

5.4 CURRENT MIRRORS/AMPLIFIERS

In the previous section we considered the subject of current sources and sinks where the objective was to implement the ideal $I-V$ characteristics of Fig. 5.3-1b. A dc voltage source was used to bias the implementation of the current sources or sinks. This section considers similar circuits, with the exception that the current source or sink is biased by a dc current rather than a dc voltage.

The circuits of this section are distinct from those of the last in that they use the principle of matched devices. This section will begin by applying the principle of matched devices to bipolar and then to MOSFET circuits resulting in current mirrors/amplifiers. It will also be shown how to analyze so-called matched circuits when they are not matched. Because the matching principle is much like looking into a mirror, the circuits of this section are called *current mirrors*. The term *current amplifier* is also used for current mirrors when an input current change creates an output current change.

One of the advantages of integrated circuits over discrete components is the ability to practically match components without trimming. This matching feature is used in this section to provide a very versatile and useful block called the current mirror. Before considering the current mirror, let us introduce the principles of matched devices. Consider initially two npn bipolar junction transistors. If the Early voltage effects are neglected, it follows from Eq. 3.3-13 that the large signal collector currents in the active region with the base-emitter junction forward-biased and the base-collector junction reverse-biased are given as

$$I_{C1} = I_{S1}\exp\left(\frac{V_{BE1}}{V_t}\right) = I_{S1}\exp\left(\frac{qV_{BE1}}{kT}\right) \qquad (5.4\text{-}1)$$

and

$$I_{C2} = I_{S2}\exp\left(\frac{V_{BE2}}{V_t}\right) = I_{S2}\exp\left(\frac{qV_{BE2}}{kT}\right) \qquad (5.4\text{-}2)$$

where from Eq. 3.3-6 and Eq. 3.3-7 of Chapter 3,

$$I_{Si} = \frac{qn_i^2\overline{D_n}A_i}{Q_{Bi}(V_{CBi})} \, , \, i = 1, 2 \qquad (5.4\text{-}3)$$

The parameters of Eq. 5.4-3 have been defined in Chapter 3. Solving for V_{BE1} and V_{BE2} gives

$$V_{BE1} = V_t \ln\left(\frac{I_{C1}}{I_{S1}}\right) \qquad (5.4\text{-}4)$$

and

$$V_{BE2} = V_t \ln\left(\frac{I_{C2}}{I_{S2}}\right) \qquad (5.4\text{-}5)$$

Now if the base and emitter of Q1 are connected to the base and emitter of Q2 and a source of base current exists, then the following relationship between I_{C1} and I_{C2} results.

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} = \frac{qn_i^2\overline{D_n}A_1}{Q_{B1}(V_{CB1})} \times \frac{Q_{B2}(V_{CB2})}{qn_i^2\overline{D_n}A_2} = \frac{A_1Q_{B2}(V_{CB2})}{A_2Q_{B1}(V_{CB1})} \tag{5.4-6}$$

If the transistors are matched and if $V_{CB1} = V_{CB2}$, $A_1 = A_2$ and $Q_{B1} = Q_{B2}$, then $I_{C1} = I_{C2}$, which illustrates the principle of matched devices. This principle is very important and will be used both in biasing and small signal design of integrated circuits.

The application of the matching principle to implement a simple bipolar current sink is shown in Fig. 5.4-1. In this circuit, the base and the collector of Q1 are physically connected together for two reasons. The first is to provide a source of base current for both Q1 and Q2. The second is to keep V_{CE1} small so that R_1 essentially defines the current I_{IN}. The reader can note that V_{CC}, R_1 and the base-collector connected transistor Q1 actually implement V_{BB} of the current sink of Fig. 5.3-4a.

The above results will now be used to calculate the ratio of I_{C2} to I_{IN}. Initially, the emitter areas of Q1 and Q2 will be assumed to be equal and the Early voltage will be neglected so that differences in V_{CB1} and V_{CB2} can be ignored. If the bases of Q1 and Q2 and the emitters of Q1 and Q2 are physically connected together, then the matching principle gives
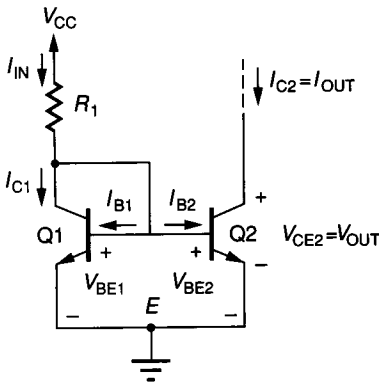
$$I_{C2} = I_{C1} \tag{5.4-7}$$

However,

$$I_{C1} = I_{IN} - I_{B1} - I_{B2} \tag{5.4-8}$$

and

$$I_{IN} = \frac{V_{CC} - V_{BE1}}{R_1} \tag{5.4-9}$$

FIGURE 5.4-1
A simple bipolar current mirror.

Using the relationship, $I_C = \beta_F I_B$ and assuming $I_{B1} = I_{B2} = I_B$ and $B_{F1} = B_{F2} = B_F$, gives

$$I_{C2} = \frac{I_{IN}}{1 + (2/\beta_F)} = \frac{V_{CC} - V_{BE1}}{R_1[1 + (2/\beta_F)]} \tag{5.4-10}$$

It should be noted that as β_F approaches infinity, I_{C2} approaches I_{IN}.

In the considerations above, the Early voltage was neglected which turns out to be a poor assumption in some applications. If the Early voltage, V_{AF} is included in the large signal expressions for the collector current, Equations 5.4-1 and 5.4-2 are modified as

$$I_C = I_S\left(1 + \frac{V_{CE}}{V_{AF}}\right) \exp\left(\frac{V_{BE}}{V_t}\right) \tag{5.4-11}$$

Using the matched transistor principle, we can solve for the ratio of I_{C2} to I_{C1} as

$$\frac{I_{C2}}{I_{C1}} = \frac{I_{S2}[1 + (V_{CE2}/V_{AF})]}{I_{S1}[1 + (V_{CE1}/V_{AF})]} = \frac{1 + (V_{CE2}/V_{AF})}{1 + (V_{CE1}/V_{AF})} = \frac{1 + (V_{CE2}/V_{AF})}{1 + (V_{BE1}/V_{AF})} \tag{5.4-12}$$

Note that even though the transistors are matched, I_{C2} is not necessarily equal to I_{C1}. As an example, assume that $V_{CE2} = 10$ V, $V_{BE1} = 0.6$ V and $V_{AF} = 100$ V. The ratio of I_{C2} to I_{C1} is 1.093. It should be apparent that the Early voltage effects cannot be neglected in some practical applications. Although a 9% error is somewhat discouraging, alternative configurations will be developed which significantly reduce this error in matched devices.

Before developing the configurations which eliminate the Early voltage effects, let us consider what happens if the transistors are not exactly matched. Assume that A, Q_B and $\alpha_F(= \beta_F/(1 + \beta_F))$ are not matched and are given by

$$A_1 = A + (\Delta A/2) \tag{5.4-13}$$

$$A_2 = A - (\Delta A/2) \tag{5.4-14}$$

$$Q_{B1} = Q_B + (\Delta Q_B/2) \tag{5.4-15}$$

$$Q_{B2} = Q_B - (\Delta Q_B/2) \tag{5.4-16}$$

$$\alpha_{F1} = \alpha_F + (\Delta\alpha_F/2) \tag{5.4-17}$$

and

$$\alpha_{F2} = \alpha_F - (\Delta\alpha_F/2) \tag{5.4-18}$$

where A, Q_B and α_F are the nominal values and corresponding parameters ΔA, ΔQ_B and $\Delta\alpha_F$ are the differences between the two values. I_{C1} may be expressed from Eq. 5.4-8 and Eq. 3.3-12 as

$$I_{C1} = \alpha_{F1}I_{IN} - \frac{\alpha_{F1}}{\beta_{F2}}I_{C2} \tag{5.4-19}$$

Substituting Eq. 5.4-19 into Eq. 5.4-6 with $V_{CB1} = V_{CB2}$ results in

$$I_{C2} = \frac{(A_2 Q_{B1}/A_1 Q_{B2})\alpha_{F1}}{1 + (\alpha_{F1}A_2 Q_{B1}/\beta_{F2}A_1 Q_{B2})}I_{IN} \approx \left(\frac{A_2 Q_{B1}}{A_1 Q_{B2}}\right)\alpha_{F1}\alpha_{F2}I_{IN} \tag{5.4-20}$$

where it has been assumed that

$$\frac{\alpha_{F1} A_2 Q_{B1}}{A_1 Q_{B2}} \approx 1 \qquad (5.4\text{-}21)$$

Substituting Eqs. 5.4-13 through 5.4-18 into Eq. 5.4-20 results in

$$I_{C2} = I_{IN}\left[\frac{(1 - \Delta A/2A)(1 + \Delta Q_B/2Q_B)(1 + \Delta\alpha_F/2\alpha_F)(1 - \Delta\alpha_F/2\alpha_F)}{(1 + \Delta A/2A)(1 - \Delta Q_B/2Q_B)}\right]$$

$$(5.4\text{-}22)$$

which can be approximated for small ΔA, ΔQ_B and $\Delta\alpha_F$ by,

$$I_{C2} \cong I_{IN}\left[1 - \frac{\Delta A}{A} + \frac{\Delta Q_B}{Q_B} + \frac{\Delta\alpha_F}{\alpha_F}\right] \qquad (5.4\text{-}23)$$

It can be shown that

$$\frac{\Delta I_S}{I_S} \cong \frac{\Delta A}{A} - \frac{\Delta Q_B}{A_B} \qquad (5.4\text{-}24)$$

so that Eq. 5.4-23 can be written as

$$I_{C2} \cong I_{IN}\left[1 - \frac{\Delta I_S}{I_S} + \frac{\Delta\alpha_F}{\alpha_F}\right] \qquad (5.4\text{-}25)$$

If a 5% mismatch for I_S and a 10% mismatch for β_F (which is a 0.1% mismatch in α_F for $\beta_F = 100$) is assumed, then Eq. 5.4-25 shows that the variation for the ratio of I_{C2} to I_{IN} is 0.949 to 1.051, or about ±5%.

The simulated performance of the simple BJT current mirror is shown in Fig. 5.4-2. The transistors have been assumed to be equal and have the model parameters of $\beta_F = 200$, $\beta_R = 0.43$, $I_S = 0.4$ fA, $V_{AF} = 200$ V and $V_{AR} = 20$ V. An ideal current mirror would have horizontal curves whose value of $I_{C2}(I_{OUT})$ would be exactly equal to $I_{C1}(I_{IN})$ independent of V_{OUT}. As in the previous section, a measure of the "horizontalness" of the curves is given by the small signal resistance or conductance looking back into Q2 from the collector to ground. We shall designate this resistance or conductance as r_{out} or g_{out}. In the circuit of Fig. 5.4-1, r_{out} is simply r_{o2} which was derived in Chapter 3 as

$$r_{out} = r_{o2} = \frac{V_{AF}}{I_{C2}} \qquad (5.4\text{-}26)$$

The small signal output resistance of the current mirror will be important in determining its performance.

When β_F is not large it can cause current ratio errors which may total a few percent, as indicated in Eq. 5.4-10. Since β_F is not accurately controlled at processing, the β_F effects are unacceptably large in some applications. Figure 5.4-3 shows a configuration which reduces the effect of β_F upon the current ratio of Q1 and Q2. Transistor Q3 requires less current by a factor of β_F from I_{IN} in order to provide the base currents for Q1 and Q2. Neglecting mismatch effects and Early voltage effects, it can be shown that
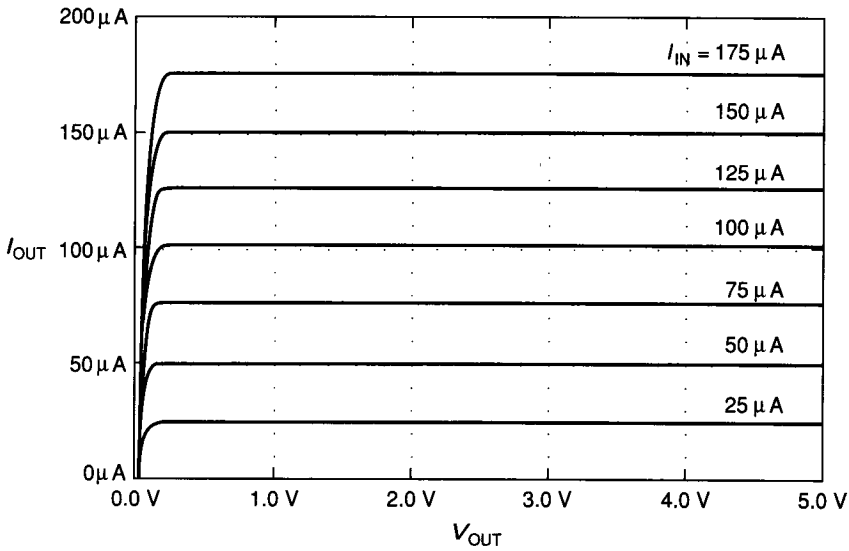
FIGURE 5.4-2
$I-V$ characteristics of the simple bipolar current mirror of Fig. 5.4-1.

$$I_{C2} = \frac{I_{IN}}{1 + 2/[\beta_F(1 + \beta_F)]} \qquad (5.4-27)$$

Comparing Eqs. 5.4-10 and 5.4-27 shows that the transistor Q3 has reduced the β_F effects by about a factor of β_F, which is quite significant. It is also observed that two base-emitter drops rather than the single drop in Eq. 5.4-9 are subtracted from V_{CC} to find the voltage drop across R_1 which determines I_{IN}. This implies that for small values of V_{CC}, I_{IN} will be less well defined in the circuit of Fig. 5.4-3 than it was in the circuit of Fig. 5.4-1.
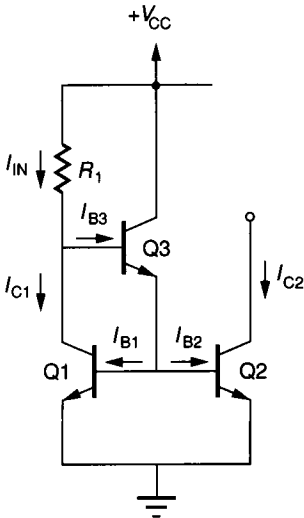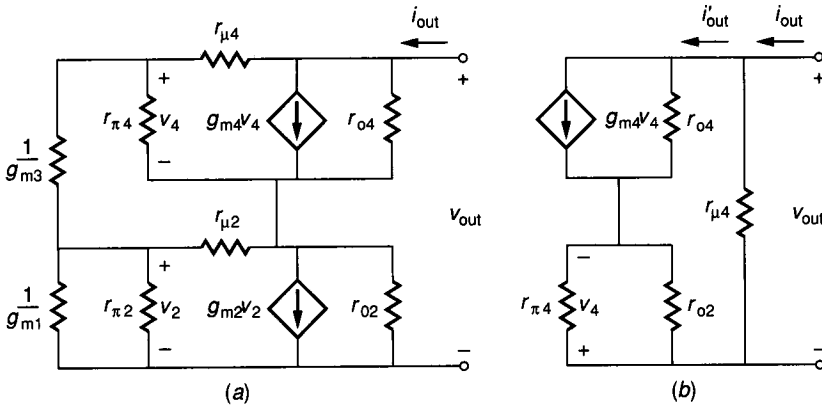

FIGURE 5.4-3
A circuit reducing the influence of β_F on the current mirror of Fig. 5.4-1.
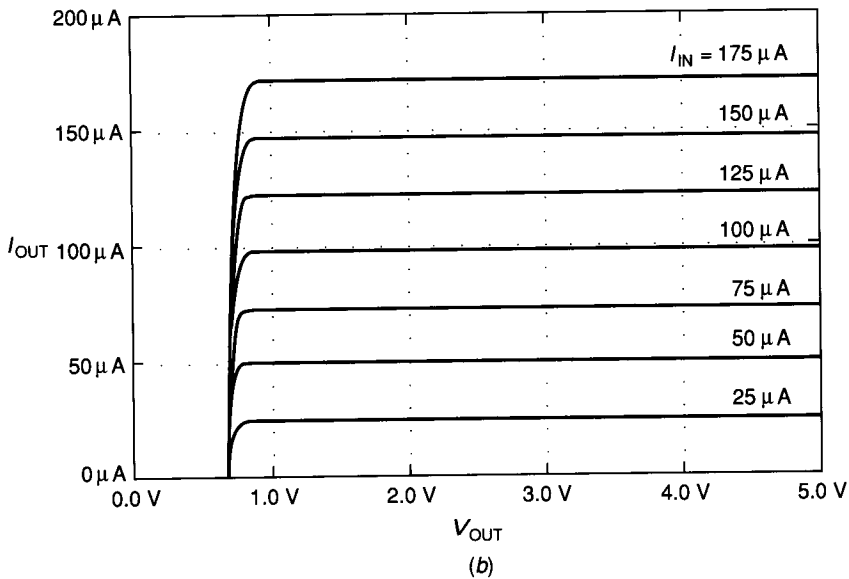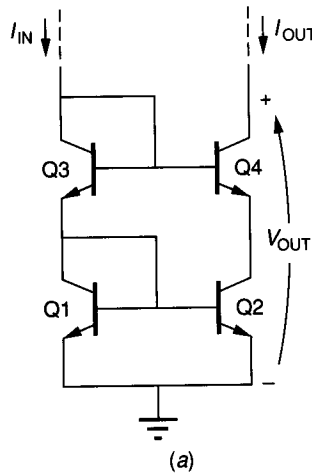
FIGURE 5.4-4
(a) Bipolar cascode current mirror, (b) Simulated performance of the BJT cascode current mirror.

Two methods of reducing Early voltage effects will now be considered. One is to constrain V_{CE1} and V_{CE2} of Fig. 5.4-1 to be equal, and the other uses negative feedback. The first method is illustrated by the cascode current mirror shown in Fig. 5.4-4a. Since the value of V_{BE3} is approximately equal to V_{BE4}, then V_{CE1} (V_{BE1}) is approximately equal to V_{CE2}, thereby eliminating the Early effect from Eq. 5.4-12. Although the effect of the Early voltage has been eliminated on the ratio of I_{C2} to I_{C1} of the cascode current mirror, one may ask about the effect of the Early voltage on Q4. Fortunately, Q4 is operating with

FIGURE 5.4-5
(a) Small signal model of Fig. 5.4-4a, (b) Simplified small signal model of a.

the base terminal at ac ground, which reduces the effect of the Early voltage by about a factor of β_F. The $I{-}V$ characteristics of the cascode current mirror are shown in Fig. 5.4-4b. The improvement of the cascode current mirror over the simple current mirror can be quantified by comparing the ac output impedances of the two circuits. The small signal model for the cascode current mirror is shown in Fig. 5.4-5a, where the frequency-independent, hybrid-pi model of Fig. 3.3-12 and the assumption that ($1/g_{m1}$) and ($1/g_{m3}$) are much less than $r_{\pi 2}$ or $r_{\pi 4}$ have been used. A simplified form of this model is shown in Fig. 5.4-5b. The small signal output resistance can be found by noting that

$$i'_{out} = g_{m4}v_4 + (v_{out} + v_4)/r_{o4} \qquad (5.4\text{-}28)$$

and

$$v_4 = -i_{out}(r_{\pi 4} \parallel r_{o2}) = -i_{out}\frac{r_{o2}}{1 + g_{m4}r_{o2}/\beta_{F4}} \qquad (5.4\text{-}29)$$

Substituting Eq. 5.4-29 into 5.4-28 gives

$$\frac{v_{out}}{i'_{out}} = r_{o4}\left[1 + \frac{r_{o2}(1 + g_{m4}r_{o4})}{r_{o4}[1 + (g_{m4}r_{o2}/\beta_{F4})]}\right] \qquad (5.4\text{-}30)$$

Finally, the small signal output resistance is found by combining the resistance represented by Eq. 5.4-30 and $r_{\mu 4}$ in parallel to give

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{\mu 4} \parallel r_{o4}\left[1 + \frac{r_{o2}(1 + g_{m4}r_{o4})}{r_{o4}[1 + (g_{m4}r_{o2}/\beta_{F4})]}\right] \cong \beta_{F4}r_{o4} \qquad (5.4\text{-}31)$$

We see that the cascode current mirror does indeed have a small signal resistance, which is approximately β_F times the small signal resistance of the simple current mirror.

The emitter areas of Q1 and Q2 should be as large as possible for best matching. All other transistors can have minimum area.

A second method of increasing the small signal output resistance uses negative feedback and is shown in Fig. 5.4-6a. This circuit is called the Wilson current mirror.[4] The Wilson current mirror uses negative current-shunt feedback to stabilize the ratio of I_{C3} to I_{IN} and to increase r_{out}. The operation of the circuit is explained by assuming that I_{IN} is constant and that an incremental increase in V_{CE3} causes an increase in I_{C3}. This increase in I_{C3} causes V_{BE3} and V_{BE1} to increase. The V_{BE1} increase causes an increase in I_{C1}. However, since I_{IN} stays constant, an increase in I_{C1} means a decrease in I_{B3}, which causes a decrease in I_{C3} counteracting the original increase in I_{C3} caused by a change in V_{CE3}. The feedback loop consists of Q3 (as a voltage follower), Q1 and Q2 (as a current mirror), and Q1-R_1 (as an inverting voltage amplifier). The loop gain of the circuit is seen to be approximately $\beta_F/2$, so that the small signal output resistance will be comparable to that of the cascode current mirror. Figure 5.4-6b illustrates the I–V characteristics of the Wilson current mirror of Fig. 5.4-6a. It can be shown that

$$I_{OUT} = I_{IN} \left[1 - \frac{2}{\beta_F^2 + \beta_F + 2} \right] \qquad (5.4\text{-}32)$$

r_{out} can be calculated from the small signal equivalent circuit of Fig. 5.4-6a shown in Fig. 5.4-7. The value of R_{eq} defined in Fig. 5.4–7 can be found to be

$$R_{eq} = \frac{v_1}{i} = \frac{r_{\pi 3} + R'}{1 + g_{m1}R'} \cong \frac{R'}{1 + g_{m1}R'} \cong \frac{1}{g_{m1}} \qquad (5.4\text{-}33)$$

Using Eq. 5.4-33 allows us to express r_{out} as (see Prob. 5.27).

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{o3}\left[1 + \frac{g_{m1}\beta_{F3}}{g_{m1} + g_{m2}} \right] + \frac{1}{g_{m1} + g_{m2}} \cong \frac{r_{o3}\beta_{F3}}{2} \qquad (5.4\text{-}34)$$

It is apparent from Eq. 5.4-34 that r_{out} has been improved over the simple current mirror of Fig. 5.4-1 by a factor of $\beta_0/2$. The small signal output resistance of current mirrors can be further increased by the use of special techniques.[5]

In many cases, the mirrored currents are designed not to be equal. This can be accomplished by making the base-emitter junction areas of the two mirror transistors unequal. They should be made as large as possible for best matching ratio accuracy. In Eq. 5.4-6, it can be seen that the ratio of the current in Q1 to that of Q2 is proportional to the ratio of the areas of the respective base-emitter junctions. This relationship can be expressed as

$$I_{C2} \cong \frac{A_2}{A_1} I_{C1} \qquad (5.4\text{-}35)$$

If the ratio of the currents is much different from unity, this approach can use significant area and will become less accurate due to the decrease in relative accuracy of large area ratios.
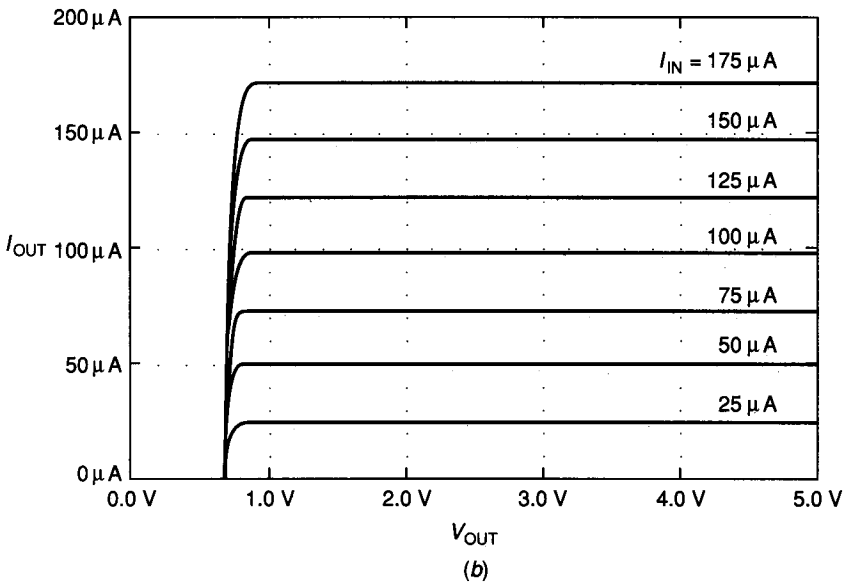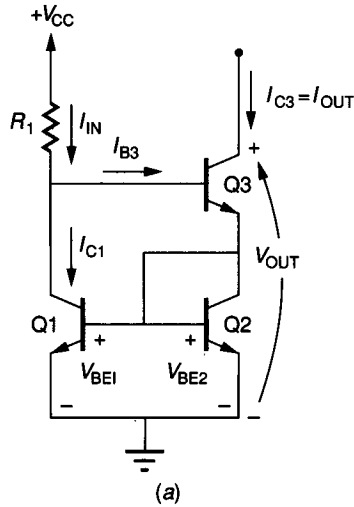
FIGURE 5.4-6
(a) Wilson BJT current mirror, (b) Simulated performance of the Wilson BJT current mirror of a.
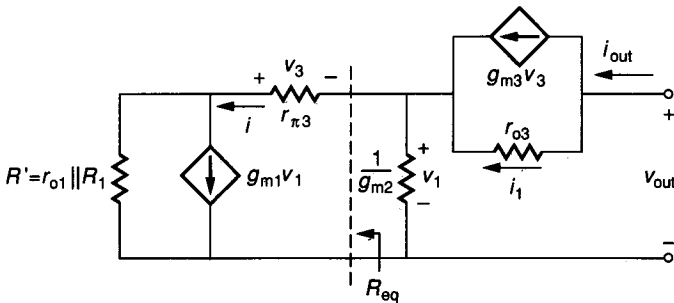
FIGURE 5.4-7
Small signal model for the Wilson current mirror of Fig. 5.4-6a.

The decrease in accuracy can be minimized using a principle called *replication*. Simply put, the replication principle states that an improvement in relative accuracy between two different sized areas occurs when the larger area is equal to an integer multiple of the smaller area. For example, suppose that $A_2 = mA_1$ where m is an integer. Improved relative accuracy is achieved when A_2 consists of m separate areas of A_1 connected appropriately. An example illustrates the replication principle.

> **Example 5.4-1.** Assume that Q1 and Q2 of Fig. 5.4-1 are being used to create a simple mirror having $I_{C2} = 5I_{C1}$. Assume further that A_1 is a rectangular area of W_1 times L_1, as shown in Fig. 5.4-8a. Q2 will have two different shapes. The first is shown in Fig. 5.4-8b and the second in Fig. 5.4-8c. Let $L_1 = L_2 = L$ and $W_1 = W$. Compare the ratio matching accuracy of the two layout approaches.

Solution. Assume resolution of any edge is given as

$$W_1 = W \pm \Delta W$$

$$W_2 = 5W \pm \Delta W$$

$$L_1 = L_2 = L \pm \Delta L$$

where ΔW and ΔL are the uncertainty of W and L. The ratio of A_2 to A_1 of Fig. 5.4-8b can be expressed as

$$\frac{A_2}{A_1} = \frac{(5W \pm \Delta W)(L \pm \Delta L)}{(W \pm \Delta W)(L \pm \Delta L)} = \frac{5 \pm (\Delta W/W)}{1 \pm (\Delta W/W)} \cong 5 \pm 4\frac{\Delta W}{W} \quad (5.4\text{-}36)$$

Similarly the ratio of A_2 to A_1 of Fig. 5.4-8c is expressed as

$$\frac{A_2}{A_1} = \frac{5(W \pm \Delta W)(L \pm \Delta L)}{(W \pm \Delta W)(L \pm \Delta L)} = 5 \quad (5.4\text{-}37)$$

The advantage of the replication principle is shown by the increased relative accuracy.

If the ratio of areas is not equal to an integer, the replication principle can still be used. If in Example 5.4-1 the value of I_{C2} were $5.5I_{C1}$, the larger transistor could consist of the replication of A_1 five times plus an area equal to $0.5A_1$. The designer has the option of making the $0.5A_1$ area the same shape as the A_1 area or choosing some other shape. The resulting ratio, while not as accurate as the integer case, will be more accurate than simply ratioing areas. If the areas represent transistors, the replicated areas are connected by connecting the collectors, bases and emitters of each replicated transistor.
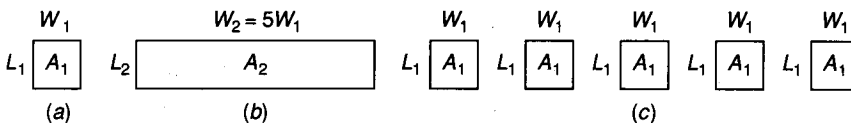
FIGURE 5.4-8
(a) Unit area A_1, (b) Area of $A_2 = 5A_1$, (c) Area of $A_2 = 5A_1$ obtained by replicating A_1 five times.

The large area ratio caused by unequal mirror currents can be avoided by using a resistor in series with the emitter of the lower current transistor, as shown in Fig. 5.4-9. This current mirror is called the Widlar current mirror[6] and can have large current differences with identical base-emitter areas. Note that the effect of R_2 will be to increase r_{out}. If Q1 and Q2 are matched and β_F is large, then the voltage drops around the base-emitter circuits can be written as

$$V_{BE1} - V_{BE2} = I_{C2}R_2 \tag{5.4-38}$$

If the V_{AF} effects are neglected, it follows from Eq. 5.4-11 that

$$V_t \ln\left(\frac{I_{IN}}{I_{C2}}\right) = I_{C2}R_2 \tag{5.4-39}$$

There are two cases in which Eq. 5.4-39 is used. The first is when I_{C2} and I_{IN} are known and R_2 is to be found. R_2 may be expressed as

$$R_2 = \frac{V_t}{I_{C2}} \ln\left(\frac{I_{IN}}{I_{C2}}\right) \tag{5.4-40}$$

For example, if $V_{CC} = 5$ V, $R_1 = 4.3$ kΩ and $I_{C2} = 10$ μA, then we find that $I_{C1} = (5 - 0.7)/4.3$ k$\Omega = 1$ mA and $R_2 = 11.97$ kΩ. We note that the ratio of I_{C1} to I_{C2} is 100 in this example. The second case, which uses Eq. 5.4-40, occurs when R_2 and I_{IN} are known. In this case, an iterative solution is required for I_{C2}. The effect of R_2 on r_{out} is to increase it. It can be shown (see Prob. 5.28) that r_{out} of the Widlar current mirror is given as

$$r_{out} = r_{\pi2} \| R_2 + r_{o2}\left[1 + g_{m2}r_{\pi2} \| R_2\right] \cong r_{o2}(1 + g_{m2}R_2) \tag{5.4-41}$$

To obtain good ratio accuracies, Q1 and Q2 should have large emitter areas.

Because the output of the current mirrors is a current sink, it is important to have a small value of V_{MIN}, which was defined in the previous section. The same considerations for V_{MIN} and r_{out} apply to current mirrors. Unfortunately, the conditions of $V_{CE1} = V_{CE2}$ in order to eliminate the Early effects may not be
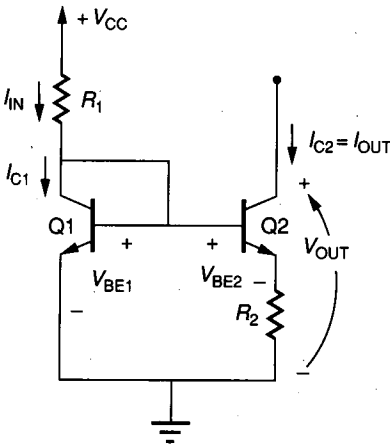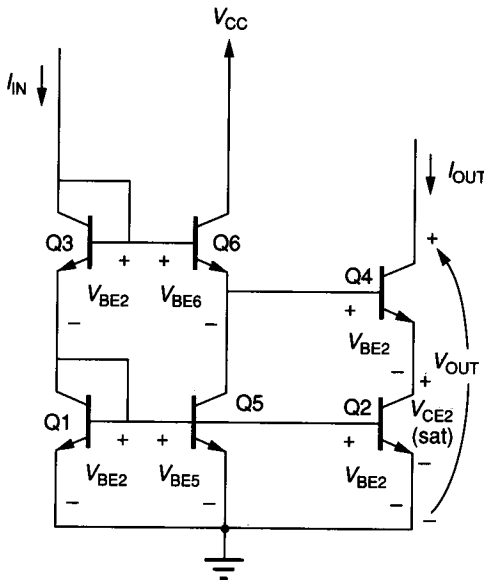

FIGURE 5.4-9
Widlar BJT current mirror.

compatible with the conditions for minimum V_{MIN}. For example, to obtain the minimum value of V_{MIN} in Fig. 5.4-4a requires that the dc voltage at the base of Q4 be equal to V_{CE2} (sat) $+ V_{BE4}$ (see Eq. 5.3-11). However, the voltage at the base of Q4 in Fig. 5.4-4a is equal to $2V_{BE2}$ assuming that all transistors are identical. A similar conflict between minimum V_{MIN} and large r_{out} exists for the Wilson current mirror of Fig. 5.4-6a. In this circuit, the minimum value of V_{MIN} is $V_{BE2} + V_{CE3}$(sat).

If one is willing to give up the constraint that V_{CE1} equals V_{CE2}, then it may be possible to achieve a minimum V_{MIN} design. Figure 5.4-10 shows one possible approach for the cascode current mirror of Fig. 5.4-4a. It has been assumed that Q1 through Q4 are identical transistors each having a base-emitter drop of V_{BE2}. It can be seen that if $V_{BE6} = V_{BE2} - V_{CE2}$(sat), that $V_{CE2} = V_{CE2}$(sat). V_{BE6} can be smaller than V_{BE2} by either decreasing the current of Q6 with respect to the current in Q1 through Q4 or by making the emitter area of Q6 much smaller than that of Q1 through Q4, or both. This can be seen by considering two different transistors designated as QA and QB. The difference in V_{BE} voltages can be expressed using Eqs. 5.4-4 and 5.4-5 as

$$\Delta V_{BE} = V_{BEA} - V_{BEB} = V_t \ln \left(\frac{I_{CA} \, I_{SB}}{I_{CB} \, I_{SA}} \right) \qquad (5.4\text{-}42)$$

Unfortunately, if ΔV_{BE} is much larger than V_t, the value of $(I_{CA}I_{SB})/(I_{CB}I_{SA})$ becomes too large to implement. For example, if the area of Q5 and Q6 of Fig.

FIGURE 5.4-10
Reduction of V_{MIN} of the BJT cascode current mirror of Fig. 5.4-4a.

5.4-10 is 50 times less than the area of Q1 through Q4, then ΔV_{BE} of Eq. 5.4-42 would be approximately 200 mV at room temperature. However, any component whose area is 50 times different than another has several disadvantages. These disadvantages include a large area requirement and poor matching between devices. The principle behind the Widlar current mirror could be employed to reduce the current in Q5 and Q6 by placing a resistor in series with the emitter of Q5. The current ratio required to obtain a ΔV_{BE} of 200 mV is approximately 2500. This ratio results in a value of $R_2 = 507$ kΩ at room temperature with $I_{C1} = 1$ mA.

The BJT current mirrors that have been presented can be characterized from the viewpoint of accuracy, output resistance, and V_{MIN}. Table 5.4-1 summarizes the performance of the BJT current mirrors considered where $I_{C2} \approx I_{C1}$. Additional considerations include the proper sizes to achieve the desired matching accuracy.

The same principles developed in this section for current mirrors using the BJT device also hold true for the MOS device. In many cases, the MOS current mirrors are simpler in concept because no base current is required. On the other hand, the bulk effects create limitations not found in BJT mirrors. The matching principle applied to MOS devices can be developed from the simple current mirror of Fig. 5.4-11a. Note that for $V_{DS1} \geq V_{T1}$, M1 will always be in saturation since $V_{DG1} = 0$. Assuming that V_{DS2} is greater than $V_{GS1} - V_{T1}$ allows the use of the saturation model for both devices. Solving for $V_{GS1} - V_{T1}$ and $V_{GS2} - V_{T2}$ from Eq. 4 of Table 3.1-1 gives

$$V_{GS1} - V_{T1} = \left[\frac{2L_1 I_{D1}}{K'_{N1} W_1 (1 + \lambda_1 V_{DS1})} \right]^{1/2} \tag{5.4-43}$$

and

$$V_{GS2} - V_{T2} = \left[\frac{2L_2 I_{D2}}{K'_{N2} W_2 (1 + \lambda_2 V_{DS2})} \right]^{1/2} \tag{5.4-44}$$

TABLE 5.4-1
Comparison of BJT current mirror performance

BJT current mirror	Accuracy $(I_{C2} = I_{C1})$	r_{out}	V_{MIN}
Simple Fig. 5.4-1	Poor	$r_o = V_{AF}/I_o$	$V_{CE}(sat)$
Cascode Fig. 5.4-4	Excellent	$r_o \beta_F$	$V_{BE} + V_{CE}(sat)$
Wilson Fig. 5.4-6	Good	$\dfrac{r_o \beta_F}{2}$	$V_{BE} + V_{CE}(sat)$
Modified cascode Fig. 5.4-10	Good	$r_o \beta_F$	$2V_{CE}(sat)$

Since the bulk-source voltages of M1 and M2 are identical, then V_{T1} and V_{T2} are identical and the following expression results.

$$\frac{I_{OUT}}{I_{IN}} = \frac{I_{D2}}{I_{D1}} = \frac{K'_{N1}W_1L_2(1 + \lambda_2 V_{DS2})}{K'_{N2}W_2L_1(1 + \lambda_1 V_{DS1})} \tag{5.4-45}$$

It can be seen that the channel modulation effect, λ, has the same influence on the MOS current mirror that the Early voltage had on the BJT current mirror. Because transistor Ws and Ls are found in Eq. 5.4-45, the geometry of the MOS devices can be used to determine the gain of the current mirror. Figure 5.4-11b gives the simulated $I–V$ characteristics using equal values of $W = 50\ \mu$ and $L = 10\ \mu$ and the model parameters of $V_T = 0.75$ V, $K'_N = 24\ \mu$A/V^2, $\gamma_N = 0.8$ V$^{-1/2}$, $\lambda_N = 0.01$ V^{-1}, and $\phi = 0.6$ V. These characteristics indicate
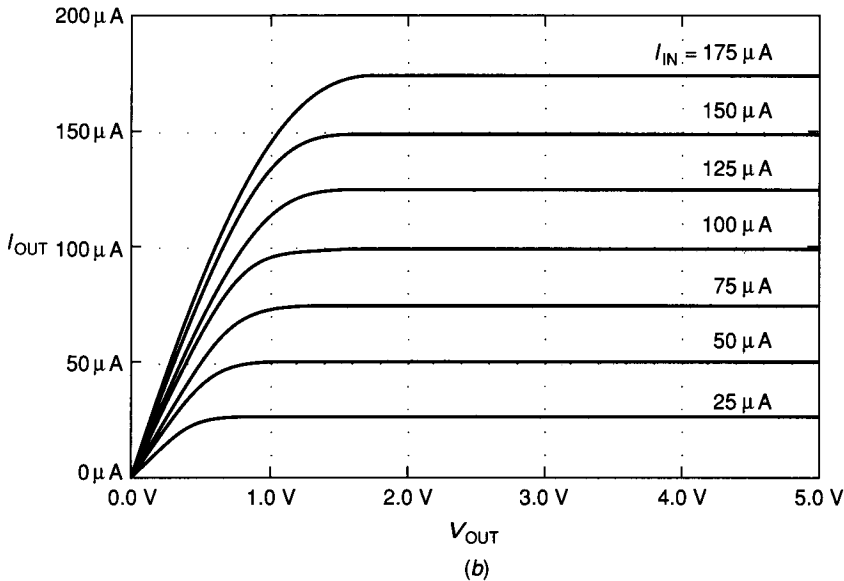

(a)

(b)
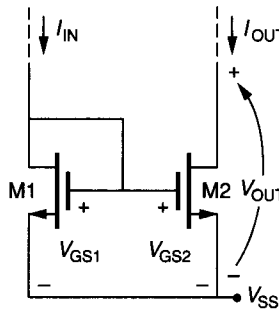
FIGURE 5.4-11
(a) Simple MOS current mirror, (b) Simulated performance of a.

that the channel modulation effect causes an increase in the slope of these curves preventing ideal current sink performance. A measure of the slope of these curves is given by the small signal output resistance and in this case is

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds2} = \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_{OUT}} \tag{5.4-46}$$

This corresponds to an output resistance of 1 MΩ when $I_{OUT} = 100\ \mu$A. The value of V_{MIN} for the circuit of Fig. 5.4-11a which occurs when M2 transitions from the saturation to the active region can be shown to be 1.2 V when $I_{IN} = 100\ \mu$A.

The matching accuracy of Eq. 5.4-45 can be determined in the same manner as was done for the BJT current mirror. The ratio of I_{D2} to I_{D1} (I_{OUT} to I_{IN}) can be expressed in general as

$$\frac{I_{D2}}{I_{D1}} = \frac{K'_{N2}(V_{GS2} - V_{T2})^2(1 + \lambda_2 V_{DS2})}{K'_{N1}(V_{GS1} - V_{T1})^2(1 + \lambda_1 V_{DS1})} \tag{5.4-47}$$

where it has been assumed that $W_2/L_2 = W_1/L_1$. In this discussion, the W/L ratios are assumed to be ideally matched. Using the following definitions

$$K'_{N1} = K'_N + (\Delta K'_N/2) \tag{5.4-48}$$

$$K'_{N2} = K'_N - (\Delta K'_N/2) \tag{5.4-49}$$

$$V_{T1} = V_T + (\Delta V_T/2) \tag{5.4-50}$$

$$V_{T2} = V_T - (\Delta V_T/2) \tag{5.4-51}$$

$$\lambda_1 = \lambda + (\Delta\lambda/2) \tag{5.4-52}$$

and

$$\lambda_2 = \lambda - (\Delta\lambda/2) \tag{5.4-53}$$

Eq. 5.4-47 may be expressed as

$$\frac{I_{D2}}{I_{D1}} = \frac{[K'_N - (\Delta K'_N/2)][V_{GS} - V_T + (\Delta V_T/2)]^2[1 + \lambda V_{DS} - (\Delta\lambda V_{DS}/2)]}{[K'_N + (\Delta K'_N/2)][V_{GS} - V_T - (\Delta V_T/2)]^2[1 + \lambda V_{DS} + (\Delta\lambda V_{DS}/2)]} \tag{5.4-54}$$

or as

$$\frac{I_{D2}}{I_{D1}} = \frac{(1 - \Delta K'_N/K'_N)[1 + \Delta V_T/2(V_{GS} - V_T)]^2(1 + \lambda V_{DS} - \Delta\lambda V_{DS}/2)}{(1 + \Delta K'_N/K'_N)[1 - \Delta V_T/2(V_{GS} - V_T)]^2(1 + \lambda V_{DS} + \Delta\lambda V_{DS}/2)} \tag{5.4-55}$$

Assuming that the differences in Eqs. 5.4-48 through 5.4-53 are small and that λV_{DS} is less than unity allows the simplification of Eq. 5.4-55 to

$$\frac{I_{D2}}{I_{D1}} \cong \left(1 - \frac{\Delta K'_N}{K'_N}\right)\left(1 + \frac{\Delta V_T}{V_{GS} - V_T}\right)^2(1 - \Delta\lambda V_{DS}) \tag{5.4-56}$$

or

$$\frac{I_{D2}}{I_{D1}} \cong 1 - \left(\frac{\Delta K_N'}{K_N'}\right) + \left(\frac{2}{(V_{GS}/V_T) - 1}\right)\left(\frac{\Delta V_T}{V_T}\right) - (\lambda V_{DS})\left(\frac{\Delta \lambda}{\lambda}\right) \qquad (5.4\text{-}57)$$

An example will illustrate these results

> **Example 5.4-1. Matching accuracy of a simple MOS mirror.** Two MOS devices are used to implement the current mirror of Fig. 5.4-11a. Suppose that at $I_{IN} = 100\ \mu A$, the various voltages were observed: $V_{GS1} = V_{GS2} = 3.6$ V and $V_{DS2} = 3.6$ V. Assume that the nominal parameters are $K_N' = 24\ \mu A/V^2$, $V_T = 0.75$ V and $\lambda_N = 0.01\ V^{-1}$. Furthermore, assume that the worst-case deviation about these values is $\pm 5\%$. Evaluate the deviation of the ratio of I_{D2}/I_{D1} from unity if $(W_1/L_1) = (W_2/L_2)$.
>
> **Solution.** Substituting into Eq. 5.4-57 gives
>
> $$\frac{I_{D2}}{I_{D1}} = 1 - (\pm 0.05) + (0.2598)(\pm 0.05) - (0.036)(\pm 0.05)$$
>
> $$= 1 \pm 0.039$$

Under these conditions, the analysis of matching accuracy shows that a deviation of $\pm 4\%$ can occur. The value of this deviation will depend upon the operating conditions. In this example, V_{DS1} was chosen to be equal to V_{DS2} in order to eliminate the error due to λ.

A current mirror with higher output resistance than that obtained from the simple MOS mirror is shown in Fig. 5.4-12a. M3 and M4 keep the values of V_{DS1} and V_{DS2} nearly equal, effectively removing the influence of the channel modulation effect. M4 increases the output resistance of the mirror using the principle demonstrated in Fig. 5.3-7a to increase the output resistance of a simple MOS current sink. Figure 5.4-12a is called an MOS cascode current mirror and is topologically identical to the BJT cascode current mirror of Fig. 5.4-4a. If the mismatch effects are neglected, the current gain of the MOS cascode current mirror is given as

$$\frac{I_{OUT}}{I_{IN}} = \frac{(W_2/L_2)}{(W_1/L_1)} \qquad (5.4\text{-}58)$$

Figure 5.4-12b shows the I–V characteristics of the circuit of Fig. 5.4-12a when all Ws are 50 μ, all Ls are 10 μ, $V_T = 0.75$ V, $K_N' = 24\ \mu A/V^2$, $\gamma_N = 0.8\ V^{1/2}$, $\lambda_N = 0.01\ V^{-1}$, and $\phi = 0.6$ V. These characteristics show that the output resistance of the MOS cascode mirror is significantly greater than the simple MOS mirror and that the accuracy is good.

The improvement in the slope reduction can be quantified by finding the small signal output resistance of the circuit of Fig. 5.4-12a. The output resistance of the MOS cascode current mirror is calculated using the small signal model of Fig. 5.4-13. First solve for v_{out}, which can be written as

$$v_{out} = v_4 + v_2 = r_{ds4}[i_{out} + g_{mb4}v_2 - g_{m4}(v_3 + v_1 - v_2)] + v_2 \qquad (5.4\text{-}59)$$
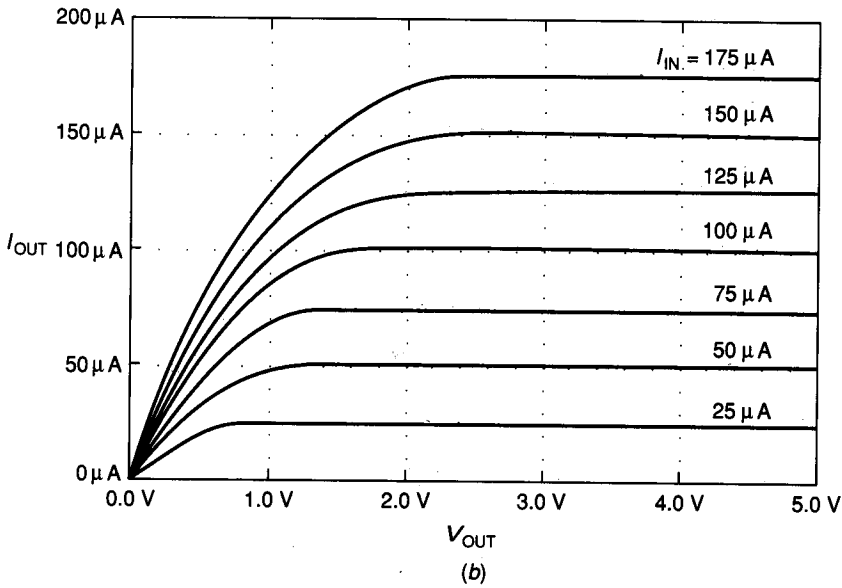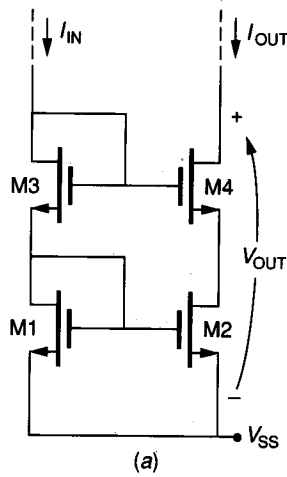
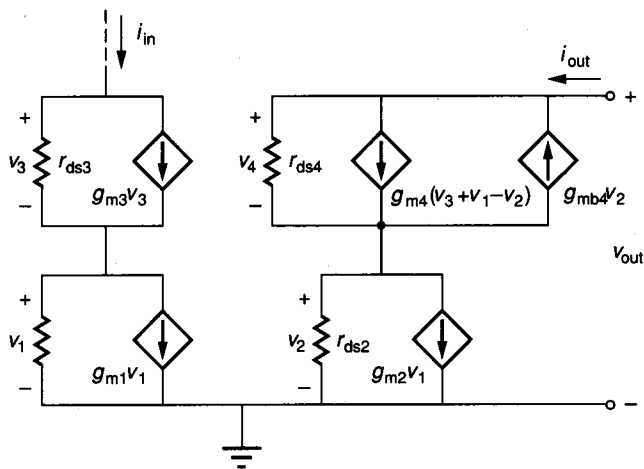**FIGURE 5.4-12**
(a) MOS cascode current mirror, (b) Simulated performance of a.

Also,

$$v_2 = r_{ds2}(i_{out} - g_{m2}v_1) \qquad (5.4\text{-}60)$$

Since $i_{in} = 0$ under small signal conditions, then v_1 and v_3 are also zero. Therefore, substitution of Eq. 5.4-60 into Eq. 5.4-59 results in,

$$v_{out} = i_{out}[r_{ds2} + r_{ds4} + r_{ds2}r_{ds4}(g_{m4} + g_{mb4})] \qquad (5.4\text{-}61)$$

FIGURE 5.4-13
Small signal model of the current mirror of Fig. 5.4-12a.

Solving for the output resistance, r_{out}, gives

$$r_{out} = r_{ds2} + r_{ds4} + r_{ds2}r_{ds4}g_{m4}(1 + \eta_4) \qquad (5.4\text{-}62)$$

where $\eta_4 = g_{mb4}/g_{m4}$ is defined in Table 3.1-3.

Comparing Eq. 5.4-62 with Eq. 5.4-46 shows that the small signal output resistance has been increased by a factor of $r_{ds4}g_{m4}(1 + \eta_4)$. The approximate value of r_{out} at 100 μA is 155 MΩ. The value of V_{MIN} at 100 μA for the MOS cascode mirror above is approximately 1.6 V, which can be a significant portion of V_{OUT}.

The MOS version of the Wilson current mirror is shown in Fig. 5.4-14a. The simulated performance of this current mirror using $W_1/L_1 = W_2/L_2 = W_3/L_3 = 50 \ \mu/10 \ \mu$ and the previous MOS model parameters is shown in Fig. 5.4-14b. Several aspects of the MOS Wilson current mirror are apparent. The first is that V_{MIN} represents a large portion of V_{OUT}. The second is that the curves are much flatter than the simple MOS mirror, indicating an increase in r_{out}. And thirdly, it can be shown that the linearity (or accuracy) of the MOS Wilson current mirror is not good for high current levels. This nonlinearity is due to the difference in V_{DS1} and V_{DS2} for larger currents. Since V_{DS2} is less than V_{DS1}, Eq. 5.4-45 shows that the channel modulation effects will cause I_{D2} to be less than I_{D1} if M1 and M2 are matched. This problem can be alleviated if a fourth, drain-gate-connected device is connected in series with M1 between the drain of M1 and the gate of M3.

The output resistance of the MOS Wilson current mirror will quantify the slope reduction compared with the simple MOS mirror. It can be shown that the small signal output resistance of the Wilson current mirror is given as (see Prob. 5.31)
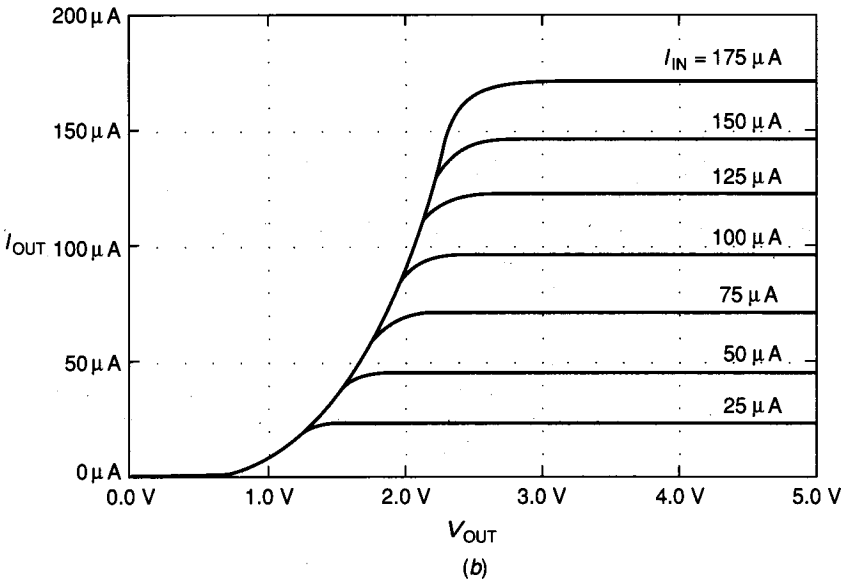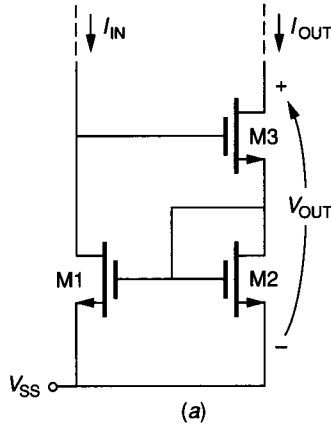
FIGURE 5.4-14
(a) MOS Wilson current mirror, (b) Simulated performance of a.

$$r_{out} = r_{ds3} + r_{ds2} \frac{1 + r_{ds3}g_{m3}(1 + \eta_3) + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + g_{m2}r_{ds2}} \qquad (5.4\text{-}63)$$

The output resistance of Fig. 5.4-14a is found to be comparable with the MOS cascode mirror of Fig. 5.4-12a. Unfortunately, both of these current mirrors require at least $2V_T$ across the input before they behave as described above.

The Widlar current mirror can also be implemented by MOS transistors and will be left as a problem (see Prob. 5.32). A practical consideration in matching the devices that are mirroring the current is to keep the channel lengths of both

devices equal. Since the channel length, L, is susceptible to lateral diffusion and the channel width is not, then the channel width, W, can be used to achieve nonunity current gains. Oxide encroachment has been ignored in this consideration. This was illustrated by the principle of replication, which was discussed earlier in this section.

In all the previous MOS current mirrors, the value of V_{MIN} became larger when the output resistance was increased. One circuit that minimizes V_{MIN} and still increases r_{out} is shown in Fig. 5.4-15a. This circuit is called the MOS regulated cascode mirror and uses the concept introduced in the regulated cascode
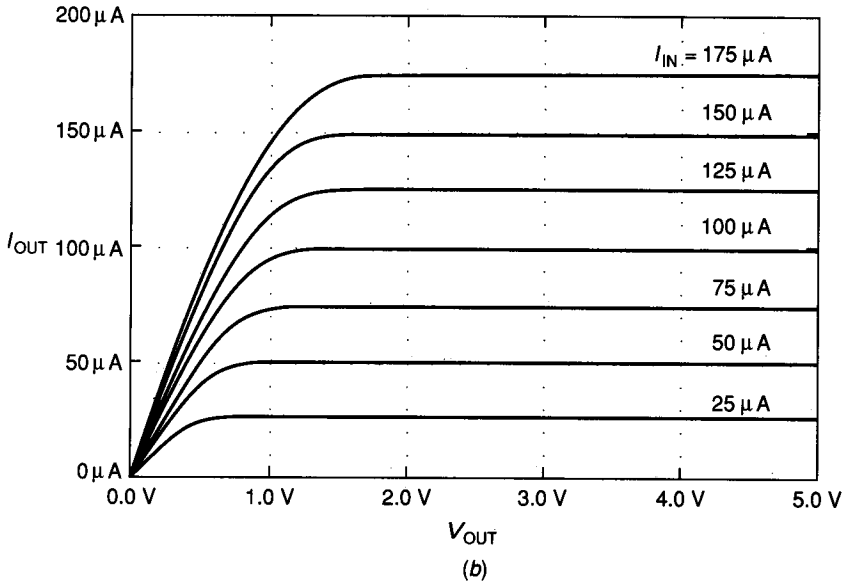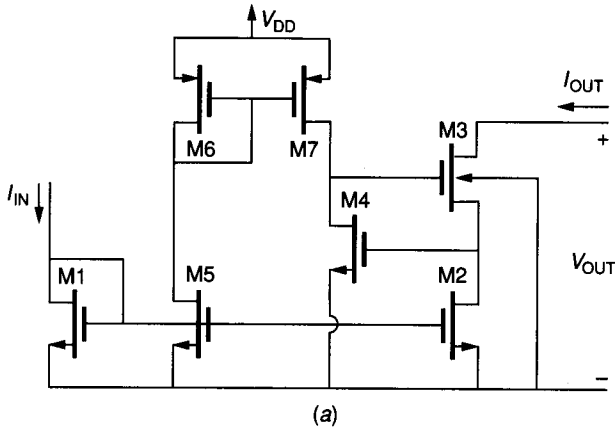

(a)

(b)

FIGURE 5.4-15
(a) MOS regulated cascode current mirror, (b) Simulated performance of a.

current sink of Fig. 5.3-16. The regulated cascode consists of M2, M3, and M4. M1 and M2 form a simple current mirror; however, because of M4, the value of V_{DS2} will not be much different than V_{DS1}, giving good accuracy. M5, M6, and M7 are used to provide a bias current for M4, which tracks the output current. If I_{D4} did not track I_{OUT} (I_{D3}), then the value of V_{GS2} would not be large enough at large values of I_{OUT} to keep M2 in saturation. If M2 is not in saturation, then the ratio of I_{D2} to I_{D1} will be smaller than what is expected. Figure 5.4-15b shows the simulated results for the regulated cascode current mirror of Fig. 5.4-15a when $W_1/L_1 = W_2/L_2 = W_3/L_3 = W_4/L_4 = W_5/L_5 = W_6/L_6 = 50\,\mu/10\,\mu$, $W_7/L_7 = 75\,\mu/10\,\mu$, and using the model parameters as before, with the addition of $K_P' = 8\,\mu\text{A/V}^2$, $V_{TP} = -0.75$ V, $\gamma_P = 0.4\,\text{V}^{-1/2}$, $\lambda_P = 0.02\,\text{V}^{-1}$, and $\phi = 0.6$ V. It is seen that V_{MIN} is almost identical to that of the simple MOS mirror of Fig. 5.4-11b. In addition, the output resistance is given by Eq. 5.3-20 and is much higher than any of the other MOS mirrors presented so far. Clearly, Fig. 5.4-15a is a superior MOS current mirror realization in many respects. If the ratio of I_{D5} to I_{D2} is decreased below the 0.5 of Fig. 5.4-15b, the value of V_{MIN} decreases, but the ratio of I_{OUT} to I_{IN} becomes nonlinear as the currents increase.

Table 5.4-2 summarizes the performance of the MOS current mirrors having unity gain from the viewpoint of accuracy (linearity), output resistance, and V_{MIN}. Additional considerations include the size of devices. More ratio accuracy will be obtained for larger size devices. All of the current mirrors presented in this section used npn BJTs or n-channel MOSFETs. Opposite-type current mirrors can be implemented using pnp BJTs or p-channel MOSFETs. The circuits perform in an identical manner. The parametric expressions for the small signal resistances are identical in either case.

The important principles developed and used in this section include the matching principle, the replication principle, and the method by which mismatches between similar devices can be calculated. These principles will be employed where appropriate in the material that follows. The circuits developed in this section will be very useful in designing more complex analog circuits. They will find use in dc biasing and as high-resistance ac loads.

TABLE 5.4-2
Comparison of MOS current mirror performance

MOS current mirror	Accuracy ($I_{D2} = I_{D1}$)	r_{out}	V_{MIN}
Simple Fig. 5.4-11a	Poor	$r_o = \dfrac{1}{\lambda I_{out}}$	$V_{DS}(\text{sat})$
Cascode Fig. 5.4-12a	Good	$g_m r_o^2$	$2V_{DS}(\text{sat})$
Wilson Fig. 5.4-14a	Good	$\dfrac{g_m r_o^2}{2}$	$V_{GS} + V_{DS}(\text{sat})$
Regulated cascode Fig. 5.4-15a	Good	$g_m^2 r_o^3$	$V_{DS}(\text{sat})$

5.5 VOLTAGE AND CURRENT REFERENCES

In Sec. 5.3, current sinks/sources were presented. These circuits can be used to create a voltage by applying the current to a resistor. Such circuits represent one method of achieving a dc voltage or current. However, many applications require a dc voltage or current that is more stable than the circuits of Sec. 5.3. Circuits that yield a precise dc voltage or current independent of external influences are called *voltage references* or *current references*. The primary external influences of concern are power supply and temperature variations. The objective of this section will be to demonstrate the principles of voltage and current references that minimize their dependence on power supply and temperature.

In order to characterize the dependence of a reference on power supply and temperature, the concepts of sensitivity and fractional temperature coefficient are introduced. Assume that the reference is a voltage designated as V_{REF}. The sensitivity of V_{REF} to changes in a power supply V_{XX} is given as

$$S_{V_{XX}}^{V_{REF}} = \lim_{\Delta V_{XX} \to 0} \frac{\Delta V_{REF}/V_{REF}}{\Delta V_{XX}/V_{XX}} = \frac{V_{XX}}{V_{REF}} \left(\frac{\partial V_{REF}}{\partial V_{XX}} \right) \tag{5.5-1}$$

Eq. 5.5-1 emphasizes how the sensitivity can be calculated. However, once the sensitivity is known, it can be applied using the following form.

$$\frac{\Delta V_{REF}}{V_{REF}} \simeq \left(S_{V_{XX}}^{V_{REF}} \right) \left(\frac{\Delta V_{XX}}{V_{XX}} \right) \tag{5.5-2}$$

Eq. 5.5-2 can be interpreted as follows: if the sensitivity of V_{REF} with respect to V_{XX} is unity then a 10% change in V_{XX} will cause a 10% change in V_{REF}. Obviously, if V_{REF} is to be independent of V_{XX}, then the sensitivity of V_{REF} with respect to V_{XX} should approach zero. Sensitivities less than 1/100 are practical values for a monolithic voltage reference. The above formulation is valid for current references by simply replacing V_{REF} by I_{REF}.

While the sensitivity measure given in Eq. 5.5-1 with V_{XX} replaced with the temperature (i.e. $S_T^{V_{REF}}$) could be used as a measure of the dependence of the reference on temperature, it is customary to use the concept of fractional temperature coefficient introduced in Eq. 2.2-5 of Chapter 2. The fractional temperature coefficient (TC$_F$) of V_{REF} is defined as

$$TC_F(V_{REF}) = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T} = \frac{1}{T} S_T^{V_{REF}} \tag{5.5-3}$$

where the relationship between the fractional temperature coefficient of V_{REF} and the sensitivity of V_{REF} to temperature (T) is also illustrated. The units of TC$_F$ are expressed in terms of parts per million per °C, or ppm/°C. Assuming that a sensitivity of V_{REF} with respect to temperature equal to 1/100 is indicative of a good voltage reference, then at room temperature $(T = 300°K)$ the fractional temperature coefficient is $(1/300) \times (1/100) \times 1,000,000 = 33.3$ ppm/°C. References with a TC$_F$ of less than 50 ppm/°C are considered to be stable with respect to temperature.

Figure 5.5-1 shows three simple voltage references which will be more useful for illustrating the analysis techniques than for implementing a good voltage reference. Figure 5.5-1*a* is simply a voltage divider providing a dc voltage between V_{XX} and ground. The value of dc voltage is

$$V_{REF} = V_{XX}\left(\frac{R_2}{R_1 + R_2}\right) \tag{5.5-4}$$

The sensitivity of V_{REF} with respect to V_{XX} is found to be

$$S_{V_{XX}}^{V_{REF}} = \frac{V_{XX}}{V_{REF}}\frac{\partial V_{REF}}{\partial V_{XX}} = 1 \tag{5.5-5}$$

The fractional temperature coefficient of this simple voltage reference is found after some algebraic manipulation to be

$$TC_F(V_{REF}) = \frac{1}{V_{REF}}\frac{\partial V_{REF}}{\partial T} = \left(\frac{R_1}{R_2}\frac{V_{REF}}{V_{XX}}\right)\left(\frac{\partial R_2}{R_2 \partial T} - \frac{\partial R_1}{R_1 \partial T}\right)$$

$$= \left(\frac{R_1}{R_2}\frac{V_{REF}}{V_{XX}}\right)[TC_F(R_2) - TC_F(R_1)] \tag{5.5-6}$$

where the resistors are assumed to be temperature-dependent and V_{XX} is temperature-independent. Equation 5.5-6 illustrates a very important property of temperature dependence. Note that if the fractional temperature coefficients of R_2, $TC_F(R_2)$, and of R_1, $TC_F(R_1)$, are equal then $TC_F(V_{REF})$ is zero. Thus, if both R_1 and R_2 are made from identical means, i.e., diffusion, polysilicon, etc., then temperature independence will be achieved. This result will hold true for ratios of similar components. It is easy to illustrate the principle from Eqs. 5.5-4 and

(a)   (b)   (c)
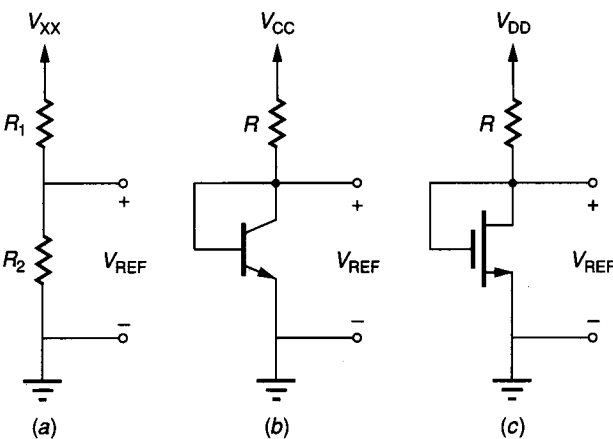
FIGURE 5.5-1
Simple voltage references: (*a*) Passive voltage divider, (*b*) BJT voltage reference and (*c*) MOS voltage reference.

5.5-6. If $TC_F(R_2)$ is equal to $TC_F(R_1)$, then the percentage changes are approximately equal. Suppose that $R_2 = 2\,\Omega$ and $R_1 = 1\,\Omega$. The value of V_{REF} is $V_{XX}/3$. If the temperature changes so that the resistors experience a 10% increase, they become $R_2' = 2.2\,\Omega$ and $R_1' = 1.1\,\Omega$. Substituting these values into Eq. 5.5-4 still gives V_{REF} of $V_{XX}/3$.

Figure 5.5-1b illustrates how a voltage reference can be achieved from a BJT and a resistor. The reference voltage can be found using the relationship for the collector current as a function of base–emitter voltage (Eq. 3.3-13 of Sec. 3.3). The result is

$$V_{REF} = V_t \ln \left(\frac{V_{CC} - V_{REF}}{R I_S} \right) \tag{5.5-7}$$

where V_t and I_S are parameters of the BJT defined in Chapter 3. Because V_{REF} is also inside the argument of the natural logarithm, an iterative solution is necessary to obtain V_{REF}. If V_{CC} is much greater than V_{REF}, then Eq. 5.5-7 simplifies to

$$V_{REF} \approx V_t \ln \left(\frac{V_{CC}}{R I_S} \right) \tag{5.5-8}$$

The sensitivity of V_{REF} with respect to V_{CC} can be found by differentiating either Eq. 5.5-7 or 5.5-8 and substituting into Eq. 5.5-1. Assuming that $V_{CC} \gg V_{REF}$ (see Prob. 5.34 when this is not true), the sensitivity of the circuit of Fig. 5.5-1b is

$$S_{V_{CC}}^{V_{REF}} \cong \frac{1}{\ln (V_{CC}/R I_S)} \tag{5.5-9}$$

If $V_{CC} = 5$ V, $R = 43\,k\Omega$ and $I_S = 0.4$ fA, the sensitivity of V_{REF} with respect to V_{CC} is 0.0379. If V_{CC} changes by 10%, V_{REF} will change by only 0.379%. Thus, a second principle emerges concerning low-sensitivity references. If two or more components which have different large signal voltage–current characteristics are used to divide voltage, it is possible to achieve sensitivities less than unity.

The temperature behavior of the circuit of Fig. 5.5-1b will be more complex than that of Fig. 5.5-1a because V_t, R, and I_S all vary with temperature. Differentiating Eq. 5.5-8 with respect to temperature yields

$$\frac{\partial V_{REF}}{\partial T} = \frac{V_{REF}}{T} - V_t \left(\frac{1}{I_S} \frac{\partial I_S}{\partial T} + \frac{1}{R} \frac{\partial R}{\partial T} \right) \tag{5.5-10}$$

Assuming that I_S is given as

$$I_S = K T^3 \exp \left(\frac{-V_{GO}}{V_t} \right) \tag{5.5-11}$$

where V_{GO} is the band gap voltage of silicon (1.205 V), which is temperature independent, allows the derivative of I_S with respect to temperature to be expressed as

$$\frac{\partial I_S}{\partial T} = \frac{3 I_S}{T} + \frac{I_S}{T} \frac{V_{GO}}{V_t} \tag{5.5-12}$$