5.5-6. If $TC_F(R_2)$ is equal to $TC_F(R_1)$, then the percentage changes are approximately equal. Suppose that $R_2 = 2\,\Omega$ and $R_1 = 1\,\Omega$. The value of V_{REF} is $V_{XX}/3$. If the temperature changes so that the resistors experience a 10% increase, they become $R_2' = 2.2\,\Omega$ and $R_1' = 1.1\,\Omega$. Substituting these values into Eq. 5.5-4 still gives V_{REF} of $V_{XX}/3$.

Figure 5.5-1*b* illustrates how a voltage reference can be achieved from a BJT and a resistor. The reference voltage can be found using the relationship for the collector current as a function of base–emitter voltage (Eq. 3.3-13 of Sec. 3.3). The result is

$$V_{REF} = V_t \ln\left(\frac{V_{CC} - V_{REF}}{RI_S}\right) \tag{5.5-7}$$

where V_t and I_S are parameters of the BJT defined in Chapter 3. Because V_{REF} is also inside the argument of the natural logarithm, an iterative solution is necessary to obtain V_{REF}. If V_{CC} is much greater than V_{REF}, then Eq. 5.5-7 simplifies to

$$V_{REF} \approx V_t \ln\left(\frac{V_{CC}}{RI_S}\right) \tag{5.5-8}$$

The sensitivity of V_{REF} with respect to V_{CC} can be found by differentiating either Eq. 5.5-7 or 5.5-8 and substituting into Eq. 5.5-1. Assuming that $V_{CC} >> V_{REF}$ (see Prob. 5.34 when this is not true), the sensitivity of the circuit of Fig. 5.5-1*b* is

$$S_{V_{CC}}^{V_{REF}} \cong \frac{1}{\ln(V_{CC}/RI_S)} \tag{5.5-9}$$

If $V_{CC} = 5$ V, $R = 43\,\text{k}\Omega$ and $I_S = 0.4$ fA, the sensitivity of V_{REF} with respect to V_{CC} is 0.0379. If V_{CC} changes by 10%, V_{REF} will change by only 0.379%. Thus, a second principle emerges concerning low-sensitivity references. If two or more components which have different large signal voltage–current characteristics are used to divide voltage, it is possible to achieve sensitivities less than unity.

The temperature behavior of the circuit of Fig. 5.5-1*b* will be more complex than that of Fig. 5.5-1*a* because V_t, R, and I_S all vary with temperature. Differentiating Eq. 5.5-8 with respect to temperature yields

$$\frac{\partial V_{REF}}{\partial T} = \frac{V_{REF}}{T} - V_t\left(\frac{1}{I_S}\frac{\partial I_S}{\partial T} + \frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-10}$$

Assuming that I_S is given as

$$I_S = KT^3 \exp\left(\frac{-V_{GO}}{V_t}\right) \tag{5.5-11}$$

where V_{GO} is the band gap voltage of silicon (1.205 V), which is temperature independent, allows the derivative of I_S with respect to temperature to be expressed as

$$\frac{\partial I_S}{\partial T} = \frac{3I_S}{T} + \frac{I_S}{T}\frac{V_{GO}}{V_t} \tag{5.5-12}$$

Substituting Eq. 5.5-12 into Eq. 5.5-10 and dividing by V_{REF} gives

$$TC_F(V_{REF}) = \frac{V_{REF} - 3V_t - V_{GO}}{V_{REF}T} - \frac{V_t}{V_{REF}}\left(\frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-13}$$

If $V_{REF} = 0.7$ V and the TC_F of R is 1500 ppm/°C, the $TC_F(V_{REF})$ of Fig. 5.5-1*b* at room temperature (300°K) is

$$TC_F(V_{REF}) = -2776 \text{ ppm/°C} - 56 \text{ ppm/°C} = -2832 \text{ ppm/°C} \tag{5.5-14}$$

It is seen that this voltage reference has a large temperature coefficient for a voltage reference.

Figure 5.5-1*c* shows how MOS technology can be used to implement a voltage reference similar to the simple BJT voltage reference of Fig. 5.5-1*b*. Since the drain and gate are physically connected, the device is in saturation for $V_{GS} \geq V_T$ and V_{REF} can be expressed as

$$V_{REF} = V_T + \sqrt{\frac{2(V_{DD} - V_{REF})}{RK'_N(W/L)}} \tag{5.5-15}$$

As before, an iterative method is used to solve for V_{REF}. If $V_{DD} = 10$ V, $V_T = 0.75$ V, $K'_N = 24\,\mu A/V^2$, $W/L = 10$, and $R = 100\,k\Omega$, then iterative methods give a V_{REF} of 1.972 V. If V_{DD} is greater than V_{REF}, then

$$V_{REF} \approx V_T + \sqrt{\frac{2V_{DD}}{RK'_N(W/L)}} \tag{5.5-16}$$

Using Eq. 5.5-16 with these parameters and values gives $V_{REF} = 2.085$. The sensitivity of the circuit of Fig. 5.5-1*c* with respect to V_{DD} can be found for the case where $V_{DD} >> V_{REF}$ as

$$S_{V_{DD}}^{V_{REF}} = \frac{0.5}{1 + V_T\sqrt{RK'_N W/2V_{DD}L}} \tag{5.5-17}$$

Using the above parameters and values gives a sensitivity of V_{REF} with respect to V_{DD} of 0.274. The sensitivity of the circuit of Fig. 5.5-1*c* is larger than the circuit of Fig. 5.5-1*b* because the power supply in the BJT case is in the argument of the logarithm, while in the MOS case it is within the argument of the square root. Since the logarithm is a weaker function than the square root, the sensitivity of the BJT voltage reference is smaller than the MOS voltage reference.

In order to analyze the temperature dependence, the temperature dependence of the MOS transistor must be characterized. The primary temperature-dependent parameters of the MOS device are K' (mobility) and V_T. Their temperature dependence will be modeled as

$$K'_N = K'_{NO}\left(\frac{T}{T_O}\right)^{1.5} \tag{5.5-18}$$

and

$$V_T = V_{TO} - \alpha(T - T_O) \tag{5.5-19}$$

where K'_{NO} and V_{TO} are the values of K'_N and V_T at T_O and α is approximately 2.3 mV/°C. Assuming R, K'_N, and V_T are temperature-dependent and differentiating Eqs. 5.5-16, 5.5-18, and 5.5-19 gives

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_T}{\partial T} - \frac{1}{2}\sqrt{\frac{2V_{DD}}{K'_N R(W/L)}}\left(\frac{1}{R}\frac{\partial R}{\partial T}\right) - \frac{1}{2}\sqrt{\frac{2V_{DD}}{K'_N R(W/L)}}\frac{1}{K'_N}\frac{\partial K'_N}{\partial T} \tag{5.5-20}$$

$$\frac{\partial K'_N}{\partial T} = -\frac{1.5}{T}K'_N \tag{5.5-21}$$

and

$$\frac{\partial V_T}{\partial T} = -\alpha \tag{5.5-22}$$

Substituting Eqs. 5.5-21 and 5.5-22 into Eq. 5.5-20 and dividing by V_{REF} gives

$$TC_F(V_{REF}) = \frac{-1}{V_{REF}}\left[\alpha + \frac{1}{2}\sqrt{\frac{2V_{DD}}{K'_N R(W/L)}}\left(\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1.5}{T}\right)\right] \tag{5.5-23}$$

Using the values above with $V_{REF} = 2.085$ V and assuming that $TC_F(R) = 1500$ ppm/°C, the fractional temperature coefficient becomes

$$TC_F(V_{REF}) = \frac{-1}{2.085}[0.0023 - 0.0016] = -336 \text{ ppm/°C} \tag{5.5-24}$$

While the $TC_F(V_{REF})$ of Fig. 5.5-1*c* is almost 10 times less than that of Fig. 5.5-1*b*, this is due to the selection of the resistor and the particular manner in which the temperature-dependent variables combine to give the overall temperature dependence.

The simple voltage references of Fig. 5.5-1 illustrate the methods by which more complex references can be characterized. The value of V_{REF} of Figs. 5.5-1*b* and 5.5-1*c* can be increased by cascading active devices or by the method illustrated in Fig. 5.5-2. It can be shown that the reference voltages of Fig. 5.5-2*a* and *b* are equal to $(1 + R_2/R_1)$ times the values given in Eqs. 5.5-8 and 5.5-16, respectively.

Current references are also of interest in this section. Figure 5.3-4*a* and Fig. 5.3-5*a* show examples of simple current references. However, one important aspect of these two current references is the implementation of V_{BB} and V_{GG}. In most cases V_{BB} and V_{GG} are implemented using the circuits of Figs. 5.5-1*b* and *c*, respectively. The result is shown in Fig. 5.5-3*a* and *b* and is in fact the simple current mirrors of Sec. 5.4, where I_{IN} is defined by the voltage across R. Using the relationships of the last section and assuming ideal current mirrors gives

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R} \tag{5.5-25}$$

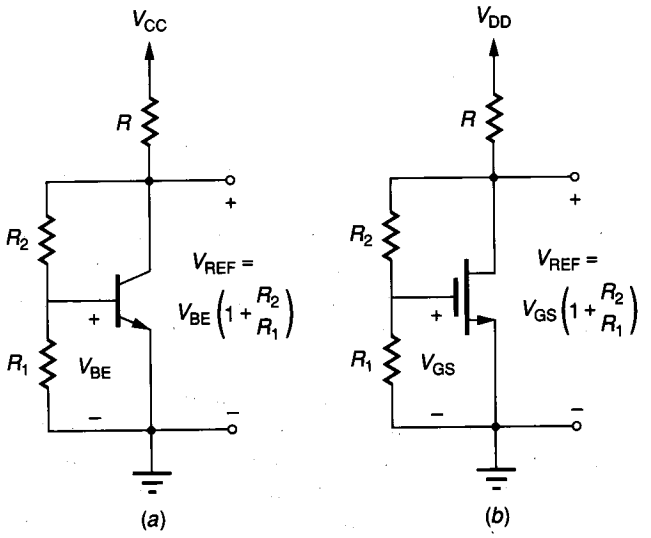

FIGURE 5.5-2
A method of increasing the value of V_{REF} for (*a*) Fig. 5.5-1*b*, (*b*) Fig. 5.5-1*c*.

and

$$I_{REF} = \frac{V_{DD} - V_{GS}}{R} \tag{5.5-26}$$

for Figs. 5.5-3*a* and 5.5-3*b*. It is obvious that the sensitivity of I_{REF} with respect to power supply is unity for both references if $V_{CC} >> V_{BE}$ or $V_{DD} >> V_{GS}$. The temperature coefficient of I_{REF} for Fig. 5.5-3*a* can be found by differentiating Eq. 5.5-25 with respect to temperature and dividing by I_{REF}. The result is

$$TC_F(I_{REF}) = \frac{-1}{I_{REF}}\left[\frac{\partial V_{BE}}{R\partial T} + I_{REF}\left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\right] \tag{5.5-27}$$

Using the previous results for $\partial V_{BE}/\partial T$ yields

$$TC_F(I_{REF}) \approx \frac{1}{I_{REF}}\left[\frac{V_{GO} + 3V_t - V_{BE}}{RT}\right] - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-28}$$

where it is assumed that V_t is much less than $V_{CC} - V_{BE}$. If $I_{REF} = 100\,\mu A$, then $V_{BE} = 0.682$ V for $I_S = 0.4$ fA. If $R = 43\,k\Omega (V_{CC} = 5\text{ V})$, $TC_F(R) = 1500$ ppm/°C and $T = 300$ K, then $TC_F(I_{REF})$ is equal to

$$TC_F(I_{REF}) = 466\text{ ppm/°C} - 1500\text{ ppm/°C} = -1034\text{ ppm/°C} \tag{5.5-29}$$

The current reference above has an additional term with an opposite sign in the expression for $TC_F(I_{REF})$, which suggests the possibility of achieving a zero value of $TC_F(I_{REF})$. Setting Eq. 5.5-28 to zero results in

$$I_{REF}R = V_{CC} - V_{BE} = \frac{V_{GO} + 3V_t - V_{BE}}{T(1/R)(\partial R/\partial T)} \tag{5.5-30}$$

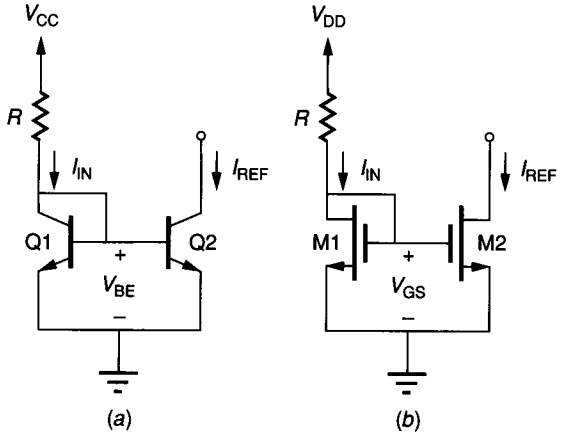

FIGURE 5.5-3
(*a*) A simple BJT current reference, (*b*) A simple MOS current reference.

Using the previous values, we can solve for the value of V_{CC} that will give a zero $TC_F(I_{REF})$. The result is $V_{CC} = 2.018$ V. To achieve $I_{REF} = 100\,\mu$A, R would have to be decreased to $(2.018 - 0.682)/100\,\mu\text{A} = 13.36\,\text{k}\Omega$, which would not change the zero value of $TC_F(I_{REF})$.

The fractional temperature coefficient of the MOS current reference of Fig. 5.5-3*b* is found by differentiating Eq. 5.5-26 with respect to temperature and dividing by I_{REF} to get the following

$$TC_F(I_{REF}) = \frac{-1}{I_{REF}}\left[\frac{\partial V_{GS}}{R\partial T} + \frac{I_{REF}}{R}\frac{\partial R}{\partial T}\right] \tag{5.5-31}$$

Using the results of Eqs. 5.5-20 through 5.5-23 in Eq. 5.5-31 gives

$$TC_F(I_{REF}) = \frac{1}{I_{REF}}\left[\frac{\alpha}{R} + \frac{1}{R}\sqrt{\frac{V_{DD}}{2K'_N R(W/L)}}\left(\frac{1}{R}\frac{\partial R}{\partial T} - \frac{3}{4T}\right)\right] - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-32}$$

Assuming that $I_{REF} = 100\,\mu$A, $K'_N = 24\,\mu\text{A/V}^2$, $V_{TN} = 0.75$ V, and $W/L = 10$ gives $V_{GS} = 1.663$ V. If $V_{DD} = 10$ V, then $R = 83.37\,\text{k}\Omega$. Finally if $\alpha = 2/3$ mV/°C and $TC_F(R) = 1500$ ppm/°C, the TC_F of the circuit of Fig. 5.5-3*b* is

$$TC_F(I_{REF}) = 216\,\text{ppm/°C} - 1500\,\text{ppm/°C} = -1284\,\text{ppm/°C} \tag{5.5-33}$$

Again, zero TC_F is possible. Setting Eq. 5.5-32 to zero and solving for $I_{REF}R$ gives

$$I_{REF}R = V_{DD} - V_{GS} = \frac{\alpha + \sqrt{(V_{DD}L)/(2K'_N RW)}[(1/R)(\partial R/\partial T) - (3/4T)]}{(1/R)(\partial R/\partial T)} \tag{5.5-34}$$

Using the above values in Eq. 5.5-34 gives a $V_{DD} = 2.863$ V for a zero $TC_F(I_{REF})$. This lower supply voltage causes R to become $28.63\,\text{k}\Omega$. The above analysis is only approximate since in calculating the temperature change of V_{GS}, Eq. 5.5-16 rather than Eq. 5.5-15 was used. The chapter problems deal with the exact case.

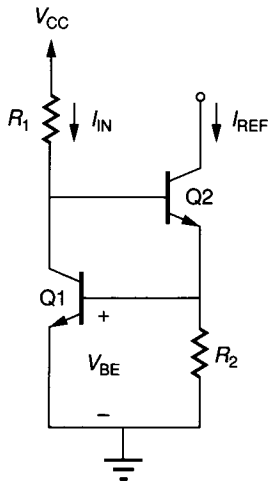

FIGURE 5.5-4
A method of obtaining a supply independent source by using V_{BE} to define the current.

So far, the references considered are not representative of stable voltage or current references. The remainder of the references presented will attempt to minimize the power supply dependence, the temperature dependence, or both. To achieve a reduction of the dependence of the current on the supply voltage, a technique of using the V_{BE} drop of a forward-biased pn junction is used. Such a circuit is shown in Fig. 5.5-4. Neglecting the base current, it follows from Eq. 3.3-10 that the reference current is expressed as

$$I_{REF} = \frac{V_{BE1}}{R_2} = \frac{V_t}{R_2} \ln\left(\frac{I_{IN}}{I_{S1}}\right) \tag{5.5-35}$$

It can be shown that

$$S_{V_{CC}}^{I_{REF}} \approx \frac{V_t}{I_{REF} R_2} \tag{5.5-36}$$

If $I_{IN} = 1$ mA, $I_{REF} = 100$ μA, and $I_{S1} = 0.4$fA, then from Eq. (5.5-35) $R_2 = 7.42$ kΩ. Therefore, the sensitivity of I_{REF} to V_{CC} is 0.035. Because the temperature performance of this current reference is not necessarily good and because the behavior is similar to that of Fig. 5.5-3*a*, it will not be pursued in further detail.

Another approach which uses the concept of generating the current from V_{BE} is shown in the bootstrap biasing circuit of Fig. 5.5-5*a*. The operating point of this circuit can be found by noting that if Q4 and Q5 are matched and if diode D1 is cutoff then these two devices form a simple unity gain current mirror. Neglecting base currents we obtain

$$I_{C1} = I_{C2} \tag{5.5-37}$$

and

$$V_{BE1} = V_t \ln (I_{C1}/I_{S1}) = I_{C2} R_1 \tag{5.5-38}$$

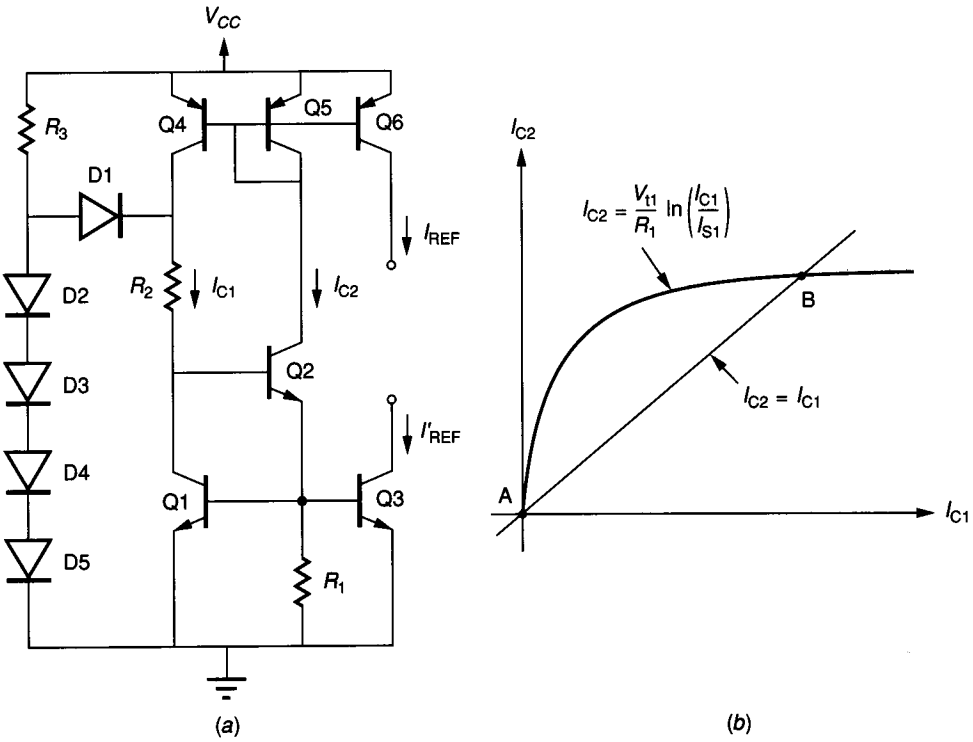

FIGURE 5.5-5
(*a*) A bootstrapped current source/sink, (*b*) Two possible operating points.

A closed form explicit expression for I_{C2} obtained by simultaneously solving Eqs. 5.5-37 and 5.5-38 in terms of basic functions does not exist. Plotting both Eqs. 5.5-37 and 5.5-38 on a curve of I_{C2} versus I_{C1} results in the curve of Fig. 5.5-5*b*. There are two operating points possible, designated as A and B. The operating point at A is undesirable since the value of $I_{C2}(I_{REF})$ is zero. Operation at the desired operating point, B, is determined by the start–up circuit consisting of R_3 and the five diodes. When V_{CC} is applied to the circuit, current flows through D_1 and R_2, forcing the circuit to the operating point at B. The value of $I_{C1}R_2$ is designed so that when the circuit is operating at B, D_1 is biased off disconnecting the start up circuit from the bootstrap current source/sink. Once the bootstrap current source/sink is operating at point B, the value of I_{REF} which is related to I_{C2} by the current mirror, Q5–Q6, should be independent of V_{CC}. I'_{REF} illustrates how a current sinking reference can be achieved.

The bootstrap current source can also be implemented in MOS technology as shown in Fig. 5.5-6*a*. The two equations corresponding to Eq. 5.5-37 and Eq. 5.5-38 are

$$I_{D1} = I_{D2} \tag{5.5-39}$$

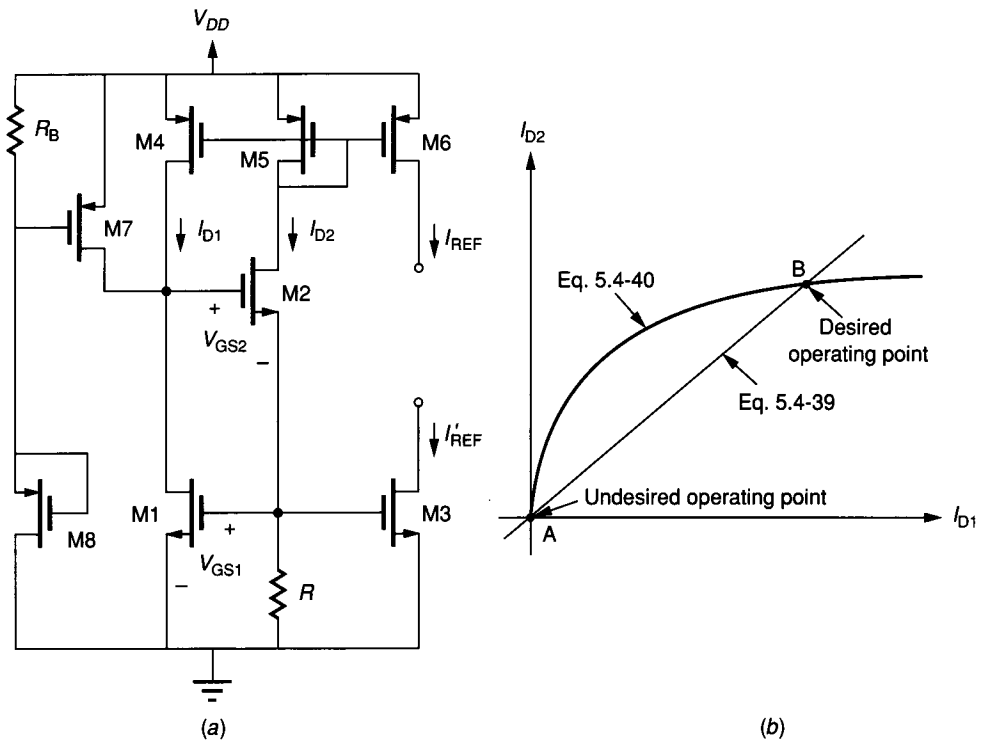

FIGURE 5.5-6
(*a*) A CMOS bootstrapped current source/sink, (*b*) Illustration of the two possible operating points.

and

$$I_{D2} = (V_{T1}/R) + \left[(2I_{D1}L_1/K'_N W_1)^{1/2}/R\right] \tag{5.5-40}$$

Plotting Eq. 5.5-39 and Eq. 5.5-40 results in the curves shown in Fig. 5.5-6*b* where again two operating points are possible. R_B, M7, and M8 are used to start up the circuit, causing it to operate at point B. The values of V_{GS2} and V_{GS1} are designed so that M7 will be cutoff if the bootstrap current source/sink is operating at point B.

Both the BJT and MOS bootstrapped current sources represent good references for independence of power supply. However, second-order effects must be taken into account to achieve a minimum dependence. These second-order effects include the errors in current mirrors (see Sec. 5.4). Without including the second-order effects such as current mirror matching, the lower limit of power supply sensitivity is about 0.01 with these circuits.

In most silicon technologies it is possible to obtain a breakdown diode from a pn junction that is heavily doped on one side of the junction. In a bipolar process, a breakdown diode can be obtained by reverse biasing the base–emitter junction. In a CMOS process, a low voltage breakdown diode results from the

overlap of the p^+ and n^+ diffusions. The I–V characteristic of a breakdown diode is shown in Fig. 5.5-7. When the voltage V exceeds the breakdown voltage, BV, the I–V characteristic becomes nearly vertical. The slope of the breakdown diode characteristic can be approximated in this region by $1/r_z$ where r_z is the ac impedance of the breakdown diode in the high-conductance region.

A power supply–independent voltage reference using the breakdown diode is shown in Fig. 5.5-8. The power supply sensitivity can be expressed as

$$S_{V_{CC}}^{V_{REF}} = \frac{V_{CC}}{V_{REF}} \frac{\partial V_{REF}}{\partial V_{CC}} = \left(\frac{V_{CC}}{BV}\right)\left(\frac{v_{ref}}{v_{cc}}\right) = \left(\frac{V_{CC}}{BV}\right)\left(\frac{r_z}{r_z + r_{out}}\right) \tag{5.5-41}$$

where v_{ref} and v_{cc} are the ac changes of V_{REF} and V_{CC} and r_{out} is the output resistance of the current source. If $BV = 6.5$ V, $V_{CC} = 10$ V, $r_z = 1000\ \Omega$ and $r_{out} = 100\ k\Omega$, the power supply sensitivity of Fig. 5.5-8 is 0.0065, which is the lowest power supply sensitivity of the circuits considered so far. It could be easily improved by using a current mirror having higher output resistance.

Unfortunately, the breakdown diode typically has a V_{REF} which is larger than 5 V. Such references can only be used with higher values of V_{DD} or V_{CC}.

The temperature coefficient of the breakdown diode depends on the doping levels and varies from negative values at low values of BV to positive values at higher values of BV. One must first measure the temperature coefficient before attempting to minimize the TC_F of the breakdown diode used as a voltage reference.

The TC_F of the MOS bootstrapped current source/sink of Fig. 5.5-6*a* can be found as

$$TC_F = \left(\frac{1}{V_{T1} + (I_{D1}L_1/K'_N W_1)^{1/2}}\right)\frac{\partial V_{T1}}{\partial T} - \frac{\partial R}{R\partial T} = \frac{1}{V_{GS1}}\frac{\partial V_{T1}}{\partial T} - \frac{\partial R}{R\partial T} \tag{5.5-42}$$

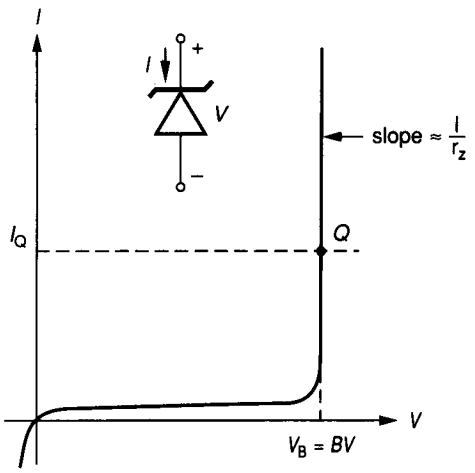

FIGURE 5.5-7
Current–voltage characteristics of a breakdown diode.

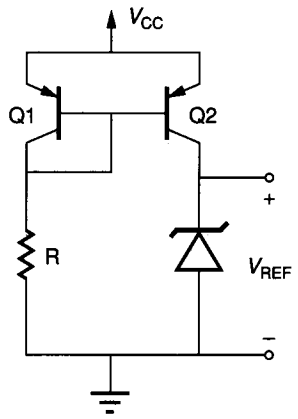

FIGURE 5.5-8
Power supply–independent voltage reference using the breakdown diode.

where we have assumed that I_{D1} and K_N' are independent of temperature. If I_{D2} has been designed such that $V_{GS1} = 1.5$ V and the value of the temperature coefficient of V_T is -0.18 mV/°C and the fractional temperature coefficient of R is $+1500$ ppm/°C (polysilicon), then the TC_F of the MOS bootstrapped current/sink is

$$TC_F = -110 \text{ ppm/°C} - 1500 \text{ ppm/°C} = -1610 \text{ ppm/°C}$$

It is interesting to note in this and previous references that R is the major contributor to temperature variation.

One approach to reducing the TC_F of current references is to try to use the opposite temperature coefficients of breakdown diodes and pn junction diodes (diode connected transistors) to cancel the dependence of the source upon temperature. Figure 5.5-9 shows a voltage reference that has the possibility of achieving this objective. It is assumed that I_o is sufficiently well-defined so that $V_B = BV$ can be assumed to be independent of V_{CC}. The reference voltage can be expressed as

$$V_{REF} = \left(\frac{R_2}{R_1 + R_2}\right) V_B - 2V_{BE}\left(\frac{R_2}{R_1 + R_2}\right) + V_{BE}\left(\frac{R_1}{R_1 + R_2}\right) \tag{5.5-43}$$

assuming all V_{BE} are equal and all diodes are matched.

If Eq. 5.5-43 is differentiated with respect to T and set equal to zero, we get

$$-\frac{\partial V_B/\partial T}{\partial V_{BE}/\partial T} = \frac{R_1}{R_2} - 2 \tag{5.5-44}$$

But if the temperature dependence of the breakdown diode is $+3$ mV/°C, then

$$\frac{\partial V_B/\partial T}{\partial V_{BE}/\partial T} \cong \frac{+3 \text{ mV/°C}}{-2 \text{ mV/°C}} \tag{5.5-45}$$

Therefore, the ratio of R_1/R_2 for zero temperature dependence is 3.5. The value of V_{REF} under this constraint is $(2/9)V_B$ or approximately 1.4 V. The voltage reference of Fig. 5.5-9 should also be relatively independent of V_{CC}.

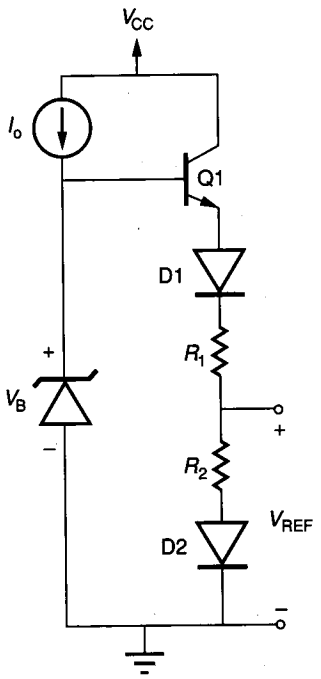

FIGURE 5.5-9
Use of cancellation between pn diode and breakdown diode temperature coefficients to obtain a temperature independent voltage reference.

One of the more popular and successful approaches to achieving a voltage reference, which is independent of both supply and temperature, is the *bandgap voltage reference*. The concept behind the bandgap voltage reference is illustrated in Fig. 5.5-10. A voltage V_{BE} is generated from a pn junction diode having a temperature coefficient of -2 mV/°C at room temperature. Also a voltage

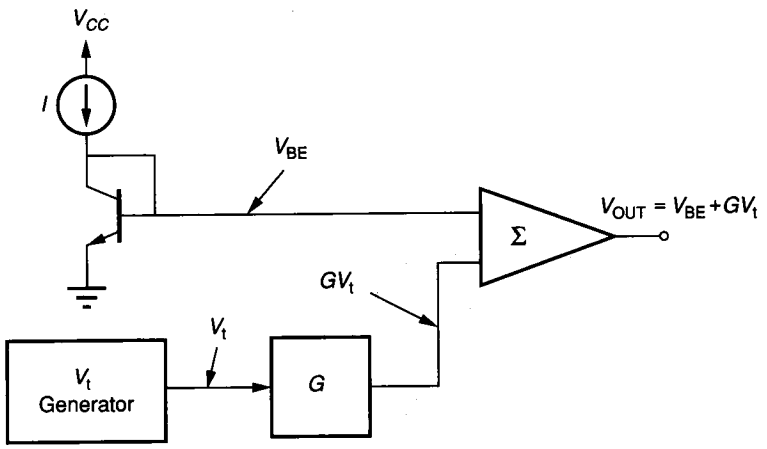

FIGURE 5.5-10
General concepts of a bandgap voltage reference.

$V_t(V_t = kT/q)$ is generated that has a temperature coefficient of $+0.085$ mV/°C at room temperature. If the V_t voltage is multiplied by a constant G and summed with the V_{BE} voltage, then the output voltage is given as

$$V_{REF} = V_{BE} + GV_t \tag{5.5-46}$$

On a first order basis, the value of G would be that which gives a zero value of temperature coefficient for V_{REF}. This value of G corresponds to 23.5 and produces a reference voltage of 1.26 V assuming V_{BE} is 0.65 V. A more detailed analysis is necessary to design the bandgap voltage reference so that zero temperature coefficient is achieved over a wide range of temperatures.[7]

A BJT version of the bandgap voltage reference is shown in Fig. 5.5-11. This voltage reference is called the Widlar bandgap reference.[8] As V_{CC} is increased from zero, Q1 and Q2 conduct when V_{BE1} is approximately 0.7 V. Since R_2 is greater than R_1, Q2 saturates. Further increase of V_1 (due to increasing V_{CC} during turn on) causes Q2 to come out of saturation due to R_3. The circuit stabilizes at $V_{BE3} = V_{BE}$ (on). Q1, Q2, and R_3 form a Widlar current mirror, as was discussed in Sec. 5.4. The current I_2 can be expressed as

$$I_2 = \frac{V_t}{R_3} \ln\left(\frac{I_1}{I_2}\right) \tag{5.5-47}$$

Equation 5.5-47 shows that the voltage V_t in Fig. 5.5-10 is generated by the difference between two base–emitter drops. The reference voltage of Fig. 5.5-11 can be given as

$$V_{REF} = V_{BE3} + \left(\frac{R_2}{R_3}\right) V_t \ln\left(\frac{I_1}{I_2}\right) \tag{5.5-48}$$

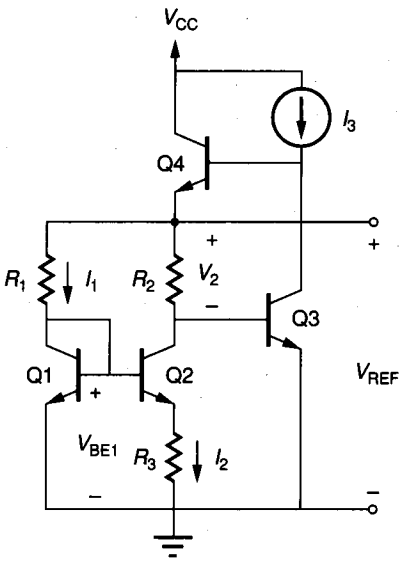

FIGURE 5.5-11
Widlar bandgap voltage reference.

Comparing (5.5-48) with (5.5-46) shows that

$$G = \left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) \tag{5.5-49}$$

If we assume that $I_1/I_2 = 10$, then at room temperature we must have $R_2/R_3 = 10.2$ to obtain a zero temperature coefficient. Selecting $I_1 = 1$ mA gives $I_2 = 0.1$ mA and R_3 is found from Eq. 5.5-47 as 60 Ω. Thus, R_2 is 610 Ω. If we assume that $V_{BE3} = 0.65$ V, then V_{REF} is equal to 1.26 V. Figure 5.5-12 shows that the bandgap reference possesses zero temperature coefficient only around a nominal temperature. Another problem with this circuit is the dependence of I_3 on the supply voltage. Better implementations of the bandgap reference are discussed below.

An improved bandgap voltage reference can be developed using an op amp, as shown in Fig. 5.5-13*a* and *b*. The advantage of the op amp is to remove the dependence of the currents upon the power supply. The method by which this is done is to force the relationship

$$I_1R_1 = I_2R_2 \tag{5.5-50}$$

and to replace I_1/I_2 in the argument of the logarithm by R_2/R_1 which is independent of supply voltage. The performance of both the circuits is identical and can be described as follows. The current I_2 is found by writing a voltage loop equation around V_{BE1}, V_{BE2} and R_3, resulting in

$$I_2 = \frac{1}{R_3} V_T \ln\left(\frac{R_2 I_{S2}}{R_1 I_{S1}}\right) \tag{5.5-51}$$

The reference voltage can be expressed as

$$V_{REF} = V_{BE1} + I_2R_2 = V_{BE1} + \frac{R_2}{R_3} V_t \ln\left(\frac{R_2 I_{S2}}{R_1 I_{S1}}\right) \tag{5.5-52}$$

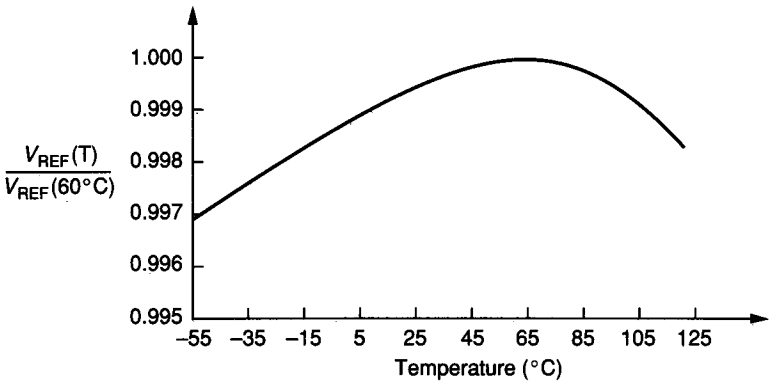

FIGURE 5.5-12
Illustration of the temperature dependence of the Widlar bandgap voltage reference.

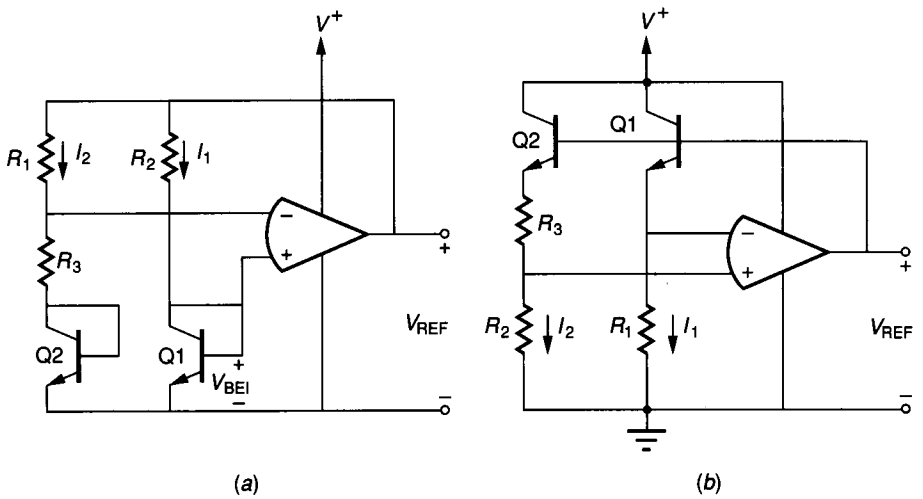

FIGURE 5.5-13
(*a*) A bandgap voltage reference using an op amp, (*b*) An alternate form of (*a*).

which is of the same form as the expression in Eq. 5.5-46. The areas of the emitters of transistors Q1 and Q2 are used to scale the argument of the logarithm. For example, if $A_{E2} = 10A_{E1}$, then $I_{S2} = 10I_{S1}$ and for zero temperature coefficient we find that $R_2/R_3 = 10.2$ if $R_2/R_1 = 1$.

The bandgap voltage reference of Fig. 5.5-10 can be implemented by either bipolar or CMOS technology. Q1 and Q2 would be the substrate transistors, which are available in CMOS technology. For p-well CMOS using an n^- substrate, the BJT is an npn substrate transistor and would be compatible with Fig. 5.5-13*b*. For an n-well CMOS technology using a p^- substrate, the circuit of Fig. 5.5-13*a* can be used if Q1 and Q2 are replaced by pnp transistors.

Exact cancellation of the dependence of V_{REF} upon temperature will not be possible because of component tolerances and second-order effects such as the nonlinearity of the dependence of V_{BE} on temperature[9] which has been neglected. Problem 5.41 shows that the influence of the op amp offset voltage is multiplied by $(1 + R_2/R_1)$ and can become a significant source of error and temperature dependence. Offset effects may be reduced by using multiple pn junctions or by offset canceling techniques.

Q1 and Q2 of Fig. 5.5-13 can be replaced by MOS devices operating in the weak inversion region if the current levels are small. Such voltage references use very little power. In the weak inversion region, the I–V characteristics of the MOS transistor are exponential and can be used to generate V_t. An equation describing the MOS transistor in weak inversion is given as (see (Eq. 3.1-32)[10]

$$I_D = \frac{W}{L} I_{DO} e^{-V_{BS}[(1/nV_t)-(1/V_t)]}(1 - e^{-V_{DS}/V_t})\, e^{(V_{GS}-V_T)/nV_t} \qquad (5.5\text{-}53)$$

where $V_t = kT/q$
n = slope factor
I_{DO} = characteristic current

Eq. 5.5-53 only holds for the weak inversion region where $V_{DS} > 3V_t$. It is found[11] that n is controllable but has a strong temperature dependence. I_{DO} is difficult to control and also has a strong temperature dependence. A voltage reference using the above concepts was proposed by Tsividis and Ulmer[12]. While the reference voltage of this circuit was independent of I_{DO}, it was dependent upon n, which prevented satisfactory reduction of the temperature coefficient. A CMOS bandgap voltage reference which eliminated the dependence on n is shown in Fig. 5.5-14. The current mirrors M1–M3 and M2–M4 form a closed loop with an initial loop gain greater than unity. Therefore, the current in both branches increases until equilibrium is achieved when the loop gain is reduced to one by the voltage V_{R1} across R_1. If we assume that M1 through M4 operate in the weak inversion region and that V_{DD} is high enough to ensure saturation of M1 and M4, then V_{R1} can be expressed as follows where $S = W/L$

$$V_{R1} = V_t \ln\left(\frac{S_1 S_4}{S_2 S_3}\right) \tag{5.5-54}$$

Note that V_{R1} depends only on the thermal voltage and the ratio of the geometry of the devices and is independent of n. I_{R1} and I_E are related as

$$\frac{I_{R1}}{I_E} = \frac{S_3}{S_6} \tag{5.5-55}$$

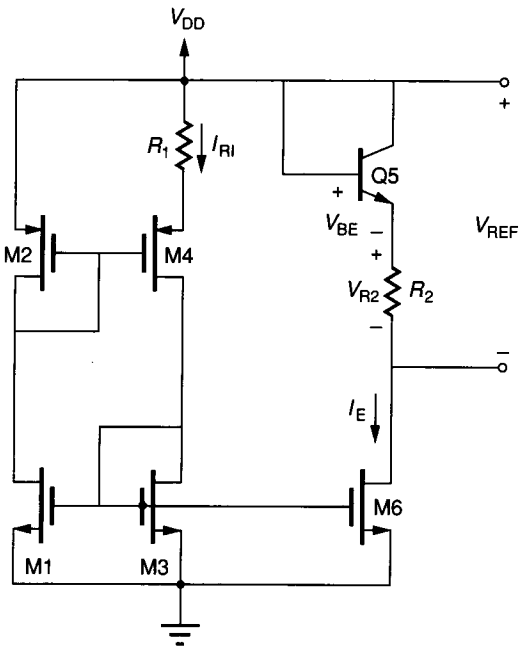

FIGURE 5.5-14
A CMOS bandgap voltage reference operating in weak inversion with no dependence on the process parameter n.

Solving for I_E gives

$$I_E = \left(\frac{S_6}{S_3}\right)\frac{V_t}{R_1}\ln\left(\frac{S_4S_1}{S_2S_3}\right) \tag{5.5-56}$$

V_{REF} is given as

$$V_{REF} = V_{BE} + I_E R_2 = V_{BE} + \left(\frac{R_2}{R_1}\right)\left(\frac{S_6}{S_3}\right)V_t \ln\left(\frac{S_1S_4}{S_2S_3}\right) \tag{5.5-57}$$

An expression for V_{BE} which emphasizes its temperature dependence is given by[13]

$$V_{BE}(T) = V_{GO}\left(1 - \frac{T}{T_o}\right) + V_{BEO}\left(\frac{T}{T_o}\right) + \frac{mkT}{q}\ln\left(\frac{T_o}{T}\right) \tag{5.5-58}$$

where V_{GO} = the extrapolated bandgap voltage of silicon
V_{BEO} = V_{BE} of a diode connected transistor at $T = T_o$
m = constant dependent on the diode fabrication and temperature characteristics

It can be shown that the condition for $dV_{REF}/dT = 0$ is given by

$$\left(\frac{R_2S_6}{R_1S_3}\right)\ln\left(\frac{S_1S_4}{S_2S_3}\right) = \frac{q(V_{GO} - V_{BEO})}{kT} + m \tag{5.5-59}$$

This results in a reference voltage of

$$V_{REF} = V_{GO} + \frac{mkT}{q} \tag{5.5-60}$$

In order to ensure proper operation of the voltage reference described, the following precautions must be taken. First, the devices must be in weak inversion even at the highest temperature of operation. Secondly, leakage currents particularly in the n-channel devices must be minimized to prevent these currents from becoming a major source of error at higher temperature. Lastly, the output resistance of the devices must be large enough to ensure proper operation of the devices as current mirrors. This can be accomplished by using long devices or by use of the various current mirrors presented earlier.

This section has introduced the techniques and methods used to design voltage and current references that minimize their dependence on power supply and/or temperature. There are other characteristics of references which are important but are beyond the scope of the treatment given in this section. One of these is the noise introduced by the reference. Noise can be reduced by minimizing the number of devices and using small values of resistance. If MOS devices are used, p-channel MOS devices generally have less noise and the noise is reduced if the area of the device is increased.

Another area that was not covered was the creation of a voltage reference from a current reference and vise versa. At least one resistor will be present in this conversion process and cause the TC_F to be different. These conversions are best accomplished by using an op amp as a current-to-voltage or voltage-to-current converter.

5.6 SUMMARY

Five categories of building blocks have been presented in this chapter. These categories include switches, active resistors, current sources and sinks, current mirrors/amplifiers, and voltage and current references. Figures 5.0-1 and 5.0-2 show how these basic building blocks can be used to design or build more complex circuits. This chapter has paved the way to combine these building blocks with others to be discussed in the next chapter to form analog circuits.

The material discussed in this chapter has provided the opportunity to describe and illustrate many important principles and concepts that can be used in other applications. The section on active resistors illustrated methods by which the drain current dependence on the drain–source and the bulk–source voltage can be minimized. The use of switches and capacitors to implement a resistor was presented. Both positive and negative feedback were used to increase the small signal output resistance of current sources and sinks. Negative series feedback was used to increase the resistance while positive feedback was used for bootstrapping a resistor, increasing its effective resistance. The principles of replication and analyzing mismatched devices were demonstrated in the section describing current mirrors/amplifiers.

Finally, the last section introduced techniques which reduced the influence of temperature and power supply variation on the value of a voltage or current reference. It was shown how the temperature dependence can be reduced to zero in some cases.

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PROBLEMS

Section 5.1

5.1. What causes the nonsymmetry between the first and third quadrants in Fig. 5.1-4 for the MOS switch?

5.2. Assume a switch is made from a MOS transistor with equal W and L. If the CMOS parameters in Table 3.1-2 are applicable to this transistor, what are the highest and lowest values of voltages that can exist on the source/drain when the bulk is at –5 V and the gate at 5 V and still keep the switch on and working properly? Define the switch as on when the switch large signal resistance is 20 kΩ or less.

5.3. Calculate R_{ON} for the transistor of Fig. 5.1-5 when $V_{GS} = 5V_T$ and $W = L$ for $V_{BS} = 0$ V, $V_{DS} \simeq 0$, and for $V_{BS} = 5$ V. Assume that $\gamma = 0.8\ V^{-0.5}$ and $\phi = 0.6$ V.

5.4. Find R_{ON} of an n-channel MOS switch if $V_D \approx V_S = 2$ V, $V_B = 0$ V and $V_G = 5$ V if $W = L$ and the n-channel parameters of Table 3.1-2 are applicable.

5.5. Calculate the voltage feedthrough from the clock of Fig. 5.1-13*a* to C_1 of Fig. 5.1-13*b* (*a*) if C_1 is 5 pF and (*b*) if C_1 is 1 pF and $C_{GD} = C_{GS} = 50$ fF.

5.6. Use the SPICE computer simulation program to plot the on resistance of the circuit of Fig. 5.1-15 if $W/L = 10$ for all transistors. Assume that $V_{DD} = 5$ V and that $\overline{\phi}$ is 0 V and ϕ is 5 V. Use the parameters of Table 3.1-2 and obtain a plot of R_{ON} as a function of the voltage at the switch terminals to ground from 0 to 5 V. Note that because the switch is on, that the terminal voltages should be approximately equal.

Section 5.2

5.7. Evaluate the ac and dc resistance of the circuit of Fig. 5.2-2*a* when $V = 2V_T$ using the model parameters of Table 3.1-2. Repeat for the circuit of Fig. 5.2-2*b*. Assume that the source and bulk are connected together.

5.8. Use the small signal model of Fig. 5.2-2*d* to rederive Eq. 5.2-5 and include the bulk effect assuming that V_{BS} is positive.

5.9. Evaluate the ac and dc resistance of the circuit of Fig. 5.2-3*a* when $V = 0.6$ V using the model parameters of $I_s = 0.4$ fA and $\beta_F = 100$ at room temperature.

5.10. Repeat Ex. 5.2-1 if V_{out} is to be -1 V.

5.11. Repeat Ex. 5.2-2 if the bulk–source voltages are not neglected using the bulk threshold parameter of Table 3.1-2.

5.12. If W/L of M1 and M2 of Fig. 5.2-6 is 5, find the value of V_C necessary to realize an ac resistance of 2000 Ω using the model parameters of Table 3.1-2. Compare your results with that of Fig. 5.2-8*a*.

5.13. If the difference between V_{C1} and V_{C2} can vary from 1 to 5 V and W/L can vary from 1 to 10, what range of ac resistance can the double-MOS resistor implementation of Fig. 5.2-9 realize?

5.14. Use the double-MOS ac resistor configuration of Fig. 5.2-9 to implement the voltage amplifier shown in Fig. P5.14. The op amp is an ideal, differential-in, differential-out op amp. Assume that $V_{C1} = 5$ V and $V_{C2} = 4$ V. Use the parameters of Table 3.1-2.

5.15. Use the approach illustrated in the text for the parallel switched capacitor of Fig. 5.2-11 to show that the equivalent resistance of the series–parallel switched capacitor resistor realization of Fig. 5.2-13 is given by Eq. 5.2-32.

5.16. Use the approach illustrated in the text for the parallel switched capacitor of Fig. 5.2-11 to show that the equivalent resistance of the bilinear switched capacitor resistor realization of Fig. 5.2-14 is given by Eq. 5.2-33.

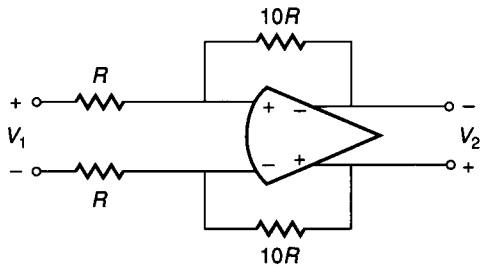

FIGURE P5.14

5.17. Figure P5.17 shows an inverting integrator. If R_1 is replaced by the series switched capacitor realization of Fig. 5.2-12, find an approximation expression for the transfer function, $V_2(s)/V_1(s)$. What is the accuracy of the integration constant $(1/R, C_2)$ in terms of the accuracy of the capacitors and the clock frequency?

Section 5.3

5.18. Assume that the model parameters of the npn transistor of Fig. 5.3-4*a* are $I_S = 0.4$ fA and $V_{AF} = 200$ V. Find the value of V_{BB} which will give a current sink of 500 μA. Using the values of Table 3.2-2, V_{MIN} and the value of the ac output resistance.

5.19. Use the model parameters of Table 3.1-2 for the MOS current sink of Fig. 5.3-5*a* to find V_{GG}, V_{MIN}, and R_o if the current is to be 500 μA.

5.20. Verify Eq. 5.3-8 for the MOS current sink of Fig. 5.3-7.

5.21. Verify Eqs. 5.3-15 and 5.3-16 for the bootstrapped current sink of Fig. 5.3-12.

5.22. Verify Eq. 5.3-19 for the output resistance of Fig. 5.3-15*a*.

5.23. Discuss a BJT realization of the regulated cascode MOS current sink of Fig. 5.3-16*a*. Give a schematic of a possible realization and find the output resistance and the minimum voltage drop across the current sink.

5.24. Verify Eq. 5.3-20 for the output resistance of Fig. 5.3-16*a*.

Section 5.4

5.25. Consider the circuit of Fig. 5.4-1 as a current amplifier. The input current will consist of a dc and an ac current. If the dc input current is 1 mA, find the ac input resistance, the ac output resistance, and the ac current gain (i_{out}/i_{in}) if $I_S = 0.4$ fA, $\beta_F = 100$, and $V_{AF} = 200$ V.

5.26. Find the ac input resistance of the circuit of Fig. 5.4-3 looking from R_1 toward the base of Q3 and collector of Q1. Compare this input resistance to that of the circuit of Fig. 5.4-1.

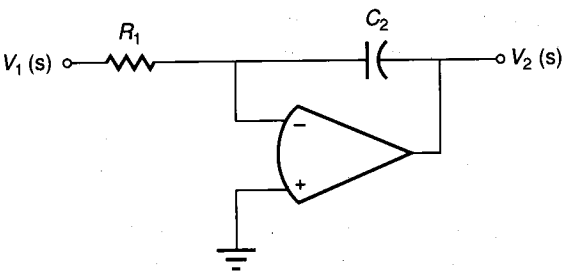

FIGURE P5.17

5.27. Verify Eqs. 5.4-33 and 5.4-34 of the BJT Wilson current mirror in Fig. 5.4-6.

5.28. Verify the ac output resistance of the BJT Widlar current mirror given in Eq. 5.4-41.

5.29. Assume that the output current is 0.5 mA for the BJT current mirrors listed in Table 5.4-1. Assume that the npn BJT parameters are $I_S = 0.4$ fA, $\beta_F = 100$, $V_{AF} = 200$ V, $V_{BE}(\text{sat}) = 0.7$ V and $V_{CE}(\text{sat}) = 0.2$ V. Find the value of r_{out} and V_{MIN} for each of the mirrors of Table 5.4-1.

5.30. Consider the circuit of Fig. 5.4-11*a* as a current amplifier. The input current will consist of a dc and an ac current. If the dc input current is 0.1 mA, find the ac input resistance, the ac output resistance, and the ac current gain (i_{out}/i_{in}) using the model parameters of Table 3.1-2 and assuming that both W/L values are equal.

5.31. Verify the ac output resistance of the MOS Wilson current mirror given in Eq. 5.4-63.

5.32. Develop a MOS realization of the BJT Widlar current mirror and find an expression for the output resistance and minimum voltage drop across the output of the mirror.

5.33. Assume that the output current is 0.2 mA for the MOS current mirrors listed in Table 5.4-2. Using the model parameters of Table 3.1-2 and assuming all W/L values are equal, find the value of r_{out} and V_{MIN} for each of the mirrors of Table 5.4-2.

Section 5.5

5.34. Redevelop Eq. 5.5-9 for the sensitivity of Fig. 5.5-1*b* when V_{CC} is not much greater than V_{REF}.

5.35. Use two collector–base connected BJTs in series in place of the single collector–base connected BJT in the circuit of Fig. 5.5-1*b* and find an expression for the sensitivity of V_{REF} with respect to V_{CC}.

5.36. If $V_{DD} = 10$ V, $W/L = 5$, and $R = 50$ kΩ, find the value of V_{REF} of the cirucit of Fig. 5.5-1*c*. Use the model parameters of Table 3.1-2. Assume that the TC_F of R is $+1000$ ppm/°C and find the TC_F of V_{REF}.

5.37. Assume for the circuit of Fig. 5.5-2*a* that $V_{CC} = 10$ V, $R_2 = 2R_1 = 2$ MΩ, $R = 100$ kΩ, and $I_S = 0.4$ fA. Assume also that $I_{R2} << I_C$ and find V_{REF}.

5.38. Repeat the development leading to Eq. 5.5-34 which gives the conditions for a zero TC_F using Eq. 5.5-15 rather than Eq. 5.5-16. Evaluate the value of V_{DD} for the conditions given in the text.

5.39. Assume that the voltage V_{GS} in Fig. P5.39 is independent of temperature. Develop an expression that will give the value of V_{GS} necessary to achieve a drain current,

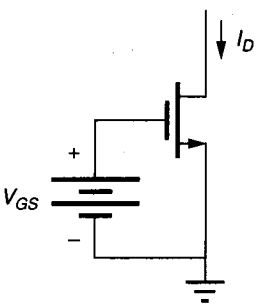

FIGURE P5.39

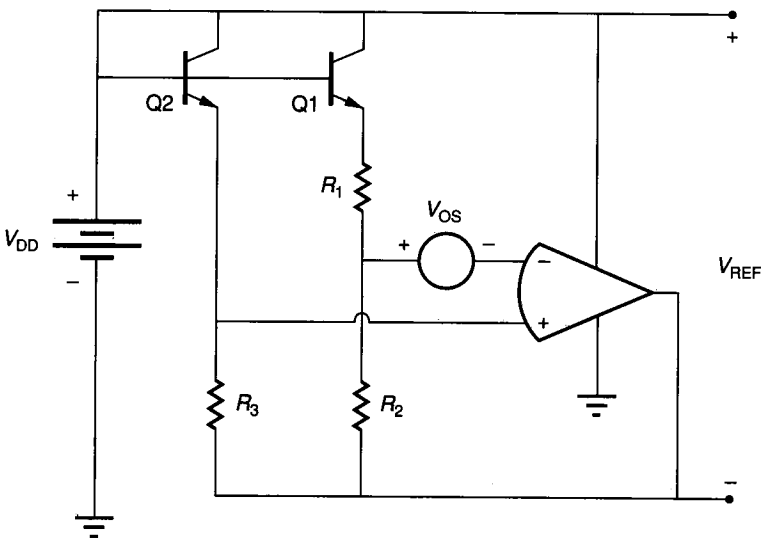

FIGURE P5.40

I_D, which will have zero temperature dependence. Assume that the temperature dependence of the MOS transistor is given by Eqs. 5.5-18 and 5.5-19. Find the value of V_{GS} and I_D which gives zero temperature dependence at (*a*) $T = 27°C$ and (*b*) $T = 200°C$.

5.40. For the bandgap voltage reference of Fig. P5.40, assume that the emitter area of Q1 is 10 times that of Q2, $V_{BE2} = 0.7$ V, $R_2 = R_3$, and $V_t = 0.026$ V. Find the value of R_2/R_1 necessary to give zero temperature coefficient at room temperature. For this problem assume $V_{OS} = 0$.

5.41. Develop an expression for V_{REF} for Fig. P5.40 if V_{OS} is not zero. Assume that R_2/R_1 is 10 and use the conditions of the previous problem to find V_{REF} if V_{OS} is 10 mV.

Design Problems

5.42. Design a switch using MOS technology which when closed will allow an uncharged 10 pF capacitor to be connected to a 5 V dc voltage source. The capacitor should reach 4.95 V within 10 ns. What is the value of the clock voltage which will meet this specification? Assume that the MOS technology to be used is defined by Table 3.1-2. Minimize the switch area in order to minimize the clock feedthrough.

5.43. Design a voltage divider which will provide 1 V dc from a 5 V dc voltage source. The temperature coefficient of the 1 V dc should not be larger than that of the 5 V dc voltage source. The sensitivity of the 1 V dc to changes in the 5 V dc supply should be less than 0.05. Keep the power dissipation of this voltage divider to less than 0.1 mW.

5.44. Design a current source having a value of 100 μA, output resistance of greater than 1 MΩ, and a minimum voltage of at most 1 V. Assume that ± 5 V power supplies are available. The design should be complete in the sense that when an external resistor is connected to it (the other end of the resistor is at -5 V) that 100 μA flows.

5.45. Use the current mirror concept to design a differential, current input amplifier which will provide an output current which is proportional to the difference between two input currents. Choose the gain control as 10 so that the expression

$$I_{out} = 10(I_1 - I_2)$$

is realized. The input resistances of this amplifier should be less than 1 kΩ and the output resistance should be greater than 1 MΩ. Assume that ±5 V power supplies are available.

5.46. Design a bandgap voltage reference using the form of Fig. 5.5-13*a* or 5.5-13*b*. Use this bandgap voltage reference to design a dc current reference which doesn't deteriorate the temperature characteristics of the bandgap voltage. Assume that ±5 V power supplies are available.