CHAPTER 6

AMPLIFIERS

6.0 INTRODUCTION

This chapter uses the building blocks of the last chapter to develop basic analog circuits and amplifiers. This material represents the middle step in the analog design hierarchy of Table 5.0-1. The primary focus of this chapter is the development of integrated circuit amplifiers using the building blocks of the last chapter. The concepts illustrated in Figs. 5.0-1 and 5.0-2 will be implemented in the following material.

The circuits included in this chapter are the inverting amplifier, the improved inverting amplifier, the differential amplifier, the output amplifier, the operational amplifier, and the comparator. The inverting amplifier, sometimes called an inverter, is one of the primary gain stages of analog amplifiers. The performance of the inverting amplifier can be improved as discussed in Sec. 6.2 by the use of additional devices. These additional devices typically appear in the cascode configuration, and are often termed *cascode amplifiers*. The improvements are not only in the area of performance, but also in the area of more degrees of design freedom.

Next in importance to the inverting amplifier is the differential amplifier. It is very useful as an input stage and is highly compatible with integrated circuit technology. The next one-stage amplifier to be considered is the output amplifier. This amplifier is necessary to interface the output of an amplifier to a low-resistance or low-capacitance load. Normally, amplifiers are incapable of driving a low-resistance/high-capacitance load. The output amplifier is difficult to design since it requires large, linear output swings across low resistive loads.

These amplifiers can be combined in the manner suggested by Figs. 5.0-1 and 5.0-2 to result in an operational amplifier. The operational amplifier is often considered the most useful circuit in analog integrated circuit design. It represents a good example in implementing circuit functions independent of its own performance characteristics using negative feedback. The last circuit presented in this chapter is the comparator. It is a circuit used to detect voltage thresholds and finds use in many analog and digital functions.

The emphasis of this chapter varies as the material progresses. The focus of the sections on inverting and differential amplifiers is on the small signal performance. This includes the ac gain, input and output resistances, bandwidth, and noise. These amplifiers are typically used as input or interstage amplifiers and do not have large signal swing requirements. The focus shifts to large signal considerations for output amplifiers. Here the key performance aspects include large signal swing, linearity, efficiency, and low output impedance. In operational amplifiers, the emphasis includes both small signal and large signal considerations. For the comparator, the focus is primarily on the large signal transient performance.

6.1 INVERTING AMPLIFIERS

One of the most useful amplifiers is the inverting amplifier, also called the inverter. As its name implies, the inverter produces an output that is inverted with respect to the input. If the input signal is changing in a positive (negative) manner, then the output will be changing in a negative (positive) manner. The inverter is widely used in both analog and digital circuits. In digital circuits, the inverter accomplishes the Boolean operation of negation or inversion. In analog circuits, the inverter is used to achieve amplification. Topologically, the simple analog and digital inverters are often identical. The use of the inverter in digital circuits will be described in more detail in Chapter 7. This section will examine the use of the inverter in analog circuits.

Coverage of the inverter naturally follows the material presented in the last chapter. Descriptions of the various forms of the inverter will use concepts from each section of Chapter 5, particularly the sections on active resistors and current sources/sinks. This section will be divided into three parts. The first part will present the general concepts of the inverter, independent of the technology used to implement it. The second part will examine inverters that use MOS technology. The last part will examine inverters using BJT technology.

The inverting amplifiers discussed in this section will be restricted to small signal, linear applications. Consequently, the emphasis will be on the fundamental concepts, the various inverter architectures, the small signal performance, and the noise performance. Large signal considerations, such as power dissipation, signal swing, nonlinearity and efficiency, will be emphasized in the section dealing with output amplifiers.

6.1.1 General Concepts of Inverting Amplifiers

The objective of the inverting amplifier used in analog circuits is to provide an inverting, small signal voltage gain greater than 1. One can appreciate the advantage of the inverting amplifier over a noninverting amplifier by noting that two cascaded inverters can implement a noninverting amplifier, but a noninverting amplifier cannot implement an inverting amplifier. Although inverting amplifiers are not restricted to voltage input and output variables, this form of the inverter will be considered here.

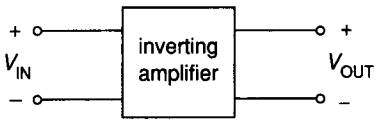

FIGURE 6.1-1
Two-port representation of an inverting voltage amplifier.

Figure 6.1-1 shows a two-port representation of the inverting voltage amplifier. The inverter can be characterized by the transfer characteristics defining the dependence of V_{OUT} on V_{IN}, the input resistance (R_{IN}), and the output resistance (R_{OUT}). In this section the characterization of the inverter is from the small signal viewpoint. Thus, an inverting voltage amplifier would be characterized by the small signal voltage gain, $v_{out}/v_{in} = A_v$, the small signal input resistance, r_{in}, and the small signal output resistance, r_{out}. It is necessary that the value of A_v should be negative and greater than unity. It is desirable but not necessary to have r_{in} large and r_{out} small.

The small signal performance of the inverter can be further characterized in the frequency or time domain. In the frequency domain, $A_v(\omega)$ of the ideal inverter should have a magnitude, A_{v0}, independent of frequency and a phase shift of $\pm 180°$. At some frequency, the magnitude of $A_v(\omega)$ of the practical inverter will decrease. The frequency at which the magnitude of $A_v(\omega)$ is equal to $A_{v0}/\sqrt{2}$ is called the -3 dB frequency ($\omega_{-3\text{ dB}}$). Although inverters built from discrete components may have a finite lower -3 dB frequency (due to coupling capacitors), the gain of integrated circuit inverters is A_{v0} for all frequencies sufficiently below $\omega_{-3\text{dB}}$. Thus the bandwidth of the inverter is equal to $\omega_{-3\text{dB}}$. It is important that the inverter have sufficient bandwidth for its given application.

The small signal frequency response can alternately be characterized by the small signal time domain response. For the case just discussed, the inverter acts as a low-pass amplifier with a cutoff frequency of $\omega_{-3\text{dB}}$. The pulse response of a first-order system would be characterized by a 10% to 90% rise time given approximately as $2.2/\omega_{-3\text{dB}}$. Another important aspect of the small signal performance of the inverter is noise. In many cases, the inverter is used as an input stage for a more complex amplifier. In order to reduce the noise of the complex amplifier, it is important to reduce the noise of the input stage.

In its most simple form, the inverting amplifier can be represented by two blocks. One of the blocks is a voltage-controlled current source, and the other is a load. It is important to recognize two types of voltage-controlled current sources. The distinction will be based on Fig. 5.3-2, which defined a current sink and a current source. In this case, the currents are controlled by the voltage at a third terminal. We shall define the blocks in Fig. 6.1-2 to schematically represent a voltage-controlled current sink and a voltage-controlled current source. V_P and V_N are defined as the most positive and negative dc voltages, respectively. The notation G will be used to designate a voltage-controlled current sink/source. The voltage-controlled current sinks/sources of Fig. 6.1-2 are three-terminal devices. The terminals are designated I for input, O for output, and X for the terminal common with V_N or V_P. The voltage between terminals I and X (X and I) controls the current at terminal O for Fig. 6.1-2*a* (Fig. 6.1-2*b*). In general, I_O for Fig. 6.1-2*a* can be expressed as

$$I_O = g_{sink}(V_{IX}, V_{OX}) \tag{6.1-1}$$

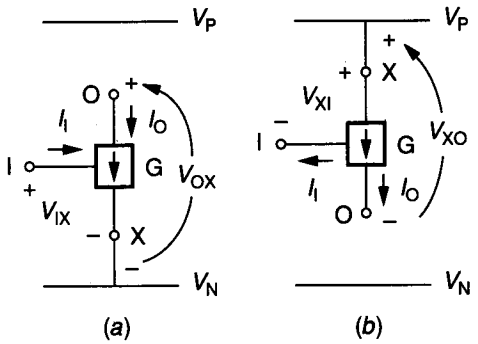

FIGURE 6.1-2
Schematic representations for (*a*) A voltage-controlled current sink and (*b*) A voltage-controlled current source.

and for Fig. 6.1-2*b* as

$$I_O = g_{source}(V_{XI}, V_{XO}) \tag{6.1-2}$$

The nonlinear functions in Eqs. 6.1-1 and 6.1-2 depend on the technology used to implement the controlled source/sink.

The voltage-controlled sources/sinks are combined with the two-terminal loads to implement the three basic types of inverter architectures shown in Fig. 6.1-3. Figure 6.1-3*a* illustrates an inverter using a voltage-controlled current sink and a load connected between O and V_P. This inverter is called a *sinking inverter* because it sinks the current through the load. Figure 6.1-3*b* uses a voltage-controlled current source and a load connected between O and V_N. This type

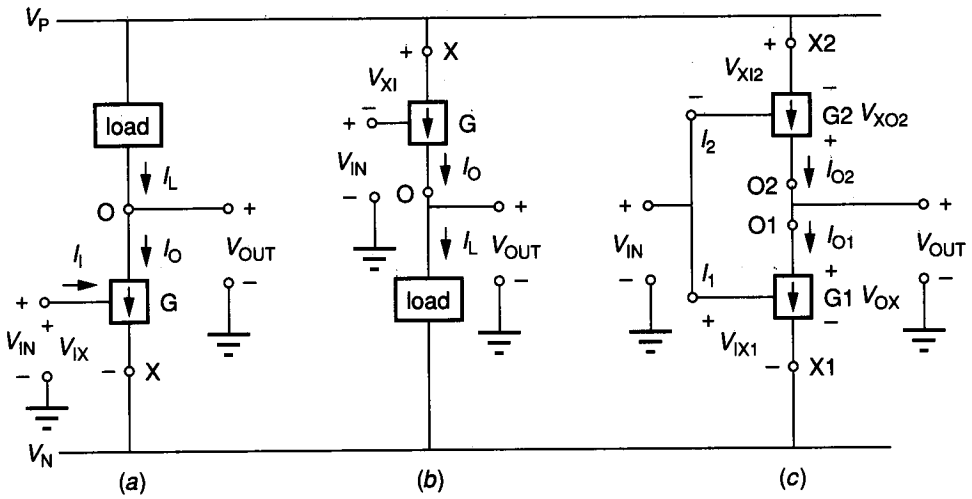

FIGURE 6.1-3
Generic representations of inverter architectures: (*a*) Sinking inverter, (*b*) Sourcing inverter, (*c*) Push-pull inverter.

of inverter is called a *sourcing inverter* because it sources the current in the load. The third architecture is shown in Fig. 6.1-3*c*. It uses a voltage-controlled current sink and a voltage-controlled current source. There is no external load in this architecture. This type of inverter is called a *push-pull inverter*. The loads in Fig. 6.1-3 can be any of the two-terminal active resistor realizations of Sec. 5.2 (Fig. 5.2-2, 5.2-3, or 5.2-6) or the dc current sources or sinks of Sec. 5.3. The use of dc current sources or sinks to realize the load will lead to high values of small signal voltage gain, A_v.

The large signal transfer behavior of the inverter can be intuitively developed. Consider the sinking inverter of Fig. 6.1-3*a*. Assume that V_{IN} is taken to V_N. With V_{IX} equal to zero, I_O will also be zero. We will call this the *off* state of the controlled sink. Because we are assuming that no external current flows, then I_L is also zero. When no current flows through the load, the voltage across it will be zero or close to zero. Therefore, V_{OUT} is approximately V_P. This corresponds to the upper left-hand corner of the plot of Fig. 6.1-4*a*. To simplify the analysis, we shall assume that the controlled sink turns on when $V_{IX} = V_{TH}$ ($V_{IN} = V_{TH} + V_N$). At this point the current I_O will start to flow. Because $I_O = I_L$, the voltage across the load starts to increase, causing V_{OUT} to decrease. As V_{IN} continues to increase, the voltage drop across the load approaches $V_P - V_N$, which implies that V_{OUT} approaches V_N. Under this condition, the controlled sink reaches a state where the current can no longer increase and the voltage V_{OX} is approximately zero. We will call this the *on* state of the controlled sink. The region between the off and on states will be called the *transition region*. The transfer curve in Fig. 6.1-4*a* is arbitrary because we have not used the actual relationships expressed by Eq. 6.1-1 for the controlled sink. It should be noted that the curve does not necessarily go through the origin, as implied in Fig. 6.1-4*a*.

Identical considerations hold for the sourcing inverter of Fig. 6.1-3*b*. In this case, when V_{IN} is at V_N, the controlled source is in the on state, where V_{XO} is approximately zero and the current through the load is limited. Therefore, V_{OUT} is approximately equal to V_P. At some point as V_{IN} is increased, the voltage V_{XO} will start to increase, causing V_{OUT} to decrease. When V_{XI} is equal to V_{TH} ($V_{IN} = V_P - V_{TH}$), I_O is zero and the voltage across the load is zero, causing V_{OUT} to be approximately V_N. The region between the on and off states of the controlled source is, again, the transition region. As with Fig. 6.1-4*a*, the transfer curve in the transition region is arbitrary because the exact relationship of Eq. 6.1-2 is not known. Again, the curve does not necessarily go through the origin as implied by Fig. 6.1-4b.

The general transfer curve for the push-pull inverter of Fig. 6.1-3*c* can be determined in a similar manner. It will be helpful to assume that a load resistor of large value is connected from the output to ground. When V_{IN} is at V_N, G1 is off and G2 is on. Because I_{O1} is zero, I_{O2} flowing through the load resistor will cause V_{OUT} to be at V_P. As V_{IN} increases from its value of V_N, V_{IX1} will equal V_{TH1} ($V_{IN} = V_N + V_{TH1}$) and the current I_{O1} begins to flow, causing the current in the load resistor to decrease and resulting in a decrease in V_{OUT}. At some point in the further increase of V_{IN}, $I_{O2} = I_{O1}$ and V_{OUT} is

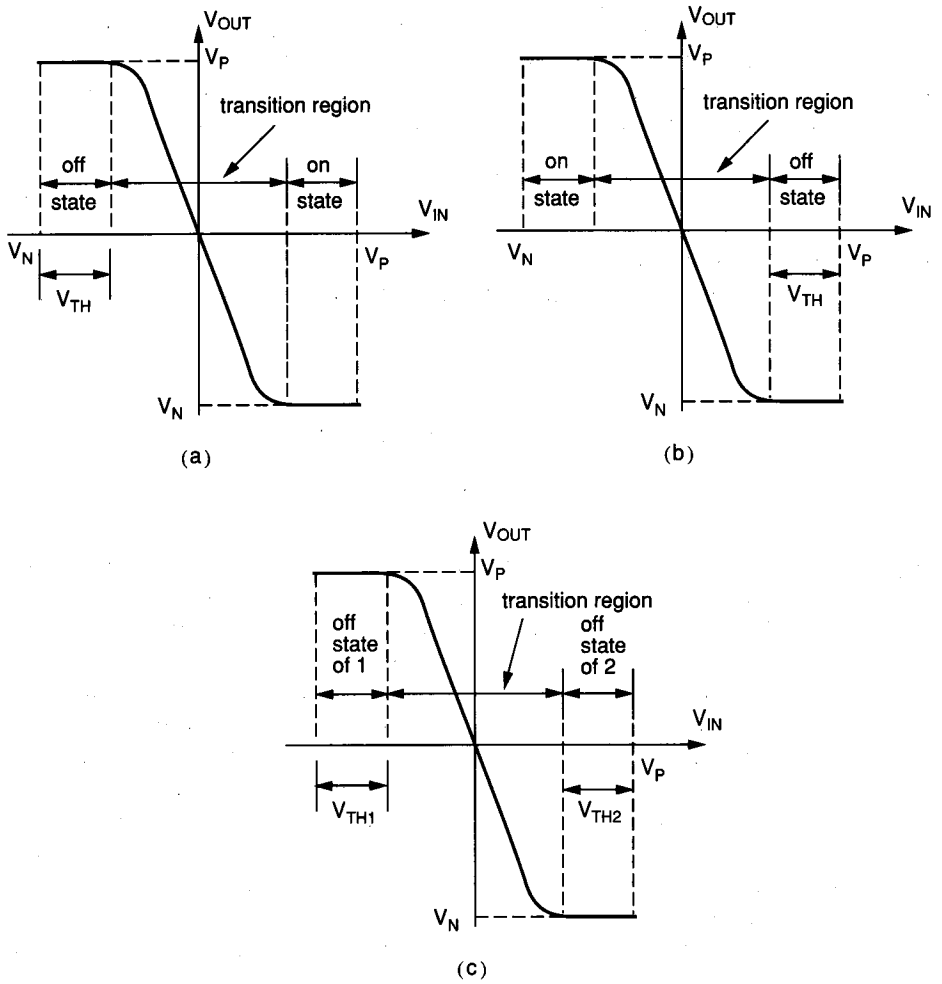

FIGURE 6.1-4
Typical voltage transfer functions for the inverters of Fig. 6.1-3: (*a*) Sinking inverter, (*b*) Sourcing inverter, (*c*) Push-pull inverter.

zero. Further increasing V_{IN} causes $I_{O1} > I_{O2}$, and V_{OUT} becomes negative and approaches V_N. When $V_{XI2} = V_{TH2}(V_{IN} = V_P - V_{TH2})$, G2 turns off and V_{OUT} is at V_N. The external load resistance used for this analysis turns out to be the output resistances associated with the controlled current sinks/sources. V_{OUT} is not necessarily zero at $V_{IN} = 0$ as implied by Fig. 6.1-4c.

The small signal voltage gain of the inverter can be related to the voltage transfer characteristics of Fig. 6.1-4 by the following definition.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\partial V_{OUT}}{\partial V_{IN}}\bigg|_{Q\text{-point}} \tag{6.1-3}$$

where the Q-point refers to a given value of the input or output voltage. Therefore, we see that the slope of the voltage transfer function of the inverter determines its gain. Obviously, the desired Q-point for a high-gain inverting amplifier is in the transition regions of Fig. 6.1-4, where the slope is the steepest. This will simplify our considerations because we can ignore the regions of operation outside of the transition region. This represents a major distinction between digital and analog circuits. In digital applications, the inverter will be operated from one extreme to the other. The two quiescent operating states of digital circuits will be in the flat portions of the voltage transfer curves of Fig. 6.1-4.

When the inverting amplifier is biased at a Q-point in the transition region, the next step is to linearize the circuit. This is done by expanding Eqs. 6.1-1 and 6.1-2 about a Q-point. While the formal mathematical characterization uses a multivariable series expansion, we shall approximate the result with only the first-order terms. Consider the approximation of Eq. 6.1-1, given as

$$I_O = g_{sink}(V_{IX}, V_{OX}) \approx I_o + \left.\frac{\partial I_O}{\partial V_{IX}}\right|_Q \Delta V_{IX} + \left.\frac{\partial I_O}{\partial V_{OX}}\right|_Q \Delta V_{OX} \quad (6.1\text{-}4)$$

where Q indicates operation at the dc bias point. Noting that the ac output current, i_o, is defined as $I_O - I_o$ allows us to express Eq. 6.1-4 as

$$i_o = I_O - I_o = \left.\frac{\partial I_O}{\partial V_{IX}}\right|_Q \Delta V_{IX} + \left.\frac{\partial I_O}{\partial V_{OX}}\right|_Q \Delta V_{OX} \approx g_m v_{ix} + g_o v_{ox} \quad (6.1\text{-}5)$$

where the signal swings are small enough so that the ac voltages v_{ix} and v_{ox} can be closely approximated by ΔV_{IX} and ΔV_{OX}, respectively. The notations g_m and g followed by other subscripts are used to relate the current dependence on a voltage at different terminals and voltage at the same terminals, respectively. g_m is called *transconductance* and g is called *conductance*. In a similar manner, the ac current of the voltage-controlled current source of Eq. 6.1-2 can be expressed as

$$i_o \approx g_m v_{xi} + g_o v_{xo} \quad (6.1\text{-}6)$$

In some of the practical voltage-controlled current sinks/sources, there may be an input current caused by the controlling voltage. This leads to two more expressions necessary to characterize the voltage-controlled current sink/source in addition to Eqs. 6.1-1 and 6.1-2. These general expressions are

$$I_I = g'_{sink}(V_{IX}) \quad (6.1\text{-}7)$$

and

$$I_I = g'_{source}(V_{XI}) \quad (6.1\text{-}8)$$

Repeating the considerations of Eqs. 6.1-1 and 6.1-2 for Eqs. 6.1-7 and 6.1-8 results in the following relationship for the voltage-controlled current sink:

$$i_i \approx g_i v_{ix} \quad (6.1\text{-}9)$$

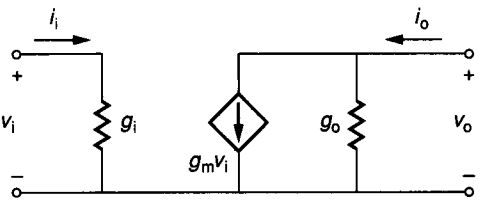

FIGURE 6.1-5
Small signal model for a voltage-controlled current sink/source.

and for the voltage-controlled current source:

$$i_i \approx g_i v_{xi} \tag{6.1-10}$$

g_i is called the input conductance and denotes the change of the input current due to a change in the input voltage.

Both Eqs. 6.1-5 and 6.1-9 or 6.1-6 and 6.1-10 can be modeled schematically as illustrated in Fig. 6.1-5. The small signal model for the voltage-controlled current sink and voltage-controlled current source are identical because small ac changes are insensitive to dc polarities. An ac model for the inverters of Fig. 6.1-3*a* and *b* can thus be obtained by adding the resistance (r_l) or a conductance (g_l) in parallel with the output of the circuit of Fig. 6.1-5, resulting in the complete model shown in Fig. 6.1-6. The value r_l was typically designated as r_o for the loads discussed in Chapter 5. Alternately, r_l could be derived by a development similar to that used in obtaining Eqs. 6.1-7 through 6.1-10.

The small signal ac performance of the sinking and sourcing inverters can be easily analyzed from the circuit of Fig. 6.1-6. It can be seen that the ac gain, the input resistance, and the output resistance are as follows.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m}{g_o + g_l} = -g_m r_{out} \tag{6.1-11}$$

$$r_{in} = r_i = \frac{1}{g_i} \tag{6.1-12}$$

and

$$r_{out} = \frac{r_o r_l}{r_o + r_l} = \frac{1}{g_o + g_l} \tag{6.1-13}$$

The small signal model for the push-pull inverter is obtained by connecting two of the models in Fig. 6.1-5 in parallel, resulting in the model of Fig. 6.1-7.

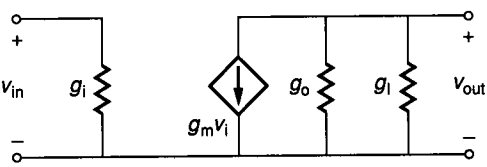

FIGURE 6.1-6
Small signal model for the inverters of Fig. 6.1-3*a* and *b*.

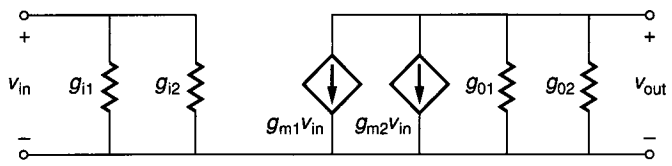

FIGURE 6.1-7
Small signal model for the push-pull inverter of Fig. 6.1-3*c*.

In this case, the ac gain, the input resistance, and the output resistance are given as follows.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{o1} + g_{o2}} = -(g_{m1} + g_{m2})r_{out} \tag{6.1-14}$$

$$r_{in} = \frac{r_{i1}r_{i2}}{r_{i1} + r_{i2}} = \frac{1}{g_{i1} + g_{i2}} \tag{6.1-15}$$

and

$$r_{out} = \frac{r_{o1}r_{o2}}{r_{o1} + r_{o2}} = \frac{1}{g_{o1} + g_{o2}} \tag{6.1-16}$$

Except for the sum of the transconductances in the numerator of A_v and the paralleling of the input resistances, the ac model for the push-pull inverter is similar to the ac model for the sinking and sourcing inverters.

In order to consider the frequency response, it is necessary to introduce parasitic capacitances into the ac models of Figs. 6.1-6 and 6.1-7. As was discussed in Chapter 3, parasitic capacitances are always present in any device and are due to actual capacitance or to the finite time required for carriers to move from one point to another. Figure 6.1-8 shows a model that is suitable for the ac frequency analysis of all three inverter architectures. r_1 is equal to r_{in}, r_2 is equal to r_{out}, and g_m is equal to g_{m1} or g_{m2} for the sinking or sourcing inverters and to $g_{m1} + g_{m2}$ for the push-pull inverter. C_1 and C_2 represent all parasitic capacitors associated with the input and output nodes, respectively. C_3 represents all capacitors connected between the input and output. Depending upon

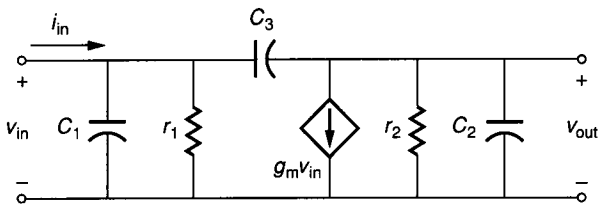

FIGURE 6.1-8
Small signal model including capacitances for the three inverter architectures of Fig. 6.1-3.

the technology used to implement the inverters, these capacitors could have values ranging from 5 fF to 5 pF.

We will consider the frequency response of Fig. 6.1-8 for two cases. The first is when the input source is a voltage, v_{in}, and the second is when the input source is a current, i_{in}. If the input source is a voltage, then the currents can be summed at the output node to give

$$V_{out}(s)(g_2 + sC_2) + sC_3[V_{out}(s) - V_{in}(s)] + g_m V_{in}(s) = 0 \tag{6.1-17}$$

In Eq. 6.1-17, s is the complex frequency variable. Solving for the complex frequency transfer function $V_{out}(s)/V_{in}(s)$ gives

$$A_v(s) = \frac{-g_m[1 - s(C_3/g_m)]}{g_2\{1 + s[(C_2 + C_3)/g_2]\}} = A_{v0}\frac{(1 - s/z_1)}{(1 + s/p_1)} \tag{6.1-18}$$

where the midband gain, A_{v0}, the zero, z_1, and the pole, p_1, are given as

$$A_{v0} = \frac{-g_m}{g_2} \tag{6.1-19}$$

$$z_1 = \frac{g_m}{C_3} \tag{6.1-20}$$

and

$$p_1 = \frac{-g_2}{C_2 + C_3} \tag{6.1-21}$$

It is seen that the voltage-driven inverter has a first-order transfer function with a midband voltage gain corresponding to the ac voltage gains of Eq. 6.1-11 or 6.1-14, a zero in the right-half complex frequency plane, and a pole in the left-half complex frequency plane. Generally, the value of g_m is much greater than g_2 so that the zero has little influence upon the frequency response. In this case, the ω_{-3dB} frequency would be given as

$$\omega_{-3dB} = \frac{g_2}{C_2 + C_3} \tag{6.1-22}$$

In some technologies, the value of g_m may not be sufficiently greater than g_2 so that the zero must be considered. The influence of the right-half plane zero has two important effects. The most obvious effect is to boost the magnitude of the frequency response. The less obvious effect is to cause a phase *lag* similar to a pole. If negative feedback is placed around such an inverter, it will have very poor stability characteristics. A typical frequency response for a voltage-driven inverter is shown in Fig. 6.1-9.

If the inverter of Fig. 6.1-8 is current-driven, then an equation in addition to Eq. 6.1-17 is required. This equation is found by summing currents at the input node and is given as

$$I_{in} = -(g_1 + sC_1)V_{in}(s) + sC_3[V_{in}(s) - V_{out}(s)] \tag{6.1-23}$$

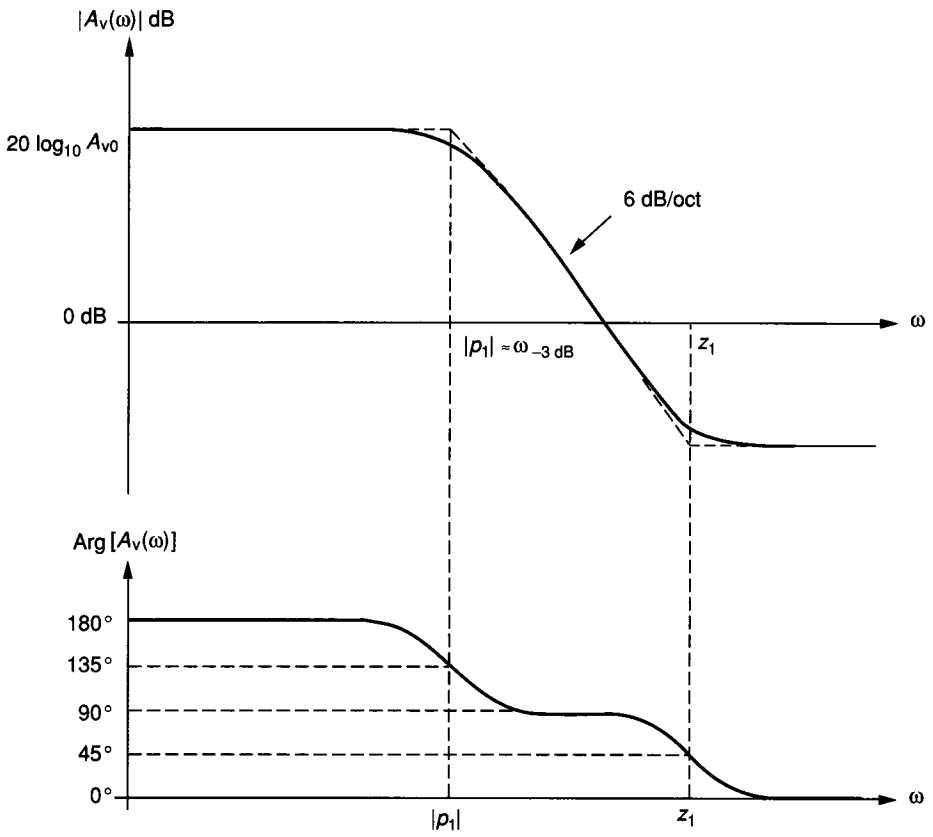

FIGURE 6.1-9
Typical frequency response for a voltage-driven inverter.

Simultaneously solving Eqs. 6.1-17 and 6.1-23 for the transfer function $V_{out}(s)/I_{in}(s)$ results in the following.

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{-g_m[1 - s(C_3/g_m)]}{g_1g_2 + s[g_1(C_2 + C_3) + g_2(C_1 + C_3) + g_mC_3] + s^2(C_1C_2 + C_1C_3 + C_2C_3)} \tag{6.1-24}$$

Equation 6.1-24 can be rewritten as

$$\frac{V_{out}(s)}{I_{in}(s)} = \left(\frac{-g_m}{g_1g_2}\right)[1 - s(C_3/g_m)] \Big/ \{1 + s[(C_2 + C_3)/g_2 + (C_1 + C_3)/g_1 + (g_mC_3)/(g_1g_2)] + s^2(C_1C_2 + C_1C_3 + C_2C_3)/(g_1g_2)\} \tag{6.1-25}$$

The frequency response of the current-driven inverter is seen to have two poles, p_1 and p_2. In most inverters, the magnitude of one of the poles is much

less than the magnitude of the other; in other words, $|p_2| \ll |p_1|$. In this case, we are able to find the pole locations in terms of the model parameters by the following method. Assume that the denominator of Eq. 6.1-25, $D(s)$, can be written as

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{6.1-26}$$

where $|p_1| >> |p_2|$. Equating the denominator of Eq. 6.1-25 to Eq. 6.1-26 results in the approximate pole locations expressed as

$$p_1 = -\left(\frac{C_2 + C_3}{g_1} + \frac{C_1 + C_3}{g_2} + \frac{g_m C_3}{g_1 g_2}\right)^{-1} \approx -\frac{g_1 g_2}{g_m C_3} \tag{6.1-27}$$

and

$$p_2 = \frac{-g_m C_3}{C_1 C_2 + C_1 C_3 + C_2 C_3} \tag{6.1-28}$$

Assuming that C_1, C_2, and C_3 are all about the same value and that g_m is much greater than g_1 or g_2 leads to the conclusion that ω_{-3dB} is approximately given by

$$\omega_{-3dB} \approx \frac{g_1 g_2}{g_m C_3} \tag{6.1-29}$$

Comparing Eqs. 6.1-22 and 6.1-29 shows that the bandwidth of the current driven inverter is approximately A_{v0} $(= g_m/g_2)$ less than that of the voltage-driven inverter. The reason for the decrease in bandwidth is the influence of the gain of the amplifier on the capacitor C_3. Because this capacitor is connected between the input and output, it has the voltage gain of the inverter across it. When viewed from the input, this makes the C_3 capacitor look $1 + A_{v0}$ larger than it really is. This effect is called the *Miller effect*. When the input is current-driven, the large Miller capacitance can create a dominant pole at the input as just shown. Figure 6.1-10 shows the typical frequency response for a current-driven inverter.

The last small signal characteristic we will examine is noise. Unfortunately, the noise models are sufficiently technology-dependent that it is more suitable to introduce the noise analysis after the technology has been selected.

In this subsection the inverter has been introduced from a generic viewpoint. The various types of inverter architectures were discussed and analyzed from both a large signal and a small signal viewpoint. In the following subsections, we will apply these ideas to inverters using MOS and BJT technologies.

6.1.2 MOS INVERTING AMPLIFIERS

The general concepts of inverting amplifiers will now be applied to MOS technology. The possible MOS implementations of the sinking inverter architecture of Fig. 6.1-3*a* are shown in Fig. 6.1-11. Each of the lower blocks is a realization of the voltage-controlled current sink using an n-channel transistor. Each of the upper blocks represents a realization of the load connected between

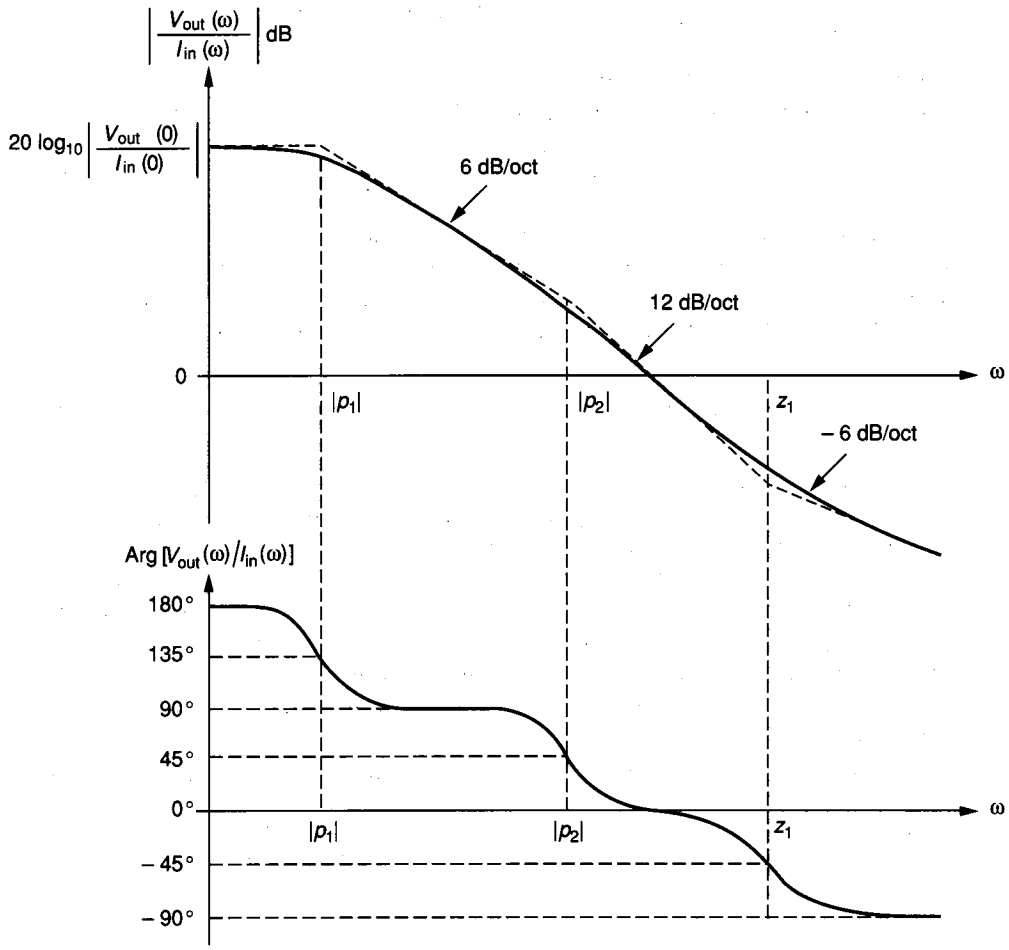

FIGURE 6.1-10
Typical frequency response for a current-driven inverter.

the output of the voltage-controlled current sink and V_{DD}. A CMOS technology having a depletion transistor capability is able to implement all of the inverters of Fig. 6.1-11. If the CMOS technology does not have a depletion transistor capability, then only the inverters of Fig. 6.1-11*a*, *b*, and *c* can be realized. An NMOS technology with a depletion transistor capability can realize the inverters of Fig. 6.1-11*c* or *d*. An NMOS technology that does not have a depletion transistor capability can realize only the inverter of Fig. 6.1-11*c*.

The voltage transfer function of the MOS inverters of Fig. 6.1-11 can be found using the approach demonstrated in Fig. 6.1-4. When V_{IN} of Fig. 6.1-11*a* is at V_{SS}, the drain current in M1 is zero. Because M2 has its drain and gate connected, it is always in the saturation region. Therefore, Eq. 9 of Table 3.1-1 shows that for zero current, the value of $V_{GS2}(V_{DS2})$ is equal to V_{T2}. Therefore, the value of V_{OUT} is $V_{DD} - V_{T2}$ until V_{IN} increases from V_{SS} to V_{T1}, where M1 turns on. At this point the output voltage starts to drop as in Fig. 6.1-4*a*.

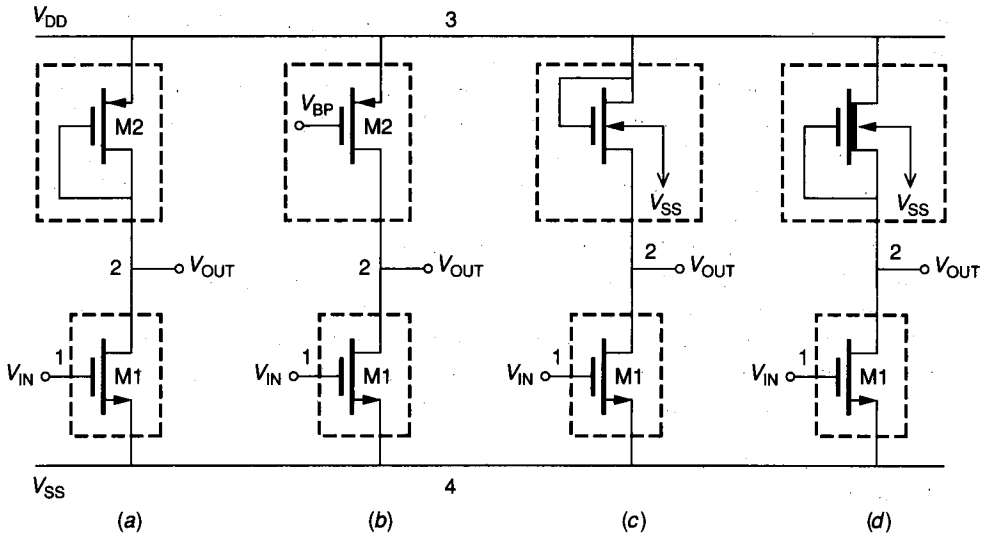

FIGURE 6.1-11
Possible realizations of the sinking inverter for Fig. 6.1-3*a*: (*a*) Active p-channel load, (*b*) Current source load, (*c*) Active n-channel load, (*d*) Depletion n-channel load. All potentials are with respect to ground.

Unlike the ciruit of Fig. 6.1-4*a*, however, the output voltage of Fig. 6.1-11*a* never reaches V_{SS}.

As the current in M1 and M2 increases because V_{IN} is approaching V_{DD}, the voltage across M1 only increases by the square root of the current. Figure 6.1-12 shows the resulting voltage transfer curve for the inverter of Fig. 6.1-11*a* when $W_1 = 15\ \mu, L_1 = 10\ \mu, W_2 = 5\ \mu, L_2 = 10\ \mu, V_{DD} = -V_{SS} = 5$ V, for a CMOS technology corresponding to the parameters in Table 3.1-2. The SPICE input file necessary to generate this plot is included in the figure.

It is of interest to identify in Fig. 6.1-12 the regions where M1 is off, ohmic, and saturated. M1 is off when $V_{IN} < V_{SS} + V_{T1} = -4.25$ V. M1 is saturated when

$$V_{DS1} > V_{GS1} - V_{T1} \Rightarrow V_{OUT} - V_{SS} > V_{IN} - V_{SS} - V_{T1} \Rightarrow V_{OUT} > V_{IN} - V_{T1} \tag{6.1-30}$$

The various regions of M1 are shown in Fig. 6.1-12. This information is important because now we know that the transition region corresponds (for the most part) to M1 operating in the saturation region. The large signal equation that governs the operation of both devices in the transition region is from Eq. 3.1-4

$$I_D \approx \frac{K'W}{2L}(V_{GS} - V_T)^2 \tag{6.1-31}$$

where we have neglected the channel modulation effect (λ). Equating I_{D1} to I_{D2} results in the following relationship.

$$\frac{K_1'W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2 = \frac{K_2'W_2}{2L_2}(V_{DD} - V_{OUT} - V_{T2})^2 \tag{6.1-32}$$

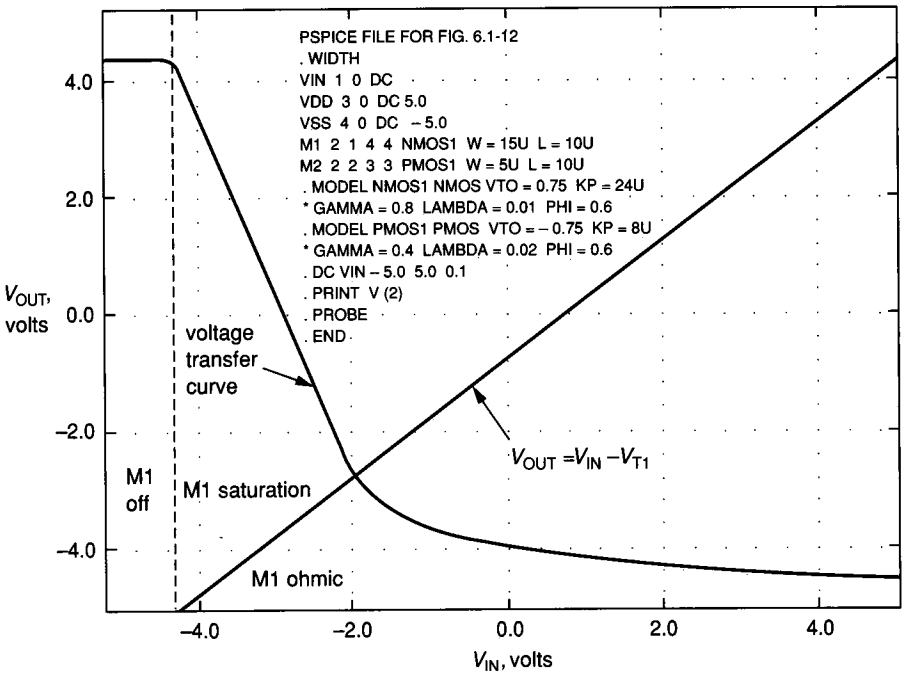

FIGURE 6.1-12
VTC of sinking inverter with active load.

If the inverter of Fig. 6.1-11*a* is biased in the transition region, then Eq. 6.1-3 can be used to find the small signal ac voltage gain. Applying Eq. 6.1-3 to Eq. 6.1-32 results in

$$A_v = \frac{v_{out}}{v_{in}} = \left.\frac{\partial V_{OUT}}{\partial V_{IN}}\right|_Q = -\left(\frac{K_1' W_1 L_2}{K_2' L_1 W_2}\right)^{0.5} \tag{6.1-33}$$

We can also use the small signal model of Fig. 6.1-6 to calculate A_v. From Chapter 3, we know that $g_i = 0$, $g_m = g_{m1}$, $g_o = g_{ds1}$, and $g_1 = g_{m2} + g_{ds2} \approx g_{m2}$. Eq. 6.1-11 and Eq. 3.1-11 give the small signal voltage gain as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{m2} + g_{ds2}} \approx -\frac{g_{m1}}{g_{m2}} = -\left[\frac{K_1'(W_1/L_1)}{K_2'(W_2/L_2)}\right]^{0.5} \tag{6.1-34}$$

The two approaches to finding A_v are seen to agree as expected. Using the small signal model, we can find the input and output resistances as

$$r_{in} = \infty \tag{6.1-35}$$

and

$$r_{out} = \frac{1}{g_{ds2} + g_{m2}} \approx \frac{1}{g_{m2}} \tag{6.1-36}$$

The frequency response of the inverter of Fig. 6.1-11*a* can be found by inserting the transistor capacitors used in Ex. 3.1-5 into the circuit of Fig. 6.1-11*a*

and comparing the result with Fig. 6.1-8. C_1, C_2, and C_3 of the circuit of Fig. 6.1-8 become

$$C_1 = C_{GS1} + C_{GB1} \tag{6.1-37}$$

$$C_2 = C_{BD1} + C_{GS2} + C_{BD2} + C_{GB2} \tag{6.1-38}$$

and

$$C_3 = C_{GD1} \tag{6.1-39}$$

Therefore, the upper -3 dB frequency for the voltage-driven inverter of Fig. 6.1-11*a* is found from Eq. 6.1-22 as

$$\omega_{-3dB} = \frac{g_{m2} + g_{ds1} + g_{ds1}}{C_{BD1} + C_{GS2} + C_{BD2} + C_{GD1} + C_{GB2}} \tag{6.1-40}$$

The noise of an inverter is also one of the small signal performance characteristics of interest when inverters are used as small signal amplifiers. Noise is a phenomenon caused by small fluctuations of the analog signal within the components themselves. Noise results from the fact that electrical current is not continuous but the result of quantized behavior and is associated with fundamental processes in a semiconductor component. Common types of noise for semiconductor devices are thermal and $1/f$ noise.

Regardless of the type of noise, the model always can be characterized by an independent voltage or current source. In general, noise is expressed in terms of its mean-square value $[V(\text{rms})^2]$. Noise spectral density is the noise mean-square value per Hertz of bandwidth $[V(\text{rms})^2/\text{Hz}]$. The model for noise in an MOS device can be modeled as an independent voltage in series with the gate as shown in Fig. 3.1-30*b*. Figure 6.1-13 shows the noise models added to the active-load sinking inverter of Fig. 6.1-11*a*. $\overline{V}_{n1}^2$ and $\overline{V}_{n2}^2$ are the mean-square

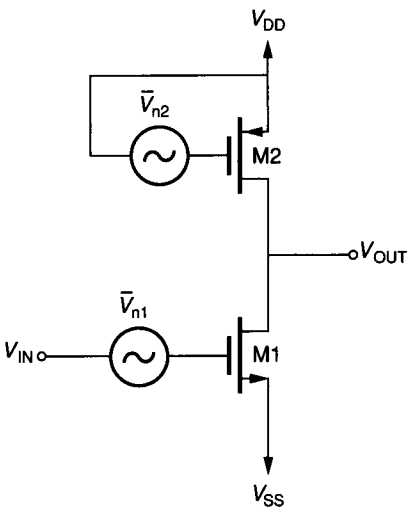

FIGURE 6.1-13
Noise model of Fig. 6.1-11*a*.

noise voltages of M1 and M2 modeled at the input (gate) of each device. Since $\overline{V}_{n1}$ and $\overline{V}_{n2}$ are uncorrelated, the output mean-square noise voltage can be calculated using superposition. The part of the output due to $\overline{V}_{n1}^2$ is

$$\overline{V}_{o1}^2 = \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{V}_{n1}^2 \tag{6.1-41}$$

The part of the output due to $\overline{V}_{n2}^2$ is

$$\overline{V}_{o2}^2 = \overline{V}_{n2}^2 \tag{6.1-42}$$

It should be noted that all gains between the input and output are positive and squared. Also, the value of output due to $\overline{V}_{n2}^2$ is equal to $\overline{V}_{n2}^2$ because the gate voltage of M2 is constant ($\overline{V}_{n2}^2$ only changes the drain voltage). Summing Eqs. 6.1-41 and 6.1-42 gives the total output mean-square noise voltage.

It is customary to reflect the output mean-square noise voltage to the input of the amplifier. This input referred noise voltage obtained by dividing the output noise voltage by the voltage gain is called the equivalent, input-referred, mean-square noise voltage of the amplifier and is given as

$$\overline{V}_{eq}^2 = \overline{V}_{n1}^2 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \overline{V}_{n2}^2 \tag{6.1-43}$$

$\overline{V}_{eq}$ is a frequency independent noise because we used the midband or frequency independent voltage gain. Equation 6.1-43 represents the equivalent input mean-square noise voltage of Fig. 6.1-11*a*. When the designer knows the form of the noise mean-square voltages, then Eq. 6.1-43 can be used to minimize the noise. For example, the $1/f$ noise of a MOSFET was given in Eq. 3.1-35 and can be expressed in terms of noise-voltage spectral density in a 1 Hz band as

$$S_{VN} = \frac{S_{IN}}{g_m^2} = \frac{B}{fWL}(V^2/\text{Hz}) \tag{6.1-44}$$

where B is a constant that is dependent on the technology. We note from Eq. 6.1-44 that the larger-area devices will have less $1/f$. It has also been empirically observed that B is less for p-channel than for n-channel devices, when everything else is equal. Substituting Eq. 6.1-44 into Eq. 6.1-43 gives

$$S_{eq(1/f)} = \left(\frac{B_N}{fW_1L_1}\right)\left[1 + \left(\frac{K_P'B_P}{K_N'B_N}\right)\left(\frac{L_1}{L_2}\right)^2\right](V^2/\text{Hz}) \tag{6.1-45}$$

If the length of M1 is much smaller than that of M2, the input $1/f$ noise will be dominated by that of M1. To minimize the $1/f$ contribution due to M1, its width must be increased as much as possible. Other types of noise substituted into Eq. 6.1-43 will provide other guidelines to reduce the noise of an amplifier. In general, the designer should try to make the gain of the first stage of an amplifier as large as possible to reduce the overall noise.

An example follows to illustrate the small signal performance of the active-load sinking inverter of Fig. 6.1-11*a*.

Example 6.1-1. AC performance of inverter of Fig. 6.1-11*a*. Determine the small signal performance of the inverter of Fig. 6.1-11*a* using the model parameters of Table 3.1-2, assuming that $W_1/L_1 = 15\ \mu/10\ \mu$ and $W_2/L_2 = 5\ \mu/10\ \mu$ and $V_{DD} = -V_{SS} = 5$ V. The drain and source area (periphery) of M1 and M2 are $150\mu^2(50\mu)$ and $50\mu^2(30\mu)$, respectively. Assume that V_{out} is biased at 0 V. Also assume that the noise is white noise given in Eq. 3.1-34 and find the equivalent input-noise-voltage spectral density.

Solution. We begin the solution by finding the dc current in M1 and M2, calculating the value of V_{G1}, and determining the region of operation for M1. In these calculations we will ignore the influence of the channel modulation (λ). The dc quiescent current can be found from the voltage drop across M2 and is

$$I = \frac{K_P' W_2}{2L_2}(V_{DD} - V_{out} - V_{T2})^2 = \frac{8(5)}{2(10)}(5 - 0.75)^2\ \mu A = 36\ \mu A$$

Assume that M1 is saturated. The value of V_{gs1} that gives 36 μA is found as

$$V_{gs1} = V_{T1} + \left(\frac{2I L_1}{K_N' W_1}\right)^{0.5} = 0.75 + \left[\frac{(2)(36)(10)}{(24)(15)}\right]^{0.5} = 0.75 + 1.41 = 2.17\ V$$

Thus, M1 is in fact saturated and $V_{out} = 0$ V corresponds to $V_{in} = -2.83$ V, as seen in Fig. 6.1-12.

Next, we calculate the small signal parameters for M1 and M2. Using the formulas of Table 3.1-3 gives $g_{m1} = 50.91\mu S$, $g_{ds1} = 0.36\mu S$, $g_{m2} = 16.97\mu S$, and $g_{ds2} = 0.72\mu S$.

Equation 6.1-11 gives

$$A_v = \frac{-50.91}{16.97 + 0.36 + 0.72} = -2.82$$

Equation 6.1-13 gives

$$r_{out} = \frac{1}{(16.97 + 0.36 + 0.72)\mu S} = 55.4\ k\Omega$$

The capacitors of Eq. 6.1-40 are found using the formulas of Fig. 3.1-19*b* and the capacitances of Table 2B.4. In this example, we shall include the sidewall capacitances and will assume that the Value of n in Eq. 3. 1-14 is 0.5 for both the bottom and sidewall junction capacitances. The capacitors of Eq. 6.1-40 are

$$C_{BD1} = (0.33)(150)[1 + (5/.6)]^{-0.5} + (0.9)(50)[1 + (5/.6)]^{-0.5} =$$
$$16.20fF + 14.73fF = 30.93fF$$

$$C_{GS2} = (0.7)(5)(0.6) + (0.67)(50)(0.7) = 2.1fF + 23.33fF = 25.43fF$$

$$C_{BD2} = (0.38)(50)[1 + (5/.6)]^{-0.5} + (1)(30)[1 + (5/.6)]^{-0.5} =$$
$$6.22fF + 9.82fF = 16.04fF$$

$$C_{GD1} = (0.7)(15)(0.45) = 4.73fF$$

$$C_{GB2} = 0$$

Substituting the above values in Eq. 6.1-40 results in

$$\omega_{-3dB} = \frac{18.05\mu S}{30.93fF + 25.43fF + 16.04fF + 4.73fF} = 234Mrps = 37.2MHz$$

Dividing the spectral noise density of Eq. 3.1-34 by g_m^2 gives for M1

$$S_{VWN} = 2.17 \times 10^{-16} V^2/\text{Hz}$$

and for M2

$$S_{VWP} = 6.51 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density can be found from Eq. 6.1-43 by replacing each mean-square noise voltage by its noise voltage spectral density and is

$$S_{eq} = S_{VWN} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VWP} = 2.2 \times 10^{-16} + \left(\frac{16.97}{50.91}\right)^2 6.5 \times 10^{-16}$$

$$= 2.89 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density is equal to 17.0 $\text{nV}/\sqrt{\text{Hz}}$.

The performance of the inverter of this example is seen to have a low gain, a moderate output resistance (for MOS devices), a large bandwidth, and an input-referred noise that depends on the noise of the MOS devices. The performance of the active-load sinking inverter can be altered by changing the bias current or the W and L values of M1 and M2.

The voltage inverter of Fig. 6.1-11*c* will have characteristics similar to Fig. 6.1-11*a* with one exception. Because M2 is n-channel, it will experience bulk effects causing V_{T2} to increase as V_{OUT} increases. Consequently, the output high value of Fig. 6.1-11*c* will be less than that of Fig. 6.1-11*a*. In addition, the back-gate (bulk) transconductance (g_{mb2}) will cause the resistance of the load to be slightly less, resulting in less ac gain. If Fig. 6.1-11*c* is used in Example 6.1-1 with the same W/L values and current for M1 and M2, the ac gain is -1.56, the ac output resistance is 30.7 kΩ, the bandwidth is 42.8 MHz, and the equivalent input noise voltage spectral density is 17.3 $\text{nV}/\sqrt{\text{Hz}}$.

The ac voltage gains of the inverters of Fig. 6.1-11*a* and *c* are low because the resistance of the load device is low. The inverter of Fig. 6.1-11*b* uses a current source as its load and achieves a much higher gain. Figure 6.1-14 shows the voltage transfer curve of the current-source-load sinking inverter of Fig. 6.1-11*b* when V_{BP} is 2 V. When V_{IN} is at V_{SS}, M1 is off and the voltage across M2 is zero, causing V_{OUT} to be at V_{DD}. At some point when V_{IN} increases, M1 will begin to turn on, causing a current to flow in the inverter. This current flow causes a drop across M2 causing the output voltage to fall. As V_{IN} is increased past this point, all of $V_{DD} - V_{SS}$ is dropped across M2, causing M1 to be in the ohmic region with little voltage across it. In this condition, V_{OUT} is approximately V_{SS}.

The regions of operation can be found as before using the transition relationship between the ohmic and saturation regions. M2 is saturated when

$$V_{SD} > V_{SG} + |V_{T2}| \Rightarrow V_{DD} - V_{OUT} > V_{DD} - V_{BP} - |V_{T2}| \Rightarrow$$

$$V_{OUT} < V_{BP} - |V_{T2}| \quad (6.1\text{-}46)$$

The state of M1 is identified by Eq. 6.1-30. The various regions of operation of M1 and M2 are identified in Fig. 6.1-14. Again, we see that the desired ac operating region occurs in the transition region, where both M1 and M2 are

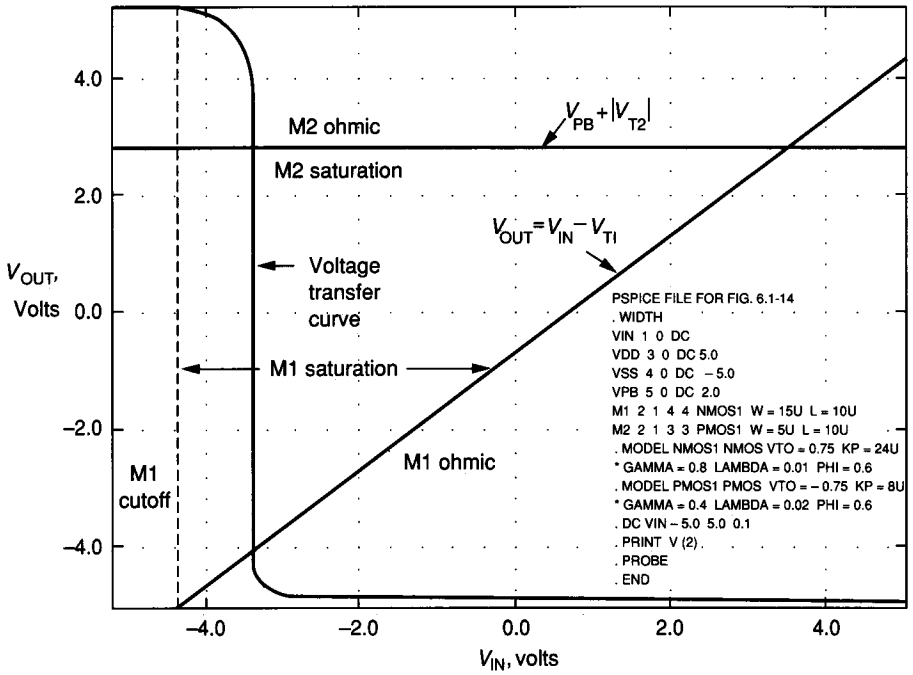

FIGURE 6.1-14
VTC of sinking inverter with current source load.

saturated. In the following discussion, we will assume that the inverter of Fig. 6.1-11*b* is biased with both M1 and M2 in the saturation region.

The operating point of the inverter of Fig. 6.1-11*b* can be found using the previous approach. This time, however, the channel modulation effects should be included in order to relate the drain-source voltage to the drain current. The relationship for M1 and M2 is given as

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{6.1-47}$$

Equating I_{D1} to I_{D2} results in the following relationship for the inverter of Fig. 6.1-11*b*.

$$\frac{K'_N W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2[1 + \lambda_N(V_{OUT} - V_{SS})] = \frac{K'_P W_2}{2L_2}(V_{DD} - V_{BP} - V_{T2})^2[1 + \lambda_P(V_{DD} - V_{OUT})] \tag{6.1-48}$$

Differentiating Eq. 6.1-48 with respect to V_{IN} results in the slope of the voltage transfer curve in the transition region. Applying Eq. 6.1-3 to Eq. 6.1-48 results in

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\partial V_{OUT}}{\partial V_{IN}}\bigg|_Q \approx -\frac{[2K'_N(W_1/L_1)I]^{0.5}}{\lambda_N I + \lambda_P I} = -\frac{[2K'_N(W_1/L_1)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \tag{6.1-49}$$

where the channel modulation effect of Eq. 6.1-47 has been ignored after differentiation and I is the dc current flowing through both M1 and M2.

We can also use the small signal model of Fig. 6.1-6 to calculate A_v. From Chapter 3, we know that $g_i = 0$, $g_m = g_{m1}$, $g_o = g_{ds1}$, and $g_l = g_{ds2}$. Equation 6.1-11 and Table 3.1-3 give the small signal voltage gain as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = -\frac{[2K'_N(W_1/L_1)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \tag{6.1-50}$$

As expected, the two approaches to finding A_v give identical results. Using the small signal model, we can find the input and output resistances as

$$r_{in} = \infty \tag{6.1-51}$$

and

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} \tag{6.1-52}$$

The current-source-load sinking inverter of Fig. 6.1-11*b* has a very unusual property. It is observed that in Eqs. 6.1-49 and 6.1-50 the dc current appears only in the denominator as the argument of the square root. This means that the ac gain is inversely proportional to the square root of the dc bias current. The reason for this can be seen from Table 3.1-3. The transconductance is proportional to the square root of the current, and the conductance is proportional to the current. This property of increasing ac gain as the dc current is reduced does not hold for the previous MOS inverters. When the dc current is reduced to subthreshold levels (~0.1 μA), the transconductance also becomes proportional to the dc current, and the ac gain is no longer dependent on the dc current.

The frequency response of the circuit of Fig. 6.1-11*b* can be found by inserting the transistor capacitors of Example 3.1-5 into the circuit of Fig. 6.1-11*b* and comparing the result with Fig. 6.1-8. C_1, C_2, and C_3 of Fig. 6.1-8 become

$$C_1 = C_{GS1} + C_{GB1} \tag{6.1-53}$$

$$C_2 = C_{BD1} + C_{GD2} + C_{BD2} \tag{6.1-54}$$

and

$$C_3 = C_{GD1} \tag{6.1-55}$$

Therefore, the upper -3 dB frequency for the voltage-driven inverter of Fig. 6.1-11*b* is found from Eq. 6.1-22 as

$$\omega_{-3dB} \approx \frac{g_{ds1} + g_{ds2}}{C_{BD1} + C_{GD2} + C_{BD2} + C_{GD1}} \tag{6.1-56}$$

The noise performance of the current-source-load sinking inverter of Fig. 6.1-11*b* can be investigated in a similar manner as before. It will be left until the problems to show that the noise performance expressed in Eq. 6.1-43 is also valid for the current-source-load sinking inverter. An example follows to illustrate the stated relationships for Fig. 6.1-11*b*.

Example 6.1-2. AC performance of the inverter of Fig. 6.1-11*b*. Determine the small signal performance of the inverter of Fig. 6.1-11*b* using the model parameters of Table 3.1-2 assuming that $W_1/L_1 = 15\ \mu/10\ \mu$, $W_2/L_2 = 5\ \mu/10\ \mu$, $V_{BP} = 2$ V, and $V_{DD} = -V_{SS} = 5$ V. The drain and source area (periphery) of M1 and M2 are $150\mu^2$ (50μ) and $50\mu^2$ (30μ), respectively. Follow the approach of Ex. 6.1-1 to calculate the capacitances. Assume that V_{out} is biased at 0 V. Also assume that the noise is white noise given in Eq. 3.1-34 and find the equivalent input-noise-voltage spectral density.

Solution. We begin by finding the dc current in M1 and M2, calculating the value of V_{G1}, and determining the region of operation for M1. From the given dc voltage, we know that M2 is saturated. The dc current can be found from the voltage drop across M2 and is

$$I = \frac{K_P' W_2}{2L_2}(V_{DD} - V_{BP} - |V_{T2}|)^2[1 + \lambda_P(V_{DD} - V_{out})] = \frac{8(5)}{2(10)}(3 - 0.75)^2(1 + 0.1)\ \mu A = 11.14\ \mu A$$

Assume that M1 is saturated. The value of V_{GS1} that gives 11.14 μA is found from the following equation ignoring channel modulation effects on M1.

$$V_{gs1} = V_{T1} + \left(\frac{2I L_1}{K_N' W_1}\right)^{0.5} = 0.75 + \left[\frac{(2)(11.14)(10)}{(24)(15)}\right]^{0.5} = 0.75 + 0.79 = 1.54\ V$$

Thus, M1 is in fact saturated and $V_{out} = 0$ V corresponds to $V_{in} = -3.46$ V, as seen in Fig. 6.1-14.

Next, we calculate the small signal parameters for M1 and M2. Using the formulas of Table 3.1-3 gives $g_{m1} = 28.32\mu S$, $g_{ds1} = 0.11\mu S$, $g_{m2} = 9.44\mu S$, and $g_{ds2} = 0.22\mu S$.
Equation 6.1-11 gives

$$A_v = \frac{-28.32}{0.11 + 0.22} = -84.74$$

Equation 6.1-13 gives

$$r_{out} = \frac{1}{(0.11 + 0.22)\mu S} = 2.99\ M\Omega$$

The capacitors of Eq. 6.1-56 are found using the formulas of Fig. 3.1-19*b* and the capacitances of Table 28.4. The value of n in Equation 3.1-14 will be 0.5 for both the bottom and sidewall junction capacitances. The capacitances of Eq. 6.1-56 are

$$C_{BD1} = (0.33)(150)[1 + (5/.6)]^{-0.5} + (0.9)(50)[1 + (5/.6)]^{-0.5} = 30.93fF$$

$$C_{GD2} = (0.7)(0.6)(5) = 2.1fF$$

$$C_{BD2} = (0.38)(50)[1 + (5/.6)]^{-0.5} + (1)(30)[1 + (5/.6)]^{-0.5} = 16.04fF$$

$$C_{GD1} = (0.7)(0.45)(15) = 4.73fF$$

Substituting the above values in Eq. 6.1-56 gives

$$\omega_{-3dB} = \frac{0.33\ \mu S}{30.93\ fF + 2.1\ fF + 16.04\ fF + 4.73\ fF} = 6.13\ Mrps$$
$$= 0.976\ MHz$$

Dividing the spectral noise density of Eq. 3.1-34 by g_m^2 gives for M1

$$S_{VWN} = 3.90 \times 10^{-16} V^2/\text{Hz}$$

and for M2

$$S_{VWP} = 11.70 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density can be found from Eq. 6.1-43 by replacing each mean-square noise voltage by its noise spectral density and is

$$S_{eq} = S_{VWN} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VWP} =$$

$$3.90 \times 10^{-16} + \left(\frac{9.44}{28.32}\right)^2 11.70 \times 10^{-16} = 5.20 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density is equal to 22.8 $\text{nV}/\sqrt{\text{Hz}}$.

The performance of the inverter of this example is seen to have a high gain, a high output resistance, a moderate bandwidth, and a noise primarily determined by that of the MOS devices rather than the inverter configuration. As before, the performance can be altered by changing the bias current or the W and L values of M1 and M2.

There is one important difference in the potential noise performance of this inverter compared with the previous ones. Assume that the inverter is used in the first stage of an amplifier. Even though the equivalent input noise levels of the inverters are approximately equal, the inverter of Fig. 6.1-11*b* would be a much better choice for lower noise performance because its gain can be higher, causing the noise of the following stages to have less effect on the overall noise of the amplifier.

The remaining sinking inverter of Fig. 6.1-11 is the depletion-load sinking inverter (Fig. 6.1-11*d*). This inverter requires the technology that offers the ability to make n-channel transistors with a negative threshold voltage. If the gate and source of a depletion transistor are connected, a well-defined drain current will flow if $V_{DS} > 0$. Unfortunately, the depletion n-channel transistor of Fig. 6.1-11*d* is susceptible to bulk effects because its source is not at V_{SS}. This causes the load resistance to be approximately g_{mb2}, which is an improvement over the active-load sinking inverter of Fig. 6.1-11*a* but not as high as the current-source-load sinking inverter. If the inverter of Fig. 6.1-11*d* is used in Example 6.1-1 with the same W/L values for M1 and M2, the ac gain is -15.89, the ac output resistance is 312 kΩ, the bandwidth is 6.83 MHz, and the equivalent input-referred noise-voltage spectral density is 17.3 $\text{nV}/\sqrt{\text{Hz}}$.

The preceding MOS inverter realizations all correspond to the sinking inverter architecture of Fig. 6.1-3*a*. MOS realizations of the sourcing inverter architecture of Fig. 6.1-3*b* can be found by simply taking the inverse of the realizations of Fig. 6.1-11. The *inverse* here means to interchange V_{DD} and V_{SS} and to interchange each p-channel and n-channel transistor. In the sourcing inverter architecture, all of the voltage-controlled current sources are p-channel devices. As a result, for the same W and L values and dc currents, the sinking inverters

will have a larger gain than the sourcing inverters because K'_N is greater than K'_P. The analysis of the sourcing inverters is left to the reader.

The remaining architecture of Fig. 6.1-3 that will be considered is the push-pull inverter of Fig. 6.1-3*c*. This inverter has only the CMOS realization shown in Fig. 6.1-15*a*. The voltage transfer curve can be found using the reasoning behind Fig. 6.1-4*c*. Figure 6.1-16 shows the resulting voltage transfer curve for the push-pull CMOS inverter when $W_1 = 5\ \mu$, $L_1 = 10\ \mu$, $W_2 = 15\ \mu$, $L_2 = 10\ \mu$, and $V_{DD} = -V_{SS} = 5$ V, using a CMOS technology corresponding to the parameters in Table 3.1-2. The SPICE input file necessary to generate this plot is included in the figure. Note that the W and L values have been changed in Fig. 6.1-16 so that the transition region is centered about $V_{IN} = 0$ V. The transition region of the push-pull CMOS inverter is much easier to design with respect to V_{IN} than any of the other inverters. The approach used in the design of the push-pull inverter of Fig. 6.1-16 is called *equal resistance*. If the product of K' and (W/L) are equal for both the n-channel and p-channel devices, then the design will have equal resistance or equal sinking and sourcing capability when V_{IN} is midway between the power supplies. An alternate approach is called *equal area* and uses equal values of W and L for both devices.

The regions of operation are identified in Fig. 6.1-16 using the previous methods. In the following analysis we will assume that both transistors are in the saturation mode, which corresponds to the steepest part of the transition region. Note that the current flowing through M1 and M2 is also plotted in Fig. 6.1-16. The scaling for the current is 20 μA = 1 V. It is seen that the current is highest in the transition region, reaching a peak value of approximately 115 μA.

The operating point of the inverter of Fig. 6.1-15*a* is difficult to calculate because both transistor drain currents are dependent on V_{IN}. The best way to

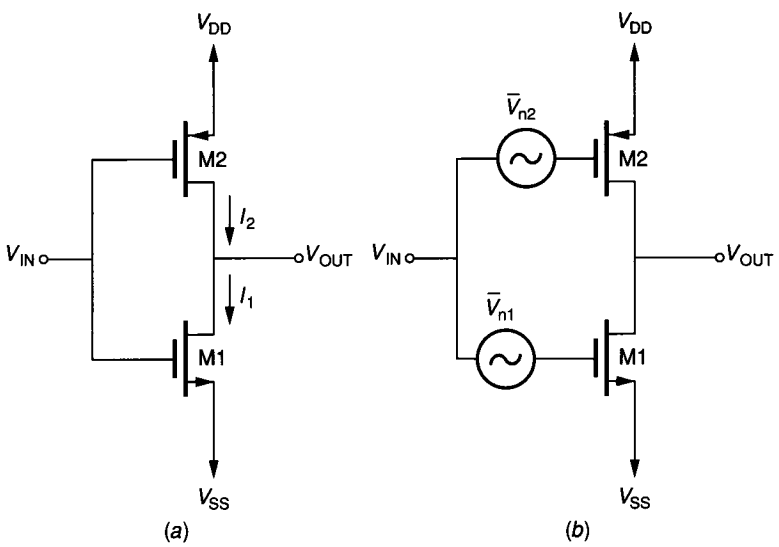

FIGURE 6.1-15
(*a*) Push-pull inverter, (*b*) Noise model of Fig. 6.1-15*a*.

design the operating point would be to use some form of negative dc feedback. For our consideration, we will assume the bias point has been established in the transition region, where both transistors are operating in saturation. Equating I_{D1} to I_{D2} results in the following relationship for Fig. 6.1-15*a*.

$$\frac{K'_N W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2[1 + \lambda_N(V_{OUT} - V_{SS})] = \frac{K'_P W_2}{2L_2}(V_{DD} - V_{IN} - V_{T2})^2[1 + \lambda_P(V_{DD} - V_{OUT})] \quad (6.1\text{-}57)$$

Differentiating Eq. 6.1-57 with respect to V_{IN} results in the slope of the voltage transfer curve in the transition region. Applying Eq. 6.1-3 to Eq. 6.1-57 results in

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\partial V_{OUT}}{\partial V_{IN}}\bigg|_Q \approx -\frac{[2K'_N(W_1/L_1)I]^{0.5} + [2K'_P(W_2/L_2)I]^{0.5}}{\lambda_N I + \lambda_P I}$$

$$= -\frac{[2K'_N(W_1/L_1)]^{0.5} + [2K'_P(W_2/L_2)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \quad (6.1\text{-}58)$$

where channel modulation effects in Eq. 6.1-57 have been ignored after differentiation, and I is the dc current flowing through both M1 and M2.

The small signal model of the circuit of Fig. 6.1-6 can also be used to calculate A_v. From Chapter 3, we know that $g_i = 0$, $g_m = g_{m1} + g_{m2}$, and $g_o = g_{ds1} + g_{ds2}$. Equation 6.1-11 gives the small signal voltage gain as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} = -\frac{[2K'_N(W_1/L_1)]^{0.5} + [2K'_P(W_2/L_2)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \quad (6.1\text{-}59)$$

As expected, the two approaches to finding A_v give identical results. Using the small signal model, we can find the input and output resistances as

$$r_{in} = \infty \quad (6.1\text{-}60)$$

and

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} \quad (6.1\text{-}61)$$

The push-pull inverter of Fig. 6.1-15*a* also has the property that the ac gain is inversely proportional to the square root of the dc bias current.

The frequency response of the circuit of Fig. 6.1-15*a* can be found by inserting the transistor capacitors of Example 3.1-5 into the circuit of Fig. 6.1-15*a* and comparing it with Fig. 6.1-8. C_1, C_2, and C_3 of Fig. 6.1-8 become

$$C_1 = C_{GS1} + C_{GB1} + C_{GS2} + C_{GB2} \quad (6.1\text{-}62)$$

$$C_2 = C_{BD1} + C_{BD2} \quad (6.1\text{-}63)$$

and

$$C_3 = C_{GD1} + C_{GD2} \quad (6.1\text{-}64)$$

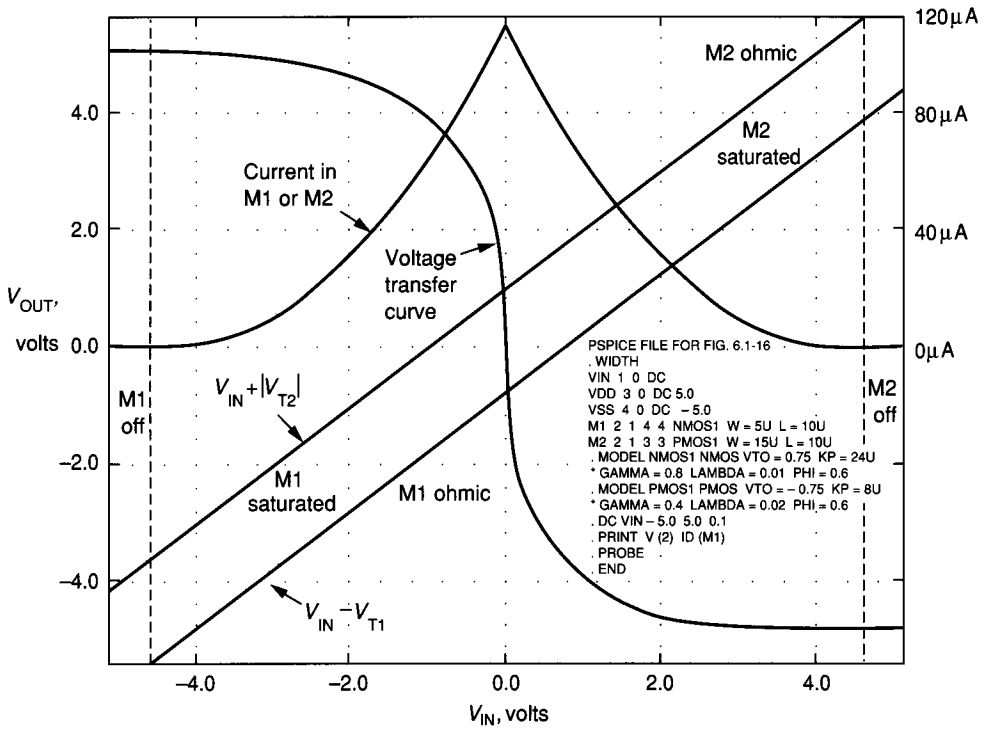

FIGURE 6.1-16
VTC of the push-pull CMOS inverter.

Therefore, the upper -3 dB frequency for the voltage-driven inverter of Fig. 6.1-15*a* is found from Eq. 6.1-22 as

$$\omega_{-3dB} \approx \frac{g_{ds1} + g_{ds2}}{C_{BD1} + C_{BD2} + C_{GD1} + C_{GD2}} \tag{6.1-65}$$

The noise of the push-pull inverter of Fig. 6.1-15*a* is modeled in Fig. 6.1-15*b*, where an input-noise-voltage spectral density source has been used to model the noise of each device. The noise spectral density at the output is

$$S_o = g_{m1}^2 (r_{out})^2 S_{VN1} + g_{m2}^2 (r_{out})^2 S_{VN2} \tag{6.1-66}$$

where r_{out} is given by Eq. 6.1-61. Dividing Eq. 6.1-66 by the square of the gain given in Eqs. 6.1-58 or 6.1-59 gives

$$S_{eq.} = \left[\frac{g_{m1}}{g_{m1} + g_{m2}}\right]^2 S_{VN1} + \left[\frac{g_{m2}}{g_{m1} + g_{m2}}\right]^2 S_{VN2} \tag{6.1-67}$$

If the transconductances are balanced ($g_{m1} = g_{m2}$), then the noise contribution of each device is 50% of the total if $S_{VN1} = S_{VN2}$. The total noise contribution can

be reduced only by reducing the noise contributed by each device. An example follows to illustrate these relationships for the CMOS push-pull inverter of Fig. 6.1-15*a*.

Example 6.1-3. AC performance of the inverter of Fig. 6.1-15. Determine the small signal performance of the inverter of Fig. 6.1-15 using the model parameters of Table 3.1-2 assuming that $W_1/L_1 = 5\ \mu/10\ \mu$, $W_2/L_2 = 15\ \mu/10\ \mu$, and $V_{DD} = -V_{SS} = 5$ V. The drain and source area (periphery) of M1 and M2 are 150 μ^2 (50 μ) and 50 μ^2 (30 μ), respectively. Assume that V_{out} is biased at 0 V. Also assume that the noise in each transistor is white noise given in Eq. 3.1-34 and find the equivalent input-noise-voltage spectral density.

Solution. The dc current in M1 and M2 can be written as

$$I_1 = \frac{K_N' W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2[1 + \lambda_N(V_{out} - V_{SS})]$$

$$I_2 = \frac{K_P' W_2}{2L_2}(V_{DD} - V_{IN} - |V_{T2}|)^2[1 + \lambda_P(V_{DD} - V_{out})]$$

Setting $I_1 = I_2$ and solving simultaneously (by iteration), we obtain $V_{IN} = 0.05$ V and $I_1 = I_2 = 116.4\mu$A. The value of V_{IN} when $V_{OUT} = 0$ is called the *systematic offset voltage*. This offset voltage should be distinguished from that due to mismatches in device model parameters.

Next we calculate the small signal parameters for M1 and M2. Using the formulas of Table 3.1-3 gives $g_{m1} = 52.88\ \mu$S, $g_{ds1} = 1.17\ \mu$S, $g_{m2} = 52.88\ \mu$S, and $g_{ds2} = 2.33\ \mu$S.

Equation 6.1-11 gives

$$A_v = \frac{-(52.88 + 52.88)}{1.17 + 2.33} = -30.3$$

Equation 6.1-13 gives

$$r_{out} = \frac{1}{(1.17 + 2.33)\mu\text{S}} = 285.7\ \text{k}\Omega$$

The capacitors of Eq. 6.1-65 are found using the formulas of Fig. 3.1-19b and the capacitances of Table 2B.4. The value of n in Eq. 3.1-14 will be 0.5 for both the bottom and sidewall junction capacitances. The capacitances of Eq. 6.1-65 are

$$C_{BD1} = (0.33)(150)[1 + (5/.6)]^{-0.5} + (0.9)(50)[1 + (5/.6)]^{-0.5} = 30.93\ \text{fF}$$

$$C_{BD2} = (0.38)(50)[1 + (5/.6)]^{-0.5} + (1)(30)[1 + (5/.6)]^{-0.5} = 16.04\ \text{fF}$$

$$C_{GD1} = (0.7)(0.45)(15) = 4.73\ \text{fF}$$

$$C_{GD2} = (0.7)(0.6)(5) = 2.10\ \text{fF}$$

Substituting the above values in Eq. 6.1-56 gives

$$\omega_{-3dB} = \frac{3.50\ \mu\text{S}}{30.93\ \text{fF} + 16.04\ \text{fF} + 2.10\ \text{fF} + 4.73\ \text{fF}} = 65.06\ \text{Mrps or } 10.35\ \text{MHz}$$

Because $S_{VWN} = S_{VWP} = S_{VW}$, equation 6.1-67 gives

$$S_{eq} = (0.25 + 0.25)S_{VW} = 1.045 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density is equal to 10.2 nV/$\sqrt{\text{Hz}}$

To compare the performance of the inverter of Example 6.1-3 with that of the previous inverters, it is necessary to have the same currents. Multiplying A_v of Ex. 6.1-3 by the square root of 116.4/11.14 gives a voltage gain of -98. With equal W/L values and dc current, the push-pull inverter will have the largest voltage gain. The push-pull inverter can both sink and source output current proportional to the input voltage, which is very useful in output amplifier applications.

The MOS inverters presented in this section represent the more useful realizations of the voltage inverter. The realizations include inverters with active loads, current sink/source loads, depletion transistor loads, and push-pull inverters. A physical layout for the inverters of Fig. 6.1-11*b*, *c*, and *d* and Fig. 6.1-15*a* is shown in Fig. 6.1-17. The technology for this layout is a p-well CMOS technology having the capability of depletion n-channel devices. The ac performance of the inverters discussed in the section is summarized in Table 6.1-1.

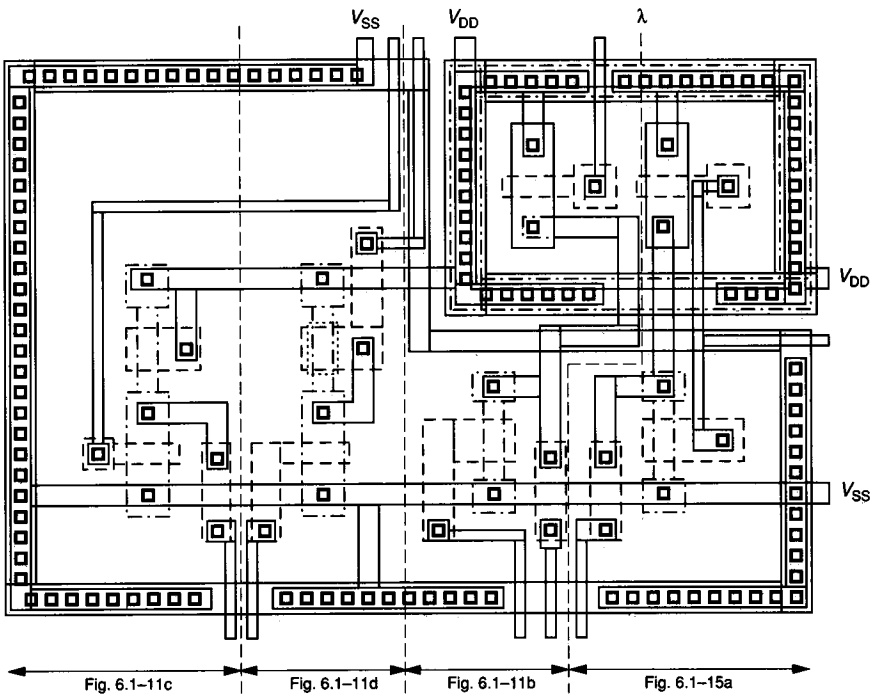

FIGURE 6.1-17
Physical layout of Fig. 6.1-11*b*, *c*, *d* and Fig. 6.1-15*a*.

TABLE 6.1-1
Comparison of the small signal performance of MOS inverters

Inverter	Figure	AC voltage gain	AC output resistance	Bandwidth ($C_{GB} = 0$)	Equivalent, input-referred, mean-square noise voltage
p-channel active load sinking inverter	6.1-11*a*	$\frac{-g_{m1}}{g_{m2}}$	$\frac{1}{g_{m2}}$	$\frac{g_{m2} + g_{mb2}}{C_{BD1} + C_{GD1} + C_{GS2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
n-channel active load sinking inverter	6.1-11*c*	$\frac{-g_{m1}}{g_{m2} + g_{mb2}}$	$\frac{1}{g_{m2} + g_{mb2}}$	$\frac{g_{m2} + g_{mb2}}{C_{BD1} + C_{GD1} + C_{GS2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
Current source load sinking inverter	6.1-11*b*	$\frac{-g_{m1}}{g_{ds1} + g_{ds2}}$	$\frac{1}{g_{ds1} + g_{ds2}}$	$\frac{g_{ds1} + g_{ds2}}{C_{BD1} + C_{GD1} + C_{GD2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
n-channel depletion load sinking inverter	6.1-11*d*	$\sim\frac{-g_{m1}}{g_{mb2}}$	$\frac{1}{g_{mb2} + g_{ds1} + g_{ds2}}$	$\frac{g_{mb1} + g_{ds1} + g_{ds2}}{C_{BD1} + C_{GD1} + C_{GD2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
Push-pull inverter	6.1-15*a*	$\frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}}$	$\frac{1}{g_{ds1} + g_{ds2}}$	$\frac{g_{ds2} + g_{ds2}}{C_{BD1} + C_{GD1} + C_{GD2} + C_{BD2}}$	$\left(\frac{\overline{V}_{n1}^2 g_{m1}}{g_{m1} + g_{m2}}\right)^2 + \left(\frac{\overline{V}_{n2}^2 g_{m2}}{g_{m1} + g_{m2}}\right)^2$

6.1.3 BJT Inverting Amplifiers

The general concepts of inverting amplifiers can also be applied to BJT technology. However, the differences between BJT and MOS transistors reduces the number of practical BJT inverter realizations to one. This conclusion can be understood by examining the BJT active loads of Fig. 5.2-3. The voltage drop across the BJT active load is found to be limited to approximately 0.8 V in the forward-biased direction. The limitation is due to the exponential characteristic of the BJT and the fact that large forward-bias voltages will create extremely large currents. The result is that, unlike MOS active loads with their square law characteristic, BJT active loads are constrained to voltages less than 0.8 V. If a BJT active load is used in the generic inverter configuration of Fig. 6.1-3*a* and *b*, the output voltage would be limited to approximately 0.8 V below V_P or above V_N, respectively. The same reasoning applies to the push-pull inverter architecture of Fig. 6.1-3*c*. Therefore, the only practical inverter configurations for BJT technology are shown in Fig. 6.1-3*a* and *b* where the load is implemented by a current source or current sink, respectively.

Figure 6.1-18 shows the two possible configurations of the BJT inverting amplifier. The voltage transfer curve of the circuit of Fig. 6.1-18*a* can be found using the approach demonstrated in the circuit of Fig. 6.1-4 for the MOS inverting amplifiers. When V_{IN} is at V_{EE}, Q1 is off and no current is flowing in the inverter. Q2 is biased so that if current can flow, it will be determined by the difference between V_{CC} and V_{BB2} and the transistor characteristics of Q2. When V_{IN} is about 0.5 V above V_{EE}, Q1 begins to turn on and current starts to flow in the inverter. At the same time, the output voltage starts to make the transition from V_{CC} to V_{EE}. As V_{IN} approaches 0.6 to 0.7 V above V_{EE}, Q1 saturates and the output voltage is at V_{EE}. In the transition region, it follows from Eq. 3.3-20 that the current flowing in the inverter is given as

$$I_{C2} = I_{s2} \exp\left(\frac{V_{CC} - V_{BB2}}{V_t}\right)\left(1 + \frac{V_{CC} - V_{OUT}}{V_{AFP}}\right) \tag{6.1-68}$$

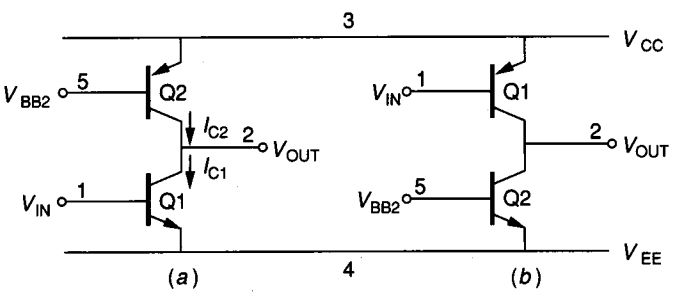

FIGURE 6.1-18
Practical BJT implementations of: (*a*) Sinking inverter, (*b*) Sourcing inverter.