Figure 6.1-19 shows the simulation of the circuit of Fig. 6.1-18*a* when $V_{CC} = -V_{EE} = 5$ V, $V_{BB2} = 4.25$ V, and the transistors have the parameters of Table 6.1-2. In the simulation both the pnp and npn transistors have an emitter area of 500 μ^2 and $V_t = 0.0259$ V. The current in the inverter is also shown in Fig. 6.1-19. Using the model parameters of Table 6.1-2 and assuming that V_{out} is -5 V gives $I_{c1} = 1.67$ mA, which is close to the 1.61 mA indicated in Fig. 6.1-19.

It should be noted that the transition region is very narrow and the slope is large, indicating a large small signal gain. The small signal voltage gain in the transition region can be found by equating the current in Q1 to the current in Q2, resulting in

$$I_{s1} \exp\left(\frac{V_{IN} - V_{EE}}{V_t}\right)\left(1 + \frac{V_{OUT} - V_{EE}}{V_{AFN}}\right) = I_{s2} \exp\left(\frac{V_{CC} - V_{BB2}}{V_t}\right)\left(1 + \frac{V_{CC} - V_{OUT}}{V_{AFP}}\right) \quad (6.1\text{-}69)$$

Differentiating Eq. 6.1-69 with respect to V_{IN} and using Eq. 6.1-3 gives the small signal voltage gain as

$$A_v = \left.\frac{\partial V_{OUT}}{\partial V_{IN}}\right|_Q = \frac{-(1/V_t)}{(1/V_{AFN}) + (1/V_{AFP})} \quad (6.1\text{-}70)$$

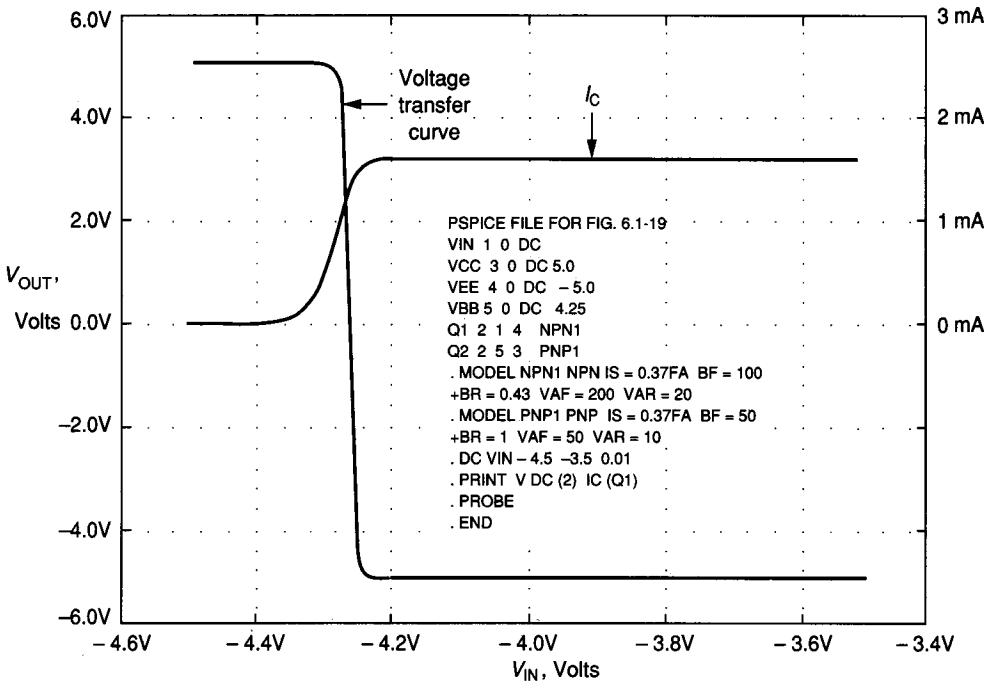


FIGURE 6.1-19
Voltage transfer curve of Fig. 6.1-18*a*.

TABLE 6.1-2
Typical BJT model parameters

Parameter	NPN	PNP	Units
J_s	6×10^{-16} 9.3×10^{-19}	6×10^{-16} 9.3×10^{-19}	A/mil^2 A/μ^2
I_s (Emitter area = 500 μ^2)	0.37	0.37	fA
β_F	100	50	A/A
β_R	0.43	1	A/A
V_{AF}	200	50	Volts
V_{AR}	20	10	Volts
τ_f	0.4	20	ns
C_{je0}	0.5	0.5	pF
C_{jc0}	0.5	0.5	pf
ϕ	0.55	0.55	Volts
$V_t = 0.0259$ V at room temperature ($300^\circ K$)			

Equation 6.1-70 shows that the voltage gain of the BJT inverter in Fig. 6.1-18 is large and is independent of bias current. Using the parameters of Table 6.1-2 gives a small signal voltage gain of -1544. The large gain is typical of BJT inverters using current sink/source loads.

The small signal model of the circuit of Fig. 6.1-18 is shown in Fig. 6.1-20. The small signal model parameters shown are related to the large signal model parameters in Table 3.2-4. The ac voltage gain can easily be shown to be

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{o1} + g_{o2}} = \frac{-(I_{C1}/V_t)}{(I_{C1}/V_{AFN}) + (I_{C2}/V_{AFP})} = \frac{-(1/V_t)}{(1/V_{AFN}) + (1/V_{AFP})} \tag{6.1-71}$$

which is identical to Eq. 6.1-70 and where $I_{C1} = I_{C2} = I_{CQ}$. The principle that the gain can be calculated from the large signal or small signal model is again verified. In the case of the BJT inverter, the small signal input resistance is not infinity and is found as

$$r_{in} = r_{\pi 1} \tag{6.1-72}$$

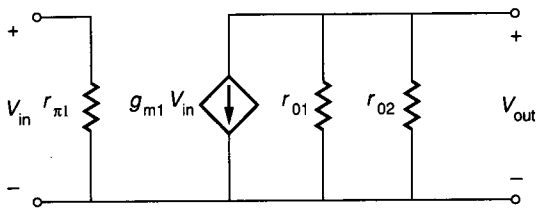


FIGURE 6.1-20
Small signal, midband model for Fig. 6.1-18 *a* or *b*.

The output resistance of Fig. 6.1-18 is

$$r_{out} = \frac{1}{g_{o1} + g_{o2}} = \frac{1}{I_{CQ}[(1/V_{AFN}) + (1/V_{AFP})]} \tag{6.1-73}$$

The frequency response of the voltage-driven BJT inverter can be found by inserting the parasitic capacitances of the BJT inverter in the small signal model of Fig. 6.1-8. Assume that Q1 is a vertical NPN and that Q2 is a lateral PNP. Fig. 3.3-11, Fig. 3.3-12, and Table 3.3-5 result in Fig. 6.1-21 where $C_{BE} + C_{AC} = C_\pi$ and $C_{CB} = C_\mu$. Therefore, the capacitances of Fig. 6.1-8 become

$$C_1 = C_{BE1} = C_{\pi 1} \tag{6.1-74}$$

$$C_2 = C_{CB2} + C_{CS1} = C_{\mu 2} + C_{CS1} \tag{6.1-75}$$

and

$$C_3 = C_{CB1} = C_{\mu 1} \tag{6.1-76}$$

The upper -3 dB frequency is given by Eq. 6.1-22 as

$$\omega_{-3dB} = \frac{g_{o1} + g_{o2}}{C_{\mu 2} + C_{\mu 1} + C_{CS1}} \tag{6.1-77}$$

The upper -3 dB frequency for a current-driven inverter is given by Eq. 6.1-29 as

$$\omega_{-3dB} \cong \frac{g_{\pi 1}(g_{o1} + g_{o2})}{g_{m1} C_{\mu 1}} \tag{6.1-78}$$

In many cases, the output of the inverter sees a load capacitance which must be incorporated into C_2 of Eq. 6.1-75.

The noise performance of the BJT inverter can be found in a similar manner as for the MOS inverters. Figure 6.1-22 shows a model suitable for calculating the noise. The noise sources will be assumed to be noise-voltage spectral density sources. The form of these sources is determined by the type of noise the designer is interested in analyzing. The noise spectral density of the output of Fig. 6.1-18 is found by superimposing the influence of S_{VN1} and S_{VN2} to get

$$S_{OUT} = S_{VN1} A_v^2 + S_{VN1} A_v^2 \left(\frac{S_{VN2}}{S_{VN1}} \right) \tag{6.1-79}$$

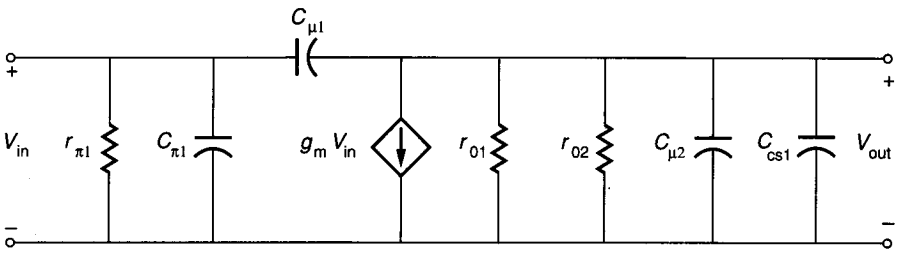


FIGURE 6.1-21
Small signal, high-frequency model for Fig. 6.1-18 *a* or *b*.

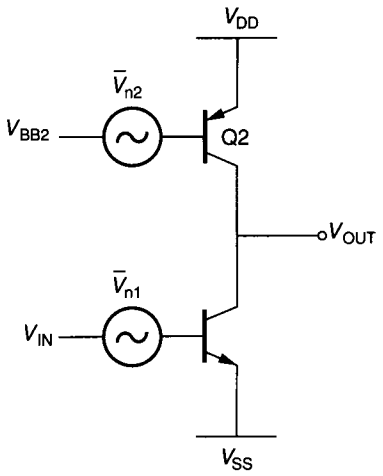


FIGURE 6.1-22
Model for noise calculations of Fig. 6.1-18*a*.

The equivalent noise-voltage spectral density at the input of the BJT can be found by dividing Eq. 6.1-79 by A_v^2. The result is

$$S_{eq} = S_{VN1}\left[1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{S_{VN2}}{S_{VN1}}\right)\right] \tag{6.1-80}$$

It is seen that the BJT inverter noise performance is the same form as that of the MOS inverter given by Eq. 6.1-43. When the form of the noise-voltage spectral density of the BJT is known, then Eq. 6.1-80 can be used to predict the noise performance. The current noise spectral densities of the BJT are given as

$$S_{IC} = 2qI_C \ (V^2/\text{Hz}) \tag{6.1-81}$$

and

$$S_{IB} = \left[2qI_B + \frac{K_F I_B^{AF}}{f}\right] (V^2/\text{Hz}) \tag{6.1-82}$$

where I_C and I_B are dc currents of the transistor, K_F is the $1/f$ noise constant, and AF is an exponent. Eq. 6.1-81 is the shot noise at the collector and Eq. 6.1-82 consists of both shot and 1/f noise at the base. These noise spectral densities are assumed to be uncorrelated.

The BJT inverters of Fig. 6.1-18 are identical in their small signal performance. An example follows to illustrate the small signal performance of the BJT inverter of Fig. 6.1-18.

Example 6.1-4. AC performance of the BJT inverter of Fig. 6.1-18*a*. Find the small signal performance of the BJT inverter of Fig. 6.1-18*a* using the model parameters of Table 6.1-2. Assume $V_{BB2} = 4.25$ V, $V_t = 25.9$ mV, $V_{CC} = -V_{EE} = 5V$, and that the inverter is biased so that V_{out} is at 0 V. Assume that the emitter

areas of both transistors are 500 μ^2 and the collector-substrate area of Q1 is 50 $\mu \times$ 100 μ. If the shot noise spectral density of Eq. 6.1-81 is dominant find the equivalent input-noise-voltage spectral density.

Solution. We begin by finding the dc current in Q1 and Q2. The dc current can be found from Eq. 6.1-68;

$$I_{C2} = (0.37\text{fA}) \left[\exp\left(\frac{0.75}{0.0259}\right)\right]\left(1 + \frac{5}{50}\right) = 1.53 \text{ mA}$$

Next we calculate the small signal parameters for Q1 and Q2. Using the formulas of Table 3.3-4 gives

$$g_{m1} = \frac{I_{C1}}{V_t} = \frac{1.53 \text{ mA}}{0.0259} = 0.059 \text{ S}$$

$$g_{o1} = \frac{I_{C1}}{V_{AFN}} = \frac{1.53 \text{ mA}}{200} = 7.67 \ \mu\text{S}$$

and

$$g_{o2} = \frac{I_{C2}}{V_{AFP}} = \frac{1.53 \text{ mA}}{50} = 30.7 \ \mu\text{S}$$

Equations 6.1-70 and 6.1-71 give

$$A_v = \frac{-0.059 \times 10^6}{7.67 + 30.7} = -1544$$

Equation 6.1-72 gives

$$r_{in} = r_{\pi 1} = \frac{\beta_F}{g_{m1}} = \frac{100}{0.059\text{S}} = 1.695 \ \Omega$$

Equation 6.1-73 gives

$$r_{out} = \frac{10^6}{7.67 + 30.7} = 26.06 \text{ k}\Omega$$

Next we must calculate the value of capacitances that determine the frequency behavior. Assuming V_{IN} is approximately 0.7 V gives $V_{CB1} = 4.3$ V. From Eq. 3.1-19 with $n = 0.5$, we find that $C_{CB1} = 0.168$ pF. Similarly, for Q2 we have $V_{CB2} = 4.25$ V, giving $C_{CB2} = 0.169$ pF. It is customary to estimate C_{BE1} of Table 3.3-5 as $2C_{je0}$, or 1 pF. With τ_f from Table 6.1-2 equal to 0.4 ns, Eq. 3.3-32 gives C_{AF1} as 23.6 pF. Table 2C.4 gives the zero-bias collector-substrate capacitance of 0.79 pF. Since the collector-substrate has a back bias of 5 V, $C_{CS1} = 0.335$ pF. Thus,

$$C_{\mu 1} = C_{CB1} = 0.168 \text{ pF}$$

$$C_{\pi 1} = C_{BE1} + C_{AF1} = 24.6 \text{ pF}$$

$$C_{CS1} = 0.335 \text{ pF}$$

and

$$C_{\mu 2} = C_{CB2} = 0.169 \text{ pF}$$

Equation 6.1-77 for the voltage driven inverter gives

$$\omega_{-3dB} = \frac{7.67 \ \mu\text{S} + 30.7 \ \mu\text{S}}{0.168 \text{ pF} + 0.169 \text{ pF} + 0.335 \text{ pF}} = 57.1 \text{ Mrps or } 9.09 \text{ MHz}$$

Equation 6.1-78 for the current driven inverter gives

$$\omega_{-3dB} = \frac{g_{\pi 1}(g_{o1} + g_{o2})}{g_{m1}C_{\mu 1}} = \frac{590\ \mu S(7.67 + 30.7)\ \mu S}{0.059(0.168\ pF)} = 2.28\ \text{Mrps} = 363\ \text{kHz}$$

From Eq. 6.1-81, the collector shot-noise spectral density is

$$S_{IC} = 4.9 \times 10^{-22}\ A^2/\text{Hz}$$

Dividing by g_m^2 gives the equivalent noise voltage spectral density at the base for both transistors as

$$S_{VB} = 4.9 \times 10^{-22}/0.059 = 1.405 \times 10^{-19}\ V^2/\text{Hz}$$

Eq. 6.1-80 gives the equivalent input noise voltage spectral density as 0.53 nV/$\sqrt{\text{Hz}}$.

The small signal analysis and design of inverting amplifiers has been addressed in Section 6.1. It was shown that these amplifiers consist of a voltage-controlled current sink/source and a load. In the case of the CMOS push-pull inverting amplifier, the load was also a voltage-controlled current source. It was seen that the voltage transfer curves of inverting amplifiers have three distinct operating regions. These regions are where the input is low and the output is high, where the input is high and the output low, and a region between these two called the transition region. Because the ac gain is proportional to the slope of the voltage transfer curve, the high gain inverting amplifier should be biased in the region with the steepest slope, which is the transition region. It was shown that in the transition region, the transistors are all operating in their normal regions of operation: the saturation region for the MOSFET and the forward-active region for the BJT. Therefore, the small signal model for the normal-region operation was used to predict the performance of the inverters considered in this section. The performance variables include the small signal voltage gain, the input resistance, the output resistance, the -3 dB bandwidth, and noise.

The inverter or inverting amplifier is a basic gain block and should be well understood before the following sections are studied. An example follows on how the designer approaches the implementation of an amplifier using an inverting amplifier. This example will show some of the tradeoffs that can be made based on the considerations presented in this section. It will also show some of the limitations of the inverter and why we must consider other types of amplifiers.

Example 6.1-5. Assume that you are to design an inverting amplifier with gain equal to or greater than -100, using power supplies of ± 2.5 V, having a power dissipation less than 1 mW, and using a dc value for both input and output voltages of 0 V. Select among the inverting amplifiers presented in this section. Assume that Tables 3.1-2 and 6.1-2 represent the model parameters of the MOS or BJT, respectively.

Solution. The first consideration is selection of one of the inverter architectures that have been discussed. From the specifications we note that the dc voltage across the voltage-controlled current sink/source will be 2.5 V. This is too much voltage to put across the base-emitter of a BJT, so we are restricted to MOS implementations.

Although only one of the MOS inverters was shown to have zero input dc voltage (the inverter of Fig. 6.1-15*a*), all could be biased with the input and output at 0 V if the *W/L* ratios were designed correctly. Thus, since the gain is large and we have no other specifications to suggest otherwise, let us select the CMOS push-pull inverter of Fig. 6.1-15*a* because it has the largest gain for similar dc current.

The dc current through the inverter will be selected to meet the power supply specification. It is seen that for power supplies of ±2.5 V, any current less than 200 μA will give a power dissipation less than 1 mW. Let us arbitrarily choose a dc current of 100 μA. The next step is to find the W_1/L_1 ratio that will give this current for a gate-source voltage of 2.5 V. Using the large signal equation in the saturation region, we get

$$\frac{W_1}{L_1} = \frac{2I_d}{K'_N(V_{gs1} - V_{TN})^2(1 + \lambda_N V_{ds1})} = \frac{2(100)}{(24)(1.75)^2(1.05)} = 2.59 \approx \frac{5}{2}$$

Solving for W_2/L_2 using the same approach gives

$$\frac{W_2}{L_2} = \frac{2I_d}{K'_P(V_{sg2} - |V_{TP}|)^2(1 + \lambda_P V_{sd2})} = \frac{2(100)}{(8)(1.75)^2(1.1)} = 7.42 \approx \frac{15}{2}$$

Putting these values into Eq. 6.1-59 gives a small signal voltage gain of −73.

Unfortunately, we now face the type of problem that a designer will encounter many times. The design meets two of the three specifications. If we are restricted to inverting amplifiers, what can be done to meet *all* of the specifications? One might be tempted to lower the current since it was shown that the ac gain was inversely proportional to the square of the dc current. However, this relationship only holds when everything else, such as *W/L* values, remains constant. If we attempt this approach, the requirement that $V_{GS1} = 2.5$ V will cause the *W/L* values to change, resulting in the same gain as before. If the preceding formulas for *W/L* are substituted into Eq. 6.1-59, it will be seen that V_{GS} must be changed to produce the correct gain. Unfortunately, this implies changing the power supplies, which is probably beyond the control of the designer. None of the other MOS configurations will meet all three specifications for the same reason that the push-pull CMOS inverter fails. One must turn to other architectures or change the specifications. This example will be reconsidered in the next section.

6.2 IMPROVING THE PERFORMANCE OF INVERTING AMPLIFIERS (CASCODE AMPLIFIERS)

A very useful amplifier called the inverting amplifier was introduced in Section 6.1. The inverting amplifier is intended to invert and amplify small signals. The objective of this section is to take a closer look at the performance of inverting amplifiers. By doing so, we will see areas where the small signal performance can be improved or design constraints eliminated. Some of the topics not addressed in the last section include controlling or designing the frequency response, achieving higher gain, and decoupling the ac and dc design constraints. These topics seriously limit the performance of the inverters of the previous section. For example, if the inverter is current-driven, the bandwidth is severely reduced from

the bandwidth of the voltage-driven inverter. In many of the MOS inverters, an ac gain larger than -100 would be difficult to achieve. Example 6.1-5 illustrated the problems that develop between ac and dc specifications. In that example, we saw that it was impossible to satisfy all the design requirements simultaneously.

Let us first examine how the designer can control the frequency response of an inverting amplifier. Assume that the source can be represented by a Thevenin or Norton form having a source resistance of R_s. If the voltage amplifier of Fig. 6.1-8 is voltage-driven, then $R_s = 0$ and the -3 dB bandwidth is given from Eq. 6.1-22 as

$$\omega_{-3dB}(R_s = 0) = \frac{g_2}{C_2 + C_3} \tag{6.2-1}$$

where R_s is the resistance of the input source. If R_s is large, then the amplifier is current-driven. If this amplifier is current-driven, we have shown in Eqs. 6.1-27 and 6.1-28 that the poles are widely spaced and the -3 dB bandwidth is from Eq. 6.1-29

$$\omega_{-3dB}(R_s \neq 0) \approx \frac{g_1 g_2}{g_m C_3} \tag{6.2-2}$$

Since g_m is typically much greater than g_1, the bandwidth of the current-driven inverter is less than the voltage-driven inverter. A useful heuristic viewpoint of the current-driven inverter is shown in Fig. 6.2-1 for the inverting amplifier of the circuit of Fig. 6.1-11*b*. In many circuits, the poles can be closely approximated by the reciprocal product of the resistance and capacitance to ground at a node. In this circuit there are two poles. p_1 is associated with the input and p_2 with the output of the inverter. Typically, R_s is the output of another inverter and is approximately equal to the r_o of a MOSFET. The resistances associated with each pole are approximately the same in most cases. However, because of the Miller effect, the C_{gd1} capacitance is reflected in parallel with the gate and source of M1, causing p_1 normally to be much less than p_2. The objective of the following discussion is to show how to obtain current-driven inverters that have bandwidths approximately equal to those of voltage-driven inverters.

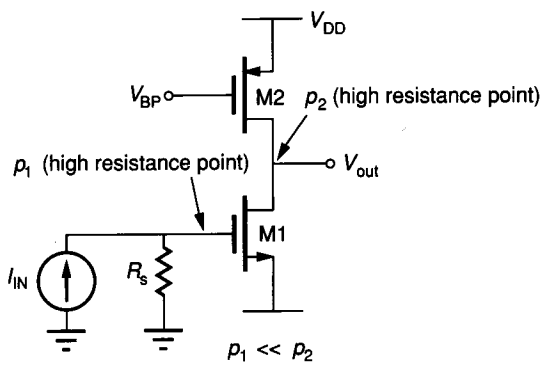


FIGURE 6.2-1
Current-driven CMOS inverter.

6.2.1 Current-Driven CMOS Cascode Amplifier

Consider Fig. 6.2-2, where the voltage-controlled current sink of Fig. 6.1-3*a* has been implemented by the architecture of Fig. 5.3-8*b* rather than the architecture of Fig. 5.3-5*a*. As in Sec. 6.1, the input is at the gate of M1. The gates of M2 and M3 are biased by the dc voltages V_{BP} and V_{BN}, respectively. M3 is called the *cascode transistor* and has a very important influence on the frequency performance. Figure 6.2-3*a* shows the small signal model for Fig. 6.2-2. Note that since the source of M3 is not on V_{SS}, bulk effects must be included. The small signal model can be redrawn as illustrated in Fig. 6.2-3*b*. An important observation is the influence of M3 on the resistance seen by the drain of M1. This resistance has been reduced from a level of $1/g_{ds}$ in the circuit of Fig. 6.1-11*b* to a level of less than $1/g'_{m3}$ (g'_{m3} refers to the sum of g_{m3} and g_{mb3}). The midband, small signal voltage gain from V_1 to V_2 is approximately $-g_{m1}/g'_{m3}$. Considerable mathematical manipulations can be avoided in finding the poles of the circuit of Fig. 6.2-2 if we assume that r_{ds3} is approximately infinity. This results in the approximate circuit shown in Fig. 6.2-3*c*, where the notation of Fig. 6.1-8 has been used for the left-hand part of the circuit. In this case, we can use Eqs. 6.1-27 and 6.1-28 to find the poles of the left-hand part of the circuit. Using the equivalent expressions given in Fig. 6.2-3*c* gives the poles of Fig. 6.2-2 as

$$p_1(\text{cascode}) = -\left[\frac{C_2 + C_3}{g_2} + \frac{C_1 + C_3}{g_1} + \frac{g_{m1}C_3}{g_1 g_2}\right]^{-1} \approx \frac{-g_1}{C_1 + C_3[1 + (g_{m1}/g'_{m3})]} \tag{6.2-3}$$

$$p_2(\text{cascode}) \approx \frac{-g'_{m3}[C_1 + C_3 + C_3(g_{m1}/g'_{m3})]}{C_1C_2 + C_1C_3 + C_2C_3} \tag{6.2-4}$$

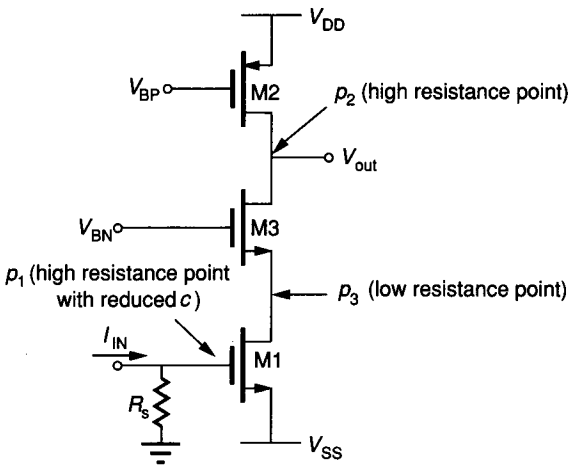


FIGURE 6.2-2
Current-driven cascode inverting amplifier ($V_{BS2} = 0$).

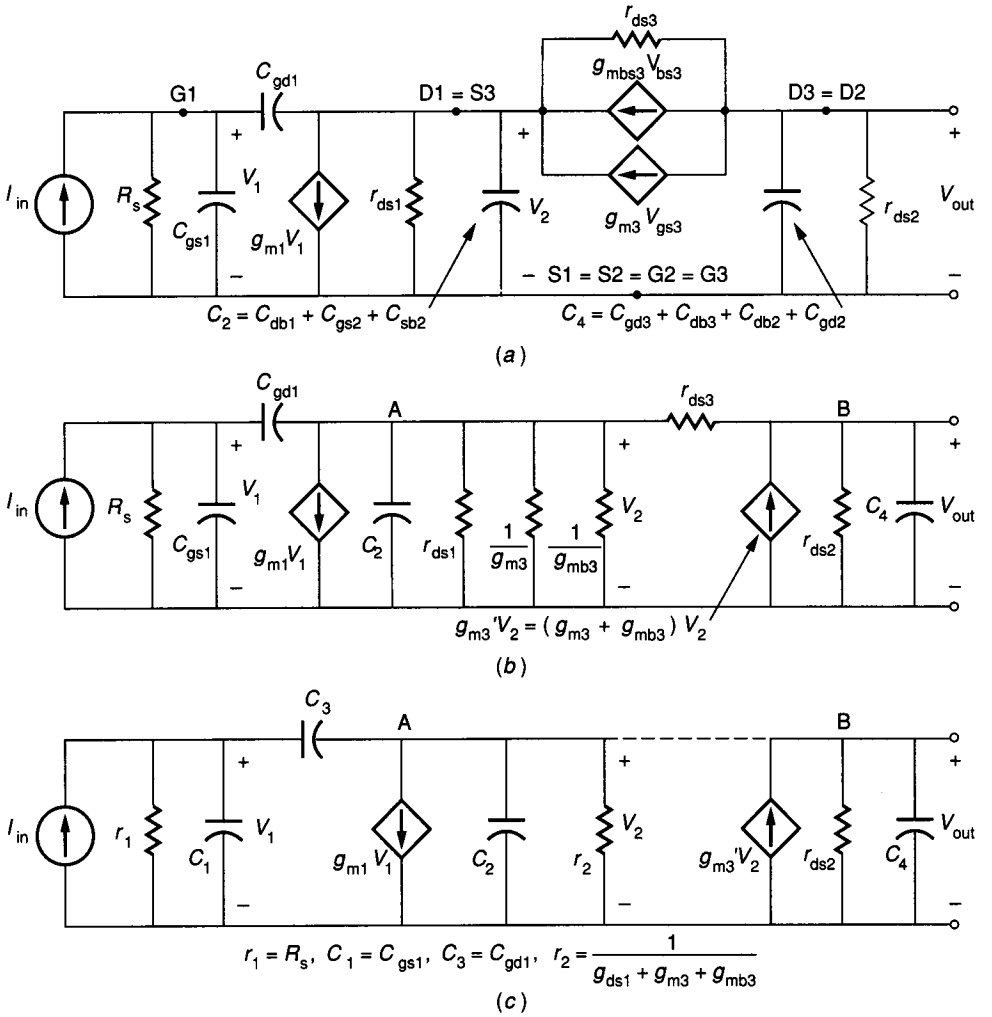


FIGURE 6.2-3
(*a*) Small signal model of Fig. 6.2-2, (*b*) Equivalent model of (*a*), (*c*) Model if r_{ds3} is assumed infinite.

The output pole associated with C_4 is

$$p_3(\text{cascode}) \approx \frac{-g_{o2}}{C_4} \tag{6.2-5}$$

Comparing Eqs. 6.2-3 and 6.2-4 with Eqs. 6.1-27 and 6.1-28 shows that the influence of the cascode transistor (M3) is to bring the input pole back to the value it would have if C_3 were zero ($-g_1/C_1$ as seen from Fig. 6.2-3*c*). The higher inverter pole corresponding to Eq. 6.1-28 and now given by Eq. 6.2-4, has not been influenced very much by the cascode transistor. Looking at

these results and assuming that all capacitors have approximately the same value within a factor of 5, that $g_{m1} \approx g'_{m3}$, and that R_s is less than or equal to r_o, we see that

$$| p_1(\text{cascode}) | \approx | p_3(\text{cascode}) | < | p_2(\text{cascode}) | \tag{6.2-6}$$

6.2.2 Voltage-Driven CMOS Cascode Amplifier

The low-frequency voltage gain of the voltage-driven cascode amplifier can be found from the equivalent circuit of Fig. 6.2-3, by replacing I_{in} with a voltage source and noting that $V_{in} \approx V_1$. The nodal equations at nodes A and B, disregarding the capacitors, can be found as

$$(g_{ds1} + g_{ds3} + g_{m3} + g_{mbs3})V_2 - g_{ds3}V_{out} = -g_{m1}V_1 \tag{6.2-7}$$

$$-(g_{ds3} + g_{m3} + g_{mbs3})V_2 + (g_{ds2} + g_{ds3})V_{out} = 0 \tag{6.2-8}$$

Solving for V_{out}/V_1 gives

$$\frac{V_{out}}{V_1} = \frac{V_{out}}{V_{in}} = \frac{g_{m1}(g_{m3} + g_{mbs3} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds2}(g_{m3} + g_{mbs3})} \approx -\frac{g_{m1}}{g_{ds2}} \tag{6.2-9}$$

This gain should be compared with that of Eq. 6.1-50 for the current-source-load sinking inverter of Fig. 6.1-11*b*. Because of the cascode influence of M3 on the output resistance of M1, $g_{ds1}(r_{ds1})$ is no longer important. Thus, under similar conditions, the cascode CMOS inverter should have an ac gain approximately twice that of the simple CMOS inverter of Fig. 6.1-11*b*.

Generally, with the addition of active devices, the equivalent input noise increases. It is of interest to determine the influence of M3 on the noise performance of the cascode CMOS inverter. Figure 6.2-4*a* shows a model appropriate for calculating the noise of the voltage-driven cascode CMOS inverter. Superposition is used to find the contribution of each noise source to the output. The contribution of $\overline{V}_{n3}$ requires particular attention. Figure 6.2-4*b* gives the small signal model that can be used to find the contribution of $\overline{V}_{n3}$. Writing nodal equations gives

$$(g_{ds1} + g_{ds3} + g_{m3} + g_{mb3})V_{s3} - g_{ds3}V_{out} = g_{m3}\overline{V}_{n3} \tag{6.2-10a}$$

$$-(g_{ds3} + g_{m3} + g_{mb3})V_{s3} + (g_{ds2} + g_{ds3})V_{out} = -\overline{V}_{n3} \tag{6.2-10b}$$

Solving for $\overline{V}_{out}/\overline{V}_{n3}$ gives

$$\frac{\overline{V}_{out}}{\overline{V}_{n3}} = \frac{-g_{ds1}g_{m3}}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds2}(g_{m3} + g_{mb3})} \cong \frac{-g_{ds1}g_{m3}}{g_{ds2}(g_{m3} + g_{mb3})} \tag{6.2-11}$$

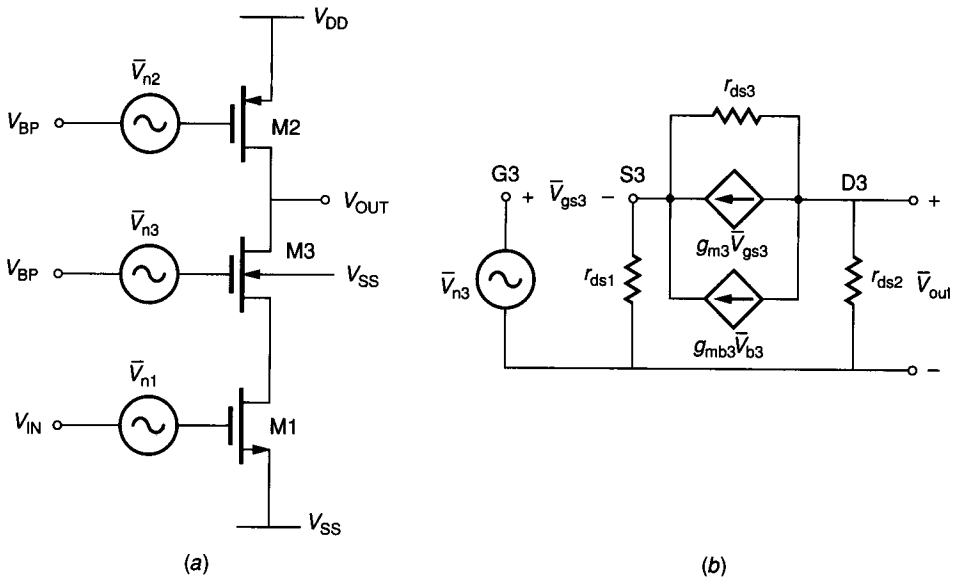


FIGURE 6.2-4
(*a*) Model for calculating the noise performance of the cascode CMOS inverter, (*b*) Model for calculating the noise of M3.

We note that under most normal circumstances, the gain of Eq. 6.2-11 will be less than unity. The reason for this is the large resistance (r_{ds1}) from the source to ground of M3. The total output-noise-voltage spectral density can be found as

$$S_{out} \approx \left(\frac{g_{m1}}{g_{ds2}}\right)^2 S_{VN1} + \left(\frac{g_{m2}}{g_{ds2}}\right)^2 S_{VN2} + S_{VN3} \tag{6.2-12}$$

The equivalent input-noise-voltage spectral density is found by dividing Eq. 6.2-12 by the square of the small signal, frequency independent voltage gain $(g_{m1}/g_{ds2})^2$ to get

$$S_{eq.} = S_{VN1} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VN2} + \left(\frac{g_{ds2}}{g_{m1}}\right)^2 S_{VN3} \approx S_{VN1} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VN2} \tag{6.2-13}$$

It is of interest to note that for all practical purposes, the addition of the cascode transistor, M3, does not influence the noise performance.

6.2.3 Improving the Gain of the CMOS Cascode Amplifier

The second performance limitation that was found particularly in the MOS inverting amplifiers of Fig. 6.1-11 was a small voltage gain. The ac voltage gain of the inverting amplifier was found to be g_m times the output resistance of the amplifier. One can increase g_m or r_{out} to increase the gain. If one could increase

the current in the transconductance transistor but not in the load transistor, then the gain would increase by the square root of this current increase. Consider the cascode CMOS inverter illustrated in Fig. 6.2-5*a* where a dc current source of value I_o has been connected between V_{DD} and the drain of M1. Because of the low resistance at the point where the current source is attached between M1 and M3, the small signal voltage gain is still given by Eq. 6.2-9. The injection of I_o will increase only g_{m1}, as shown below.

$$A_v \approx \frac{-g_{m1}}{g_{ds2}} = \left(\frac{2K'_N W_1 I_{D1}}{L_1 I_{D2} \lambda_{P2}}\right)^{0.5} = \left(\frac{2K'_N W_1}{L_1 I_{D2} \lambda_{P2}}\right)^{0.5} \left(1 + \frac{I_o}{I_{D2}}\right)^{0.5} \tag{6.2-14}$$

The first product in the rightmost part of Eq. 6.2-14 is the normal gain of the cascode CMOS inverter. The second product in the rightmost part of Eq. 6.2-14 is the amount by which the gain is increased by the injection of the dc current I_o. If the value of I_o is 15 times I_{D2}, the gain enhancement is 4. Unfortunately, the square root factor restricts this method to small gain increases.

Fig. 6.2-5*b* shows a method of reducing the gain of the cascode CMOS inverter. It may seem strange to reduce the gain, but many times the gain needs to be reduced. In this case, Eq. 6.2-14 is written as

$$A_v \approx \frac{g_{m1}}{g_{ds2}} = \left[\frac{2K'_N W_1 I_{D1}}{L_1 I_{D2} \lambda_{P2}}\right]^{0.5} = \left[\frac{2K'_N W_1}{L_1 I_{D2} \lambda_{P2}}\right]^{0.5} \left[1 - \frac{I_o}{I_{D2}}\right]^{0.5} \tag{6.2-15}$$

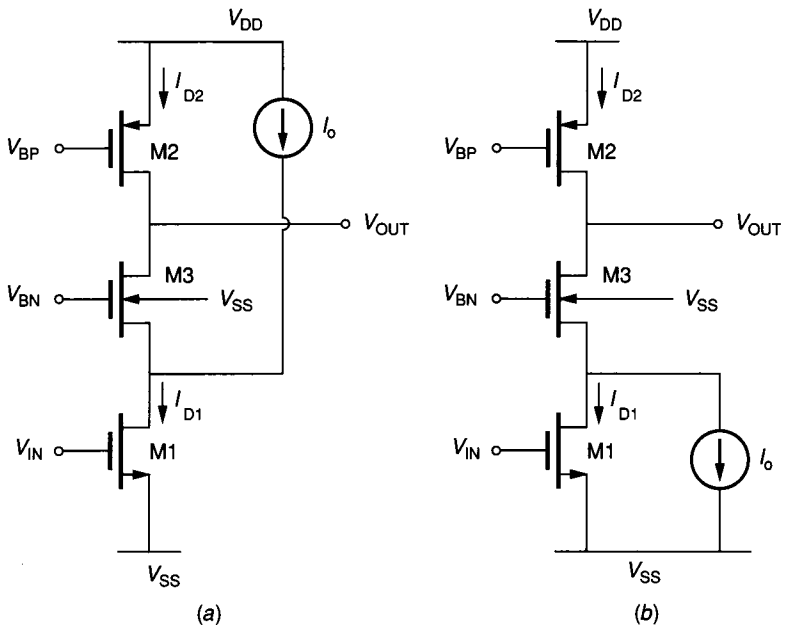


FIGURE 6.2-5
Modification of the ac gain by changing g_{m1}: (*a*) Gain enhancement, (*b*) Gain reduction.

We note that I_o cannot be larger than I_{D2}. The dc current control methods proposed in Fig. 6.2-5 for adjusting the dc gain of the CMOS inverter work primarily because of the low resistance seen at the source of M3.

The addition of a fourth transistor to achieve the cascode CMOS inverter of Fig. 6.2-6 is probably the best method of significantly increasing the ac gain of the CMOS current-source-load inverter. The effect of M4 is to cascode the current source M2 and to boost its output resistance seen by M1 and M3 by roughly a factor of $g_{m4}r_{ds4}$. This causes the output resistance of the inverter to increase the gain. An easy way to calculate the ac gain is to take advantage of previous work. The output resistance of the circuit of Fig. 6.2-6 can be calculated using the result of Eq. 5.3-10. This resistance is the parallel combination of two cascoded current sinks/sources and is expressed as

$$r_{out} = \frac{1}{(g_{ds1}g_{ds3})/(g_{ds1}+g_{ds3}+g_{m3}+g_{mb3})+(g_{ds2}g_{ds4})/(g_{ds2}+g_{ds4}+g_{m4}+g_{mb4})}$$

$$\approx \frac{1}{(g_{ds1}g_{ds3}/g_{m3})+(g_{ds2}g_{ds4}/g_{m4})} \qquad (6.2\text{-}16)$$

Multiplying r_{out} by $-g_{m1}$ gives the ac small signal voltage gain of the circuit of Fig. 6.2-6 as

$$A_v \approx \frac{-g_{m1}g_{m3}g_{m4}}{g_{ds1}g_{m4}g_{ds3}+g_{ds2}g_{m3}g_{ds4}} \qquad (6.2\text{-}17)$$

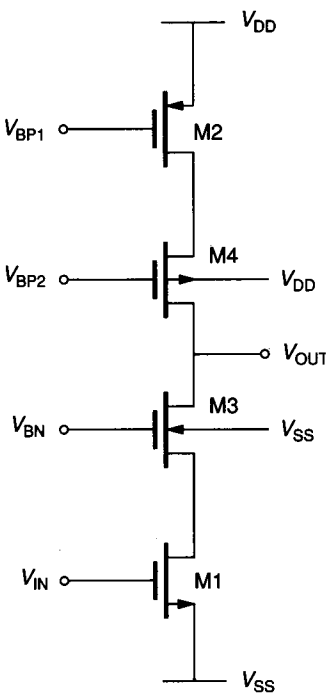


FIGURE 6.2-6
Fully cascoded current-sinking inverter.

It can be seen by comparing Eq. 6.1-50 with Eq. 6.2-17 that the ac voltage gain of the current-source-load inverter has been increased by a factor of approximately $g_m r_o/2$ assuming $g_{m3} \approx g_{m4}$ in Eq. 6.2-17. An example will illustrate some of the preceding concepts.

Example 6.2-1. Improving the performance of a CMOS inverting amplifier. Repeat Example 6.1-2 for the circuit of Fig. 6.2-6 with the following changes. Let all W/L ratios be 10 μ/10 μ and let $V_{BP1} = 3$ V, $V_{BP2} = 1$ V, and $V_{BN} = -1$ V. Assume that the values of capacitances still hold, although the widths of the transistors have changed.

Solution. The current can be found from knowing the voltages across M2. Ignore the drain voltage for the moment. The current is

$$I_{d2} \approx \frac{8}{2}(2 - 0.75)^2 = 6.25\ \mu\text{A}$$

Ignoring the bulk effects on M4 and equating drain currents, it follows that $V_{GS4} = V_{GS2}$. Therefore, the source of M4 or drain of M2 is at 3 V. Using the fact that $V_{sd2} = 2$ V allows the recalculation of I_{d2} including the channel modulation as

$$I_{d2} = 6.25\ \mu\text{A}[1 + (0.02)(2)] = 6.625\ \mu\text{A}$$

Assuming that $V_{sb4} \approx 2$ V gives V_{T4}:

$$V_{T4} \approx 0.75 + 0.4[(2.6) - 0.6]^{0.5} = 1.085\ \text{V}$$

This value of V_{T4} gives $V_{gs4} = 2.372$ V or $V_{sd2} \approx 1.628$ V. We could iterate toward a closer solution, but these results are sufficient. Assuming that the dc value of the output is at 0 V, both M2 and M4 are in saturation.

The dc value of V_{IN} can be found assuming $I_{d1} = 6.625\ \mu$A, to get

$$V_{gs1} = 0.75 + \left[\frac{2(6.625)}{24}\right]^{0.5} = 1.493\ \text{V}$$

Therefore, the quiescent value of V_{in} is -3.507 V. Ignoring the bulk effect on M3 gives $V_{gs3} = V_{gs1} = 1.493$ V so that $V_{d1} = V_{s3} \approx -2.493$ V. Using this value to calculate the threshold voltage of M3 including bulk effects gives

$$V_{T3} \approx 0.75 + 0.8(3.093 - 0.6)^{0.5} = 1.537\ \text{V}$$

This value of V_{T3} gives $V_{gs3} = 2.280$ V. Subtracting this value from -1 V gives $V_{d1} = -3.280$ V or $V_{ds1} = 1.720$ V. We see that both M1 and M3 are also in saturation. As above, we could continue to iterate, but these values are sufficient for this example.

The small signal parameters are found from Table 3.1-3 as

$$g_{m1} = g_{m3} = [2(24)(6.626)]^{0.5}\ \mu\text{S} = 17.83\ \mu\text{S}$$

$$g_{ds1} = g_{ds3} = 0.0663\ \mu\text{S}$$

$$g_{mb3} = \frac{0.8(17.83\ \mu\text{S})}{2(1.720 + 0.6)^{0.5}} = 4.683\ \mu\text{S}$$

$$g_{m2} = g_{m4} = [2(8)(6.626)]^{0.5}\ \mu\text{S} = 10.3\ \mu\text{S}$$

$$g_{ds2} = g_{ds4} = 0.1325\ \mu\text{S}$$

and

$$g_{mb4} = \frac{0.4(10.3\ \mu S)}{2(1.628 + 0.6)^{0.5}} = 1.380\ \mu S$$

Putting these values in Eq. 6.2-15 yields an output resistance of 601 MΩ. Multiplying by $-g_{m1}$ gives an ac voltage gain of −10,716. This gain has been increased over that of Example 6.1-2 for two reasons. The first is the addition of M3 and M4, and the second is the fact that the current is approximately one-half that of the previous example.

Assuming that the dominant pole is the one associated with the output, the −3 dB bandwidth can be found as

$$\omega_{-3dB} = \frac{1}{601\ M\Omega(C_{GD3} + C_{DB3} + C_{GD4} + C_{DB4})} =$$

$$\frac{1}{601\ M\Omega(4.73 + 30.93 + 2.1 + 16.04)pF} = 30.93 \text{ rps or } 4.92 KHz$$

This extremely low bandwidth is a consequence of the high output resistance. The noise-voltage spectral density of the inverter in Fig. 6.2-6 can be found as

$$S_{eq.} \approx \left(100\ nV/\sqrt{Hz}\right)[1 + (10.31/17.83)2]^{0.5} = 115.5\ nV/\sqrt{Hz}$$

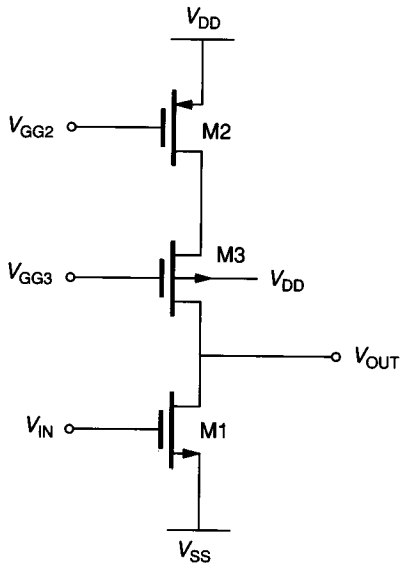
The noise performance is seen to be essentially identical to that of the CMOS inverting amplifier of Example 6.1-2.

One of the purposes of this section is to expand the degrees of design freedom for the inverting voltage amplifier. Example 6.1-5 of the preceding section depicted a case where not all of the design specifications could be met. It is appropriate to reconsider this example to show how the ideas of this section permit the specifications of Example 6.1-5 to be satisfied. The following example gives the details.

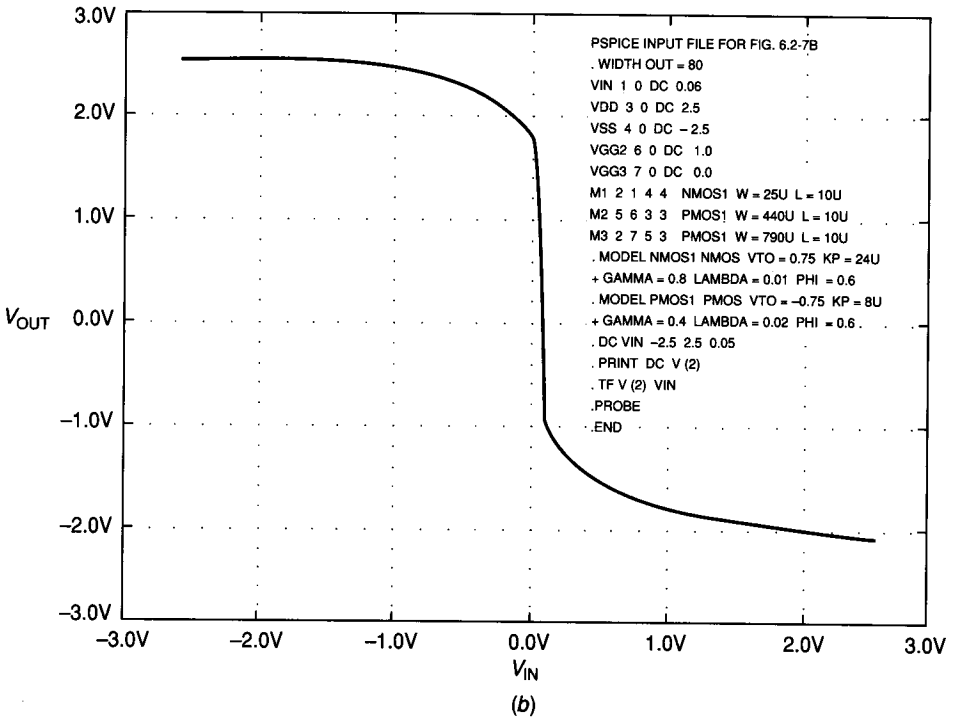
Example 6.2-2. The objective of this example is to show how to meet all of the specifications of Example 6.1-5 using the information introduced in this section. Recall that the design was to achieve a small signal voltage gain greater than −100 using ±2.5 V power supplies and a dissipation less than 1 mW. The amplifier is also to be designed so that the dc value of input and output is 0 V.

Solutions. It was seen in Example 6.1-5 that MOS devices had to be used in order to allow a 2.5 V drop on the input device between the gate (base) and source (emitter). Unfortunately, the dc voltages defined the *W/L* ratios, resulting in a voltage gain of −73.

We will again choose MOS devices for the same reason. If we insert cascode devices in the design of Example 6.1-5, two problems will result. The first is that very little output voltage swing is possible if all transistors are to be kept in saturation. The second is that the gain will be much larger than −100. A better compromise is shown in Fig. 6.2-7*a*. A single n-channel transistor serves as the voltage-controlled current sink (M1) which is the input device and a cascoded current source (M2 and M3) is the load. It is important for the reader to understand the motivation for this choice. If we assume the same dc current level as in Example



(*a*)



(*b*)

FIGURE 6.2-7
(*a*) Circuit for Example 6.2-2, (*b*) Simulation results.

6.1-5, then an inverter such as that of Fig. 6.1-11*b* would have a gain of $-g_{m1}/(g_{ds1} + g_{ds2})$, which for 100 μA of bias current gives

$$A_v \approx \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \frac{-109.5\ \mu S}{1\ \mu S + 2\ \mu S} = -36.5$$

Because we are not using the push-pull configuration, the gain is one-half of -73. Next, we note that if we can use a cascode (M3) in the load, then the effective g_{ds2} in this expression becomes much less than g_{ds1}. Thus, the ac gain will be approximately -109.5, which exceeds the -100 gain specification. Note that this would not have worked if the input device (M1) were p-channel and the load devices (M2 and M3) were n-channel. Because the gate voltage of M2 is under our control (not required to be 0 V), we can carefully design the dc voltages associated with M2 and M3 to provide as much signal swing as possible and still keep these devices in saturation.

Although we are not yet really concerned with signal swing, let us attempt to bias M2 and M3 to achieve a good result. We begin by picking the voltage across the source-drain of M2 as 1 V. The gate voltage is selected to keep M2 in saturation using the following relationship.

$$V_{SD2} > V_{SG2} - |V_{TP}| \rightarrow V_{SG2} < V_{SD2} + |V_{TP}| = 1.75\ \text{V}$$

If we pick V_{GG2} as 1 V, V_{sg2} is 1.5 V, which satisfies the constraint. Assuming the dc current is 100 μA gives W_2/L_2 as

$$\frac{W_2}{L_2} = \frac{2I_D}{K_P'(V_{sg2} - |V_{TP}|)^2(1 + \lambda_P V_{ds2})} = \frac{2(100)}{8(0.75)^2(1.02)} = 43.6 \approx \frac{44}{1}$$

The large value of W/L is due to the choices of dc voltages.

With $V_{bs3} = -2.5$ V, we calculate $|V_{T3}|$ as 1.144 V due to bulk effects. For M3 to remain in saturation, $V_{SG3} < V_{SD3} + |V_{T3}|$ or $V_{DG3} < |V_{T3}|$. Therefore, selecting $V_{GG3} = 0$ V gives a maximum positive output voltage of $|V_{T3}|$ or 1.144 V. This could be increased by increasing V_{GG3}, however with $V_{GG3} = 0$ V no additional bias supply is required. The negative swing can be found by noting that

$$V_{DS1} > V_{GS1} - V_{TN} = 1.75\ \text{V}$$

Therefore, the negative swing is limited to 0.75 V. The value of W_3/L_3 is found from

$$\frac{W_3}{L_3} = \frac{2I_D}{K_P'(V_{sg3} - |V_{T3}|)^2(1 + \lambda_P V_{DS3})} = \frac{2(100)}{8(1.50 - 0.946)^2(1.03)} = 79.11 \approx \frac{79}{1}$$

Again, this large value of W/L is due to the small dc voltage drop associated with M3. If $V_{GG3} > 0$ V, then W_3/L_3 would be even larger, but the positive signal swing would be increased. Since the output signal swing was not a specification, we will leave the design as it is. With the given values, the ac resistance of M2 and M3 seen by M1 is approximately 89 MΩ. The ac gain turns out to be approximately -108, which meets the specification of Example 6.1-5. Figure 6.2-7*b* shows the simulation results of this example. The simulation output file shows that the ac gain is -112.5 and the power dissipation is 0.5 mW. The positive output voltage swing is higher than anticipated because the gain is not influenced significantly when M3 is in the triode region. The value of the output is not 0 V when $V_{in} = 0$ V because the gain is too high and the W/L values have not been precisely chosen. It is not worthwhile

to go back and make this adjustment because the values of the model parameters are not that well known. The best approach is to get as close as possible (as illustrated) and assume that external negative feedback will be used to achieve the desired voltage levels.

6.2.4 The BJT Cascode Amplifier

The principles of increasing the performance of MOS inverting amplifiers covered in this section can also be applied to BJT inverting amplifiers. In the case of the BJT, it is not so important to increase the gain. Therefore, we will focus on the control of the frequency performance of the BJT inverting amplifier. Figure 6.2-8 shows the use of a cascode BJT (Q3) to reduce the Miller effect of the capacitance $C_{\mu 1}$ of Q1 when the amplifier is driven by a high-resistance source (current driver). The circuit of Fig. 6.2-9*a* shows the small signal model of Fig. 6.2-8. We assume initially that the input to the circuit is a current source I_{in}. Figure 6.2-9*b* shows the circuit after rearranging the $g_{m3}V_2$ transconductance source. If we assume that r_{o3} can be ignored, then Fig. 6.2-9*c* results. This simplified small signal model allows us to take advantage of the previous results. The previous development for the MOS version can be used for the BJT. The equations equivalent to Eqs. 6.2-3 through 6.2-5 for the BJT are

$$p_1(\text{cascode}) = -\left[\frac{C_2 + C_3}{g_2} + \frac{C_1 + C_3}{g_1} + \frac{g_{m1}C_3}{g_1 g_2}\right]^{-1} \approx \frac{-g_1}{C_1 + C_3[1 + (g_{m1}/g'_{m3})]} = \frac{-g_{\pi 1}}{C_{\pi 1} + C_{\mu 1}[1 + (g_{m1}/g_{m3})]} \tag{6.2-18}$$

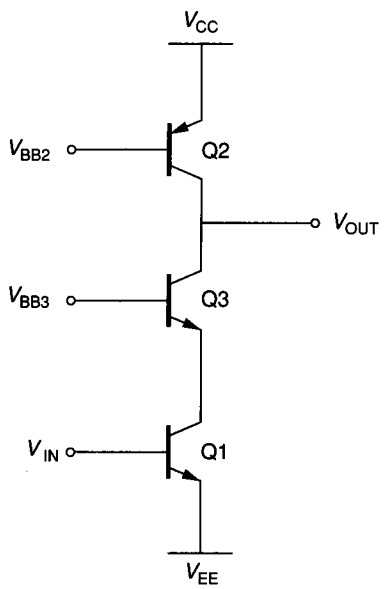


FIGURE 6.2-8
BJT cascoded inverting amplifier.

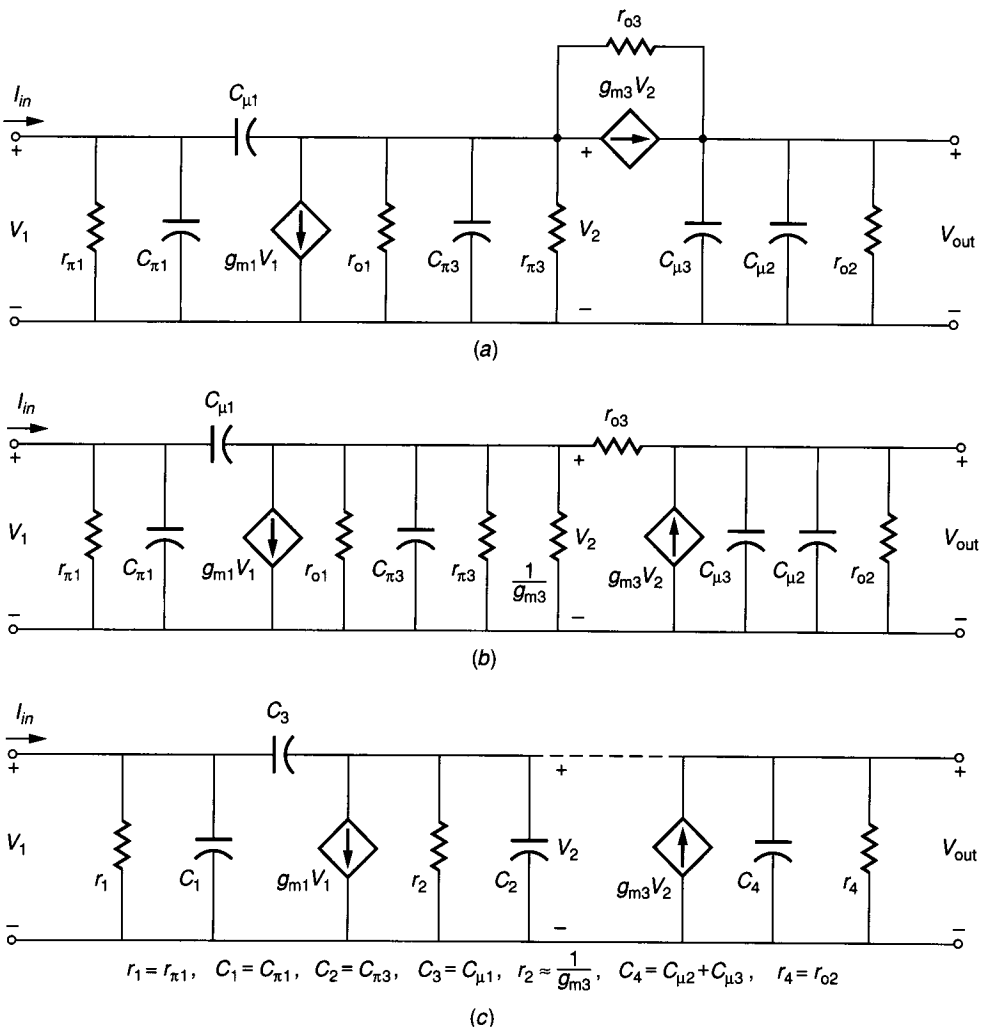


FIGURE 6.2-9
(*a*) Small signal model for Fig. 6.1-8, (*b*) Equivalent model, (*c*) Simplified model.

$$p_2(\text{cascode}) \approx \frac{-g_{m3}[C_1 + C_3 + C_3(g_{m1}/g_{m3})]}{C_1C_2 + C_1C_3 + C_2C_3} =$$

$$\frac{-g_{m3}[C_{\pi 1} + C_{\mu 1} + C_{\mu 1}(g_{m1}/g_{m3})]}{C_{\pi 1}C_{\pi 3} + C_{\pi 1}C_{\mu 1} + C_{\pi 3}C_{\mu 1}} \qquad (6.2\text{-}19)$$

The output pole associated with C_4 is

$$p_3(\text{cascode}) \approx \frac{-g_4}{C_4} = \frac{-g_{o2}}{C_{\mu 2} + C_{\mu 3}} \qquad (6.2\text{-}20)$$

Normally, C_π is greater than C_μ, so the results simplify to

$$p_1(\text{cascode}) \approx \frac{-g_{\pi 1}}{C_{\pi 1}} \tag{6.2-21}$$

and

$$p_2(\text{cascode}) \approx \frac{-g_{m3}}{C_{\pi 3}} \tag{6.3-22}$$

From Eqs. 6.2-20 through 6.2-22, we see that

$$p_3(\text{cascode}) < p_1(\text{cascode}) < p_2(\text{cascode}) \tag{6.2-23}$$

The result is similar to the MOS cascode amplifier. The dominant pole has now been shifted to the output of the amplifier. Note that the p_1 pole of the BJT cascode amplifier is not as sensitive to the source resistance as was the MOS cascode amplifier because of the presence of $r_{\pi 1}$.

The low-frequency gain of the voltage-driven cascode BJT amplifier can also be found from Fig. 6.2-3 using the proper substitutions for the elements, which are obtained by comparing Fig. 6.2-3*a* with Fig. 6.2-9*a*:

$$\frac{V_{\text{out (o)}}}{V_{\text{in (o)}}} = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{v_{\text{out}}}{v_1} = \frac{-g_{m1}(g_{m3} + g_{o3})}{g_{o1}g_{o2} + g_{o1}g_{o3} + g_{o2}g_{o3} + g_{o2}g_{m3}} \approx \frac{-g_{m1}}{g_{o2}} \tag{6.2-24}$$

Comparing this result with Eq. 6.1-71 shows that the influence of the output conductance of Q1 has been eliminated from the voltage gain. Therefore, by comparing Eq. 6.1-71 with Eq. 6.2-24 it follows that the small signal voltage gain of the cascode BJT inverting amplifier should be greater than the gain of a BJT current sink inverting amplifier of Fig. 6.1-8 by approximately a factor of 2 if $|V_{\text{AFN}}| \approx |V_{\text{AFP}}|$. The output resistance is found by the reciprocal sum of the output conductances of Q3 and Q1. From Eqs. 5.3-3 and 5.3-9, the output resistance of Fig. 6.2-8 is

$$r_{\text{out}} = r_{o2} \| r_{o3}[1 + (g_{m3} + g_{o3})(r_{\pi 3} \| r_{o1})] \approx r_{o2} = \frac{I_1}{V_{\text{AFP}}} \tag{6.2-25}$$

Comparing Fig. 6.2-9*c* with Fig. 6.2-3*c* and assuming that the dominant pole is equal to p_3(cascode), then Eq. 6.2-5 gives the -3 dB bandwidth as

$$\omega_{-3\text{dB}} \approx \frac{g_4}{C_4} = \frac{g_{o2}}{C_{\mu 2} + C_{\mu 3}} \tag{6.2-26}$$

Any capacitance at the output of the BJT cascode inverting amplifier must be added to C_4 in Eq. 6.2-26. The noise performance of the BJT cascode inverting amplifier is characterized by the previous analysis for the CMOS cascode inverter amplifier. It can be shown that Eqs. 6.2-12 and 6.2-13 also hold for the BJT cascode inverting amplifier of Fig. 6.2-8.

Example 6.2-3. Repeat Example 6.1-4 for the BJT cascode inverting amplifier of Fig. 6.2-8. Assume that V_{BB3} is -2 V.

Solutions. Using the results of Example 6.1-4, the current in all transistors is seen to be approximately 1.53 mA. Using the values calculated in Example 6.1-4 gives the small signal voltage gain as

$$A_v \approx \frac{-g_{m1}}{g_{o2}} = -\frac{0.059 \text{ S}}{30.7}\ \mu\text{S} = -1928$$

The gain is not increased much due to the fact that g_{o2} is approximately four times g_{o1}. The input resistance is still 1659 Ω and the output resistance is 13 MΩ$\|$32.57 kΩ = 32.49 kΩ. The three poles of the current-driven amplifier are given from Eq. 6.2-20:

$$p_3(\text{cascode}) = 91.06 \text{ Mrps or } 14.5 \text{ MHz}$$

from Eq. 6.2-21:

$$p_1(\text{cascode}) \approx 23.98 \text{ Mrps} = 3.817 \text{ MHz}$$

and from Eq. 6.2-22:

$$p_2(\text{cascode}) \approx 2398 \text{ Mrps} = 381 \text{ MHz}$$

We see that the inequalities of Eq. 6.2-23 are not satisfied in this case. The low output resistance and the high value of C_π compared with C_μ has caused p_1(cascode) to determine the bandwidth. If we assume a 10 pF load at the output, then p_3(cascode) becomes 2.977 Mrps or 0.474 MHz and p_3(cascode) determines the bandwidth. If the poles are closely grouped, then an approximation to the -3 dB bandwidth is given as

$$\omega_{-3\text{dB}} \approx [p_1^2 + p_2^2 + p_3^2]^{1/2}$$

It can be seen that the noise is the same as for Example 6.1-4 if we make the assumption that the contribution of Q3 is negligible. One of the largest differences between this example and Example 6.1-4 is that the -3dB bandwidth of the current-driven cascode is approximately 10 times larger.

One of the reasons for introducing the cascode transistors was to enable a boosting or reduction in gain by current injection or removal from the circuit of Fig. 6.2-8. Because of the high gain available from BJT amplifiers, these techniques are less important and will not be considered. We will complete this section by considering the tremendous gain that can be achieved from the fully cascoded current-sinking inverter of Fig. 6.2-10. This inverter has an output resistance given as

$$r_{\text{out}} = \{r_{o3}[1 + (g_{m3} + g_{o3})(r_{\pi 3}\|r_{o1})]\}\|\{r_{o4}[1 + (g_{m4} + g_{o4})(r_{\pi 4}\|r_{o2})]\}$$

$$\approx r_{o3}(1 + \beta_{FN})\|r_{o4}(1 + \beta_{FP}) = \frac{1}{I_{C3}/[V_{AFN}(1 + \beta_{FN})] + I_{C4}/[V_{AFP}(1 + \beta_{FP})]} \tag{6.2-27}$$

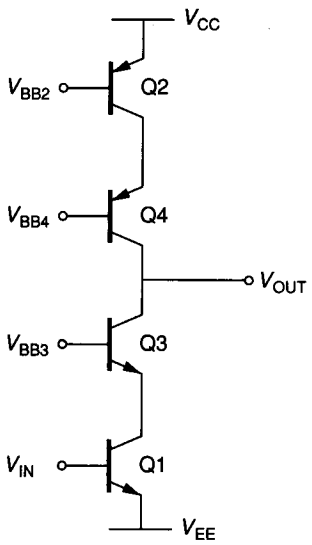


FIGURE 6.2-10
Fully cascoded BJT push-pull inverting amplifier.

The small signal voltage gain of the circuit of Fig. 6.2-10 is given as

$$A_v = -g_{m1}r_{out} = \frac{-I_{C1}/V_t}{I_{C3}/[V_{AFN}(1 + \beta_{BN})] + I_{C4}/[V_{AFP}(1 + \beta_{FP})]} \tag{6.2-28}$$

Normally $I_{C1} = I_{C3} = I_{C4}$ so Eq. 6.2-28 can be written as

$$A_v = -g_{m1}r_{out} = \frac{-1/V_t}{1/[V_{AFN}(1 + \beta_{FN})] + 1/[V_{AFP}(1 + \beta_{FP})]} \tag{6.2-29}$$

Note that the small signal gain of Eq. 6.2-29 is dependent only on the parameters of the BJT models and therefore is the maximum achievable gain given the BJT model parameters. If we assume the values given in Table 6.1-2, the voltage gain of the circuit of Fig. 6.2-10 is −87,420. The reason the gain is so large is that the output resistance is equal to 2.264 MΩ if the dc currents are 1 mA. This high output resistance also causes a low bandwidth. If $C_{\mu 3} = C_{\mu 4} = 0.2$ pF, the −3 dB bandwidth is 1.104 Mrps or 175 kHz if the output resistance is 2.264 MΩ. Typically, the capacitance at the output is more on the order of 10 pF (an oscilloscope probe is typically 14 pF). This causes the −3 dB bandwidth to be 6.81 kHz.

It has been shown how the use of additional devices can improve the small signal performance of the inverting amplifiers covered in Sec. 6.1. The bandwidth is extended in the case of the current-driven inverter. In addition, the gain is increased by two means. The first is the injection of dc current into the transistor acting as a voltage-controlled current sink (or source), and the second is the use of the cascode configuration to increase the ac output resistance.

The additional devices also give an extra degree of design freedom. The techniques presented in this section will be useful in improving or modifying the performance of more complex amplifiers containing inverting amplifiers.

6.3 DIFFERENTIAL AMPLIFIERS

The differential amplifier has become a very useful circuit because of its compatibility with integrated circuit technology, in addition to its ability to amplify differential signals. Any two signals can be decomposed into a *difference-mode* signal, V_D, and a *common-mode* signal, V_C. This is illustrated by the following relations, where V_1 and V_2 are two arbitrary input signals.

$$V_1 = \frac{V_D}{2} + V_C \tag{6.3-1}$$

$$V_2 = -\frac{V_D}{2} + V_C \tag{6.3-2}$$

It is easy to see that V_D and V_C are defined as

$$V_D = V_1 - V_2 \tag{6.3-3}$$

and

$$V_C = \frac{V_1 + V_2}{2} \tag{6.3-4}$$

The objective of the differential amplifier is to amplify only the difference between two input signals, regardless of the level of the common-mode signal.

The differential amplifier is characterized by its differential-mode gain and its common-mode gain. The ratio of the differential-mode gain to the common-mode gain is called the *common-mode rejection ratio (CMRR)*. Ideally, the CMRR should be as large as possible. This normally means that the common-mode gain should be as small as possible. Another characteristic of the differential amplifier is the *input common-mode signal range*, which specifies the range of common-mode values over which the differential amplifier continues to sense and amplify the differential-mode signal. Yet another characteristic that affects the performance of the differential amplifier is offset. When the input differential voltage or the input differential current is zero the output of the differential amplifier may not be zero. *Input offset voltage*, V_{OS}, is the magnitude of a voltage source connected between the inputs of a differential amplifier that would make the output equal to zero. Typically, the common-mode input voltage is also given, since the input offset voltage or current may be dependent on its value. V_{OS} should be treated as a random variable. The *input offset current*, I_{OS}, is the difference between two current sources applied to the inputs of the differential amplifier that is required to make the output equal to zero. I_{OS} should also be treated as a random variable. Both V_{OS} and I_{OS} are dependent on temperature in most differential amplifiers.

6.3.1 CMOS Differential Amplifiers

Figure 6.3-1 shows the circuit of a general MOS differential amplifier. The blocks labeled *active load* can consist of any of the circuits previously discussed that will replace resistances. The key aspect of the differential amplifier is the input source-coupled pair, M1 and M2.

We will first examine the large signal characteristics of the circuit of Fig. 6.3-1. Assume that M1 and M2 are in saturation. Neglecting channel modulation and assuming $V_{T1} = V_{T2}$, it follows that the pertinent relationship describing the large signal behavior is given as

$$V_{ID} = V_{G1} - V_{G2} = V_{GS1} - V_{GS2} = \left[\frac{2I_{D1}}{\beta_1}\right]^{1/2} - \left[\frac{2I_{D2}}{\beta_2}\right]^{1/2} \tag{6.3-5}$$

and

$$I_{SS} = I_{D1} + I_{D2} \tag{6.3-6}$$

where $\beta = K'(W/L)$. Assuming that $\beta_1 = \beta_2 = \beta$, substituting Eq. 6.3-6 into Eq. 6.3-5 and forming a quadratic allows the solution for I_{D1} and I_{D2} as

$$I_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left[\frac{\beta V_{ID}^2}{I_{SS}} - \frac{\beta^2 V_{ID}^4}{4I_{SS}^2}\right]^{1/2} \tag{6.3-7}$$

and

$$I_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\left[\frac{\beta V_{ID}^2}{I_{SS}} - \frac{\beta^2 V_{ID}^4}{4I_{SS}^2}\right]^{1/2} \tag{6.3-8}$$

These relationships are valid only for

$$|V_{ID}| \leq \left[\frac{2I_{SS}}{\beta}\right]^{1/2} \tag{6.3-9}$$

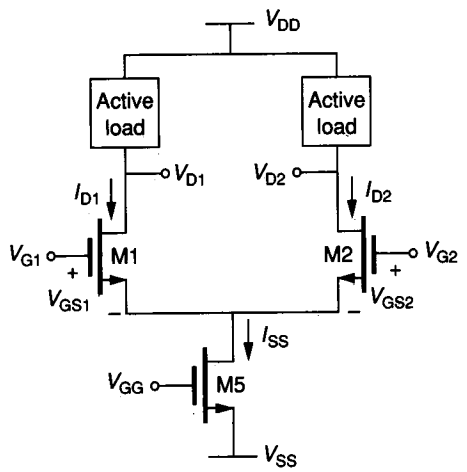


FIGURE 6.3-1
A general MOS differential amplifier configuration. $V_{BS1} = V_{BS2} = 0$.

and for M1 and M2 in saturation. Figure 6.3-2 shows a plot of the normalized drain current of M1 versus the normalized differential input voltage. The large signal voltage transfer characteristics of the differential amplifier can be found by using the results of Eqs. 6.3-7 and 6.3-8 along with the voltage-current characteristics of the active-load devices.

It is of interest to find the regions where M1 and M2 are in saturation. These regions can be found by using the definition in Eq. 6.3-3, rewritten as

$$V_{ID} = V_{G1} - V_{G2} \tag{6.3-10}$$

If we assume symmetry and no common mode excitation, then

$$V_{G1} = \frac{V_{ID}}{2} \tag{6.3-11}$$

and

$$V_{G2} = -\frac{V_{ID}}{2} \tag{6.3-12}$$

Therefore, M1 is in saturation if

$$V_{D1} \geq V_{G1} - V_{TN} = \frac{V_{ID}}{2} - V_{TN} \tag{6.3-13}$$

and M2 is in saturation if

$$V_{D2} \geq -\frac{V_{ID}}{2} - V_{TN} \tag{6.3-14}$$

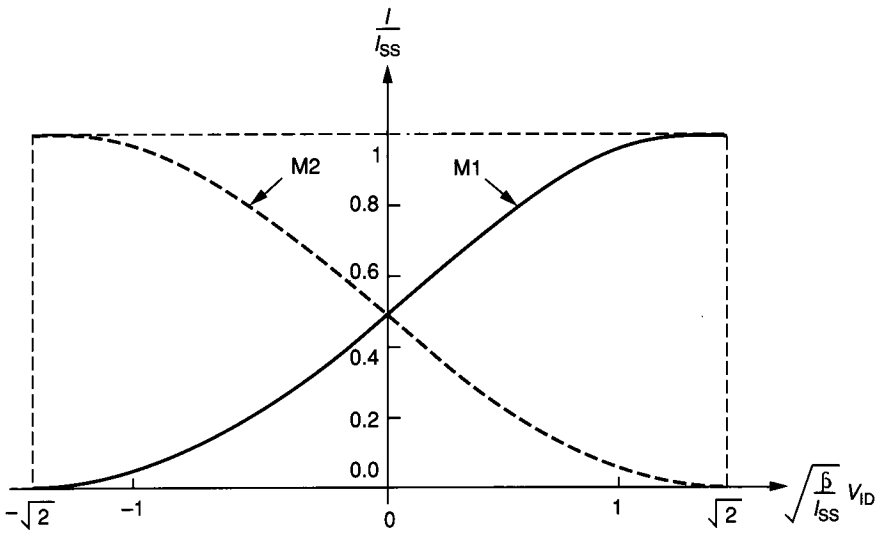


FIGURE 6.3-2
Large signal transconductance characteristic of the MOS differential amplifier.

One way to illustrate these constraints is to plot V_{D1} or V_{D2} as a function of V_{ID}. Assume that the loads of the circuit of Fig. 6.3-1 are resistors of value R_L. Figure 6.3-3 shows a plot of V_{D1} and V_{D2} for an arbitrary value of R_L. Equations 6.3-13 and 6.3-14 are plotted in Fig. 6.3-3 to show the regions where M1 and M2 are saturated. It is seen that the value of R_L will determine how much of the transfer characteristic is in the saturated region. For example, if $I_{SS}R_L \approx V_{DD}$, most of the transfer characteristic of M1 and M2 will be in the saturation region.

It is of interest to find an expression for the large signal transconductance of Fig. 6.3-1. Differentiating Eq. 6.3-7 with respect to V_{ID} and setting the quiescent value of V_{ID} equal to zero gives the differential transconductance of Fig. 6.3-1 as

$$g_m = \left.\frac{\partial I_{D1}}{\partial V_{ID}}\right|_{V_{ID}=0} = \left(\frac{\beta_1 I_{SS}}{4}\right)^{1/2} = \left(\frac{K' I_{SS} W_1}{4L_1}\right)^{1/2} = \left(\frac{K' I_{D1} W_1}{2L_1}\right)^{1/2} \tag{6.3-15}$$

Comparing this result with the expression for g_m of a single transistor (see Table 3.1-3) shows that a difference of 2 exists. The reason for this difference is that only half of the input voltage is applied to M1 or M2 of Fig. 6.3-1, resulting in half the output current. Correspondingly, the transconductance of Eq. 6.3-15 is called the *differential-in, single-ended output transconductance*. The *differential-out transconductance* (g_{md}), can be found by defining a differential output current I_{OD} as

$$I_{OD} = I_{D1} - I_{D2} \tag{6.3-16}$$

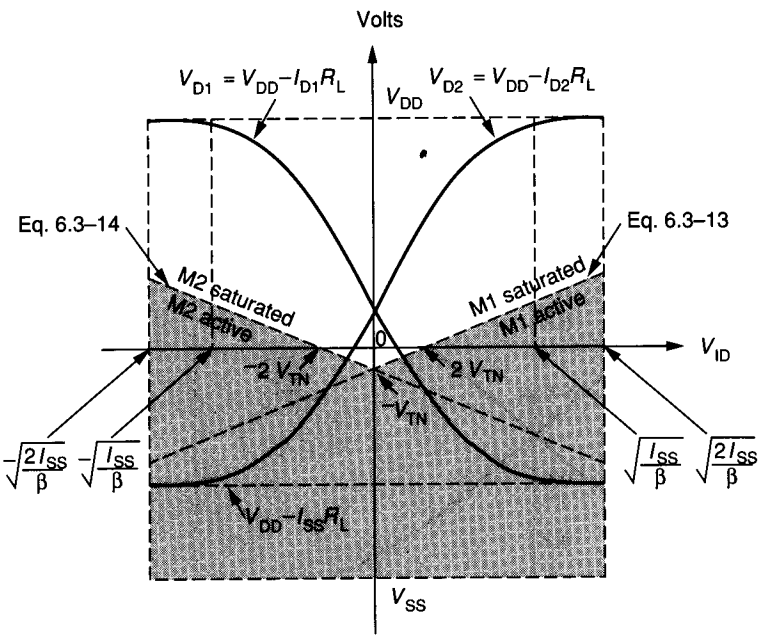


FIGURE 6.3-3
Voltage transfer characteristics of the differential amplifier.

g_{md} can be written as

$$g_{md} = \left.\frac{\partial I_{OD}}{\partial V_{ID}}\right|_{V_{ID}=0} = (\beta_1 I_{SS})^{1/2} = \left(\frac{K' I_{SS} W_1}{L_1}\right)^{1/2} = \left(\frac{2K' I_{D1} W_1}{L_1}\right)^{1/2} \quad (6.3\text{-}17)$$

This transconductance is exactly equal to the transconductance of the common-source transistor if I_D is half of I_{SS}. The presence of I_{SS} in Eqs. 6.3-15 and 6.3-16 illustrates once more the important property that the dc performance is controlled by the dc variables.

The output voltage of the differential amplifier depends on how the active loads of Fig. 6.3-1 are implemented. Assume for the moment that the active loads are replaced by the n-channel enhancement active resistor of Fig. 5.2-2*a*, resulting in the circuit of Fig. 6.3-4*a*. The single-ended output voltages V_{D1} and V_{D2} are given as

$$V_{D1} = V_{DD} - V_{T3} - \left(\frac{2I_{D1}}{\beta_3}\right)^{1/2} \quad (6.3\text{-}18)$$

and

$$V_{D2} = V_{DD} - V_{T4} - \left(\frac{2I_{D2}}{\beta_4}\right)^{1/2} \quad (6.3\text{-}19)$$

where M3 and M4 are saturated. Equations 6.3-7 and 6.3-8 could be substituted into Eqs. 6.3-18 and 6.3-19 to achieve expressions for the drain voltages of M1 and M2 as a function of V_{ID}. These expressions, however, are complex and will be reserved for the problems. Instead, the large signal, differential to single-ended voltage gain will be evaluated at $V_{ID} = 0$ V. Differentiating Eq. 6.3-18 with respect to V_{ID} and multiplying by Eq. 6.3-17 gives

$$A_{vds} = \left(\frac{\partial V_{D1}}{\partial I_{D1}}\right)\left(\left.\frac{\partial I_{D1}}{\partial V_{ID}}\right|_{V_{ID}=0}\right) = -\left(\frac{1}{\beta_3 I_{SS}}\right)^{1/2}\left(\frac{\beta_1 I_{SS}}{4}\right)^{1/2} = -\frac{1}{2}\left(\frac{\beta_1}{\beta_3}\right)^{1/2} \quad (6.3\text{-}20)$$

This gain should be half that of the MOS inverter in Fig. 6.1-11*c* since only half of the input is applied to M1. Comparing Eq. 6.3-20 with Eq. 6.1-34 shows that this relationship holds if the bulk effects, which have been neglected here, are ignored. The differential-in to differential-out voltage gain, A_{vdd}, is equal to the voltage difference between the drains of M1 and M2 divided by V_{ID}. This gain is twice A_{vds} and thus equal to that of an inverter with an enhancement active-load resistor (see Eq. 6.1-33 or 6.1-34).

The ac small signal model of the circuit of Fig. 6.3-4*a* is shown in Fig. 6.3-5*a*. It has been assumed under differential mode excitation that half of v_{id} is applied to the input of each transistor according to the relationship

$$v_{gs1} = -v_{gs2} = \frac{v_{id}}{2} \quad (6.3\text{-}21)$$

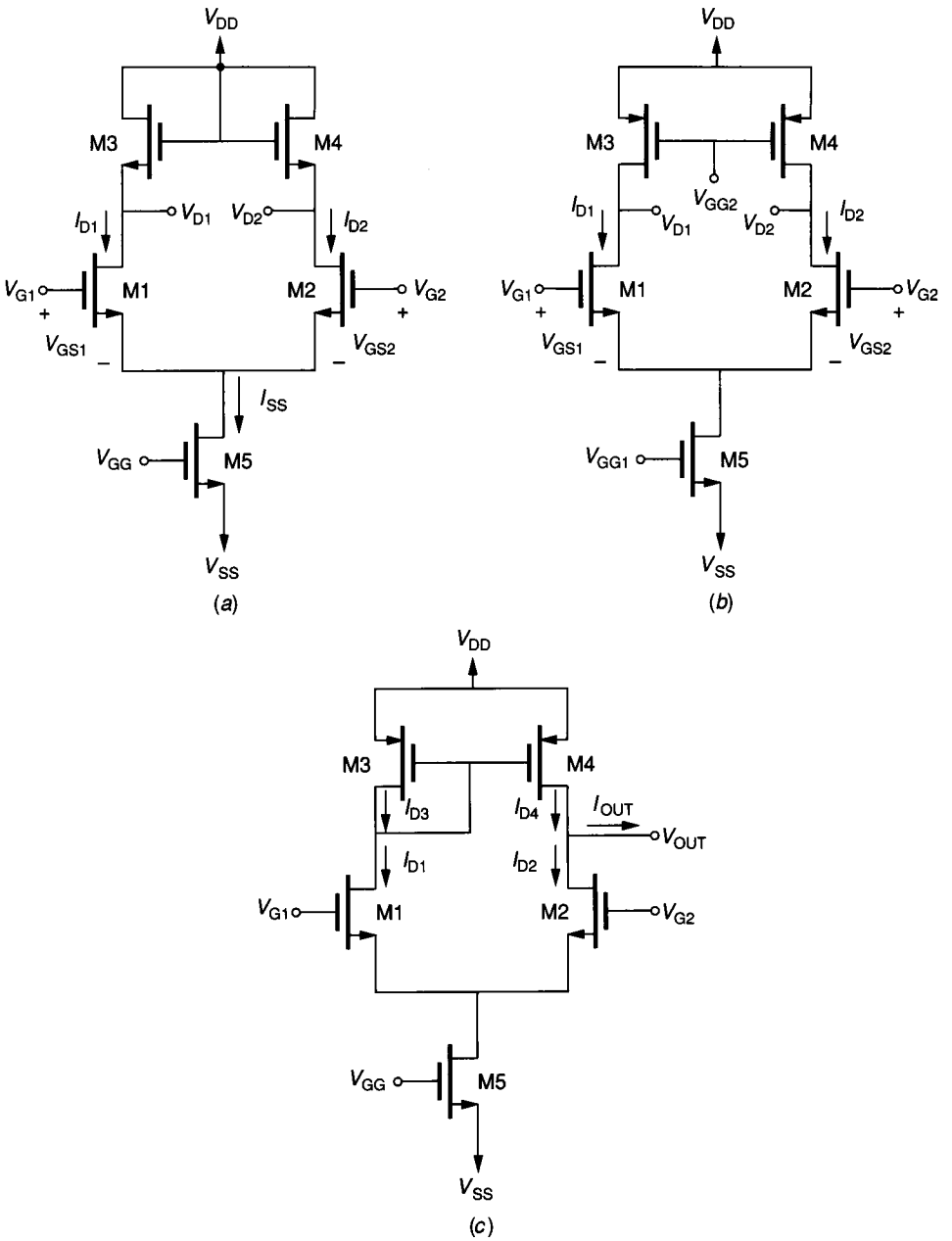


FIGURE 6.3-4
MOS differential amplifiers: (*a*) Enhancement active loads, (*b*) Current source loads, (*c*) Current mirror load.

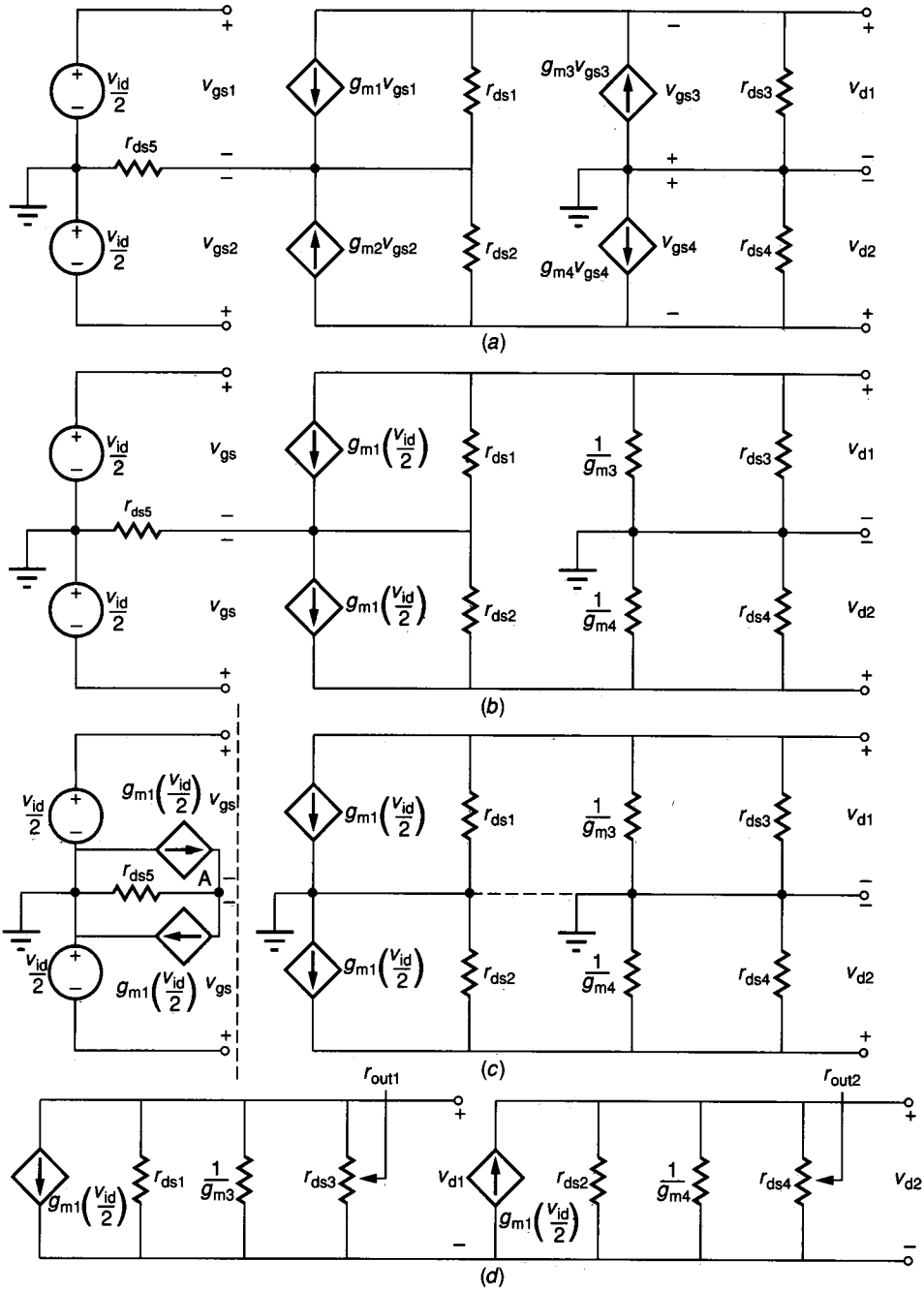


FIGURE 6.3-5
(*a*) Small signal model for differential amplifier of Fig. 6.3-4*a*, (*b*) Use of symmetry to simplify the input circuit, (*c*) Simplification by rerouting the controlled sources $g_{m1}v_{id}/2$, (*d*) Final small signal model.