CHAPTER 7

BASIC DIGITAL BUILDING BLOCKS

7.0 INTRODUCTION

Digital microelectronic circuits dominate the applications of integrated circuits in terms of both sales volume and number of device types. Applications include subcomponents for computer systems and accessories, electronic games, hand-held calculators, digital instrumentation, and the ubiquitous microprocessor. Each of these applications uses circuits that are similar to those previously studied except that they are designed to operate with two-valued, or binary, inputs and outputs. Because these circuits require only two disjoint output voltage ranges to function correctly, practical circuits exist that can function reliably over wide ranges of voltages, currents, temperatures, and process characteristics. A relatively small number of basic digital circuits are used as building blocks. These building blocks are often interconnected to form complex circuits that perform tasks such as those just listed. Following an overview of the digital design process, these basic digital building blocks will be analyzed in this chapter.

MOS digital logic rather than bipolar digital logic is considered in the analysis presented here. The subject of small-scale circuits built from bipolar technology is adequately covered in many references. Most VLSI digital circuits are constructed using MOS technology. Exceptions are I^2L, GaAs, and bipolar gate arrays. These are limited applications compared to MOS VLSI circuits.

In digital circuits it is customary to drop the notations for a bulk connection on MOS transistors and to ignore the bulk effect on threshold voltages for simple logic analysis. When more accurate analysis is required, circuit simulators that include bulk effects are used. As a transition from the notation of previous

chapters (see Fig. 2.2-4), the arrows on the source terminals that indicate n- or p-channel polarity will be dropped for digital circuits. Instead, a bubble on the gate of a transistor indicates a p-channel transistor. The plain enhancement transistor symbol will be used for n-channel transistors, and the filled drain-to-source bar will continue to indicate depletion transistors.

7.1 DESIGN ABSTRACTION

One powerful resource for digital integrated circuit design is the capability to use several levels of abstraction for a complete design. These design levels, as shown in Fig. 7.1-1, can include functional blocks, register transfer descriptions, logic diagrams, circuit schematics, and geometrical circuit layout.

The functional block level is usually described by a block diagram showing the major subcomponents of a design. For a computer, these blocks might include processor, memory, input/output, and special functions such as memory cache or A/D interfaces. These blocks are usually described textually rather than with a formal language, although this is changing.[1] The functional block level is the highest description level from which a designer works.

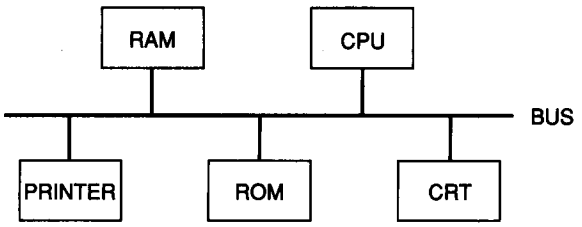
The next highest level, the register transfer level (RTL), consists of programlike statements describing the movement or processing of data between storage elements. One such language, the Instruction Set Processor Specification language,[2] has been used to describe many recent computers and other digital systems. The RTL level allows a formal definition of the operation of a digital processor system. Figure 7.1-1*b* shows a sequence of register transfer operations for a processor that adds the contents of two registers and stores the result in a third register.

The logic diagram is widely used to define the internal operation of blocks described at higher levels. A logic diagram contains well-defined logic functions such as NAND gates and latches, whose digital operation can be accurately described via Boolean logic.[3] For some styles of design, for example, gate array circuits, this is the lowest level of description required from a designer.

The circuit schematic is used to describe integrated circuits at the electrical level as in Fig. 7.1-1*d*. Circuit schematics may be provided for each logic block or may be used to describe portions of the circuit not directly describable by logic blocks—for example, MOS selector circuits or charge storage elements. The circuit level is characterized by discrete electronic components and their corresponding equations of operation. Within classical digital design, this level of detail is used infrequently. Because of the nature of MOS circuits, mixed descriptions are common, with classical logic functions described via logic symbols, and other functions—such as selectors—described by circuit schematics.

The geometrical layout level, depicted in Fig. 7.1-1*e*, most closely describes the physical realization of circuits and gates symbolized at the higher levels. Designer knowledge of this level is desirable because, to a large extent, the geometrical characteristics of circuit layout determine the performance and size of digital integrated circuits.

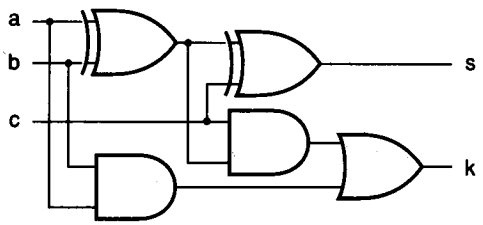
This chapter provides detailed information about several different types of logic circuits and their characteristics. In a later chapter we show that these simple



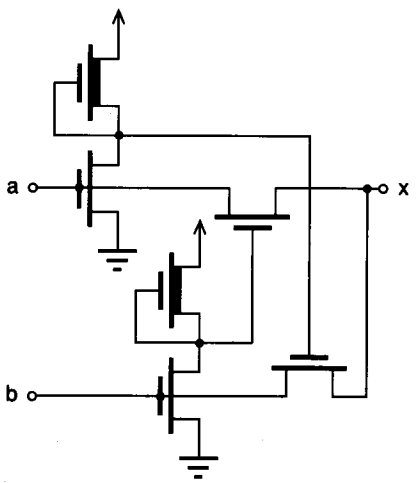
(a)

ADRBUS ← PC
PC ← PC + 1
IR ← DATABUS
ALUINA ← Reg (5)
ALUINB ← Reg (6)
REG (2) ← ALUOUT

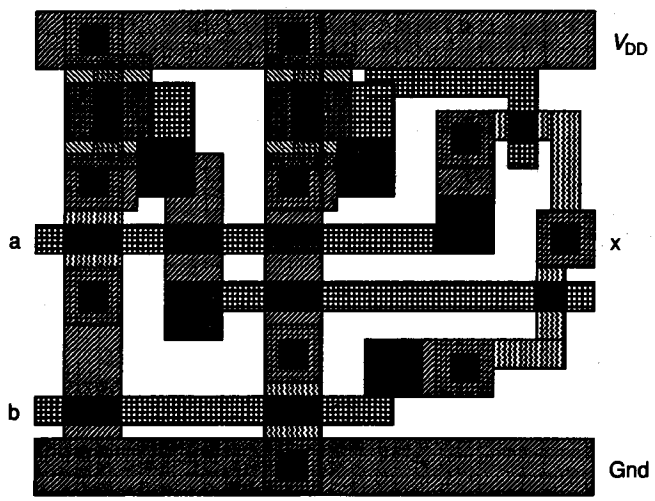
(b)



(c)



(d)



(e)

FIGURE 7.1-1
Levels of abstraction: (*a*) Functional blocks, (*b*) Register transfer level, (*c*) Logic diagram, (*d*) Circuit schematic, (*e*) Geometrical layout.

circuits can be composed into larger subsystems and that these subsystems can be used without specific attention to minute details of each transistor within a design. The capability to provide a hierarchy of increasing functionality with decreasing detail allows a digital circuit designer to create complex systems in a relatively short period of time.

For good digital system design, a designer must be aware of the characteristics and constraints of several levels of abstraction. The purpose of this chapter is to introduce concepts that are important for designing individual logic functions at the logic, circuit, and layout levels. A familiarity with the definitions and interaction of classical logic gates is assumed.

7.2 CHARACTERISTICS OF DIGITAL CIRCUITS

Digital circuits are almost always operated in a two-level, or binary, mode. This means that at steady state, each input and output is in one of two conditions. These conditions (or *states*) are often referred to as the true and false states, the high and low levels, or the 1 and 0 states, respectively. Because circuit outputs are generally voltages, these two states are characterized by two voltage ranges based on V_{IH} and V_{IL}, where $V_{IH} > V_{IL}$. V_{IH} and V_{IL} are called the high and low *logic thresholds*, respectively. It is agreed that if a nodal voltage V satisfies the inequality $V > V_{IH}$, then this node is in the high state; if $V < V_{IL}$, the node is in the low state. Nominally, the extreme limits of the allowable voltage ranges are ground and the supply voltage. If a nodal voltage V satisfies the inequality $V_{IL} < V < V_{IH}$, the state is indeterminate. Indeterminate states must be avoided in digital systems that have reached steady state. The designation of a state thus refers to a voltage range for a nodal voltage in a circuit. Because we are only interested in states, the exact value of the voltage within a range should not be of major concern. A procedure to determine values for V_{IL} and V_{IH} based on the dc voltage transfer characteristic will be given in Sec. 7.11.

7.2.1 Logic Level Standards

Although it might appear that the designer has total control in selecting V_{IH} and V_{IL}, this is not the case, for several practical reasons. First, each integrated circuit technology can generate certain high and low voltage levels more naturally than others. Second, the ability to interconnect distinct integrated circuits requires compatibility of electrical characteristics. Thus, standard voltage ranges and current capabilities for logic states have been defined for different technologies, and integrated circuit vendors from around the world attempt to adhere to these standards for their products. This standardization makes possible the design of complex digital systems that include ICs from different manufacturers. Moreover, it is common for systems manufacturers to insist that two or more sources (vendors) exist for all ICs used in a design. This eliminates sole dependence on the product of a single manufacturer. This *second-source* requirement provides additional incentive for integrated circuit manufacturers to adhere to standards.

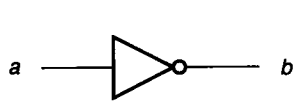
TABLE 7.2-1
Logic voltage specifications

Family	V_{CC}	V_{IL}	V_{IH}
TTL	5.0	0.8	2.0
ALSTTL[1]	5.0	0.8	2.0
ECL	−5.2	−1.5	−1.1
HCMOS[2]	4.5	0.9	3.2
MOS		No standard	
I^2L		No standard	

[1] Advanced Low-Power Schottky TTL
[2] High-speed CMOS

The recognized interface voltage levels for several different logic families are shown in Table 7.2-1.[4,5] Note that standard logic specifications are not provided for MOS and I^2L. Some technologies do not have standard logic voltage specifications because they are used only within large-scale integrated circuits. These large-scale circuits contain input and output interface circuitry to adhere to some widely accepted standard for small-scale logic, usually the TTL logic standard. Although adherence to standards is essential at the input and output terminals of most integrated circuits, such standards are not usually applied internally. Thus, interface circuitry is normally required at all inputs and outputs of an integrated circuit to maintain compatibility with other circuits.

The standard electrical interface characteristics of a logic family are determined essentially by the characteristics of the basic inverter. The symbol for the inverter along with its truth table are shown in Fig. 7.2-1. To investigate the characteristics of a logic family, consider the cascade of inverters shown in Fig. 7.2-2. Assume that all inverters are identical and that the voltage transfer characteristic of an inverter, loaded by a following stage, is as shown in Fig. 7.2-3. Assume the input of the first inverter of Fig. 7.2-2 is at a voltage level V_{i1}, where V_{i1} is in the range that characterizes a high level. The output of the first inverter, V_{o1}, serves as the input to the second stage and is designated as V_{i2} in Fig. 7.2-2. Because of the transfer characteristic of Fig. 7.2-3, $V_{o1} = V_{i2}$ will be in the range that characterizes a low level. Continuing in this manner, one obtains the sequence of input voltages, V_{ik}, where V_{ik} is the input voltage to the kth inverter stage. By repeated application of the inversions of Fig. 7.2-3, it is found that the sequence of high-level voltages, $V_{i1}, V_{i3}, \ldots$, is decreasing and converging to a limit, whereas the sequence of low-level voltages $V_{i2}, V_{i4}, \ldots$, is also converging, typically to a different limit, but in an increasing manner. The limits of these sequences, specifically, V_L and V_H, are termed *equilibrium values*.



(a)

a	b
0	1
1	0

(b)

FIGURE 7.2-1
Basic inverter: (*a*) Symbol, (*b*) Truth table.

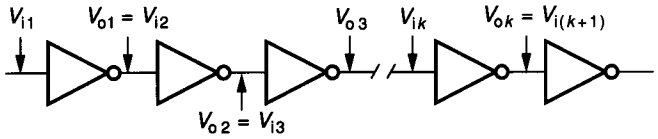


FIGURE 7.2-2
Inverter cascade.

If an inverter with the transfer characteristic of Fig. 7.2-3 is to be useful in a logic family, the low-level sequence must remain in the voltage range that characterizes one of the logic states, and the high-level sequence must remain in the voltage range that characterizes the second logic state. It should be apparent from this example that the shape of the inverter transfer characteristic completely determines the typical logic levels, V_L and V_H, of a logic family. Instead of specifying high and low voltage levels a priori and checking to see if these levels are satisfied for a given inverter, we can ask the related questions: If an inverter has a given transfer characteristic, can this inverter be used as the basis for a viable family of logic? If so, what are the high and low logic voltage levels? These questions are easily answered. We look for the answers by analyzing a pair of cascaded inverters in the next section.

7.2.2 Inverter-Pair Characteristics

First, we examine a pair of inverters in the inverter cascade of Fig. 7.2-2 in greater detail. Assume that the cascade is long enough so that at stage k, the circuit is at equilibrium; that is, $V_{ik} = V_{i(k+2)}$. An *inverter pair*, shown in Fig. 7.2-4*a*, can be thought of as the kth and $(k + 1)$th inverters in the cascade. The transfer characteristic for the inverter pair is shown in Fig. 7.2-4*b* where V_i and V_o are the input and output voltages, respectively. The slope of the transfer characteristic

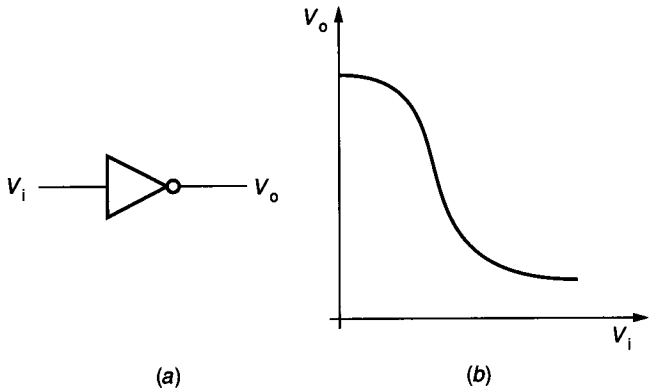


FIGURE 7.2-3
(a) Inverter, (b) Voltage transfer characteristic.

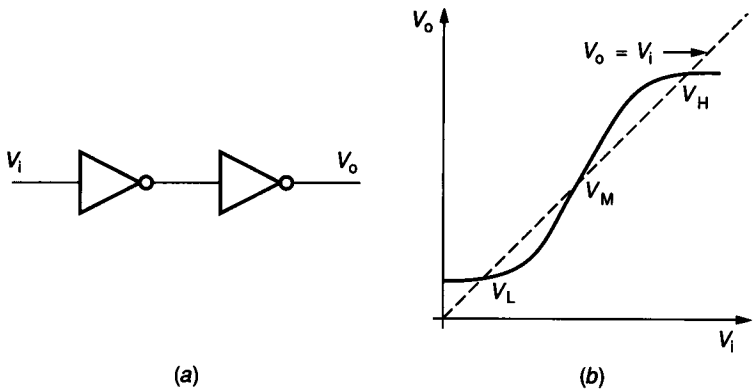


FIGURE 7.2-4
(*a*) Inverter pair, (*b*) Voltage transfer characteristic.

represents the voltage gain of the inverter pair. Note that for an input voltage of zero, the gain is less than one. As the input voltage increases, the gain increases to a value greater than one and then decreases to a value less than one as the input voltage reaches its maximum value. A logic family with an inverter-pair voltage transfer curve that exhibits a gain greater than unity for some region is called a *restoring* logic family. As a counter example, simple diode logic is a *nonrestoring* logic family. Restoring logic is so named because logic signals that are degraded in some way can be restored by the gain of subsequent logic. All widely used electronic logic circuits are of the restoring type.

The inverter-pair characteristic of Fig. 7.2-4*b* can be used to better understand the voltages representing the high and low logic states for a logic family. Note that the input and output voltages of an inverter pair must be equal for equilibrium voltages to exist in the inverter cascade of Fig. 7.2-2. Thus, the equilibrium voltages can be obtained by intersecting the straight line $V_o = V_i$ with the inverter-pair transfer characteristic of Fig. 7.2-4. Note that there are three points of intersection. The extreme intersection points are the high and low equilibrium values, designated by V_H and V_L, respectively. (V_H and V_L should not be confused with the logic threshold voltages V_{IH} and V_{IL} introduced at the beginning of this section.) The equilibrium voltages V_H and V_L represent stable values, as the voltage gain about these points is less than unity. Thus, any small input voltage perturbation about these equilibrium points will be diminished by the inverter pair. The middle intersection point in Fig. 7.2-4*b*, called the *switching threshold voltage* and denoted by V_M, represents an unstable value. Any small input voltage perturbation about V_M will be amplified by the (usually) large voltage gain about this point.

From the preceding analysis, it is apparent that two stable voltage ranges exist for an inverter pair when its characteristic exhibits less than unity gain in two regions. Yet the voltage transfer characteristic should exhibit greater than unity gain to restore degraded signals. Thus, an inverter forms the basis of a viable two-level logic family provided that its inverter-pair transfer characteristic crosses the

unity gain line at exactly three points: V_L, V_M, and V_H. The high and low logic thresholds, V_{IH} and V_{IL}, will be chosen so that $V_H > V_{IH} > V_M > V_{IL} > V_L$.

Additional useful information can be derived from the inverter-pair transfer characteristic. If this characteristic is monotonically increasing and $V_L < V_i < V_H$, then the sequence of high-level output voltages of an inverter cascade with V_i as input will monotonically increase toward V_H and the sequence of low-level output voltages will monotonically decrease toward V_L. For $V_i < V_L$ or $V_i > V_H$, the high-level output voltage sequence will monotonically decrease toward V_H and the low-level output voltage sequence will monotonically increase toward V_L. Thus, the high- and low-level sequences converge to V_H and V_L, respectively.

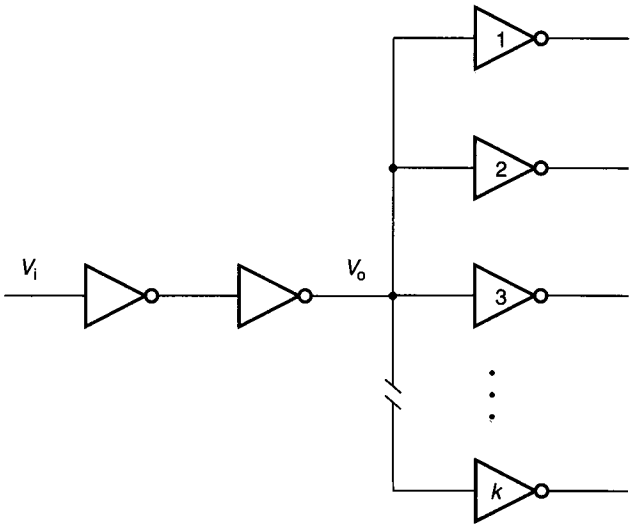
7.2.3 Logic Fan-out Characteristics

The preceding analysis for a cascade of inverters was performed with the assumption that each inverter was loaded by a single, identical inverter to obtain the inverter-pair transfer characteristic. If an inverter output must be capable of driving more than a single load, as shown in Fig. 7.2-5*a*, then the analysis must be performed again to establish high and low logic levels. Assume each inverter output drives k identical inverter inputs. A new inverter-pair transfer characteristic curve can be obtained as in Fig. 7.2-5*b* to show the effects of this loading. Note that increasing the loading on each stage decreases the high-level equilibrium point and increases the low-level equilibrium point, thereby changing the desired voltages for logic levels. However, for MOS logic, the static loading caused by driving multiple loads is so small as to be imperceptible in a transfer characteristic curve such as that of Fig. 7.2-5*b*. Whether a given inverter structure with a specified loading is satisfactory for a logic family depends on the inverter-pair transfer characteristic with loading. The number of identical inverter loads to which a circuit is connected is defined as the *fan-out* of that circuit. The second inverter of Fig. 7.2-5*a* has a fan-out of k. Usually logic level voltage specifications for a logic family are defined for a specific maximum fan-out.

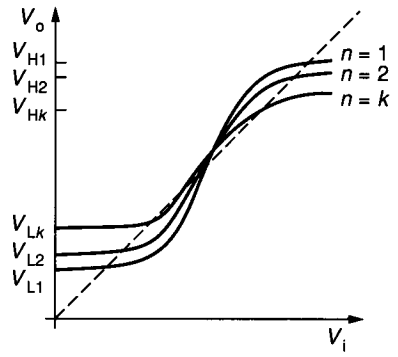
Inverter-pair dc transfer characteristics of some practical logic families are essentially unaffected by fan-out. Specifically, the inputs to logic functions fabricated with MOS technology are oxide-insulated gates of transistors that draw negligible quiescent input currents. Hence, dc characteristics of MOS logic functions are unaffected by fan-out to other MOS logic inputs. However, it will be shown later that the load capacitance attributed to a large fan-out seriously degrades the switching speed of MOS logic.

7.2.4 Digital Logic Analysis

Because the nodal voltages within a digital circuit can assume one of two distinct ranges, such circuits can be analyzed mathematically with Boolean algebra. This systematic way of characterizing digital systems is widely used by digital designers. It is assumed that readers of this book are familiar with the use of Boolean algebra to characterize digital systems. Relevant background information can be found in many references.[3,6]



(a)



(b)

FIGURE 7.2-5
Logic fan-out characteristics (*a*) Inverter with fan-out of k, (*b*) Inverter pair transfer characteristics with fan-out n.

Basic logic building blocks are often combined to realize complex logic functions. The most primitive set of logic functions consists of the AND, OR, and INVERT functions. This set is complete in the sense that any combinational logic function can be realized using only these three functions. However, the simplest electronic circuits used to realize logic functions always provide signal inversion (even diode logic circuits require signal amplification, and thus inversion, to restore voltage levels). Thus, basic electronic circuits provide the NOR rather than the OR and the NAND rather than the AND function. The NAND and the NOR functions are each individually complete in the sense defined previously. Either the NAND or the NOR logic circuit is the preferred structure in a given

technology, causing one of these logically complete functions to be the basic building block for a logic family. This will be described more fully in Sec. 7.4 and Sec. 7.6.

The basic logic circuits are typically termed *logic gates* or simply *gates* because of their ability to control or *gate* logic signal flow. (This term should not be confused with the gate terminal of the MOS transistor.) The characteristics and structure of integrated circuit implementations of these basic logic gates will be studied in the remainder of this chapter.

7.3 SINGLE-CHANNEL MOS INVERTERS

Single-channel MOS technology has been widely used to create large-scale integrated circuits. Early MOS digital circuits used PMOS technology because the natural gate threshold voltage of a p-channel transistor was more suitable for logic applications than was the gate threshold voltage of the n-channel transistor. With the advent of processing techniques such as ion implantation to control the threshold voltage, NMOS became the dominant single-channel technology. Most early microprocessors, including the Motorola 6800 and 6809, the Intel 8080 and 8086, and the Zilog Z80, were manufactured with NMOS processes.

NMOS technology is preferred over PMOS technology primarily because of the greater switching speed achievable with n-channel transistors. MOS transistors are majority carrier devices; thus, the current for an n-channel transistor is carried by electrons whereas that for a p-channel transistor is carried by holes. A silicon semiconductor has an electron mobility that is two to three times its hole mobility. This advantage in charge mobility allows NMOS circuits to operate faster than comparable PMOS circuits. Because the analysis of PMOS and NMOS logic is identical except for a reversal of voltage signs, the predominant device type, NMOS, is used for explanation of single-channel logic circuits in this text.

7.3.1 Basic Inverter

Two basic n-channel inverters are shown in Fig. 7.3-1. Each consists of a pull-down transistor, denoted by M1, and a pullup transistor or load device, denoted by M2. A device connected so as to pull the output voltage to the lower supply voltage—usually 0 V—is called a *pulldown* device; a device connected so as to pull the output voltage to the upper supply voltage—usually V_{DD}—is called a *pullup* device. The circuit of Fig. 7.3-1*a* is termed a *depletion-load* inverter because the pullup device, M2, is a depletion transistor. The circuit of Fig. 7.3-1*b* with an enhancement transistor M2 is termed an *enhancement-load* inverter. Note that these inverters are topologically identical to the analog inverters of Fig. 6.1-11*c* and *d*.

A typical plot of the transfer characteristic for each of these inverters is shown in Fig. 7.3-2, along with the inverter-pair transfer characteristics for devices sized according to the relationship $(W_1L_2)/(L_1W_2) = 4$, where the subscript 1 refers to M1 and the subscript 2 refers to M2. Figure 7.3-2*b* shows that the enhancement-load inverter is incapable of pulling the output any higher

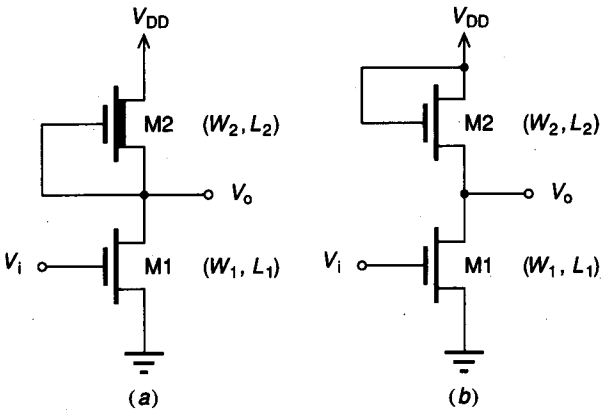


FIGURE 7.3-1
Basic NMOS inverters: (*a*) Depletion-load, (*b*) Enhancement-load.

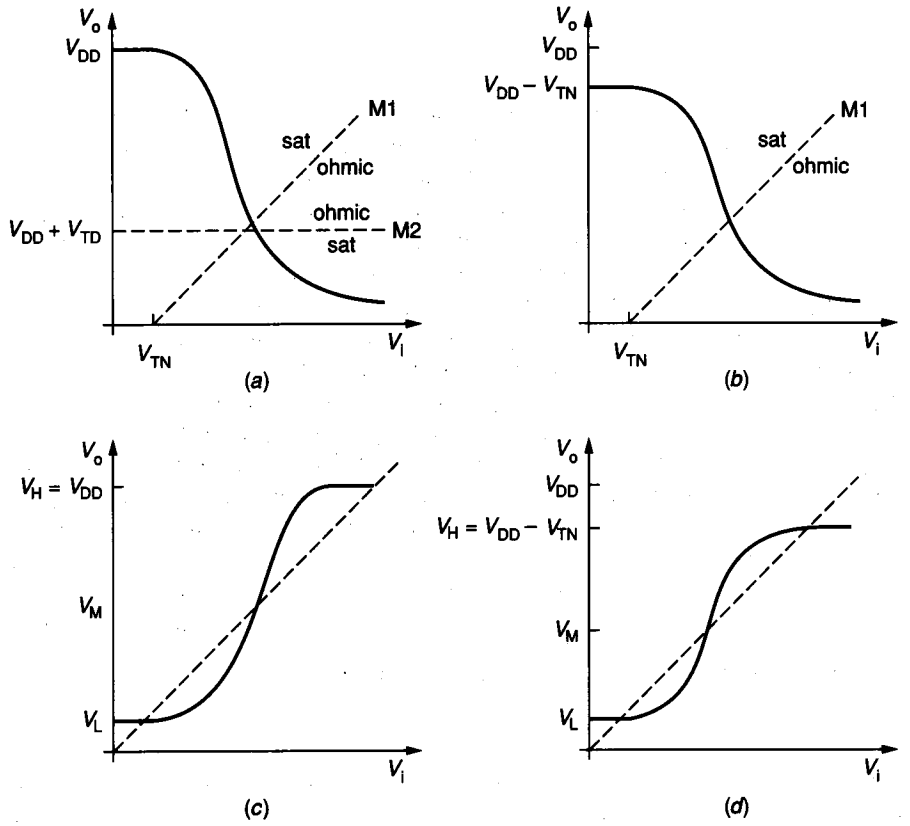


FIGURE 7.3-2
Transfer characteristics of NMOS inverters: (*a*) Depletion-load inverter, (*b*) Enhancement-load inverter, (*c*) Depletion-load inverter pair, (*d*) Enhancement-load inverter pair.

than one enhancement threshold voltage V_{TN} below V_{DD} when the input is at a low level, whereas the output voltage of the depletion-load inverter of Fig. 7.3-2*a* can be pulled to V_{DD}. These high-level output voltages are determined by the pullup transistor types and are nearly independent of device sizing. From the inverter-pair transfer characteristics, it can be seen that a better separation between high and low logic levels is possible with the depletion-load inverter. Good separation between logic voltage levels is important for proper operation of an inverter in the presence of noise voltages.

A layout of a depletion-load inverter with $(W_1L_2)/(L_1W_2) = 4$ is shown in Fig. 7.3-3. From this figure, it should be apparent that the area for the depletion-load transistor is four times as large as that of the input transistor. It should also be observed that inverter layout area is dominated by interconnection and spacing area rather than gate area.

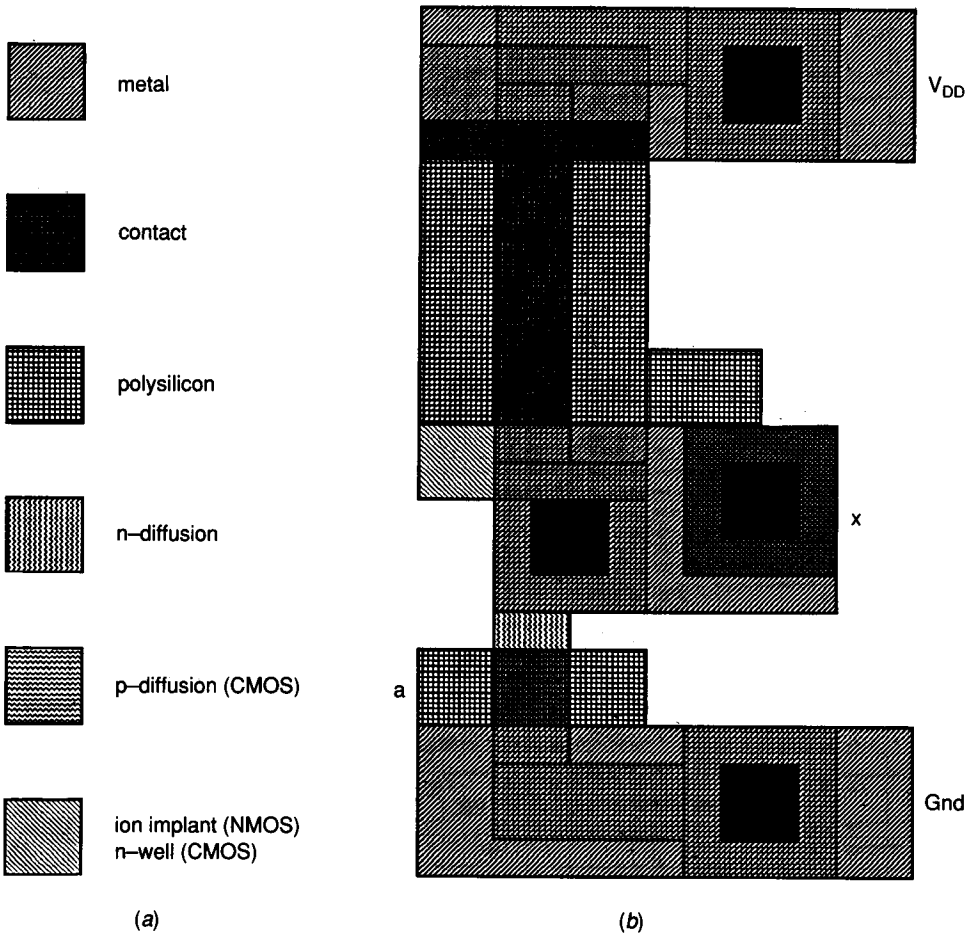


FIGURE 7.3-3
Depletion-load NMOS inverter. (a) Legend, (b) Layout with input *a* and output *x*.

7.3.2 Inverter Device Sizing

The question of how the two transistors forming an inverter should be practically sized naturally arises. Note that for the inverter circuits of Fig. 7.3-1, the highest voltage is determined by the pullup type rather than the pullup size. For example, the depletion-mode pullup acts as a resistor whose I-V characteristic has zero offset voltage from the origin. This causes the output voltage to be pulled to V_{DD} when the enhancement pulldown is off, irrespective of the relative sizes of the transistors. Because transistor sizing has minimal effect on V_H, relative sizing can be advantageously used to put V_M and V_L at acceptable levels.

Consider the depletion-load inverter of Fig. 7.3-1*a*. Because $V_H = V_{DD}$, it would be desirable to have the switching voltage V_M near $V_{DD}/2$ and V_L near 0 V. Observe from the voltage transfer characteristic (Fig. 7.3-2*a*) that M1 and M2 are typically in or near saturation for V_o near $V_{DD}/2$ using reasonable device sizes and process parameters. Hence, assuming that M1 and M2 are saturated, neglecting λ effects and assuming that $V_o = V_i = V_{DD}/2$, it follows from Eq. 3.1-4, upon equating drain currents, that

$$K'\frac{W_1}{L_1}\frac{[(V_{DD}/2) - V_{TN}]^2}{2} = K'\frac{W_2}{L_2}\frac{(V_{TD})^2}{2} \tag{7.3-1}$$

where V_{TN} and V_{TD} are the threshold voltages of the enhancement and depletion devices, respectively. Solving for the relationship between the design parameters, we obtain the expression

$$\frac{W_1L_2}{L_1W_2} = \left[\frac{V_{TD}}{(V_{DD}/2) - V_{TN}}\right]^2 \tag{7.3-2}$$

Defining the geometric device sizing parameter k by

$$k = \frac{W_1L_2}{L_1W_2} \tag{7.3-3}$$

it follows that although the designer has control of the four parameters W_1, W_2, L_1, and L_2, only a single degree of freedom as determined by the parameter k is actually available for controlling V_M. In a typical 5 V digital NMOS process with a desired voltage of 2.5 V for V_M, V_{TD} is set near -3 V and V_{TN} is set near 1 V. Solving Eq. 7.3-2 for the device size ratio gives

$$k = \frac{W_1L_2}{L_1W_2} = \left(\frac{-3}{2.5 - 1}\right)^2 = 4 \tag{7.3-4}$$

This inverter size ratio is important for digital logic circuits and is often termed the *4 : 1 inverter sizing rule*.

With the 4 : 1 size ratio and typical threshold voltages, it is easy to verify the initial assumption that M1 and M2 are at or near saturation when $V_o = V_i = V_{DD}/2$. For positive V_{TN}, the pulldown transistor is saturated for any $V_o = V_i$. For the pullup transistor with $V_{GS} = 0$, saturation occurs when $V_{DD} - V_o > -V_{TD}$. This condition is not satisfied for our example with $V_{DD} = 5$ V, $V_{TD} = -3$ V, and

$V_o = 2.5$ V; however, the shape of the *I–V* characteristic of Fig. 7.8-11 for the depletion-load device shows that the current is nearly constant for voltages near the saturation value. Because V_{DS} for the pullup transistor is within 0.5 V of the saturation value, the assumption of saturation current is reasonable.

Having used the device sizing ratio k to set V_M to $V_{DD}/2$, it is necessary to verify that V_L is near 0 V. To obtain V_L, assume that the inverter input is at V_H, causing $V_o = V_L$. Assume that M1 is in the ohmic region and M2 is saturated (Fig. 7.3-2*a*). Using Eq. 3.1-1 for the ohmic operating region of M1, again neglecting λ effects and equating drain currents, we obtain the expression

$$K'\frac{W_2}{L_2}\frac{(V_{TD})^2}{2} = K'\frac{W_1}{L_1}\left(V_i - V_{TN} - \frac{V_o}{2}\right)V_o \tag{7.3-5}$$

Substituting $V_o = V_L$ and $V_i = V_H = V_{DD}$, it follows from Eq. 7.3-5 with the approximation

$$\left(V_{DD} - V_{TN} - \frac{V_L}{2}\right) \approx (V_{DD} - V_{TN}) \tag{7.3-6}$$

that

$$V_L \approx \frac{W_2 L_1}{L_2 W_1}\frac{V_{TD}^2}{2(V_{DD} - V_{TN})} = \frac{1}{k}\frac{V_{TD}^2}{2(V_{DD} - V_{TN})} \tag{7.3-7}$$

Using the parameters specified earlier and our typical device sizing strategy, it follows that

$$V_L \approx \left(\frac{1}{4}\right)\frac{9}{2(5-1)} = \frac{9}{32}\text{ V} \tag{7.3-8}$$

The assumptions that M1 is ohmic and M2 is saturated are readily verified.

From the previous analysis, we can examine the operation of inverter logic more closely. Consider the flat segment of the transfer characteristic of Fig. 7.3-2*a* corresponding to $V_i < V_{TN}$. For this range of input voltages, the output voltage of a depletion-mode inverter will be at V_{DD}. If the output voltage $V_o = V_{DD}$ is used as the input voltage to a subsequent inverter, its output voltage will be less than V_{TN}, as shown by Eq. 7.3-8. In fact, for depletion-load inverters sized according to the 4 : 1 rule and with normal threshold voltages, any stable interconnection of inverters will have all logic voltages at either V_L or V_H for valid logic inputs.

The previous analysis showed that the 4 : 1 sizing rule gives attractive high and low logic levels that are approximately equidistant from V_M for an inverter. Because no dc loading is experienced when an inverter output drives many inverter inputs within MOS technology, these logic levels are maintained even in the presence of high fan-out. For this reason, the 4 : 1 sizing rule is widely followed in digital logic systems using depletion-load devices.

From a practical viewpoint, it is desirable to minimize area associated with layout. The 4 : 1 sizing ratio specifies only pullup/pulldown ratios and not the width and length of each transistor. Each process technology file specifies design rules for the minimum width and length of a transistor. Often M1 will be a minimum-

size transistor and M2 will have a minimum width resulting in a length for M2 given by

$$L_2 = \frac{4L_1W_2}{W_1} \tag{7.3-9}$$

An alternate construction for an inverter, still satisfying the minimum length and width rules but using less area, can be found (see Prob. 7.12). Subsequently, it will be shown that power and speed considerations may override the minimum area requirement in the determination of the appropriate device sizes.

Throughout the remainder of this book, performance comparisons will be made between a *reference inverter* and other logic circuits. It will be assumed that in any logic family, the sizing of a basic or reference inverter has been specified. The reference inverter used for NMOS will be a depletion-mode inverter formed from a minimum-size enhancement transistor and a minimum-width depletion-mode transistor with length given by Eq. 7.3-9. Although the following discussions are based on this reference inverter, equivalent results may be obtained for reference inverters of other sizes.

It might be instructive to question what improvements, if any, could be obtained by working with a sizing strategy other than 4 : 1. For smaller values of the device sizing parameter k, a modest reduction in area would be attained at the expense of a significant increase in V_L as given by Eq. 7.3-7. This reduces the separation between V_H and V_L, causing the inverter to be more susceptible to noise voltages. Larger values for k offer slight improvements in the signal swing, $V_H - V_L$, at the expense of increases in silicon area. More importantly, it will be shown later that larger k values seriously degrade the switching speed of an inverter.

Finally, it is worth emphasizing that threshold voltages are easily set through process changes. Thus, threshold voltages are chosen specifically to enhance the size and speed characteristics of logic devices. The values $V_{TN} = 1$ V, $V_{TD} = -3$ V and $V_{DD} = 5$ V used in deriving the 4:1 sizing rule are typical for processes used in building digital integrated circuits because they offer reasonable signal swings with practical silicon area requirements.

7.3.3 Enhancement-Load versus Depletion-Load Inverters

Following an analysis similar to the one used for the depletion-load inverter, a sizing rule can be derived for the enhancement-load inverter of Fig. 7.3-1*b*. This analysis would show that the same 4 : 1 sizing rule offers reasonable tradeoffs between signal swing and switching speed. The 4 : 1 sizing rule is thus widely used for single-channel logic circuits.

A comparison of depletion-load and enhancement-load inverters is in order. From a size viewpoint, the silicon area requirements of both types of inverters are nearly the same. From a signal-swing viewpoint, the depletion-load inverter is preferred because the output voltage of the enhancement-load inverter cannot be pulled higher than $V_{DD} - V_{TN}$. From a processing viewpoint, an extra process

step is required for the depletion implant, raising the cost of depletion-mode logic relative to enhancement-mode logic. In terms of switching speed, the depletion-mode inverter is considerably faster than an enhancement-mode inverter in going from a low output voltage to a high output voltage. The reason for this variation is the large difference in equivalent resistances for the two transistors. (Fig. 7.8-11 shows this graphically).

For modern single-channel circuits, the advantages of the depletion-mode inverter far outweigh the cost disadvantage. As a result, enhancement-mode inverters are used only in specialized applications.

Single-channel MOS inverters were analyzed in this section. The inverter device sizing ratio was defined and a ratio of $k = 4$ was found to set the logic threshold near $V_{DD}/2$. Corresponding values of $V_H = V_{DD}$ and $V_L < V_{TN}$ were found with this ratio. A reference inverter was defined as the basis for analyzing a logic family. Depletion-load inverters were found to be preferable to enhancement-load inverters for most applications.

7.4 NMOS NOR AND NAND LOGIC CIRCUITS

In this section NMOS logic gates will be analyzed as extensions of the reference inverter of the previous section. Simple NOR, NAND, and multi-input gates will be considered.

7.4.1 Basic NMOS NOR Logic Circuits

The positive logic NOR function, in which the output is low if any of the inputs are high, is easily realized with NMOS circuits by a parallel connection of two or more pulldown transistors in place of the single pulldown transistor of the inverter circuits of Fig. 7.3-1. Figure 7.4-1 shows a circuit that realizes the positive logic NOR function along with the corresponding logic truth table. Also shown are the Boolean logic equation and the distinctive-shape logic symbol.

The operation of the depletion-load NOR gate will now be considered from a qualitative viewpoint. The analysis of the enhancement-load NOR gate is similar and is left to the reader. If inputs a and b of this circuit are both at a voltage near 0 V, neither of the two parallel pulldown transistors will conduct, and the pullup transistor will pull the circuit output to a voltage near V_{DD}. If either the a or the b input is connected to a voltage near V_{DD}, the corresponding pulldown transistor will conduct, causing the output to be pulled near 0 V irrespective of the other parallel pulldown transistor. Of course, if both inputs are connected to voltages near V_{DD}, then both pulldown transistors conduct, pulling the output to a voltage near 0 V as well.

The device sizing problem for the NOR gate must be addressed. It will be assumed that the device sizing of the NOR gate is done so that for normal input conditions, the high and low logic voltages at the output will be at least as high and low, respectively, as those established for the reference inverter. Thus, a

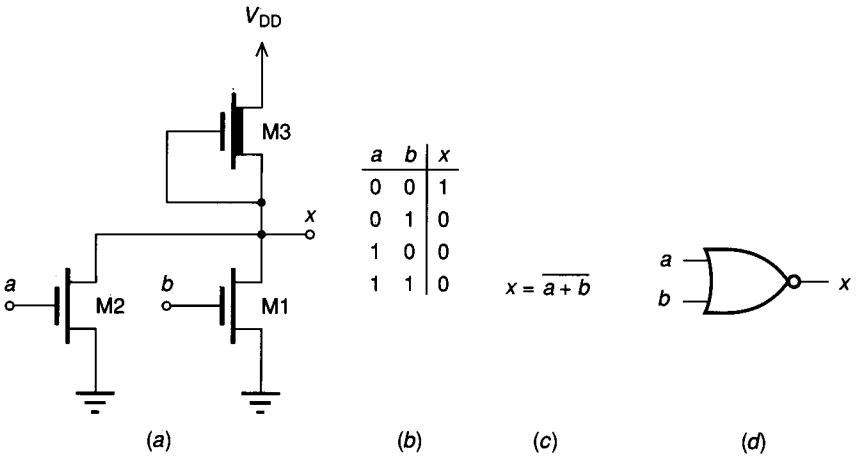


FIGURE 7.4-1
NMOS NOR gate with depletion pullup transistor: (*a*) Circuit, (*b*) Truth table, (*c*) Boolean equation, (*d*) Distinctive-shape symbol.

NOR gate will not cause a deterioration in logic signal levels. The same strategy is generally used to size all logic blocks in a family of logic.

By symmetry, it can be assumed that the pulldown transistors of Fig. 7.4-1, M1 and M2, are the same size. From the corresponding truth table, it is clear that there are only four possible logic conditions for the inputs. These will now be exhaustively considered. If both inputs are low, M1 and M2 are off, causing the output to go to V_{DD} irrespective of any device sizing. If the input to M1 is low and the input to M2 is high, M1 is off and hence allows no current to flow into its drain terminal. This makes the remainder of the NOR gate look like the reference inverter of Fig. 7.3-1*a* with M2 playing the role of the pulldown transistor and M3 the role of the load transistor. To maintain a low voltage level at least as low as that for the reference inverter, M2 and M3 must satisfy the 4 : 1 sizing rule. This results in the requirement

$$\frac{L_3 W_2}{W_3 L_2} \geq 4 \tag{7.4-1}$$

Likewise, if the input to M1 is high and the input to M2 is low, we obtain the requirement

$$\frac{L_3 W_1}{W_3 L_1} \geq 4 \tag{7.4-2}$$

These requirements are equivalent since it was assumed that M1 and M2 are the same size. Finally, if the inputs to both M1 and M2 are high, the M1–M2 combination behaves as a single transistor of width $2W_1$ and length L_1. To maintain the low voltage level, the combination must satisfy the expression

$$\frac{L_3 2W_1}{W_3 L_1} \geq 4 \tag{7.4-3}$$

From Eq. 7.3-7 we can determine that a sizing ratio greater than 4 : 1 causes a lower V_L. The requirements of Eqs. 7.4-1 and 7.4-2 dominate the requirement of Eq. 7.4-3, resulting in the following sizing rule for the NOR gate:

$$\frac{L_3W_2}{W_3L_2} = \frac{L_3W_1}{W_3L_1} = 4 \tag{7.4-4}$$

If each pulldown transistor for a NOR gate is of minimum size, as was the pulldown transistor for the reference inverter, then the load device for the NOR gate should be the same size as the load device for the reference inverter. With this sizing strategy, it is obvious that when both inputs to a NOR gate are high, the output is pulled even lower than the V_L level obtained for the reference inverter. In general, if the sizing rule for the reference inverter is k:1, the corresponding sizing rule for the N-input NOR gate of Sec. 7.4.3 is also k:1.

7.4.2 Basic NMOS NAND Logic Circuits

Figure 7.4-2 shows a circuit that realizes the positive NAND logic function along with its logic truth table, Boolean logic equation, and distinctive-shape logic symbol. For the NAND logic function, the pulldown transistors M1 and M2 are arranged in series rather than in parallel, as was the case for the NOR circuit. The operation of the depletion-load NAND gate will now be considered qualitatively. If either (or both) input a or b is near 0 V, the pulldown transistor corresponding to that input will not conduct. If either pulldown transistor does not conduct, the series path to ground is broken, and the pullup transistor M3 pulls the output

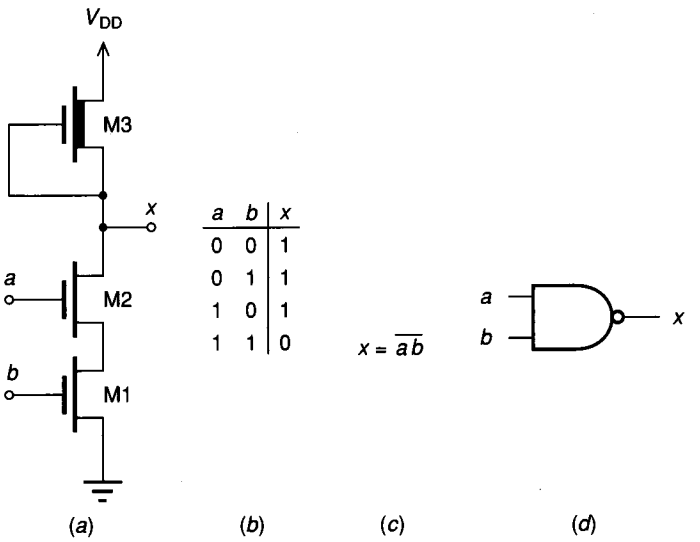


FIGURE 7.4-2
NMOS NAND gate with depletion pullup transistor: (*a*) Circuit, (*b*) Truth table, (*c*) Boolean equation, (*d*) Distinctive-shape symbol.

voltage near to V_{DD}. If both inputs a and b are set to V_{DD}, then both pulldown transistors conduct, pulling the output to a low voltage. This relationship between inputs a and b and output x realizes the NAND logic function.

Device sizing for the NAND gate must be addressed. Once again, it is assumed that the device sizing of the NAND gate is done so that for normal input conditions, the high and low logic voltages at the output will be at least as high and low, respectively, as those established for the reference inverter. With this choice, a NAND gate will not cause a deterioration in logic voltage levels.

The constraint that determines the sizing for the NOR gate corresponds to the weakest pulldown path that will force the output to the low state. For the NAND gate, the *only* pulldown path requires high input levels for both inputs a and b. This condition will determine the sizing for the NAND gate. From a quantitative viewpoint, if M1 and M2 are the same size and both inputs are high, the M1–M2 combination acts as a single transistor of length $2L_1$ and width W_1. To maintain the required output voltage for a low logic level, the 4 : 1 sizing rule can be applied. For the two-input NAND gate this results in

$$\frac{L_3 W_1}{W_3 2L_1} = 4 \tag{7.4-5}$$

or

$$\frac{L_3 W_1}{W_3 L_1} = \frac{L_3 W_2}{W_3 L_2} = 8 \tag{7.4-6}$$

as the sizing rule. In general, if the sizing rule for the reference inverter is k:1, the corresponding sizing rule for the N-input NAND gate of Sec. 7.4.3 is Nk:1.

Two approaches can be followed to achieve the 8:1 ratio for two-input NAND gates. In one approach, the two pulldown transistors are minimum-area devices ($L_1 = W_1 = L_2 = W_2 =$ minimum dimension), requiring the depletion pullup transistor to have the ratio $L_3/W_3 = 8$. In an alternate approach, the load device is sized like the depletion load for the reference inverter, and the two pulldown transistors are sized equally, with $W_1/L_1 = W_2/L_2 = 2$. The first approach is preferred because it provides minimum capacitive loading on preceding logic stages. It can be shown that the total transistor gate area requirement is slightly different for the two sizing strategies (see Prob. 7.14). Also note that, in either case, the minimum total gate area required for the NAND function is larger than that required for the NOR function.

7.4.3 Multi-Input NAND and NOR Logic Circuits

For simplicity, two-input gates were analyzed in the preceding section. Multi-input logic functions, with three or more inputs to a gate, are also widely used. An N-input NOR gate is easily formed by adding $N - 2$ enhancement transistors in parallel with the M1 and M2 transistors of Fig. 7.4-1. An N-input depletion-load NOR gate is shown in Fig. 7.4-3. Multi-input NOR gates that follow the same k:1 sizing rule given for the two-input NOR gate have the same V_L and V_H values as the reference inverter with a sizing ratio of k.

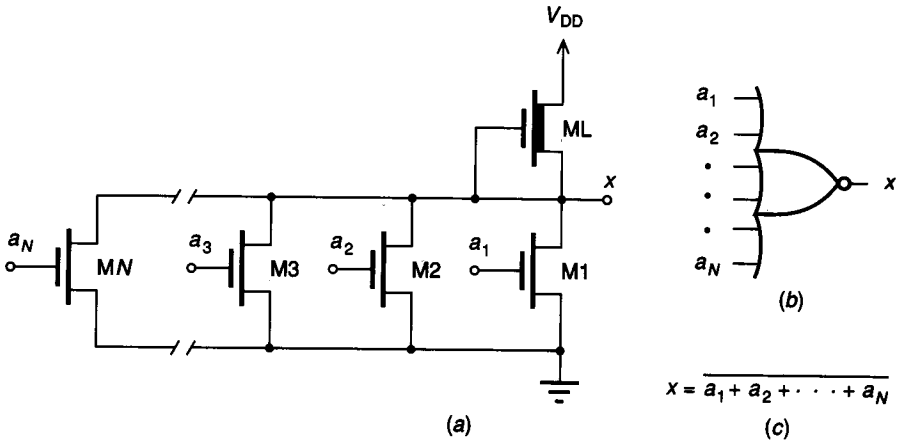


FIGURE 7.4-3
Multi-input NOR gate: (*a*) Circuit, (*b*) Distinctive-shape symbol, (*c*) Boolean equation.

Multi-input NAND gates are formed by adding enhancement transistors in series with the M1 and M2 pulldown transistors shown in Fig. 7.4-2. An N-input NAND gate requires the addition of $N - 2$ transistors in series, as shown in Fig. 7.4-4. Unfortunately, the ratio of the size of the load device to that of the pulldown devices increases with the number of inputs to maintain a good low logic voltage. This sizing ratio becomes Nk:1. An increase in this size ratio increases area and decreases switching speed. As a consequence, single-channel NAND gates with more than two or three inputs are seldom used. Rather, an equivalent multi-input NAND circuit is formed from the appropriate interconnection of inverters and multi-input NOR gates (see Prob. 7.17).

NAND and NOR logic gates are realizable directly as simple modifications to the reference inverter and are more widely used than AND or OR logic gates. When the AND or OR functions are required, they are realized by cascading a basic inverter after a NAND or a NOR gate, respectively.

The structure and sizing of two-input NOR and NAND gates in the NMOS technology were presented in this section. The analysis was generalized to N-input NAND and NOR gates.

7.5 COMPLEMENTARY MOS INVERTERS

The first MOS-based technology to be widely applied at the small-scale integration level was complementary MOS, or CMOS. However, because of the relative simplicity of processing and layout for single-channel MOS circuits, PMOS and then NMOS technologies were the first to achieve widespread use in large-scale integrated circuits. The few early large-scale CMOS circuits were reserved for applications that required the low power dissipation, stable temperature characteristics, or high noise immunity achievable with a CMOS process. Although such characteristics are desirable for all applications of integrated circuit technology, CMOS integrated circuits had disadvantages that limited their use in early VLSI designs.

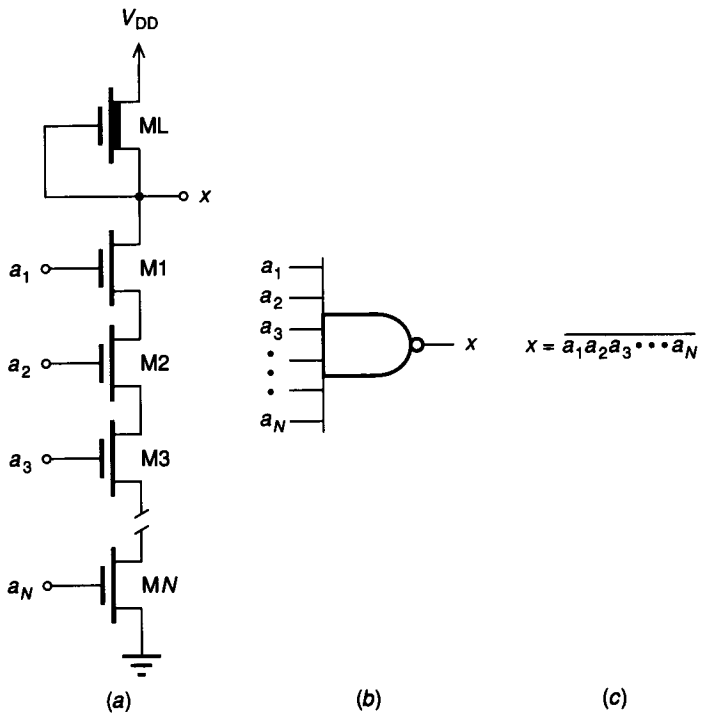


FIGURE 7.4-4
Multi-input NAND gate: (*a*) Circuit, (*b*) Distinctive-shape symbol, (*c*) Boolean equation.

The CMOS fabrication process is more complicated than NMOS fabrication, requiring additional steps to complete the processing of a wafer. Addition of p-channel transistors to a p-substrate process requires creation of an n-well area for the p-channel transistors. This reduces the achievable circuit density compared to an NMOS process. Similarly, a p-well area is required to add n-channel transistors to an n-substrate process. Also, traditional CMOS logic circuits require additional transistors compared to their NMOS counterparts. These disadvantages translate to increased fabrication costs with lower integrated circuit yield for CMOS.

Recent advances in fabrication methods for CMOS technology and in circuit design techniques for CMOS digital circuits have made CMOS more practical for large-scale applications. Also, the need to provide multiple-threshold n-channel devices for speed and power purposes has complicated the standard NMOS process. These factors have changed the relative merits of NMOS versus CMOS technologies for large-scale digital circuit design. Most integrated circuit manufacturers now use CMOS for new designs. For example, both the Intel 80386 and the Motorola 68030 microprocessors are fabricated with CMOS processes. Also, many integrated circuit manufacturers offer CMOS gate array circuits to provide large-scale integration of digital systems functions. In this section, basic CMOS inverter circuits are discussed.

7.5.1 A Basic CMOS Inverter

A CMOS inverter is similar to an NMOS inverter in that two transistors are required. In the CMOS inverter of Fig. 7.5-1*a*, the p-channel transistor M2 acts as a pullup device, and the n-channel transistor M1 acts as a pulldown device. In fact, for some CMOS processes (n-well process), the pulldown transistor is identical to its NMOS counterpart. The primary distinction between NMOS and CMOS inverters lies in the characteristics of the pullup transistors. For NMOS, either a passive enhancement pullup device or a passive depletion pullup device is used, with the depletion pullup preferred from a speed standpoint. In a CMOS process, an actively driven p-channel transistor is normally used as the pullup device. This p-channel pullup transistor is turned on by a gate signal that is opposite in polarity to the gate signal required to turn on the n-channel pulldown transistor. The digital symbol for the p-channel pullup device, shown in Fig. 7.5-1*b*, emphasizes this complementary polarity by showing the gate connection with a bubble to represent signal inversion. This symbol is preferred for digital CMOS circuits. As explained in Sec. 7.0, source designations are assumed understood with this notation. The use of opposite-polarity (complementary-polarity) transistors for load devices characterizes the CMOS inverter.

7.5.2 CMOS Inverter Logic Levels

Note that in the CMOS inverter of Fig. 7.5-1, the gates of both transistors are connected to the inverter input, unlike the comparable NMOS inverter circuit of Fig. 7.3-1. This circuit functions as an inverter because of the opposite transfer characteristics of the n-channel pulldown transistor and the p-channel pullup transistor. The threshold voltages, V_{TP} and V_{TN}, are established so that a voltage $V_i > V_{DD} + V_{TP} = V_{DD} - |V_{TP}|$ on the common gate node causes the n-channel device to conduct while it causes the p-channel device to turn off. (To reduce the potential for error, the notation $(-|V_{TP}|)$ will replace (V_{TP}) to ensure that

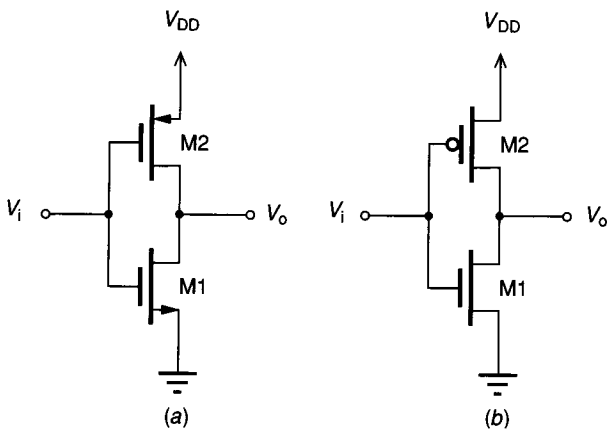


FIGURE 7.5-1
CMOS inverter circuit: (*a*) n-channel and p-channel designation, (*b*) Preferred notation for digital circuits.

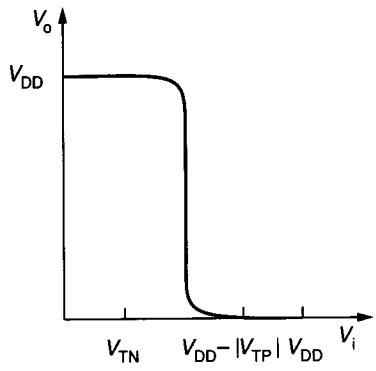


FIGURE 7.5-2
Voltage transfer characteristic for CMOS inverter.

a negative value is used in calculations with V_{TP}.) This results in an active pulldown capability at the output of the circuit. Because the pullup device is off, the pulldown transistor does not have to compete to establish a low-voltage condition on the output. At steady state, the output voltage will reach $V_o = 0$ V. On the other hand, a voltage $V_i < V_{TN}$ on the common gate node causes the n-channel device to turn off while it causes the p-channel device to conduct. This condition provides an active pullup transistor without competition from a pulldown device, allowing the inverter output to be pulled high. At steady state, $V_o = V_{DD}$ for this condition. Figure 7.5-2 shows a typical voltage transfer characteristic for a CMOS inverter.

For valid logic input voltages, note that when one transistor of a CMOS inverter is conducting, the complementary transistor is off. This condition is especially important for two reasons. First, it virtually eliminates static power dissipation in CMOS logic circuits because no current can flow from the voltage supply to ground through the inverter in steady state. Second, it allows a maximum logic voltage swing equal to the supply voltage V_{DD}.

Consider the steady state effect of a logic high voltage on the cascade of CMOS inverter stages of Fig. 7.5-3. Assume that a logic high voltage $V_{i1} > V_{DD} - |V_{TP}|$ is provided at the input to the first inverter. The output of this inverter will reach $V_{o1} = 0$ V because the pullup transistor is off for this input condition. Thus, the input to the second inverter is $V_{i2} = V_{o1} = 0$ V. This gives the condition $V_{i2} < V_{TN}$, causing the n-channel pulldown device of the

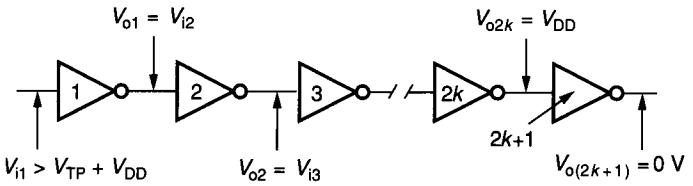


FIGURE 7.5-3
CMOS inverter cascade.

second inverter to be off. The output is then pulled to $V_{o2} = V_{DD}$ by the p-channel transistor. An extension of this analysis to the kth inverter pair shows that $V_{TN} > V_L = 0$ V and $V_{DD} - |V_{TP}| < V_H = V_{DD}$. This provides an ideal voltage swing of

$$V_H - V_L = V_{DD} - 0 \text{ V} = V_{DD} \tag{7.5-1}$$

The best possible voltage swing for a single-polarity inverter output is equal to the difference between the upper and lower supply voltages to the inverter—in this case, V_{DD} and 0 V. It should be obvious that an analysis starting with a logic low voltage of $V_{il} < V_{TN}$ for the CMOS inverter cascade will yield the same values for V_H and V_L.

7.5.3 Inverter Device Sizing

Device sizing for a CMOS inverter will now be considered. The ability of either transistor in a CMOS inverter to act as a low-resistance device with the complementary transistor turned off allows the design of ratioless inverters. A *ratioless* logic device is one in which, from a logic-level viewpoint, the steady state output voltage levels are independent of the ratio of the pullup and pulldown transistor sizes. This is in contrast to the single-channel inverters of Sec. 7.3, which are known as *ratio* logic devices because the pullup/pulldown size ratio k determines one of the equilibrium voltages V_L. The independence of logic voltage levels and transistor sizes allows other considerations to determine the relative sizes of the pullup and pulldown transistors in a CMOS inverter.

The primary effect of the sizes of the pullup and pulldown transistors is on the equivalent resistance of the transistors in the conducting state. Thus, sizing can be used to provide approximately equal capability to source or sink load current; this equality is termed *symmetric output drive*. In contrast, NMOS inverters provide asymmetric output drive because of the difference in pullup and pulldown resistance needed to achieve useful logic levels. The symmetric drive capability of CMOS allows comparable transition times for output voltages irrespective of the direction of the transition.

It is interesting to determine the relative sizes of n-channel and p-channel transistors required to achieve symmetric output drive for a CMOS inverter. An n-channel transistor for either an NMOS or an n-well CMOS process can be fabricated with similar characteristics. The minimum channel lengths and widths of transistors in both processes are set primarily by the resolution of the fabrication process. The transconductance parameter K'_N of an n-channel transistor is about two or three times greater than the transconductance parameter K'_P of a p-channel transistor; a factor of 2.5 is used in this analysis. This factor is caused primarily by the difference in majority carrier mobility for the p- and n-channel transistors described previously. The transconductance parameter difference influences the effective pullup and pulldown resistances of the p-channel and n-channel transistors. The equivalent resistances for the n-channel transistor R_N and for the p-channel transistor R_P are directly proportional to L and inversely proportional to K' and W as indicated by equations

$$R_N \propto \frac{L_N}{W_N K'_N} \tag{7.5-2}$$

and

$$R_P \propto \frac{L_P}{W_P K'_P} \tag{7.5-3}$$

Simple models for the n-channel and p-channel transistors composed of an ideal switch and the effective pullup and pulldown resistances are shown in Fig. 7.5-4 (also see Sec. 3.1-9). The switch is open or closed corresponding to the gate-to-source voltage that turns the transistor off or on, respectively. This simple model is useful for predicting current drive capability and approximating propagation delays in digital applications. Because the proportionality constants for Eqs. 7.5-2 and 7.5-3 are comparable, it follows that

$$R_N \approx \left(\frac{L_N}{W_N K'_N}\right)\left(\frac{W_P K'_P}{L_P}\right) R_P \tag{7.5-4}$$

For symmetric output drive, it is required that $R_N = R_P$. If $K'_N = 2.5K'_P$, then according to Eq. 7.5-4, the devices must be sized with

$$\frac{L_N W_P}{W_N L_P} = \frac{K'_N}{K'_P} = 2.5 \tag{7.5-5}$$

With this sizing, the n-channel and p-channel transistors have symmetric *I–V* characteristics. The layout for a CMOS inverter with these characteristics is given in Fig. 7.5-5. Note that the p-channel transistor width is 2.5 times the width of the n-channel transistor. In practice, symmetric drive capability is often sacrificed by the use of minimum-size transistors to reduce layout area.

In this section a basic CMOS inverter was analyzed. It was found that the output logic voltage levels of $V_L = 0$ V and $V_H = V_{DD}$ were ideal. Because the CMOS inverter is a ratioless logic circuit, device geometries can be used to obtain symmetric output drive.

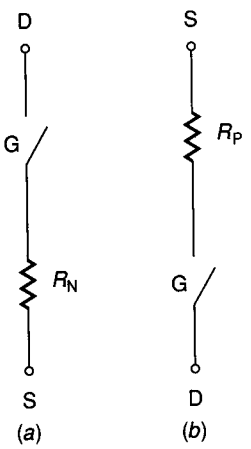


FIGURE 7.5-4
Simple transistor models for digital applications: (*a*) n-channel, (*b*) p-channel.