power dissipation (heat flow) can be specified. The thermal resistance θ_{JA} for a plastic 40-lead package is about 100°C/W, and a maximum integrated circuit junction temperature T_J of about 150°C is specified for reliability considerations. The thermal resistance θ_{JA} is the sum of junction to die, die to package, and package to ambient resistances.[9] If the maximum ambient temperature T_A is expected to be 50°C, then the maximum power dissipation is limited to

$$P_D = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 50}{100} = 1 \text{ W} \tag{7.10-1}$$

Most plastic or ceramic integrated circuit packages can dissipate 1–2 W of power in an ambient temperature of 70°C. As a second, special consideration, low power dissipation is important in applications that must operate from batteries. In this section the main sources of power dissipation are identified, first for NMOS circuits and then for CMOS circuits.

7.10.1 NMOS Power Dissipation

To help explain integrated circuit power dissipation, consider the reference inverter of Fig. 7.10-1. When V_i is low, M1 is off, causing a supply current I_D of 0 A. Hence, the power dissipation is essentially zero! If, however, V_i is high (V_{DD}), then M1 is ohmic and M2 is saturated, so from Eq. 3.1-4

$$I_D = K'\left(\frac{W_2}{L_2}\right)\frac{V_{TD}^2}{2} \tag{7.10-2}$$

With $K' = 20\ \mu\text{A/V}^2$, $L_2 = 4W_2$, and $V_{TD} = -3.5$ V, the drain current is $I_D = 31\ \mu$A. Hence, the power dissipation of this single inverter with $V_i = V_{DD} = 5$ V is approximately 150 μW. Although the power dissipation of a single inverter is small, VLSI circuits contain thousands of inverters and gates. If, on the average, half of the inputs are in the low state and half are in the high state, then a circuit with N reference inverters will have an average *static power dissipation* of

$$P_{avg} = \left(\frac{N}{2}\right)150\ \mu\text{W} \tag{7.10-3}$$

and a worst-case power dissipation of

$$P_{wc} = (N)150\ \mu\text{W} \tag{7.10-4}$$

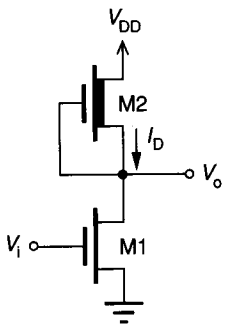

FIGURE 7.10-1
NMOS reference inverter.

From the NOR gate of Fig. 7.4-3, it can be concluded that if the pullup device ML is the same size as the pullup device of the reference inverter, then the power dissipation of the multi-input NOR is the same as that of the reference inverter. This is true irrespective of the number of inputs to the NOR gate.

Example 7.10-1. If a packaged IC can dissipate a maximum average power of 1 W, how many NMOS NOR gates can be accommodated? Assume the NOR gate pullup is sized to match the reference inverter.

Solution. From Eq. 7.10-3,

$$N = \frac{(1\text{ W})2}{150\ \mu\text{W}} = 13,333 \text{ NOR gates} \tag{7.10-5}$$

In the worst case, the circuit could be limited to about 6667 gates.

Note that if greater driving capability is required, for example, to drive highly capacitive loads as described in Sec. 7.9, then the W_2/L_2 ratio in Eq. 7.10-2 will increase, causing a corresponding increase in average static power dissipation. From Example 7.9-4, W_2/L_2 for the pullup device of the last stage of an optimally sized seven-stage pad driver is e^6 times as large as the width-to-length ratio of the load device of a reference inverter. Consequently, the last inverter alone in the seven-stage pad driver would have a power dissipation of 60 mW when it conducts! This is more than twice the static power dissipation of all preceding stages combined.

Logic circuits with inputs that change rapidly can dissipate considerable additional power over their static power requirements. This additional power is referred to as *dynamic power dissipation*. For example, immediately after a low-to-high input transition for the reference inverter of Fig 7.10-1, the output voltage will be near V_{DD} as the load capacitance starts to discharge. While the output is near V_{DD}, the pulldown device M1 is in the saturation region, causing an instantaneous drain current of

$$I_{D1} = K' \frac{W_1}{L_1} \frac{(V_{DD} - V_{TN})^2}{2} \tag{7.10-6}$$

With $V_{DD} = 5$ V, $K' = 20\ \mu\text{A/V}^2$, $W_1 = L_1$, and $V_{TN} = 1$ V, the drain current becomes 160 μA and the initial power dissipation is 800 μW. This is considerably higher than the static power dissipation of 150 μW found earlier. The actual power dissipation will vary in a continuous manner from 800 μW to 150 μW during an output high-to-low transition. With fast input signals to a digital integrated circuit, the dynamic power dissipation obtained from a time average of the instantaneous power dissipation minus the static power dissipation can be much larger than the static power dissipation and must be taken into consideration.

The two primary components of power dissipation for NMOS circuits are static power dissipation and dynamic power dissipation. For circuits with average logic signal changes less frequent than about 10 MHz, static power dissipation is dominant. For higher-frequency signal changes, dynamic power becomes the major consideration. Following is a quantitative analysis of dynamic power dissipation for CMOS circuits. The corresponding analysis for NMOS circuits is similar.

7.10.2 CMOS Power Dissipation

CMOS logic has long been used for circuits in applications requiring extremely low power, such as space probes, calculators, and wristwatches. Perhaps the most important asset of CMOS for today's digital logic designs is its low power dissipation and attendant minimal cooling requirements. Power dissipation in CMOS can be classified into three categories: static power dissipation, *dc switching power* occurring when both transistors conduct momentarily during a transition, and *ac switching power* lost while charging (discharging) capacitive loads. The combination of dc switching power and ac switching power is often called dynamic power dissipation.

Static power dissipation is negligible for CMOS logic circuits. The dc path from power to ground is always broken by an off transistor when the circuit is quiescent. With today's digital CMOS circuits, static power dissipation is not a consideration compared with dynamic power dissipation.

The second component of power dissipation, dc switching power, occurs during the time that the inputs to a logic gate are between the valid logic levels. During this time, both transistors conduct, providing a path from V_{DD} to ground. For an individual gate, the average power dissipated increases with switching time for its input logic signal; that is, the longer the input stays between valid logic levels, the longer the conductive path from V_{DD} to ground exists. The power lost to this cause is typically less than 10% of total power dissipation for digital CMOS circuits such as memories and microprocessors.

The ac switching power is the main component of power dissipation for digital CMOS circuits. This power loss can be analyzed by considering the circuit of Fig. 7.10-2*a*. This circuit models a capacitively loaded inverter output during a low-to-high transition initiated at time zero. Assume no charge on the capacitor when the switch is initially closed. Since this is a simple *RC* circuit, it is well known that the current *i(t)* from the battery is

$$i(t) = \left(\frac{V}{R}\right)e^{-t/RC} \tag{7.10-7}$$

The total energy supplied by the battery is given by

$$e = \int_0^\infty V\, i(t)dt = V^2C \tag{7.10-8}$$

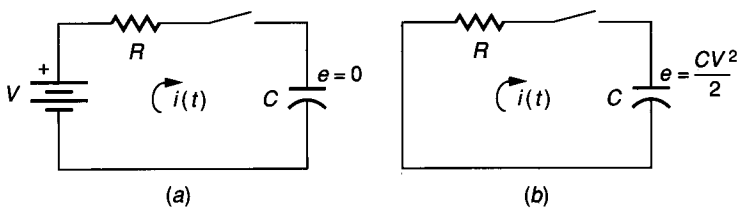

FIGURE 7.10-2
Equivalent circuits for ac power dissipation: (*a*) Charging circuit, (*b*) Discharging circuit.

Because the final energy stored on the capacitor is only (1/2) CV^2 then half the total energy supplied by the battery must be dissipated in the resistance while the capacitor is being charged. Now consider that the switch is opened momentarily, the battery is replaced by a short, and the switch is reclosed as shown in Fig. 7.10-2*b*. As the capacitor discharges, all its stored energy will be dissipated in the resistor. The total energy lost (dissipated in the resistor) during a capacitor charge/discharge cycle e_{cycle} must be CV^2.

For CMOS logic circuits, the capacitance in Eq. 7.10-8 represents the sum of the parasitic gate and interconnection capacitance. Note that Eq. 7.10-8 is independent of the charging and discharging resistances. The power dissipation is just the rate of use of energy. If the charge/discharge cycle occurs periodically with a period T, the average power dissipation is

$$P = \frac{e_{\text{cycle}}}{T} \tag{7.10-9}$$

In terms of operating frequency $f = 1/T$, the average power used is

$$P = e_{\text{cycle}} f = CV^2 f \tag{7.10-10}$$

This analysis shows that the average ac power dissipation for a CMOS circuit is proportional to the total capacitance, to the square of the supply voltage, and to the operating frequency. A similar analysis holds for NMOS circuits, except that the voltage swing is smaller because the lower logic level is above ground. For CMOS circuits, the ac power dissipation dominates, and both the ac power dissipation and the dc switching power increase with frequency.

Example 7.10-2. Consider an approximate limitation on the number of gates in a CMOS integrated circuit if the total power dissipation is limited to 1 W, the operating frequency is 10 MHz, and the supply voltage is 5 V.

Solution. It will be assumed that the ac power dissipation is dominant. From Example 7.8-1, a single gate load capacitance for a reference CMOS inverter is 0.016 pF. With the addition of interconnection capacitance, assume that the total capacitance driven by each logic gate is 0.032 pF. The total ac power dissipation is equal to the number of active gates N_a times the power dissipation of each gate. Under the assumptions given, the number of active gates to gve 1 W power dissipation is

$$N_a = \frac{P}{CV^2 f} = \frac{1}{0.032 \times 10^{-12} 5^2 10^7} = 125,000$$

In typical integrated circuits, only 10% to 25% of the gates switch during a given clock cycle. Using a conservative 25% figure, the total number of gates required to dissipate 1 W is

$$N_{\max} = \frac{N_a}{0.25} = 500,000$$

This can be compared with the required number of NMOS gates from Example 7.10-1 to show why CMOS is preferred in terms of power dissipation.

It is important to consider how future fabrication and operating conditions will affect power limitations on the number of gates in a CMOS integrated circuit. As CMOS circuits are reduced in size, it is expected that the operating frequency will increase and supply voltages and gate capacitance will decrease. If clock frequency is increased and power supply voltages and gate capcitance are reduced proportionally for a constant number of gates, the total CMOS power dissipation decreases rapidly because it is a linear function of frequency and capacitance and a squared function of voltage. The ability to operate faster and at reduced power is one of the driving forces for scaling down minimum device sizes.

In this section, static and dynamic power dissipation were introduced. Dynamic power dissipation includes both dc and ac switching power. Static power dissipation dominates for NMOS logic, whereas dynamic power dissipation dominates for CMOS logic.

7.11 NOISE IN DIGITAL LOGIC CIRCUITS

Electrical noise in integrated circuits represents an unwanted perturbation of desired signal voltages. Noise can arise from many sources and may or may not affect the operation of a circuit, depending on the magnitude of the noise disturbance and the sensitivity of the circuit to the disturbance. Noise disturbances may come from the external environment, as in electromagnetic interference or alpha particles, or may be internally generated from causes that can be controlled by the designer. Internal noise in digital integrated circuits comes from two primary sources: noise coupled from a common resistive path to power or ground, and noise that is capacitively coupled from another signal path. In this section the common causes of internal noise in digital integrated circuits are considered, the parameters used to specify digital integrated circuit immunity to noise are defined, and the noise immunity for NMOS and CMOS inverters is investigated.

7.11.1 Resistive Noise Coupling

Figure 7.11-1*a* shows a resistance R_c in the common ground path for two inverters. In practical circuits, this might be caused by a common diffusion path to a metal ground bus. The model of Fig. 7.11-1*b*, where each transistor is replaced by an equivalent resistance, is used for the following simplified analysis. If switch S1 is closed and switch S3 is open, the output voltage V_1 is determined as

$$V_1 = \frac{V_{DD}(R_1 + R_c)}{R_1 + R_2 + R_c} \tag{7.11-1}$$

Note that if $R_c = 0$ ohms, Eq. 7.11-1 reduces to Eq. 7.8-1. This output voltage corresponds to the low logic state. If R_c is nonzero, the output voltage is increased, thereby degrading the low logic voltage level.

A shift occurs in the output voltage V_1 if switch S3 of Fig. 7.11-1*b* is closed. This shift produces an unwanted noise voltage that, if large enough, can affect the logic value seen by subsequent stages. An equivalent circuit when both inverters

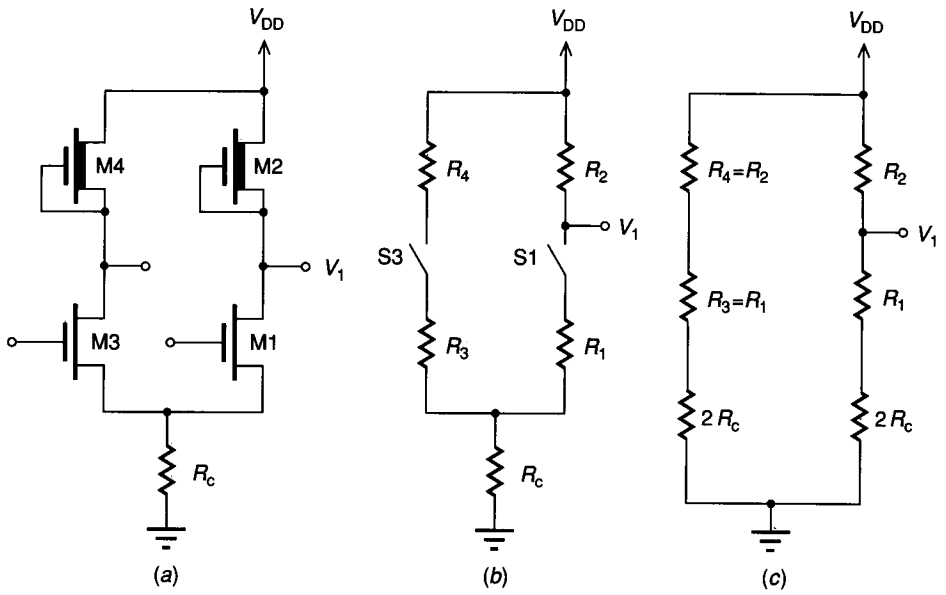

FIGURE 7.11-1
Resistive noise coupling: (*a*) Two inverters with common resistance to ground, (*b*) Resistive model for (*a*), (*c*) Model for matched inverters.

are identical and both switches are closed is given in Fig. 7.11-1*c*. Under these conditions, the output voltage V_1 is

$$V_1 = \frac{V_{DD}(R_1 + 2R_c)}{R_1 + R_2 + 2R_c} \tag{7.11-2}$$

The increase in output voltage depends on the relative resistance of R_c and the equivalent inverter output resistance.

The preceding example with simple inverters demonstrates resistive noise coupling, but in practice this case does not cause serious noise problems because logic gates are usually connected to low-resistance power and ground buses through relatively short paths. Resistance in a common supply path to two inverters is another source of resistive noise coupling. As a general rule, resistance in any segment of power and ground paths may cause unwanted noise voltages. For this reason, power and ground buses are almost always run in a low-resistance metal layer.

Although resistive noise coupling is not serious for the preceding simple case, two related conditions are important. If a large number of gates common to a power supply bus change state in concert, the combined effect may produce significant voltage shifts that detrimentally affect logic states. Second, output pad drivers and fast bus drivers draw considerable current and thus may generate noise voltages in other parts of the circuit from voltage drops even in a low-resistance power supply or ground path. The second condition is more easily detected than the first, but both are important considerations in integrated circuit design.

7.11.2 Capacitive Noise Coupling

Capacitive noise coupling is caused by physical relationships of signal paths. For integrated circuits, the two conditions that cause significant mutual capacitance are long adjacent signal paths, and overlapping but disjoint signal paths. In either case, the coupling capacitance will be called C_c. A general model of the coupling is given in Fig. 7.11-2*a*. (Standard Laplace transform notation is used in this analysis.) If the admittance to ground of the affected circuit at the point of coupling is $Y(s)$, and the effective noise signal is $V_s(s)$, the noise voltage $V_n(s)$ is given by

$$V_n(s) = \frac{V_s(s)sC_c}{Y(s) + sC_c} \tag{7.11-3}$$

Two cases will be considered to show the effects of capacitively coupled noise. First, the effect on the dynamic storage node of Fig. 7.11-2*b* will be considered. A dynamic storage node can be adequately represented as a capacitance C_d to ground with an admittance $Y_s(s) = sC_d$. From Eq. 7.11-3, the noise voltage is

$$V_n(s) = \frac{V_s(s)sC_c}{sC_d + sC_c}$$

or, after canceling the s term,

$$V_n = \frac{V_sC_c}{C_d + C_c} \tag{7.11-4}$$

The coupled noise voltage is just the noise voltage times the ratio of the coupling capacitor to the sum of the two capacitances. Because C_d is normally the small gate capacitance of a transistor, even a small coupling capacitance can be significant. If C_c is equal to C_d, a high-to-low voltage change in V_s can destroy

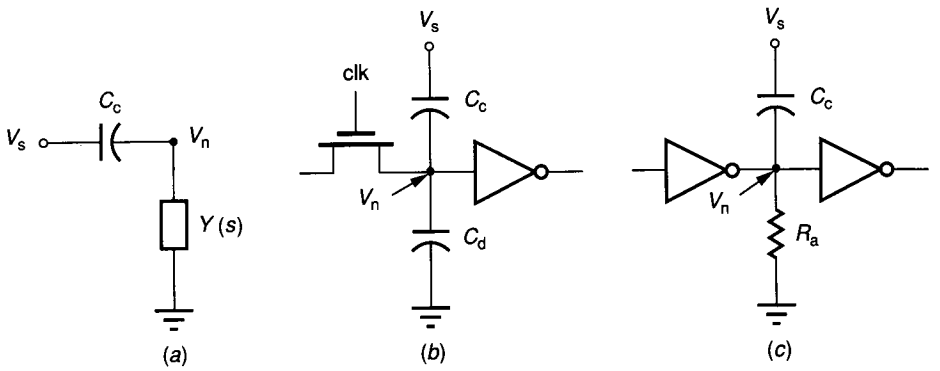

FIGURE 7.11-2
Capacitive noise coupling: (*a*) General noise model for capacitive noise coupling, (*b*) Dynamic storage node, (*c*) Actively driven node.

information on a dynamic storage node. It is important to keep the connection from the gating transistor to the dynamic storage node short and to ensure that no other signal lines cross the connection.

A second consideration is capacitive coupling to a driven logic node, as in Fig. 7.11-2*c*. Here the impedance to ground can be adequately modeled by the equivalent resistance R_a of the active output transistor of the first inverter. Again, from Eq. 7.11-3, the noise voltage is

$$V_n(s) = \frac{V_s(s)sC_c}{1/R_a + sC_c} = \frac{V_s(s)R_aC_cs}{1 + R_aC_cs} \tag{7.11-5}$$

For the normal condition of $|R_aC_cs| << 1$, Eq. 7.11-5 reduces to

$$V_n(s) = V_s(s)R_aC_cs \tag{7.11-6}$$

If $R_a = 10\ \text{k}\Omega$, $C_c = 0.1$ pF, and $f = 1.59$ MHz, then with $\omega = 2\pi f = 10$ Mrad/sec and $s = j\omega$

$$|V_n| = |V_s|/100$$

These values show that significant capacitive coupling is necessary to change the logic level for an actively driven node.

7.11.3 Definition of Noise Margins

Explanation of noise margins for digital logic gates requires the definition of several voltages in the voltage transfer characteristic of a logic circuit.

1. V_{IL}: the highest voltage reliably recognized as a logic low
2. V_{IH}: the lowest voltage reliably recognized as a logic high
3. V_{OL}: the nominal logic low voltage generated by a stage
4. V_{OH}: the nominal logic high voltage generated by a stage

V_{OL} and V_{OH} were introduced previously as V_L and V_H, the nominal output voltages of a reference inverter. V_{IL} and V_{IH} were introduced as the logic threshold voltages.

The voltages V_{IL} and V_{IH} require further explanation. As was shown in Sec. 7.2.2, the voltage transfer function of an inverter contains two regions with less-than-unity inverting gain separated by a region with greater-than-unity inverting gain. V_{IL} and V_{IH} are defined to denote the intersections of these regions, as shown in Fig. 7.11-3. The slope of the transfer characteristic is -1 at the two points representing an inverting gain of unity. Consider V_{IL} first. If the input voltage $V_i < V_{IL}$, the inverting gain of the inverter is less than unity and any small noise perturbation will be reduced in amplitude by the inverter. Otherwise, if $V_{IL} < V_i < V_M$, the input represents a low logic level, but any small noise perturbation is amplified as it is passed to the next stage. This condition may cause erroneous logic voltages to appear in subsequent stages. Thus, V_{IL} represents

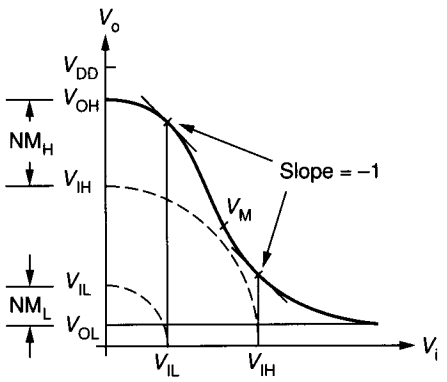

FIGURE 7.11-3
Generic dc voltage transfer characteristic for inverter.

the highest allowable input voltage level that is considered to reliably function as a logic low value. A similar analysis for V_{IH} reveals that it is the lowest allowable input voltage level that is considered to reliably function as a logic high value.

With suitable definitions for high and low logic voltages, the high and low noise margins can be defined. The low-level noise margin is

$$\text{NM}_\text{L} = V_{\text{IL}} - V_{\text{OL}} \tag{7.11-7}$$

and the high-level noise margin is

$$\text{NM}_\text{H} = V_{\text{OH}} - V_{\text{IH}} \tag{7.11-8}$$

NM_H and NM_L represent the largest noise voltages that can be sustained at an inverter input and still allow the inverter to function reliably. Noise margins for logic gates other than inverters are similarly defined based on their voltage transfer characteristics. Subsequent sections examine high and low noise margins for both NMOS and CMOS devices.

7.11.4 NMOS Noise Margins

The noise margins for an NMOS gate can be found from its voltage transfer characteristic. The voltages V_{OL} and V_{OH} were identified in Sec. 7.3 for the reference inverter as V_L and V_H. The depletion-load inverter and its voltage transfer characteristic of Fig. 7.11-4 will be used to help determine V_{IL} and V_{IH}. Note the straight lines that separate the ohmic and saturated regions for the enhancement and depletion transistors of the inverter. These help show that V_{IL} will be found with the depletion transistor in the ohmic region and the enhancement transistor in the saturation region. The voltage transfer characteristic in this region is given by

$$K'\frac{W_\text{N}}{L_\text{N}}\frac{(V_\text{i} - V_\text{TN})^2}{2} = K'\frac{W_\text{D}}{L_\text{D}}\left(-V_\text{TD} - \frac{V_\text{DD} - V_\text{o}}{2}\right)(V_\text{DD} - V_\text{o}) \tag{7.11-9}$$

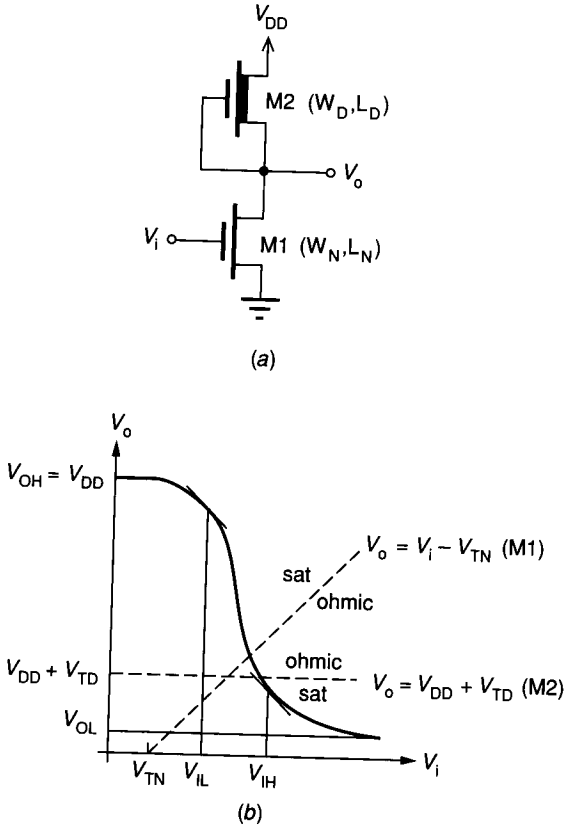

FIGURE 7.11-4
NMOS inverter noise model: (a) Circuit, (b) Voltage transfer characteristic.

Assuming an inverter with a pullup/pulldown ratio of k and solving Eq. 7.11-9 for V_i gives

$$V_i = V_{TN} + \sqrt{(1/k)(-2V_{TD} - V_{DD} + V_o)(V_{DD} - V_o)} \quad (7.11\text{-}10)$$

Taking the derivative with respect to V_o, setting it equal to -1, and solving for V_o gives

$$V_o = V_{DD} + V_{TD}\left(1 - \sqrt{k/(1+k)}\right) \quad (7.11\text{-}11)$$

The corresponding input voltage is

$$V_i = V_{IL} = V_{TN} - \frac{V_{TD}}{\sqrt{k(1+k)}} \quad (7.11\text{-}12)$$

Substituting typical values of $V_{TN} = 1$ V, $V_{TD} = -3.5$ V, $k = 4$, and $V_{DD} = 5$ V into Eqs. 7.11-11 and 7.11-12 gives

$$V_o = 4.63 \text{ V} \quad \text{and} \quad V_{IL} = 1.78 \text{ V} \quad (7.11\text{-}13)$$

To find V_{IH}, Fig. 7.11-4 indicates that the operating regions for the two transistors are reversed. The voltage transfer characteristic is now

$$K'\frac{W_N}{L_N}\left(V_i - V_{TN} - \frac{V_o}{2}\right)V_o = K'\frac{W_D}{L_D}\frac{V_{TD}^2}{2} \tag{7.11-14}$$

Solving Eq. 7.11-14 for V_i gives

$$V_i = V_{TN} + \frac{V_o}{2} + \frac{V_{TD}^2}{2kV_o} \tag{7.11-15}$$

Taking the derivative with respect to V_o, setting it equal to -1, and solving for V_o gives

$$V_o = \frac{-V_{TD}}{\sqrt{3k}} \tag{7.11-16}$$

The corresponding input voltage is

$$V_i = V_{IH} = V_{TN} - \frac{2V_{TD}}{\sqrt{3k}} \tag{7.11-17}$$

Substituting typical values into Eqs. 7.11-16 and 7.11-17 gives

$$V_o = 1.01 \text{ V and } V_{IH} = 3.02 \text{ V} \tag{7.11-18}$$

The noise margins can now be calculated. Using the results of Eqs. 7.11-13 and 7.11-18,

$$NM_L = V_{IL} - V_{OL} = 1.78 - 0.40 = 1.38 \text{ V} \tag{7.11-19}$$

and

$$NM_H = V_{OH} - V_{IH} = 5.00 - 3.02 = 1.98 \text{ V} \tag{7.11-20}$$

These noise margins are typical for NMOS logic gates, with the high noise margin greater than the low noise margin.

7.11.5 CMOS Noise Margins

The noise margins for a CMOS gate can be found from its voltage transfer function. The voltages $V_{OL} = 0$ V and $V_{OH} = V_{DD}$ were found in Sec. 7.5 for the CMOS reference inverter as V_L and V_H. The inverter and its voltage transfer characteristic of Fig. 7.11-5 will be used to help determine V_{IL} and V_{IH}. Note the straight lines that separate the ohmic and saturated regions for the n- and p-channel transistors of the inverter. These help show that V_{IL} will be found with the p-channel transistor in the ohmic region and the n-channel transistor in the saturation region. The voltage transfer characteristic in this region is given by

$$K_N'\frac{W_N}{L_N}\frac{(V_i - V_{TN})^2}{2} = K_P'\frac{W_P}{L_P}\left(V_i - V_{DD} - V_{TP} - \frac{V_o - V_{DD}}{2}\right)(V_o - V_{DD}) \tag{7.11-21}$$

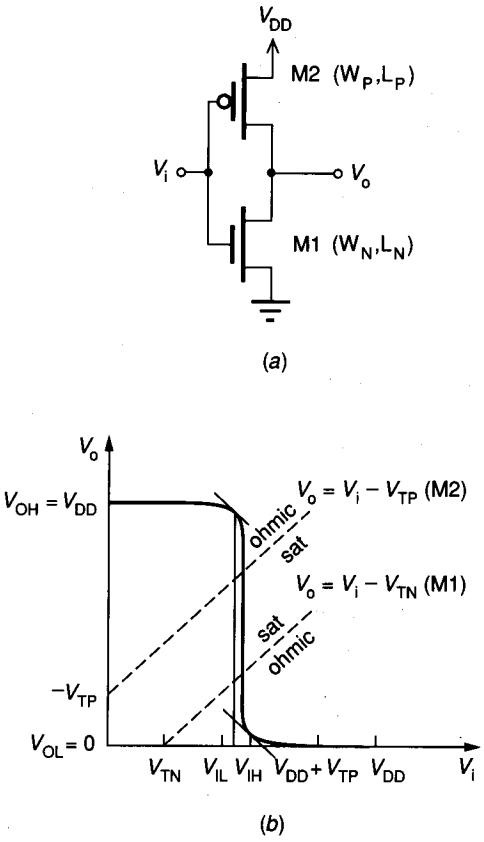

FIGURE 7.11-5
CMOS inverter noise model: (a) Circuit, (b) Voltage transfer characteristic.

Note that V_{TP} is negative for CMOS circuits. The substitution

$$x = \frac{K'_N}{K'_P}\frac{W_N}{L_N}\frac{L_P}{W_P}$$

and solving Eq. 7.11-21 for V_o gives

$$V_o = V_i - V_{TP} - \sqrt{(V_i - V_{TP})^2 - 2V_{DD}(V_i - V_{TP} - V_{DD}/2) - x(V_i - V_{TN})^2} \tag{7.11-22}$$

Letting $x = 1$ for symmetric output drive, taking the derivative with respect to V_i, setting it equal to -1, and solving for V_{IL} gives

$$V_{IL} = \frac{3V_{DD} + 3V_{TP} + 5V_{TN}}{8} \tag{7.11-23}$$

To find V_{IH}, Fig. 7.11-5 indicates that the operating regions for the two transistors are reversed. The voltage transfer characteristic is now

$$K'_N\frac{W_N}{L_N}\left(V_i - V_{TN} - \frac{V_o}{2}\right)V_o = K'_P\frac{W_P}{L_P}\frac{(V_i - V_{DD} - V_{TP})^2}{2} \tag{7.11-24}$$

Note that V_{TP} is negative for CMOS circuits. The substitution

$$y = \frac{K'_P}{K'_N}\frac{W_P}{L_P}\frac{L_N}{W_N}$$

and solving Eq. 7.11-24 for V_o gives

$$V_o = V_i - V_{TN} - \sqrt{(V_i - V_{TN})^2 - y(V_i - V_{DD} - V_{TP})^2} \tag{7.11-25}$$

Letting $y = 1$ for symmetric output drive, taking the derivative with respect to V_i, setting it equal to -1, and solving for V_{IH} gives

$$V_{IH} = \frac{5V_{DD} + 5V_{TP} + 3V_{TN}}{8} \tag{7.11-26}$$

The noise margins can now be calculated. Using typical values of $V_{TN} = 1$ V, $V_{TP} = -1$ V, $V_{DD} = 5$ V, and the results of Eqs. 7.11-23 and 7.11-26,

$$NM_L = V_{IL} - V_{OL} = 2.125 - 0 = 2.13 \text{ V} \tag{7.11-27}$$

and

$$NM_H = V_{OH} - V_{IH} = 5.00 - 2.875 = 2.13 \text{ V} \tag{7.11-28}$$

These noise margins are typical for CMOS logic gates. For symmetrical output drive, the noise margins are equal. Note that the sum of the CMOS noise margins (4.26 V) is much greater than the sum of the NMOS noise margins (3.36 V). CMOS logic is preferred in high-noise environments.

Primary causes of noise voltages in digital MOS circuits were described and analyzed in this section. Noise margins for digital circuits were defined, and these definitions were used to derive noise margins for both NMOS and CMOS inverters. Typical noise margins were calculated for each inverter type.

7.12 SUMMARY

Most digital designers accept a characterization of design abstraction that includes functional, register transfer level, logic, circuit, and layout descriptions as shown in Fig. 7.1-1 Practical digital design is sometimes accomplished by starting with cell layout and working up the abstraction hierarchy from layout to the functional level—often termed *bottom-up design*. At the other extreme, designs are defined at the functional level and then filled in with details at each lower level of abstraction until layout is created—termed *top-down design*. In fact, most design is accomplished using a combination of top-down and bottom-up design styles based on a prerequisite knowledge of basic digital building blocks.

The goal of this chapter has been to introduce basic digital building blocks at the logic, circuit, and layout levels. To accomplish this, salient characteristics of digital logic were described followed by explanations of NMOS and CMOS inverters, logic gates, and pass transistors. With knowledge of the primitive building blocks in hand, important electrical characteristics such as signal propagation delays, parasitic capacitance, power dissipation, and noise margins were detailed.

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PROBLEMS

Section 7.1

7.1. Provide a multilevel description of a full adder having inputs A, B, and C and outputs Sum and Carry. Include a block diagram, an RTL-level description (use Boolean equations), and a logic diagram.

Section 7.2

7.2. Find V_L and V_H for the following piecewise-linear voltage transfer characteristic (VTC) of an inverter. Let the VTC intersect the points $(V_i, V_o) = (0,5.0)$, $(2.5,3.5)$, $(3.5,0.5)$, $(5.0,0.5)$.

7.3. What primary characteristic distinguishes restoring logic from nonrestoring logic?

7.4. Verify by using DeMorgan's theorem that the Boolean logic function $X = AB + AC + BC$ can be realized using only NAND logic gates. Show the NAND gate logic diagram for this function.

7.5. Assume that $V_{IL} = 1$ V, $V_{IH} = 4.5$ V, and $V_{DD} = 5$ V. Give the allowable voltage ranges for V_L and V_H for a practical logic device.

7.6. Given an inverter voltage transfer characteristic where $V_o = (2.5 + 2\cos(\pi V_i/5))$ V, find the values V_L, V_M, and V_H.

Section 7.3

7.7. Solve for the inverter ratio k with $V_{TD} = -4$ V, $V_{TN} = 1$ V, $V_{DD} = 5$ V, and $V_M = 2.5$ V. Assume both transistors are in saturation. Is this assumption valid?

7.8. If $V_{TD} = -3.5$ V, $V_{TN} = 1$ V, $V_{DD} = 5$ V, and $V_M = 2.5$ V, determine the inverter ratio k using the appropriate equations (ohmic or saturation) for both transistors of an inverter.

7.9. For a depletion-load inverter with $V_{TD} = -4$ V, $V_{TN} = 1$ V, $V_{DD} = 5$ V, and $k = 4$, calculate the value of V_L without the approximation of Eq. 7.3-6.

7.10. For a depletion-load inverter with $V_{TD} = -4$ V, $V_{TN} = 1$ V, $V_{DD} = 5$ V, and $k = 3$, calculate the approximate value of V_L.

7.11. Using an analysis similar to that used to derive Eq. 7.3-2, determine the sizing ratio for an enhancement-load inverter.

7.12. Assume that L and W are sized in integral multiples of dimension λ. Find values of L and W in terms of λ for both transistors of an inverter having a 4 : 1 pullup/pulldown ratio so that the total gate area is minimized.

Section 7.4

7.13. Calculate V_L for a two-input depletion-load NOR gate with one input high and with both inputs high. Assume $V_{TD} = -3.5$ V, $V_{TN} = 1$ V, $V_{DD} = 5$ V, and $k = 4$.

7.14. Assume that L and W are sized in integral multiples of dimension λ. Find values of L and W for all three transistors in a two-input depletion-load NAND gate to minimize the total gate area. Assume the pulldown transistors are sized equally and $k = 4$.

7.15. Analytically determine V_L for an n-input depletion-load NOR gate with all inputs high as n goes to infinity.

7.16. For a two-input NAND gate with $V_{TD} = -3.5$ V, $V_{TN} = 1$ V, and $V_{DD} = 5$ V, determine V_L if the pullup transistor is sized according to $k = 4$ instead of $k = 8$.

7.17. Show that a four-input NAND function can be realized with a multi-input NOR gate and inverters.

Section 7.5

7.18. Based on the VTC of Fig. 7.5-2, provide the VTC for a CMOS inverter pair consisting of two identical inverters.

7.19. Assume a 2 μ process with $K'_N = 2K'_P$ and a CMOS inverter with symmetrical output drive. Find the minimum L and W for the p-channel pullup if the n-channel pulldown is of minimum size. Next assume the p-channel pullup is of minimum size, and find the minimum L and W for the n-channel pulldown. The smallest transistor for a 2 μ process is 2 μ by 2 μ.

7.20. Assume the transistors are in the ohmic region with V_{DS} near 0 V. Determine the constant of proportionality for Eq. 7.5-2 and for Eq. 7.5-3.

Section 7.6

7.21. For a NOR gate with $K'_N = 2K'_P$ and with both n-channel pulldown transistors set to minimum size, find the L and W of equally sized p-channel pullups for symmetrical drive.

7.22. Assuming that $K'_N = 2K'_P$, compare the minimum total gate area in terms of dimension λ for a two-input NOR and a two-input NAND gate in CMOS if approximately symmetrical output drive is required for the worst-case condition (series resistance with all transistors on equal to parallel resistance with all but one transistor off).

7.23. Determine the transistor sizes for a three-input CMOS NAND gate with minimum-size pulldown transistors if symmetric output drive is desired for the worst-case pullup and pulldown conditions. Determine the maximum and minimum resistance considering all possible input combinations.

7.24. Compare the minimum total gate area for a four-input NAND gate in both NMOS and CMOS if $K'_N = 2K'_P$, using proper pullup/pulldown ratios for the NMOS gate.

Section 7.7

7.25. Assume a series string of NMOS pass transistors having a lumped-parameter model, as in Fig. 7.7-3, with $R = 10$ kΩ and $C = 0.1$ pF. Calculate the time constant for a single stage and for 10 series stages using the square-law delay approximation.

7.26. If five NMOS pass transistors are cascaded source to gate, find the highest output voltage from the fifth pass transistor if the gate of the first pass transistor is tied to 5 V. Assume $V_{TN} = 1$ V.

7.27. Consider a 4-to-1 selector circuit with select inputs a and b. Compare a solution using standard NMOS logic gates to the pass-transistor solution of Fig. 7.7-2. Give the number of transistors required for each solution.

7.28. Does a series cascade of CMOS transmission gates have the same square-law delay characteristic as a string of NMOS pass transistors? Why or why not?

Section 7.8

7.29. For $L = W = 2\ \mu$, $K' = 25\ \mu A/V^2$, $V_{TN} = 1$ V, and $V_{DD} = 5$ V, find R_{ss} from Eq. 7.8-3 and the exact value of R_1 from Eq. 7.8-4. If $V_{TD} = -4$ V and $k = 4$, find the value of R_1 from Eq. 7.8-5.

7.30. Verify that the 10%-to-90% rising transition time for the exponential voltage $V = 1 - e^{-t/\tau}$ is 2.2τ.

7.31. For the parameters of Prob. 7.29, find t_{LH} and t_{HL} if $C_{ox} = 0.75\ fF/\mu^2$.

7.32. Find the process characteristic time constant for the parameters of Prob. 7.29 if $C_{ox} = 0.75\ fF/\mu^2$.

7.33. With the parameters used to derive the process characteristic time constant for the preceding problem, use SPICE to calculate the inverter-pair delay by simulation.

7.34. If the dimensions and voltages of Prob. 7.29 are scaled down by a factor of 2, calculate the resulting process characteristic time constant and compare it with the unscaled value (remember to scale the gate oxide thickness).

7.35. Compare the current for an enhancement transistor with $V_{GS} = V_{DS} = V_{DD}$ to the current for an equally sized depletion transistor with $V_{GS} = 0$ and $V_{DS} = V_{DD}$. Now calculate the depletion transistor current with $V_{GS} = V_{DD}$. Use the parameters of Prob. 7.29

7.36. Calculate t_{ipd} for a three-input NOR gate, and compare it with t_{ipd} for a three-input NAND gate in NMOS with typical parameter values of Prob 7.29.

7.37. Compute the CMOS t_{ipd} for Ex. 7.8-1 if $K'_P = 15\ \mu A/V^2$ and the p-channel transistor is sized for symmetrical drive.

Section 7.9

7.38. If the process characteristic time constant is $\tau_p = 0.01$ ns and $C_G = 0.1$ pF for an NMOS inverter with $k = 4$, calculate the average delay to drive a 10 pF load.

7.39. Assume that a logic signal drives the root of a binary tree that has 16 outputs, each driving a single reference inverter. Calculate the path delay from the root to the load in terms of t_{apd}. Now calculate the delay if the same logic signal drives the 16 loads directly.

7.40. Repeat the preceding problem, but include the effects of interconnection loading by assuming that the interconnection capacitance for each driven node is twice the gate load capacitance.

7.41. For a geometrically sized cascade of four inverters with each inverter having twice the drive of the preceding stage, compute the average propagation delay in terms of t_{apd} for each of the four stages. Assume the final load is geometrically sized.

7.42. Calculate t_{dir} versus t_{cas} in terms of t_{apd} for a load equivalent to 500 reference inverters when driven (*a*) directly, (*b*) by an optimal cascade (calculate n and truncate to an integer), and (*c*) by a cascade of two drive stages.

Section 7.10

7.43. If $\theta_{JA} = 20°C/W$ because of special packaging, the maximum junction temperature is $T_J = 150°C$, and the ambient temperature is $T_A = 30°C$, find the allowable power dissipation for the integrated circuit.

7.44. Calculate the static power dissipation for an NMOS inverter in the on state with $k = 5$, $K' = 40\ \mu A/V^2$, and $V_{TD} = -4$ V. As long as the low logic voltage is below $V_{DD} + V_{TD}$, does the size of the enhancement pulldown affect the power dissipation? Why or why not?

7.45. Based on Eq. 7.10-6, what is the maximum instantaneous power dissipated in the inverter of the preceding problem? Assume $V_{TN} = 1$ V.

7.46. Show that the energy dissipated in the resistor of the circuit of Fig. 7.10-2*b* is $CV^2/2$ during the capacitor discharge.

7.47. A new CMOS microprocessor is advertised as having a complexity of 300,000 transistors, uses a 20 MHz clock, and operates from a 5 V supply. Assume the microprocessor is composed entirely of gates with an average of five transistors per gate and that the average gate loading capacitance is 0.1 pF. Calculate the dynamic power dissipated by this chip. Is this a reasonable value? If not, which assumptions of the problem are probably incorrect? Explain.

Section 7.11

7.48. For the circuit of Fig. 7.11-1, assume that $R_1 = 10\ k\Omega$, $R_2 = 40\ k\Omega$, and $R_c = 5\ k\Omega$. Calculate the voltage V_1 (*a*) when only switch S1 is closed, and (*b*) when both switches S1 and S3 are closed, if $V_{DD} = 5$ V.

7.49. A dynamic storage node has capacitance $C_n = 0.2$ pF and initial voltage $V_n = 4$ V. If a nearby signal line is coupled to the storage node by capacitance $C_c = 0.1$ pF, find the voltage on V_n after the signal line switches from 5 V to 1 V.

7.50. For $V_{TD} = -4$ V, $V_{TN} = 1$ V, $V_{DD} = 5$ V, and $k = 5$, find V_{IL}, V_{OL}, V_{IH}, V_{OH}, NM_L, and NM_H.

7.51. For an NMOS inverter, derive a simplified expression for V_{OL} based on V_{DD}, V_{TD}, V_{TN}, and k.

7.52. How do NM_L and NM_H behave as k increases without limit?

7.53. Verify Eqs. 7.11-11 and 7.11-12.

7.54. Verify Eqs. 7.11-16 and 7.11-17.

7.55. For a CMOS inverter, give the expressions to calculate NM_L and NM_H directly in terms of V_{DD}, V_{TN}, and V_{TP}.

7.56. For $V_{DD} = 5$ V, calculate the noise margins for a CMOS inverter under the following conditions

(*a*) $V_{TN} = 0.5$ V, $V_{TP} = -0.5$ V
(*b*) $V_{TN} = 1.5$ V, $V_{TP} = -1.5$ V
(*c*) $V_{TN} = 0.5$ V, $V_{TP} = -1.5$ V