CHAPTER 8

ANALOG SYSTEMS

8.0 INTRODUCTION

The systems viewpoint of microelectronic design for analog integrated circuits is presented in this chapter. This material represents the highest level in the design hierarchy illustrated in Table 5.0-1. It is built on the circuits of Chapter 6, which are in turn built on the blocks and components of Chapter 5. A parallel hierarchy is presented in Chapters 7 and 9 for digital integrated circuit design. The subject matter in this chapter deals with the design of systems rather than the design of circuits. In this sense, the designer moves to a higher plateau of design. For example, rather than the design of op amps, the subject will include design *with* op amps.

The material presented in this chapter has been selected to be representative of the concepts and techniques in analog signal processing. In this chapter, we will discuss digital-to-analog and analog-to-digital conversion; review the concepts of continuous-time filter theory; and present switched capacitor filters, modulators and multipliers, waveshaping circuits, and oscillators. Although these subjects may be classified as either subsystems or systems, they are representative of analog design concepts applied at a system level. A microelectronic system often contains both digital and analog circuits and systems, so that in this sense, the material in Chapters 8 and 9 should be treated as a subsystem.

8.1 ANALOG SIGNAL PROCESSING

Figure 8.1-1 shows a simple block diagram of a typical signal processing system. As IC technology begins to exploit VLSI techniques and capabilities, many systems with this format will be built on a single chip. An example of this approach is the analog signal processor.[1] The advent of analog sampled data techniques and MOS technology has made the design of a general signal processor a viable

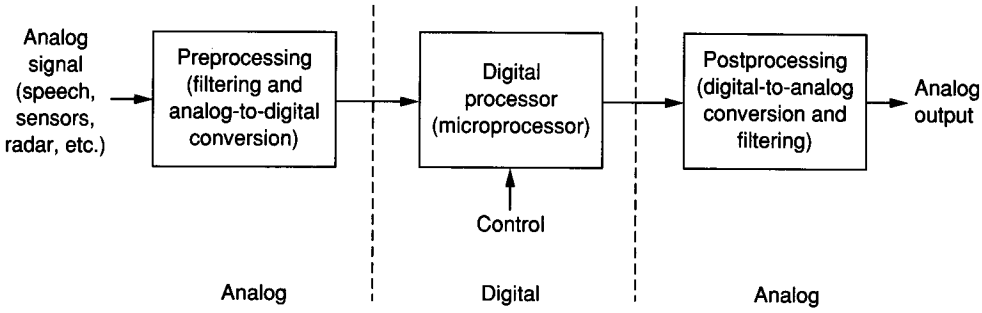


FIGURE 8.1-1
A block diagram of a typical signal processing system.

approach. At the present, CMOS technology is more suitable for combining analog and digital techniques. The primary reason for this situation is that digital VLSI circuits are typically implemented in CMOS. For this reason we will emphasize CMOS over BJT technology in this chapter. Recently, BJT and CMOS technologies have been combined to produce a new technology called BiMOS. BiMOS technology gives the designer an additional degree of freedom to select the most suitable devices for a given application.

The first step in the design of an analog signal processing system is to examine the specifications and to partition the system into the analog part and the digital part. In most cases, the input signal is analog. It could be a speech signal, a sensor output, a radar return, etc. The first block of Fig. 8.1-1 is a preprocessing block. Typically, this block will consist of filters and an analog-to-digital converter. Often, there are very strict speed and accuracy requirements on the components in this block. The next block of the analog signal processor is essentially a microprocessor. An obvious advantage of this approach is that the function of the processor can easily be controlled and changed. Finally, it is often necessary to provide an analog output. In this case, a postprocessing block is necessary. It will typically contain a digital-to-analog converter and some filtering. An interesting decision for the system designer is deciding where to place the interfaces indicated by the dotted lines.

For signal processing, probably the most important system consideration is the bandwidth of the signal to be processed. A graph of the bandwidths of a variety of signals is given in Fig. 8.1-2. The bandwidths in this figure cover the enormous range of 10 orders of magnitude in frequency. At the low end are the seismic signals, which do not extend much below 1 Hz because of the absorption characteristics of the earth. At the other extreme are the microwave signals, which are not used much above 30 GHz because of the difficulties in performing even the simplest forms of signal processing at higher frequencies.

To perform signal processing over this range of frequencies, a variety of techniques have been developed that are almost exclusively analog above 10 MHz and digital below 100 Hz, as shown in Fig. 8.1-3. In the overlap region, a tradeoff must be made between the accuracy and flexibility of a digital approach

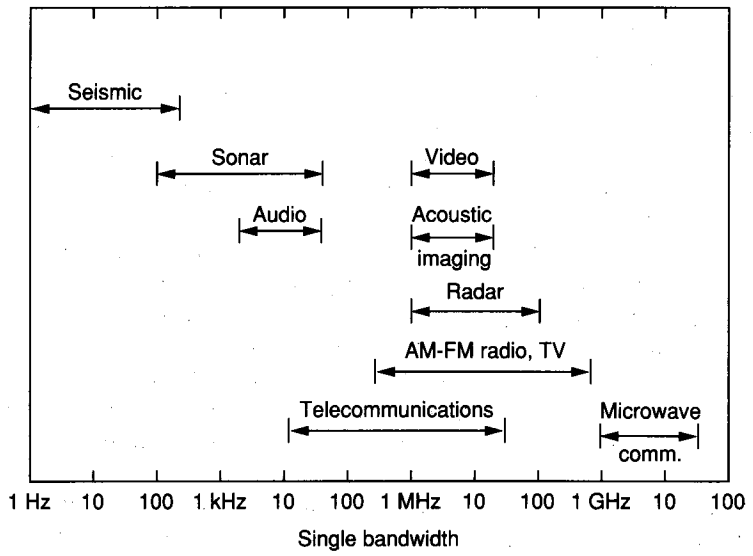


FIGURE 8.1-2
Bandwidths of signals used in signal processing applications.

and the low cost, power, and size of analog techniques. These considerations illustrate some of the advantages of a combined MOS-BJT technology.

By assuming the continuing development of MOS and bipolar technology, it is possible to extrapolate the trends of the past 10 years to obtain predictions about the capability of IC technology in the next 10 years. Some of the implications of these predictions have been considered and show that even at the limits of scaling, the processing bandwidth of MOS technology will have improved only to the point where it is equivalent to today's advanced bipolar technologies.

The ranges indicated in Fig. 8.1-3 are due to technology and are constantly increasing. One of the fastest-moving boundaries in Fig. 8.1-3 is the upper limit of the MOS digital logic, which, as the technology progresses to VLSI, should be able to process signals by the year 1992 at bandwidths of 50–100 MHz. This will be accomplished by using greatly increased density along with moderately increased device speeds. However, as can be seen in Fig. 8.1-3, bipolar digital techniques are already able to process at these rates. Therefore, VLSI will not make possible increased processing rates over what can now be achieved with processors built with bipolar technology, but rather will offer the primary advantages of reduced cost, size, and power requirements of the MOS VLSI signal processors. This will make it possible for signal processing techniques to make an impact in such cost-sensitive areas as consumer products that until now have been unable to afford the costs of using more sophisticated techniques. The combination of BJT and MOS technology offers the best promise of high performance, VLSI signal processing capability.

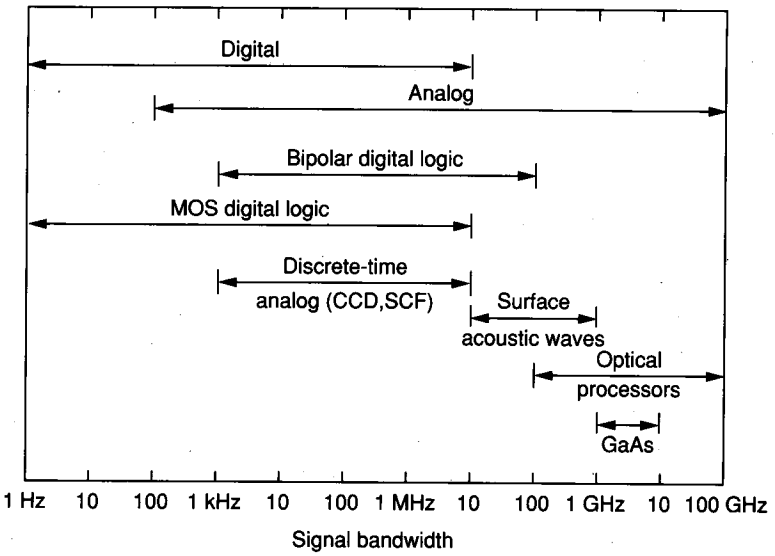


FIGURE 8.1-3
Signal bandwidths that can be processed by present-day (1989) technologies.

8.2 DIGITAL-TO-ANALOG CONVERTERS

The ability to convert digital signals to analog and vice versa is very important in signal processing. This section will examine the digital-to-analog conversion aspect of this important interface. Analog-to-digital conversion will be discussed in the next section. Most of the discussion in these two sections will be independent of whether the technology is BJT or MOS. The op amps and comparators used can be of either type. The switches will be MOS. The resistors and capacitors can be implemented by either technology, depending on the performance requirements.

Figure 8.2-1 illustrates how analog-to-digital (A/D) and digital-to-analog (D/A) converters are used in data systems.[2] In general, an A/D conversion process will convert a sampled and held analog signal to a digital word that is a representation of the analog sampled signal. Often, many analog inputs are multiplexed to the A/D converter. The D/A conversion process is essentially the inverse of the A/D process. Digital words are applied to the input of the D/A converter to create from a reference voltage an analog output signal that is a representation of the digital word.

This section will introduce the principles of D/A converters and will then discuss the performance characterization of D/A converters. The various types of linear D/A converters that will be examined include current-scaling, voltage-scaling, charge-scaling, combinations of the preceding types, and serial D/A converters. In the next section, we will see that D/A converters have an important role in the design and implementation of some A/D converters.

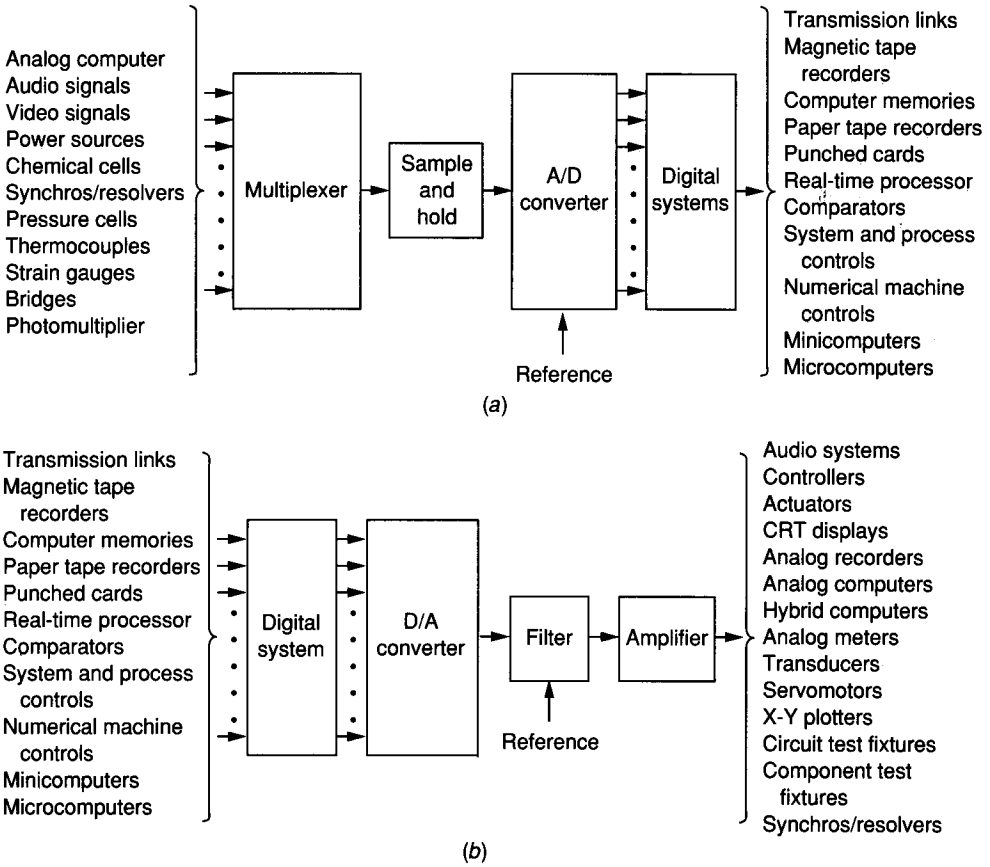


FIGURE 8.2-1
Converters in signal processing systems: (*a*) A/D, (*b*) D/A.

Figure 8.2-2*a* shows a conceptual block diagram of a D/A converter. The inputs are a digital word of N bits ($b_1, b_2, b_3, \ldots, b_N$) and a reference voltage, V_{ref}. The voltage output, V_{OUT}, can be expressed as

$$V_{\text{OUT}} = K V_{\text{ref}} D \tag{8.2-1}$$

where K is a scaling factor and the digital word D is given as

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} \tag{8.2-2}$$

N is the total number of bits of the digital word, and b_i is the ith bit coefficient and is either 0 or 1. Thus, the output of a D/A converter can be expressed by combining Eqs. 8.2-1 and 8.2-2 to get

$$V_{\text{OUT}} = K V_{\text{ref}} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} \right) \tag{8.2-3}$$

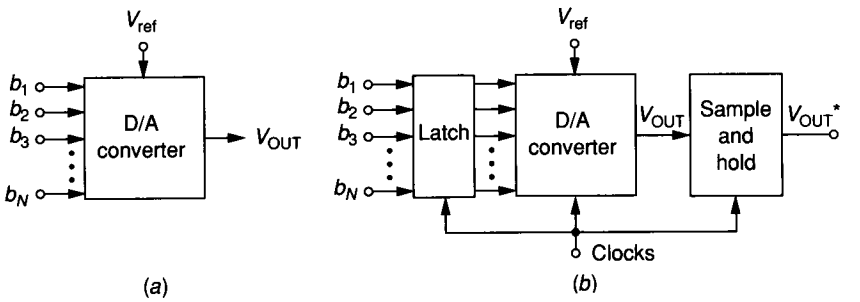


FIGURE 8.2-2
(*a*) Conceptual block diagram of a D/A converter, (*b*) Clocked D/A converter.

or

$$V_{OUT} = K V_{ref}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N})$$
$$= K V_{ref} \sum_{j=1}^{N} b_j 2^{-j} \tag{8.2-4}$$

In many cases, the digital word is synchronously clocked. In this case it is necessary to use latches to hold the word for conversion and to provide a sample-and-hold circuit at the output, as shown in Fig. 8.2-2*b*. A voltage that has been sampled and held is denoted by an asterisk. The sample-and-hold circuit consists of a circuit such as that shown in Fig. 8.2-3, where the analog signal is sampled

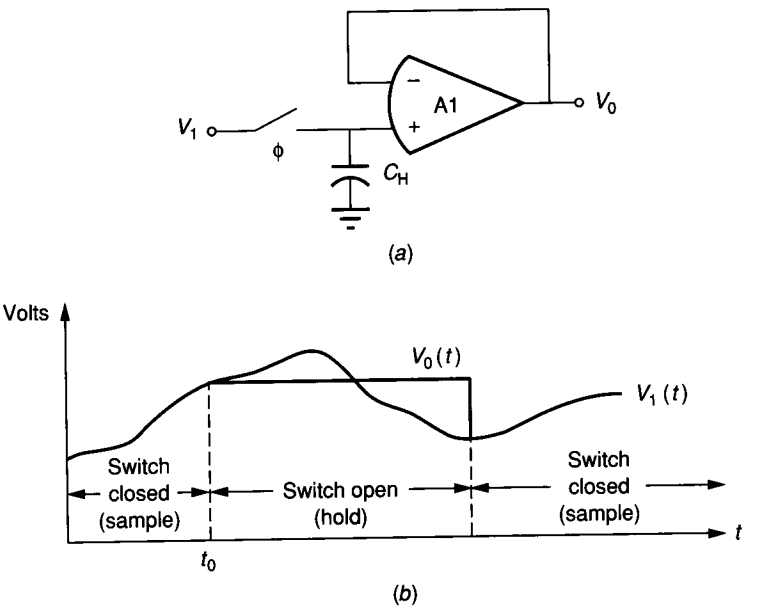


FIGURE 8.2-3
(*a*) Simple sample-and-hold circuit, (*b*) Waveforms illustrating the operation of the sample-and-hold.

on a capacitor, C_H, when the switch is closed; this is called the *sample mode*. During the time that the switch is open, or the *hold mode*, the voltage at time t_0 remains available at the output. An alternate version of the sample-and-hold circuit with higher performance is shown in Fig. 8.2-4. It is important that the sample-and-hold circuit be able to rapidly track changes in the input voltage when in the sample mode and not discharge the capacitor when in the hold mode.

The basic architecture of the D/A converter without an output sample-and-hold circuit is shown in Fig. 8.2-5. The various blocks are a voltage reference, which can be externally supplied, binary switches, a scaling network, and an output amplifier. The voltage reference, binary switches, and scaling network convert the digital word as either a voltage or current signal, and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of the conversion.

The characterization of the D/A converter is very important in understanding its use and design. The characteristics of the D/A converter can be divided into static and dynamic properties. The static properties are independent of time and include the converter transfer characteristic, quantization noise, dynamic range, gain, offset, and nonlinearity.[3]

Figure 8.2-6 shows the transfer characteristic of an ideal D/A converter. This D/A converter has been designed so that the analog output occurs at odd multiples of the full scale signal (FS) divided by 16. The right-most bit of the digital input code is called the *least significant bit* (LSB). Each time the LSB changes, the analog output changes by $FS/2^N$, where N is equal to the number of digital bits. Although this change is an analog quantity, it is often called an LSB change and should be interpreted as the analog change due to a change in the LSB of the digital input code.

The *resolution* of a converter is the smallest analog change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of FS, but is commonly expressed in number of bits, N, where the converter has 2^N possible states. The finite resolution of converters causes an inherent uncertainty in digitizing an analog value. This uncertainty is called the *quantization noise* and has a value of up to ± 0.5 LSB. In the characteristic of Fig. 8.2-6, the quantization noise is seen to be ± 0.5 LSB

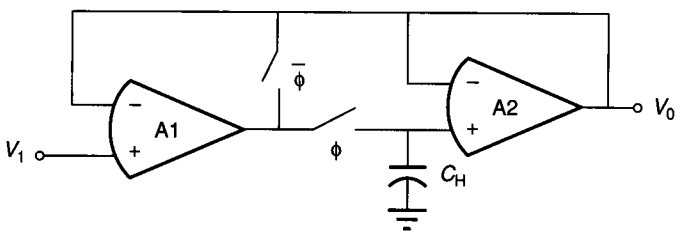


FIGURE 8.2-4
An improved sample-and-hold circuit.

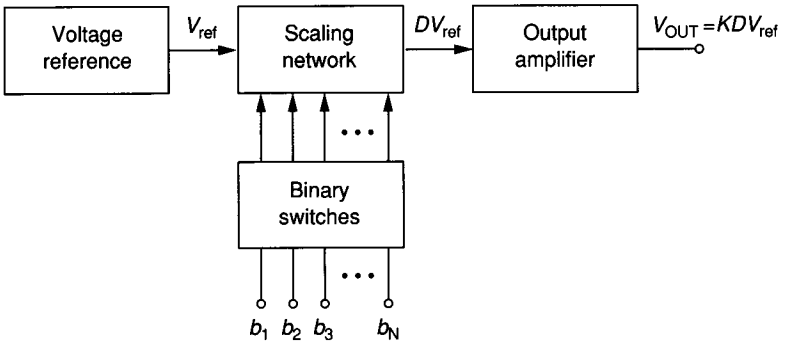


FIGURE 8.2-5
Block diagram of a D/A converter.

or $\pm FS/2^{N+1}$ about each of the multiples of FS/8. The straight line in Fig. 8.2-6 through the midpoint of each analog step change represents the ideal performance of the D/A converter as N approaches infinity.

The *full scale range* (FSR) is the difference between the maximum and minimum analog values and is equal to FS in Fig. 8.2-6 as N approaches infinity. The *dynamic range* (DR) of a noiseless converter is the ratio of the FSR to the smallest difference it can resolve. Thus, the DR can be given as

$$DR = 2^N \tag{8.2-5}$$

or in terms of decibels as

$$DR(dB) = 20\log_{10}(2^N) = 6.02N \tag{8.2-6}$$

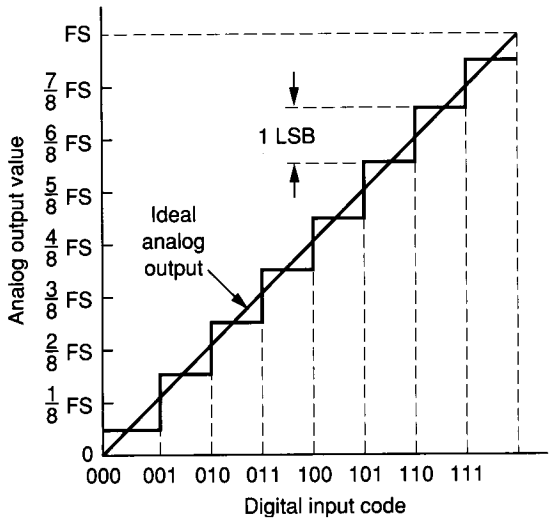


FIGURE 8.2-6
Ideal input-output characteristics for a 3-bit D/A converter.

The *signal-to-noise ratio* (S/N) is also useful in characterizing the capability of a converter. Assume that an analog ramp input is applied to an ideal A/D converter cascaded with an ideal D/A converter. If the analog output of the D/A converter is subtracted from the original analog ramp input, a sawtooth waveform of $\pm FS/2^{N+1}$ results. This sawtooth waveform represents the ideal quantization noise and has an rms value of $(FS/2^N)/\sqrt{12}$. The S/N expressed as a power ratio in dB can be found from the ratio of the peak-to-peak signal, FS, to the noise as

$$S/N(dB) = 10\log_{10}\left[\frac{FS}{FS/[2^N(12)^{1/2}]}\right]^2$$

$$= 20\log_{10}(2^N) + 20\log_{10}(12)^{1/2} = 6.02N + 10.8 \quad (8.2\text{-}7)$$

It can be seen that the S/N ratio increases by a factor of approximately 6 dB for each additional bit of resolution.

The remaining static characteristics include *offset error*, *gain error*, *nonlinearity*, and *nonmonotonicity*. Figure 8.2-7 illustrates the first three of these characteristics for a 3-bit D/A converter. In each case the ideal characteristic of Fig. 8.2-6 is shown by dashed lines for comparison. An illustration of offset error is shown in Fig. 8.2-7*a*. An offset error is seen to be a vertical shift in the D/A transfer characteristic of the ideal D/A transfer characteristic. The offset error is defined as the analog output value by which the transfer characteristic fails to pass through zero. It may be expressed in millivolts or percent of FS.

Figure 8.2-7*b* illustrates the gain or scale factor error of a 3-bit D/A converter. The gain or scale factor error is defined as the difference in the full scale values between the ideal and actual transfer characteristics when the offset error is zero and may be expressed in percent of full scale.

Figure 8.2-7*c* is an illustration of nonlinearity error in a 3-bit D/A converter. Nonlinearity is further divided into integral nonlinearity and differential nonlinearity. Integral linearity is a global measure of nonlinearity of the converter and is defined as the maximum deviation of the actual transfer characteristic from a straight line drawn between zero and the FS of the ideal converter. Integral nonlinearity is expressed in terms of percent of FS or in terms of LSBs. In the characteristics of Fig. 8.2-7*c*, the maximum deviation, which occurs at 111, is -1.5 LSB or -18.75% of FS.

Differential nonlinearity is defined as the maximum deviation of any of the analog output changes caused by an LSB change from its ideal size of $FS/2^N$ or 1 LSB. It is typically expressed in terms of $\pm$LSBs. In the characteristic of Fig. 8.2-7*c*, the maximum deviation also occurs at 111 and is a differential nonlinearity of ± 1 LSB. The characteristic of Fig. 8.2-8 shows how differential nonlinearity differs from integral nonlinearity. Figure 8.2-8*a* is for a 4-bit D/A converter having ± 2 LSB integral nonlinearity and ± 0.5 LSB differential nonlinearity. Figure 8.2-8*b* illustrates a 4-bit D/A converter having $\pm$ 0.5 LSB integral nonlinearity and $\pm$ 1 LSB differential nonlinearity.

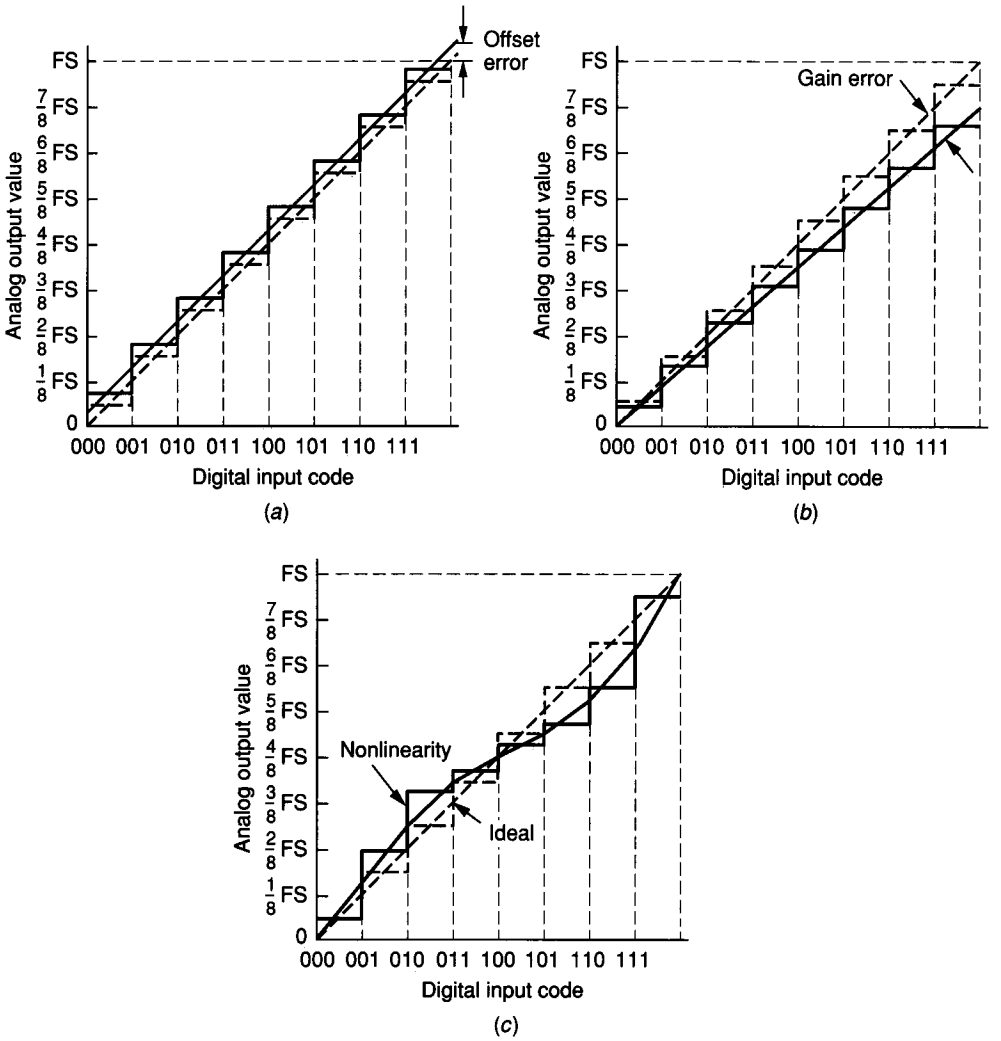


FIGURE 8.2-7
Examples of various types of static characteristics for a 3-bit D/A converter: (*a*) Offset error, (*b*) Gain error, (*c*) Nonlinearity.

Figure 8.2-9 illustrates a 3-bit D/A converter that is not monotonic. A monotonic D/A converter is one in which an increasing digital input code produces a continuously increasing analog output value. A nonmonotonic D/A converter can result if the differential nonlinearity error exceeds ± 1 LSB. In Fig. 8.2-9, a differential nonlinearity of ± 1.5 LSB occurs at a digital input code of 001. Note that there are two occurrences of nonmonotonicity in Fig. 8.2-9.

The dynamic characteristics of the D/A converter are associated with changes in the input digital word. The time required for the output of the converter to

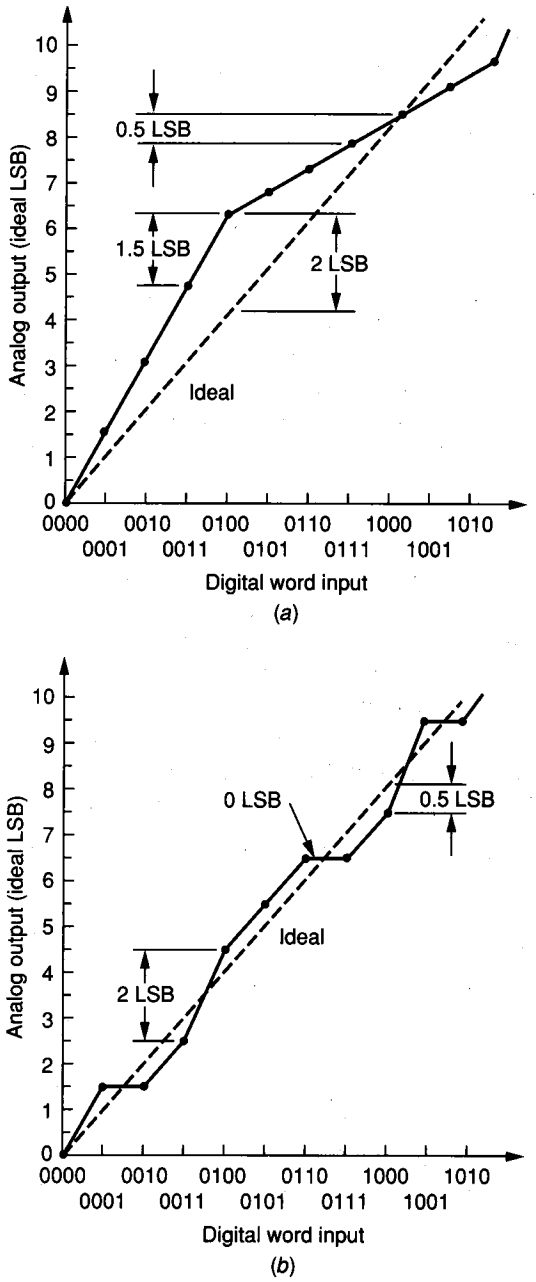


FIGURE 8.2-8
Distinction between integral and differential nonlinearity for a D/A converter: (*a* D/A converter with ±2 LSB integral nonlinearity and ±0.5 LSB differential nonlinearity, (*b*) D/A converter with ±0.5 LSB integral nonlinearity and ±1 LSB differential nonlinearity.

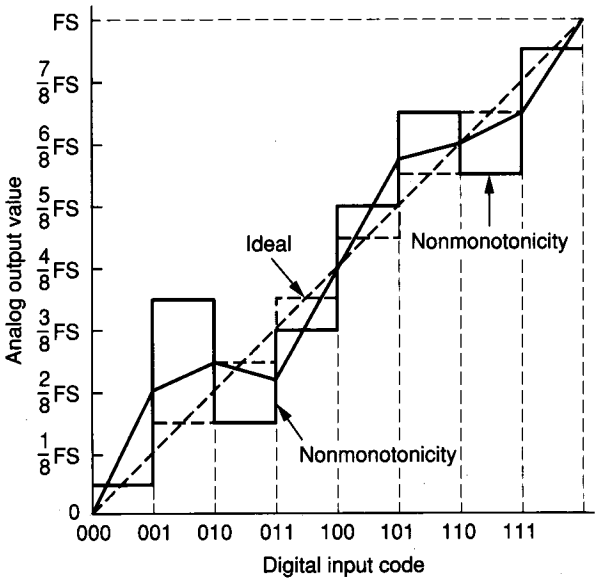


FIGURE 8.2-9
Example of a 3-bit D/A converter that is not monotonic.

respond to a bit change is called the *settling time* and is defined similarly to the settling time for op amps in Fig. 6.5-21. Settling time for D/A converters depends on the type of converter and can range from as much as 100 μs to less than 100 ns.

Many techniques have been used to implement D/A converters. Three approaches that are compatible with integrated circuit technology will be examined. These methods are current-scaling or division, voltage-scaling or division, and charge-scaling or division. Current-scaling is widely used with BJT technology, whereas voltage- and charge-scaling are popular for MOS technology.

8.2.1 Current-Scaling D/A Converters

The general principle of current-scaling or division D/A converters is shown in Fig. 8.2-10*a*. The reference voltage is converted to binary-weighted currents, $I_1, I_2, I_3, \ldots, I_N$. An implementation of this technique using resistors is shown in Fig. 8.2-10*b*. Each of the switches, S_i, is connected to V_{ref} if the ith bit, b_i, is 1 and to ground if b_i is 0. It is seen that the output voltage of the op amp can be expressed as

$$V_{\text{out}} = \frac{-R}{2} I_{\text{O}} = \frac{-R}{2}\left(\frac{b_1}{R} + \frac{b_2}{2R} + \frac{b_3}{4R} + \cdots + \frac{b_{\text{N}}}{2^{N-1}R}\right) V_{\text{ref}}$$

$$= -V_{\text{ref}}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N}) \quad (8.2\text{-}8)$$

The feedback resistor, R_F, can be used to achieve the scaling factor K of Eq. 8.2-1. The switches can be moved from the V_{ref} side of the resistors to the

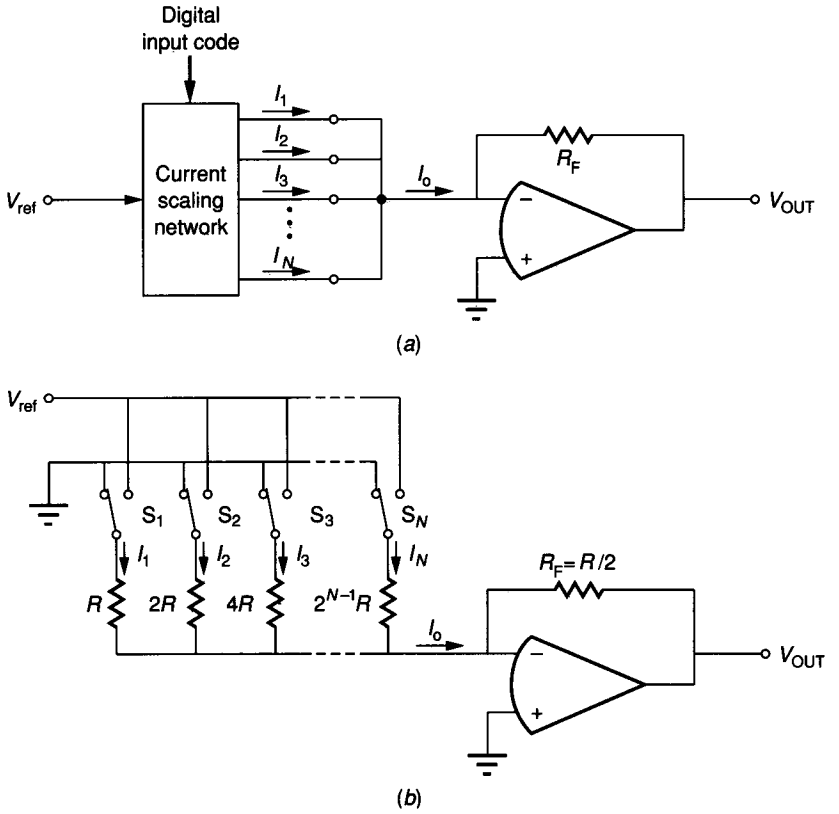


FIGURE 8.2-10
(*a*) Conceptual illustration of a current-scaling D/A converter, (*b*) Implementation of (*a*).

side connected to the inverting input of the op amp. The advantage of the latter configuration is that the voltages at the switch terminals are always ground. As a consequence, the switch parasitic capacitances are not charged or discharged.

The binary-weighted resistor ladder configuration of Fig. 8.2-10*b* has the disadvantage of a large ratio of component values. For example, the ratio of the resistor for the MSB, R_{MSB}, to the resistor for the LSB, R_{LSB}, is

$$\frac{R_{MSB}}{R_{LSB}} = \frac{1}{2^{N-1}} \tag{8.2-9}$$

For an 8-bit D/A converter, this gives a ratio of 1/128. The difficulty with this approach is that the accuracy of R_{MSB} must be much better than that of the value of R_{LSB} for the converter to work properly. For example, R_{MSB} of an 8-bit D/A converter must have a relative accuracy with respect to R_{LSB} to within $\pm 0.78\%$, and preferably better. Such accuracy is difficult to achieve without trimming the resistors, which is done for high-resolution D/A converters using binary-weighted components.

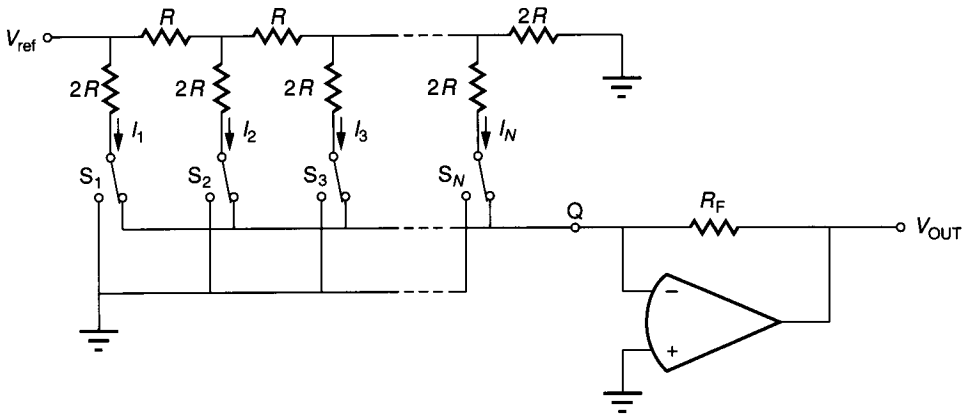


FIGURE 8.2-11
A current-scaling D/A converter using an *R*-2*R* ladder.

An alternative to the binary-weighted approach is the use of an *R*-2*R* ladder, shown in Fig. 8.2-11. Each of the switches, S_i, is connected to Q if the *i*th bit is 1 and to ground if the *i*th bit is 0. Q is the inverting input of the op amp. Obviously, the current I_1 is equal to $V_{ref}/2R$. Using the fact that the resistance to the right of any of the vertical $2R$ resistors is $2R$, we see that the currents I_1, I_2, I_3, . . . , I_N are binary-weighted and given as

$$I_1 = 2I_2 = 4I_3 = \ldots = 2^{N-1}I_N \tag{8.2-10}$$

Thus, the output voltage of the *R*-2*R* D/A converter of Fig. 8.2-11 is given by Eq. 8.2-8. Figure 8.2-11 is an example of using the switches connected either to ground or the inverting terminal of the op amp. V_{ref} and the inverting input of the op amp (point Q) can be interchanged if desired. While the *R*-2*R* D/A converter has twice as many resistors as the binary-weighted resistor D/A converter, it requires resistors with only the ratio of 2:1, which is more practical to accomplish. One disadvantage of the *R*-2*R* configuration is that there are up to 2^{N-1} floating nodes, which are sensitive to parasitic capacitances. Floating nodes are nodes with relatively large resistance to ground. The charging and discharging of these capacitances will require time and delay the response of the converter. Possible architectures for bipolar D/A converters using the *R*-2*R* ladder approach are shown in Fig. 8.2-12. Note that the emitter areas of the BJT devices must be proportional to the emitter current in Fig. 8.2-12*a*.

Two approaches for using binary-weighted D/A converters while keeping the MSB and LSB resistor ratios small deserve mention. The first is called *cascading* and is illustrated in Fig. 8.2-13*a*. The use of a current divider allows two 4-bit, binary-weighted current sources to be cascaded to achieve an 8-bit D/A converter. The accuracy of the 1:16 attenuating resistors must be within the magnitude of the LSB of the entire ladder. A second approach is shown in Fig. 8.2-13*b* and is called the *master-slave ladder*. In this approach, a master ladder consists of the

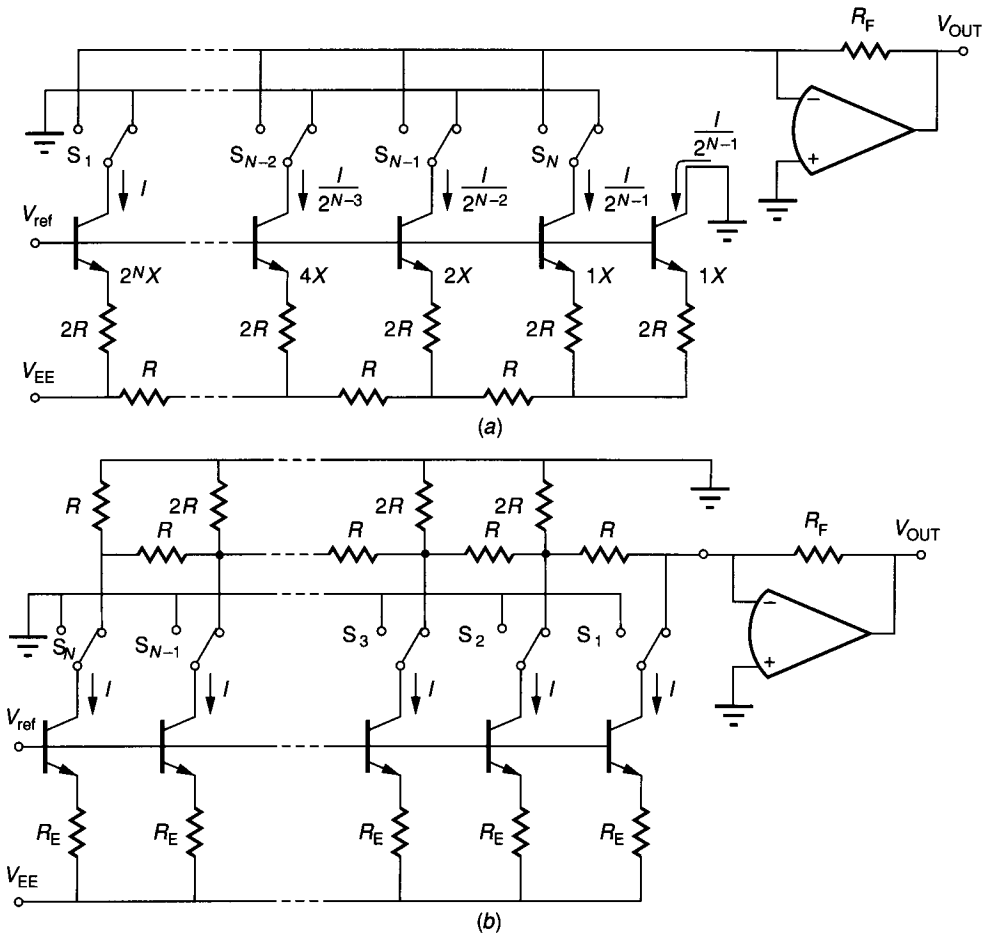


FIGURE 8.2-12
Two implementations of D/A converters using R-$2R$ ladders and BJT current sinks. (a) Binary-weighted emitter areas, and (b) Equal emitter areas. Both converters are described by $V_{OUT} = -R_F I\,[b_1 + 2^{-1}b_2 + \ldots + 2^{N-1}b_N]$.

half of the bits that are most significant, and the slave ladder consists of the half of the bits that are least significant. The crucial point in this approach is the accuracy of the $I/16$ current source for the slave ladder. It must have accuracy better than ± 0.5 LSB.

8.2.2 Voltage-Scaling D/A Converters

Voltage-scaling uses series resistors connected between V_{ref} and ground to selectively obtain voltages between these limits. For an N-bit converter, the resistor string would have at least 2^N segments. These segments can all be equal or

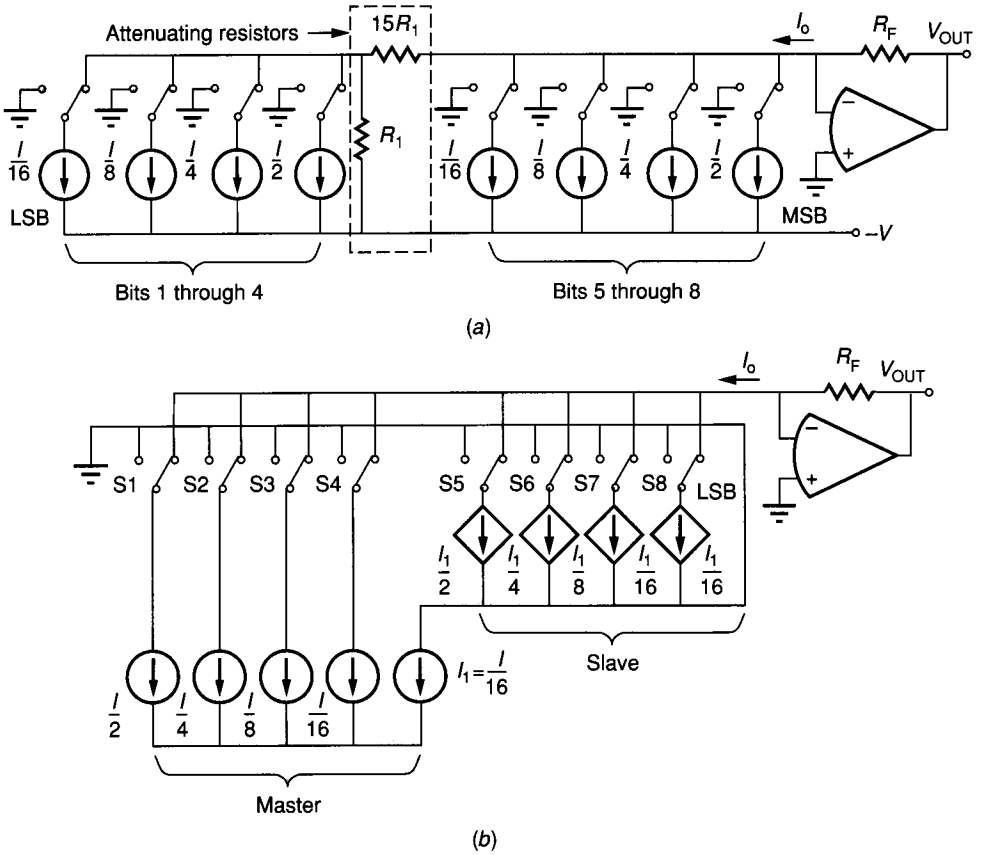


FIGURE 8.2-13
(*a*) Use of current division to cascade two 4-bit, binary-weighted current sinks to get an 8-bit D/A converter, (*b*) Master-slave technique to combine two 4-bit binary weighted current sources to obtain an 8-bit D/A converter. Note that $I_1 = I/16$.

the end segments may be partial values, depending on the requirements. Figure 8.2-14*a* shows a 3-bit voltage scaling D/A converter. Note that the op amp is used simply to buffer the resistor string. Each tap is connected to a switching tree whose switches are controlled by the bits of the digital word. If the ith bit is 1, then the switches controlled by b_i are closed. If the ith bit is 0, then the switches controlled by $\overline{b_i}$ are closed.

The voltage-scaling D/A converter of Fig. 8.2-14*a* works as follows. Suppose that the digital word to be converted is $b_1 = 1, b_2 = 0$, and $b_3 = 1$. Following the sequence of switches, we see that V_{OUT} is equal to 11/16 of V_{ref}. In general, the voltage at any tap i of Fig. 8.2-14*a* can be expressed as

$$V_i = \frac{V_{ref}}{8}(i - 0.5) \tag{8.2-11}$$

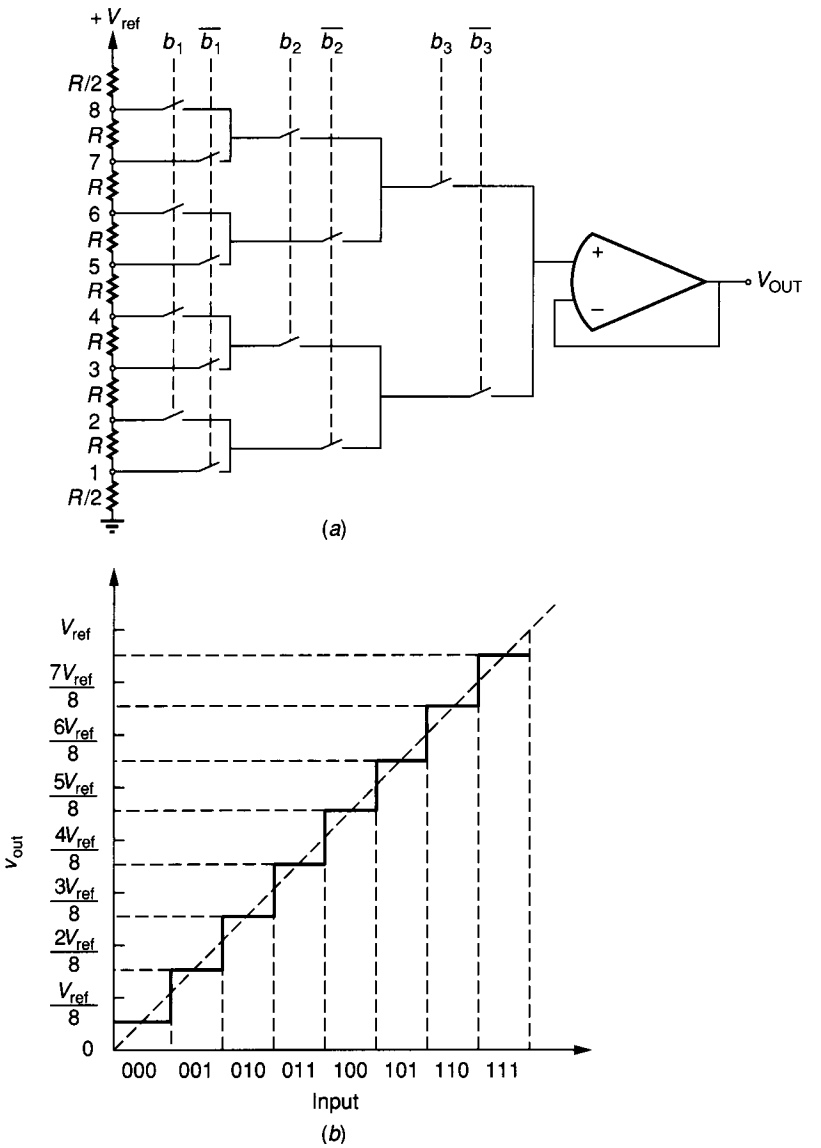


FIGURE 8.2-14
(*a*) Illustration of a 3-bit voltage-scaling D/A converter, (*b*) Input-output characteristics of *a*.

Figure 8.2-14*b* shows the input-output characteristics of the D/A converter of Fig. 8.2-14*a*. It may be desirable to connect the bottom tap to ground, so that a well-defined output (ground) is available when the digital word is all 0s.

Example 8.2-1. Find the accuracy requirement for a resistor string consisting of N equal segments as a function of the number of bits N. If the relative resistor accuracy is 2%, what is the largest number of bits than can be resolved to within $\pm$ 0.5 LSB?

Solution. The ideal voltage to ground across k resistors can be expressed as

$$V_k = \frac{kR}{2^N R} V_{\text{REF}}$$

The worst case variation in this voltage can be found by assuming that all resistors above this point in the string are maximum and below this point are minimum. Therefore, the worst case lowest voltage to ground across k resistors is

$$V'_k = \frac{kR_{\min} V_{\text{REF}}}{(2^N - k)R_{\max} + kR_{\min}}$$

The difference between the ideal and worst case voltages can be expressed as

$$\frac{V_k}{V_{REF}} - \frac{V'_k}{V_{REF}} = \frac{kR}{2^N R} - \frac{kR_{\min}}{(2^N - K)R_{\max} + kR_{\min}}$$

Since this difference must be less that 0.5 LSB, then the desired relationship can be obtained as

$$\frac{k}{2^N} - \frac{kR_{\min}}{(2^N - k)R_{\max} + kR_{\min}} < \frac{0.5}{2^N}$$

The relative accuracy of the resistor R can be expressed as $\Delta R/R$, which gives $R_{\max} = R + 0.5\Delta R$ and $R_{\min} = R - 0.5\Delta R$. Normally, the worst case occurs when k is midway in the resistor string or $k = 0.5(2^N)$. Assuming a relative accuracy of 2% and substituting the above values gives

$$|0.01| < 2^{-N}$$

Solving this equation for N gives $N = 6$ as the largest integer.

It is seen that the voltage-scaling D/A structure is very regular and thus well suited for MOS technology. An advantage of this architecture is that it guarantees monotonicity, since the voltage at each tap cannot be greater than the tap below it. The area required for the voltage-scaling D/A converter is large if the number of bits is 8 or more. The converter will be sensitive to parasitic capacitances at each of the floating nodes resulting in signal delays.

8.2.3 Charge-Scaling D/A Converters

Charge-scaling D/A converters operate by dividing the total charge applied to a capacitor array. Typically, all capacitors are discharged first. Figure 8.2-15*a* shows an illustration of a charge-scaling D/A converter. A nonoverlapping, two-phase clock is used. ϕ_1 indicates that a switch is closed during phase 1, and similarly for ϕ_2. During ϕ_1, all capacitors in the array are discharged. Next, during ϕ_2, the capacitors associated with bits that are 1 are connected to V_{ref} and those with bits that are 0 are connected to ground. The resulting situation can be described by equating the charge on the capacitors connected to V_{ref} (C_{eq}) to the charge in the total capacitors (C_{tot}). This is expressed as

$$V_{\text{ref}} C_{\text{eq}} = V_{\text{ref}} \left(b_1 C + \frac{b_2 C}{2} + \frac{b_3 C}{2^2} + \cdots + \frac{b_N C}{2^{N-1}} \right) = C_{\text{tot}} V_{\text{OUT}} = 2CV_{\text{OUT}} \tag{8.2-12}$$

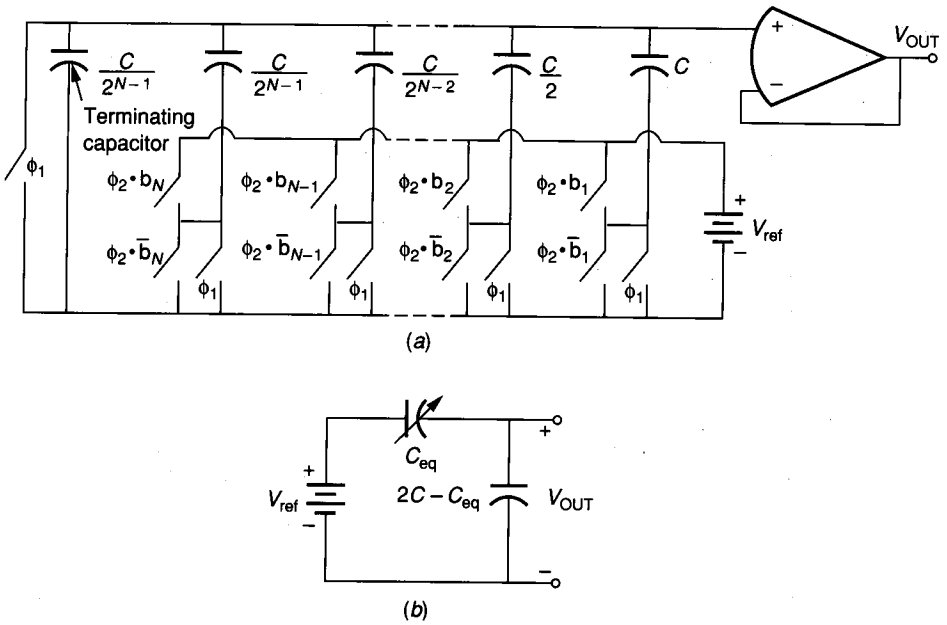


FIGURE 8.2-15
(*a*) Charge-scaling D/A converter, switches designated as $\phi_2 \cdot b_i (\phi_2 \cdot \bar{b}_i)$ close if both ϕ_2 and $b_i (\bar{b}_i)$ are true during ϕ_2, (*b*) Equivalent circuit of *a*.

From Eq. 8.2-12 we may solve for V_{OUT} as

$$V_{OUT} = (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N}) V_{ref} \qquad (8.2\text{-}13)$$

Another approach to understanding the circuit of Fig. 8.2-15*a* is to consider the capacitor array as a capacitive attenuator, illustrated in Fig. 8.2-15*b*. As before, C_{eq} consists of the sum of all capacitances connected to V_{ref}, and C_{tot} is the sum of all the capacitors in the array.

The D/A of Fig. 8.2-15*a* can be extended to have both + and − analog outputs if the bottom plates of all capacitors are connected to V_{ref} during the ϕ_1 phase period. During the ϕ_2 phase period, the capcitance associated with b_i, C_i is connected to ground if b_i is 1 or to V_{ref} if b_i is 0. The resulting output voltage is

$$V_{OUT} = -(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N}) V_{ref} \qquad (8.2\text{-}14)$$

The decision to select the + or − output will require an additional sign bit. If V_{ref} is also bipolar, then a four-quadrant D/A converter results.

The accuracy of the capacitors and the area required are both factors that limit the number of bits used. The accuracy of the D/A converter is seen to depend totally on the capacitor ratios and any parasitics. The accuracy of the equal-valued capacitor ratios for an MOS technology can be as low as 0.1% or better. If all of the capacitor ratios have this accuracy, then the D/A converter

of Fig. 8.2-15*a* should be capable of a 10-bit resolution. However, this implies that the ratio between the MSB and LSB capacitors will be 1024:1 which is undesirable from an area viewpoint. Also, the 0.1% capacitor ratio accuracy is applicable only for ratios in the neighborhood of unity.

Example 8.2-2. Assume that unit capacitors of 50 $\mu \times 50$ μ are used in the charge-scaling D/A converters of Fig. 8.2-15*a* and that the relative accuracy is 0.1%. Find the number of bits possible using a worst case approach assuming that the worst conditions occur at midscale (1 MSB). Next, assume that the relative accuracy of the unit capacitors deteriorates with N as given by

$$\frac{\Delta C}{C} \simeq 0.001 + 0.0001N$$

and find the number of bits possible using a worst case approach.

Solution. From Fig. 8.2-15*b* the ideal output voltage of the charge-scaling D/A converter can be expressed as

$$\frac{V_{\text{OUT}}}{V_{\text{REF}}} = \frac{C_{\text{eq}}}{2C}$$

Assume the worst-case output voltage is given as

$$\frac{V'_{\text{OUT}}}{V_{\text{REF}}} = \frac{C_{\text{eq}}(\text{min})}{[2C - C_{\text{eq}}](\text{max}) + C_{\text{eq}}(\text{min})}$$

The difference between the ideal and the worst case output can be written as

$$\frac{V_{\text{OUT}}}{V_{\text{REF}}} - \frac{V'_{\text{OUT}}}{V_{\text{REF}}} = \frac{C_{\text{eq}}}{2C} - \frac{C_{\text{eq}}(\text{min})}{[2C - C_{\text{eq}}](\text{max}) + C_{\text{eq}}(\text{min})}$$

If we assume that the worst-case condition occurs at midscale, then C_{eq} is equal to C. Therefore the difference between the ideal output and the worst-case output is

$$\frac{V_{\text{OUT}}}{V_{\text{REF}}} - \frac{V'_{\text{OUT}}}{V_{\text{REF}}} = \frac{1}{2} - \frac{C(\text{min})}{C(\text{max}) + C(\text{min})}$$

Replacing $C(\text{max})$ by $C + 0.5\Delta C$ and $C(\text{min})$ by $C - 0.5\Delta C$ and setting the difference between the ideal and worst-case output voltage equal to ± 0.5 LSB results in the following equation

$$\frac{\Delta C}{2C} = \frac{1}{2^N}$$

Using a value of 0.001 for $\Delta C/C$ gives approximately 11 bits. Using the approximation for $\Delta C/C$ of

$$\frac{\Delta C}{C} \simeq 0.001 + 0.0001N$$

shows that a 9-bit D/A converter should be realizable.

The cascade configuration of Fig. 8.2-13*a* can also be applied to the charge-scaling configuration. Figure 8.2-16*a* shows a 13-bit D/A converter with bipolar capability for V_{ref}. The 1.016 pF capacitor acts as a 64:1 divider,

which scales up the last 6 bits by a factor of 64. An equivalent circuit to the 13-bit D/A converter is shown in Fig. 8.2-16*b*. Two voltage sources are shown that depend on the state of each of the switches. The right-hand voltage source is given as

$$V_R = \sum_{i=1}^{7} \frac{\pm b_i C_i V_{ref}}{127} \tag{8.2-15}$$

where $C_i = C/2^{i-1}$ and the polarity of V_{ref} depends on the polarity of the digital word. The left-hand voltage source is given as

$$V_L = \sum_{k=8}^{13} \frac{\pm b_k C_k V_{ref}}{64} \tag{8.2-16}$$

where $C_k = C/(2^{k-7})$. The overall output of the D/A converter of Fig. 8.2-16*a* can be written as

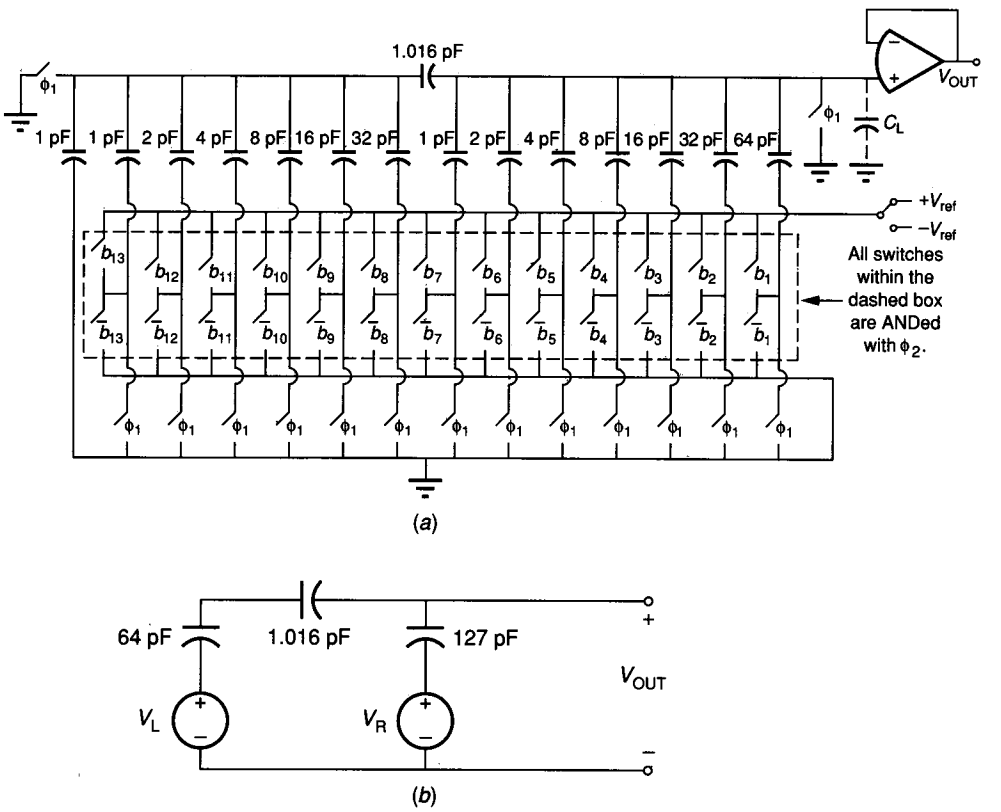


FIGURE 8.2-16
(*a*) A 13-bit, cascaded, charge-scaling D/A converter where C = 64 pF. Note that whether or not the switches in the dashed box close depends on the state of the binary variables, (*b*) An equivalent circuit of *a*.

$$V_{OUT} = \frac{\pm V_{ref}}{128}\left(\sum_{i=1}^{7} b_i C_i + \sum_{k=8}^{13} b_k \frac{C_k}{64}\right) \tag{8.2-17}$$

The charge-scaling D/A converters are sensitive to capacitive loading at the summing node. If this capacitance is designated as C_L, then Eq. 8.2-17 is modified as

$$V_{OUT} = \left(1 - \frac{C_L}{128}\right)\left(\frac{\pm V_{ref}}{128}\right)\left(\sum_{i=1}^{7} b_i C_i + \sum_{k=8}^{13} b_k \frac{C_k}{64}\right) \tag{8.2-18}$$

We see that C_L has caused an error of $\left[1 - (C_L/128)\right]$. If C_L is 1% of the total ladder capacitance, then a 1% error is introduced by the capacitance C_L.

The accuracy of the capacitor attenuator must also be good enough for the cascade approach to work. A deviation of the 1.016 pF divider capacitance from the desired ratio of 1.016:1 introduces both gain and linearity errors. Assuming a variation of $\pm\Delta C$ in the 1.016 pF capacitor modifies the output given in Eq. 8.2-17 to

$$V_{OUT} = \left(\frac{\pm V_{ref}}{128}\right)\left(1 - \frac{\Delta C}{128}\right)\left[\sum_{i=1}^{7} b_i C_i + (1 + \Delta C)\sum_{k=8}^{13} b_k \frac{C_k}{64}\right] \tag{8.2-19}$$

If we assume that $\Delta C/C = \pm 0.016$ (1.6% error), then the gain term has an error of

$$\text{Gain error term} = 1 - \left(\frac{\Delta C}{128}\right) = 1 - \left[\frac{1}{(64)(128)}\right] \tag{8.2-20}$$

which is negligible. The linearity error term is given by

$$\text{Linearity error term} = \Delta C \sum_{k=8}^{13} \frac{b_k C_k}{64} \tag{8.2-21}$$

The worst-case error occurs for all $b_i = 1$ and is essentially ΔC. It is also important to keep $+V_{ref}$ and $-V_{ref}$ stable and equal in amplitude. This influences the long-term stability and gain tracking of the D/A converter.

A different, charge redistribution, two-stage, 8-bit D/A converter is shown in Fig. 8.2-17. An op amp is connected in its inverting configuration with the $2C$ capacitor fed back from the output to the inverting input of the op amp. Because the input node is a virtual ground during operation, the capacitive parasitics associated with the input node to the op amp are eliminated. The converter of Fig. 8.2-17 should give better transient response and less error because of the removal of the influence of the capacitive parasitic at the op amp input.

8.2.4 D/A Converters Using Combinations of Scaling Approaches

The voltage-scaling and charge-scaling approaches to implementing D/A converters can be combined, resulting in converters having a resolution that exceeds the number of bits of the separate approaches. An M-bit resistor string and a K-bit binary-weighted capacitor array can be used to achieve an $N = (M + K)$-bit

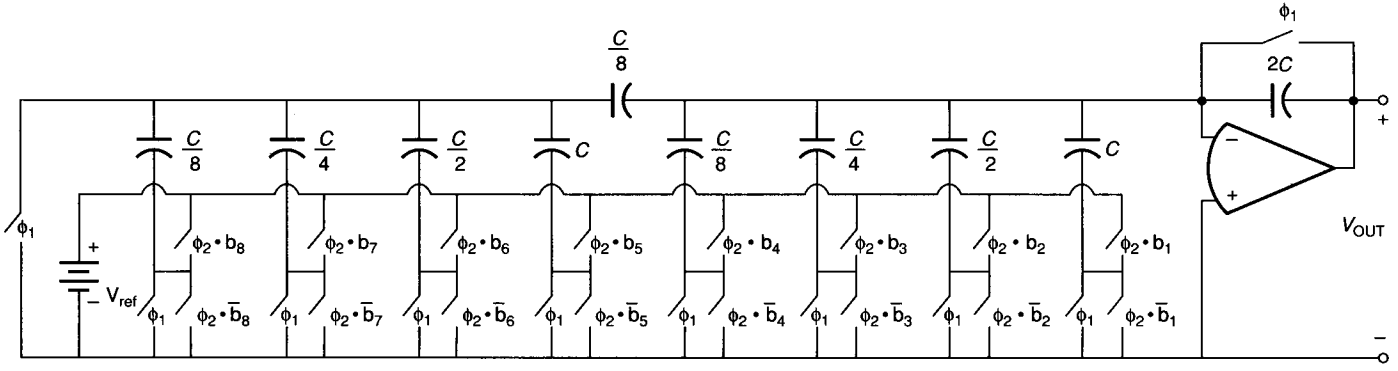


FIGURE 8.2-17
A cascade charge-scaling D/A converter that is insensitive to nodal capacitive parasitics for the MSB part.

conversion. Figure 8.2-18 gives an example of such a converter, where $M = 4$ and $K = 8$. The resistor string, R_1 through R_{2^M}, provides inherently monotonic V_{ref} for 2^M nominally identical voltage segments. The binary-weighted capacitor array, C_1 through C_K, is used to subdivide any one of these voltage segments into 2^K levels. This is accomplished by the following sequence of events. First, the switches S_F, S_B, and S_{M+1B} through $S_{K+M,B}$ are closed, connecting the top and bottom plates of the capacitors C_1 through C_K to ground. If the output of the D/A converter is applied to any circuit having an offset, switch S_B could be connected to this circuit rather than ground to cancel this offset. After opening switch S_F, the buses A and B are connected across one of the resistors of the resistor string as determined by the M MSBs. The upper and lower voltages across this resistor will be $V'_{\text{ref}} + 2^{-M} V_{\text{ref}}$ and V'_{ref}, respectively, where

$$V'_{\text{ref}} = V_{\text{ref}} (b_1 2^{-1} + b_2 2^{-2} + \cdots + b_{M-1} 2^{-(M-1)} + b_M 2^{-M}) \quad . \quad (8.2\text{-}22)$$

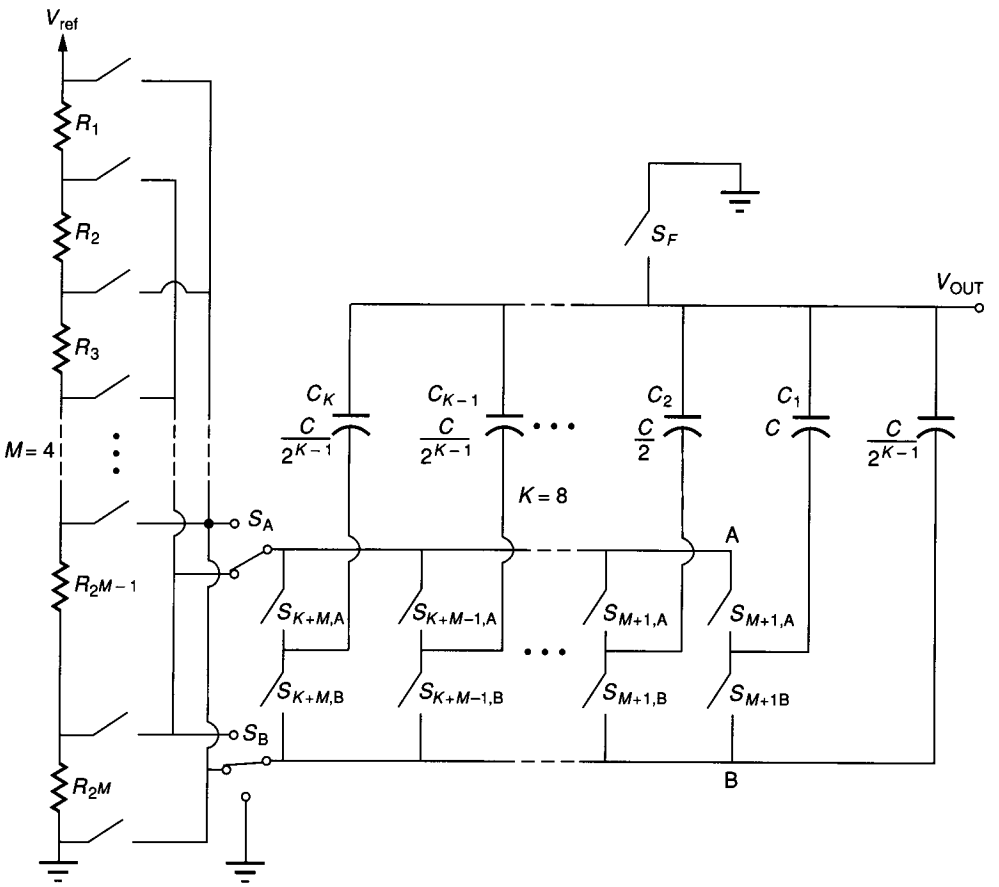


FIGURE 8.2-18
A D/A converter using a combination of voltage-scaling and charge-scaling techniques. The 4 MSBs are accomplished by voltage-scaling, and the 8 LSBs are accomplished by charge-scaling.

Although the resistor string could take the form of Fig. 8.2-14*a*, the configuration used in Fig. 8.2-18 switches both buses A and B. This causes any switch imperfections, such as clock feedthrough, to be canceled. The proper switch closures including S_A and S_B will require decoding of the M bits. After $2^{-M} V'_{ref}$ is applied between the buses A and B, we have the equivalent circuit of Fig. 8.2-19*a*. The final step is to decide whether or not to connect the bottom plates of the capacitors to bus A or bus B. This is determined by the bits of the digital word being converted. The equivalent circuit for the analog output voltage of the D/A converter of Fig. 8.2-18 is shown in Fig. 8.2-19*b*. The output of the D/A converter of fig. 8.2-18 is given as

$$V_{OUT} = V'_{ref} + V_{ref}\left[\frac{b_{M+1}}{2^{M+1}} + \frac{b_{M+2}}{s^{M+2}} + \cdots + \frac{b_{M+K+1}}{2^{M+K+1}} + \frac{b_{M+K}}{2^{M+K}}\right] \tag{8.2-23}$$

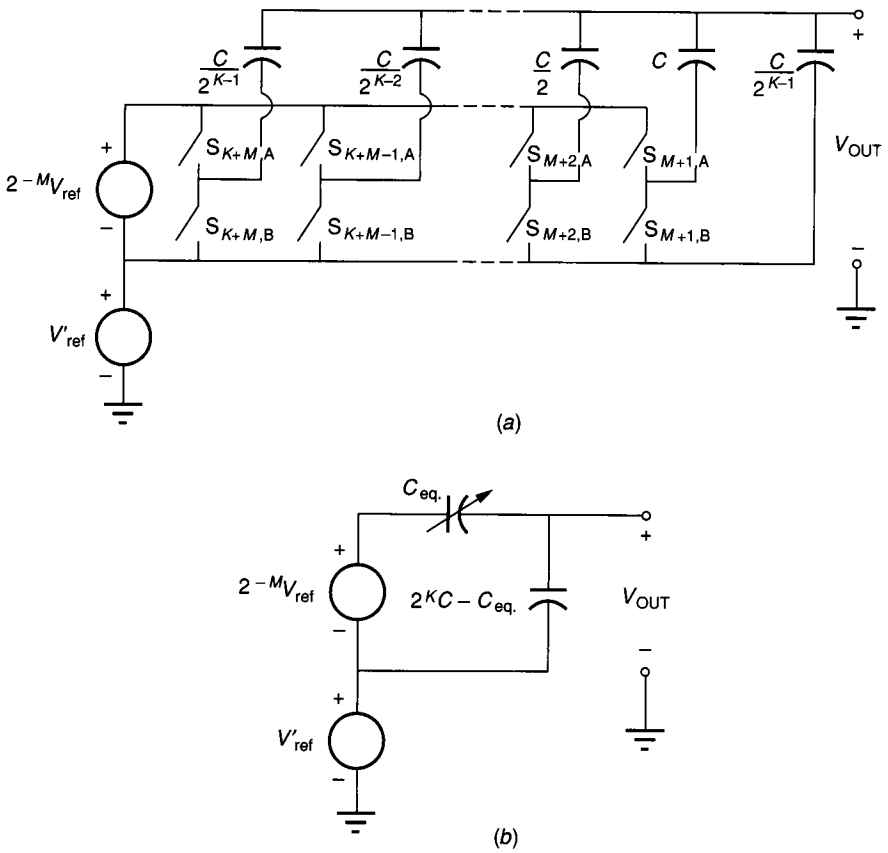


FIGURE 8.2-19
(*a*) Equivalent circuit of Fig. 8.2-18 for the voltage scaling part, (*b*) Equivalent circuit of the entire Fig. 8.2-18. C_{eq} is the sum of all the capacitors whose bit is 1.

The D/A converter of Fig. 8.2-18 has the advantage that, because the resistor string is inherently monotonic, the M MSB bits will be monotonic regardless of any resistor mismatch. This implies that the capacitor array has to be ratio-accurate to only K bits and still be able to provide $(M + K)$-bit monotonic conversion. The conversion speed for the resistors is faster than for the capacitors because no precharging is necessary. Therefore, some interesting tradeoffs can be made between area and speed of conversion. Techniques such as trimming the resistor string using polysilicon fuses can help to improve the integral linearity of this approach.

Other combinations of voltage scaling and charge scaling techniques are also possible. Instead of using resistive string techniques for the MSBs and binary-weighted capacitors for the LSBs, one can use binary-weighted capacitors for the MSBs and the resistor string for the LSBs. It is necessary to trim the resistors to maintain sufficient integral and differential nonlinearity for this case. Figure 8.2-20 illustrates how such a D/A converter could be implemented. The 3 to 4 MSBs will probably have to be trimmed, using a technique such as polysilicon fuses. The trimmed components are indicated by the dashed arrows through the appropriate capacitors in Fig. 8.2-20.

The combination of the voltage scaling and charge scaling allows for optimizing the performance. The choices are whether the MSBs will be resistors or capacitors and how the total number of bits will be divided into MSBs and LSBs.

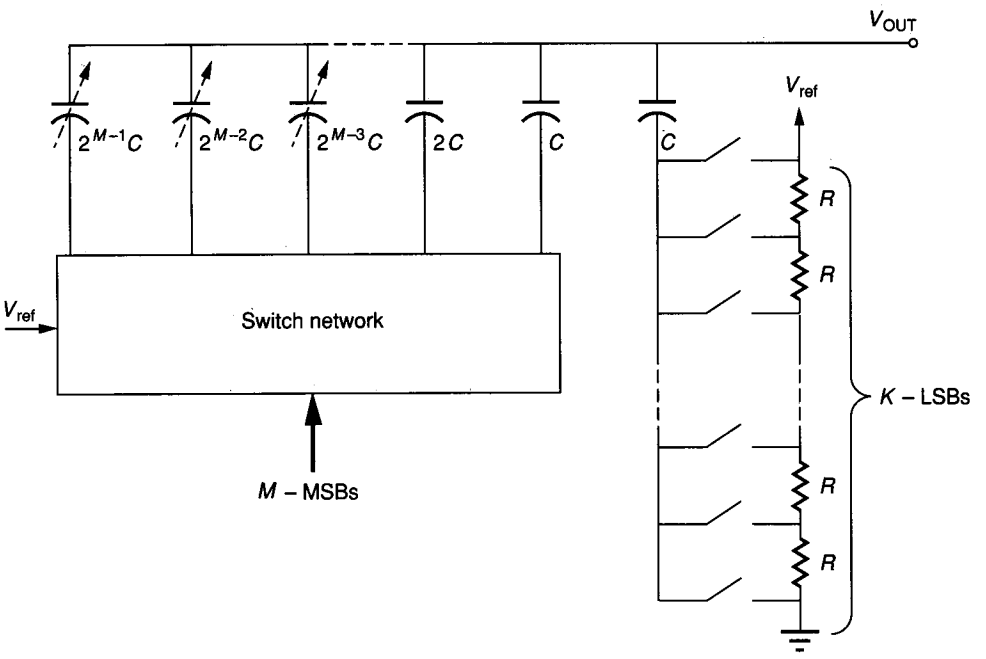


FIGURE 8.2-20
An illustration of a D/A converter using charge-scaling for MSBs and voltage-scaling for LSBs

For example, knowing the area of a unit resistor and a unit capacitor and their relative accuracies allows a tradeoff to be made in decreasing the area required and decreasing the nonlinearity of the D/A converter.

8.2.5 Serial D/A Converters

The last category of D/A converters to be considered in this section is the serial D/A converter. A serial D/A converter is one in which the conversion is done sequentially. In the best case, one clock cycle is required to convert one bit. Thus, N clock pulses would be required for the typical serial N-bit D/A converter. The two types of serial converters that will be examined here are the charge redistribution and the algorithmic D/A converters.

Figure 8.2-21 shows the simplified schematic of a serial charge redistribution D/A converter. We see that this converter consists of four switches, two equal-valued capacitors, and a reference voltage. The function of the switches is as follows. S1 is called the *redistribution switch* and places C_1 in parallel with C_2 causing their voltages to become identical through charge redistribution. Switch S2 is used to precharge C_1 to V_{ref}, if the ith bit, b_i, is a 1, and switch S3 is used to precharge C_1 to 0 V if the ith bit is 0. Switch S4 is used at the beginning of the conversion process to initially discharge C_2. An example is used to illustrate the operation of this D/A converter.

Example 8.2-3. Operation of the serial D/A converter. Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_1 = 1, b_2 = 1, b_3 = 0$, and $b_4 = 1$. Find the final voltage across C_1 and C_2 in terms of V_{ref}.

Solution. The conversion starts with the closing and opening of switch S4, so that $V_{C2} = 0$. Since $b_4 = 1$, then switch S2 is closed causing $V_{C1} = V_{ref}$. Next, switch S1 is closed, after switch S2 is opened, causing $V_{C1} = V_{C2} = 0.5V_{ref}$. This completes the conversion of the LSB. Figure 8.2-22 illustrates the waveforms across C_1 and C_2 in this example. Going to the next LSB, b_3, switch S3 is closed, discharging C_1 to ground. When switch S3 opens and switch S1 closes, the voltage across both C_1 and C_2 is $0.25V_{ref}$. Because the remaining bits are both 1, C_1 will be connected to V_{ref} and then connected to C_2 two times in succession. The final voltage across C_1 and C_2 will be $(13/16)V_{ref}$. This sequence of events will require nine sequential switch closures to complete the conversion.

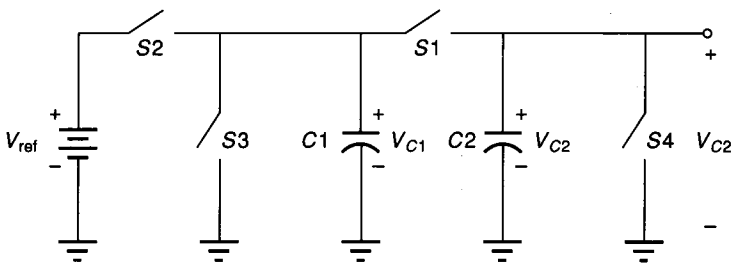


FIGURE 8.2-21
Simplified schematic of a serial charge redistribution D/A converter.

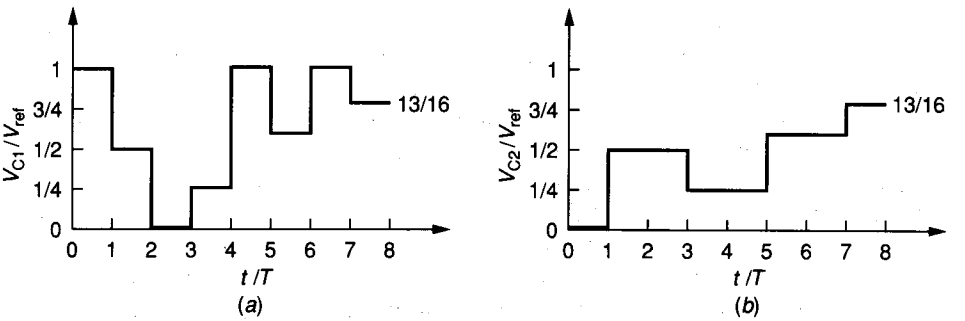


FIGURE 8.2-22
Waveforms of Fig. 8.2-21 for the conversion of 1101: (*a*) Voltage across C1, (*b*) Voltage across C2.

From this example, it can be seen that the serial D/A converter requires considerable supporting external circuitry to make the decision of which switch to close during the conversion process. Although the circuit for the conversion is extremely simple, several sources of error will limit the performance of this type of D/A converter. These sources of error include the capacitor parasitic capacitances, the switch parasitic capacitances, and the clock feedthrough errors. The capacitors C_1 and C_2 must be matched to within ± 0.5 LSB accuracy. This converter has the advantage of monotonicity and requires very little area for the portion shown in Fig. 8.2-21. An 8-bit converter using this technique has been fabricated and has demonstrated a conversion time of 13.5 μs.[4]

A second approach to serial D/A conversion is called *algorithmic*.[5] Figure 8.2-23 illustrates the pipeline approach to implementing an algorithmic D/A converter, consisting of unit delays and weighted summers. It can be shown that the output of this circuit is

$$V_{\text{out}}(z) = (d_1 z^{-1} + 2^{-1} d_2 z^{-2} + \cdots + 2^{-(N-1)} d_N z^{-N} + 2^{-N} d_{N+1} z^{-(N+1)}) V_{\text{ref}} \quad (8.2\text{-}24)$$

where d_i is a modified binary variable with a high state of $+1$ and a low state of -1 and z^{-1} is defined as the unit delay operator. Figure 8.2-23 shows that it takes n clock cycles for the digital word to be converted to an analog signal, even though a new digital word can be converted on every clock cycle. An advantage

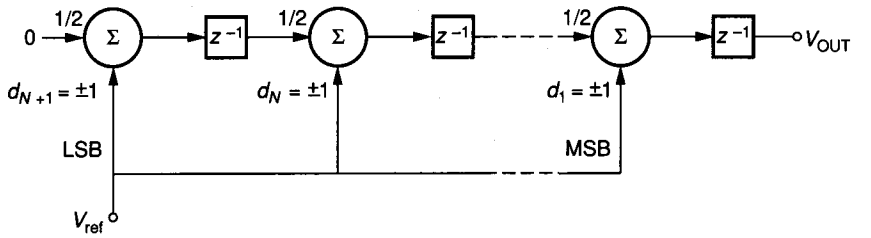


FIGURE 8.2-23
Pipeline approach to implementing an algorithmic D/A converter.

of the pipeline converter is that it can consist of similar stages. If a zero is input to the first amplifier, then the first stage is similar to the remaining stages.

The complexity of Fig. 8.2-23 can be reduced using the techniques of *replication* and *iteration*. Here we shall consider only the iteration approach. Equation 8.2-23 can be rewritten as

$$V_{\text{out}}(z) = \frac{d_i z^{-1} V_{\text{ref}}}{1 - 0.5z^{-1}} \tag{8.2-25}$$

where the d_i are either $+1$ or -1, determined as follows. Figure 8.2-24 shows a block diagram realization of Eq. 8.2-24. It consists of two switches, A and B. Switch A is closed when the ith bit is 1, and switch B is closed when the ith bit is 0. $d_i V_{\text{ref}}$ is summed with one-half of the previous output and applied to the sample-and-hold circuit, which outputs the results for the ith-bit conversion. The following example illustrates the conversion process.

Example 8.2-4. D/A conversion using the algorithmic method. Assume that the digital word to be converted is 11001 in the order of MSB to LSB and find the analog value of this digital word in terms of V_{ref}.

Solution. The conversion starts by zeroing the output (not shown in Fig. 8.2-24). Figure 8.2-25 is a plot of the output of this example. T is the period for the conversion of one bit. The process starts with the LSB, which in this case is 1. Switch A is closed and V_{ref} is summed with zero to give an output of $+V_{\text{ref}}$. On the second conversion, the bit is 0 so that switch B is closed. Thus, $-V_{\text{ref}}$ is summed with $(1/2)V_{\text{ref}}$ giving $-(1/2)V_{\text{ref}}$ as the output. On the third conversion, the bit is also 0, so that $-V_{\text{ref}}$ is summed with $-(1/4)V_{\text{ref}}$ to give an output of $-(5/4)V_{\text{ref}}$. On the fourth conversion, the bit is 1; thus, V_{ref} is summed with $-(5/8)V_{\text{ref}}$, giving $+(3/8)V_{\text{ref}}$ at the output. Finally, the MSB is unity, which causes V_{ref} to be summed with $(3/16)V_{\text{ref}}$, giving the final analog output of $+(19/16)V_{\text{ref}}$. Because the actual FSR of this example is $\pm V_{\text{ref}}$ or $2V_{\text{ref}}$, the analog value of the digital word 11001 is $(19/32) \times 2V_{\text{ref}}$, or $(19/16)V_{\text{ref}}$.

The algorithmic converter has the primary advantage of being independent of capacitor ratios; thus, it is often called the *ratio-independent* algorithmic D/A converter. However, the amplifier with a gain of 1/2 will still depend on capacitor

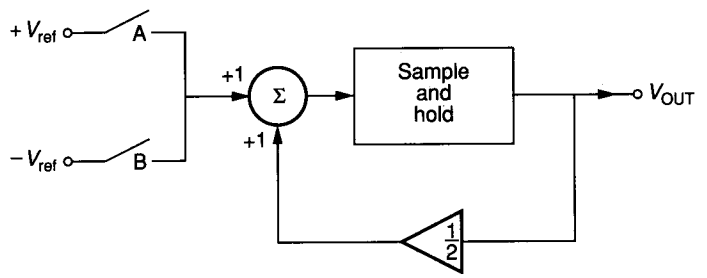


FIGURE 8.2-24
Equivalent realization of Fig. 8.2-23 using iterative techniques.

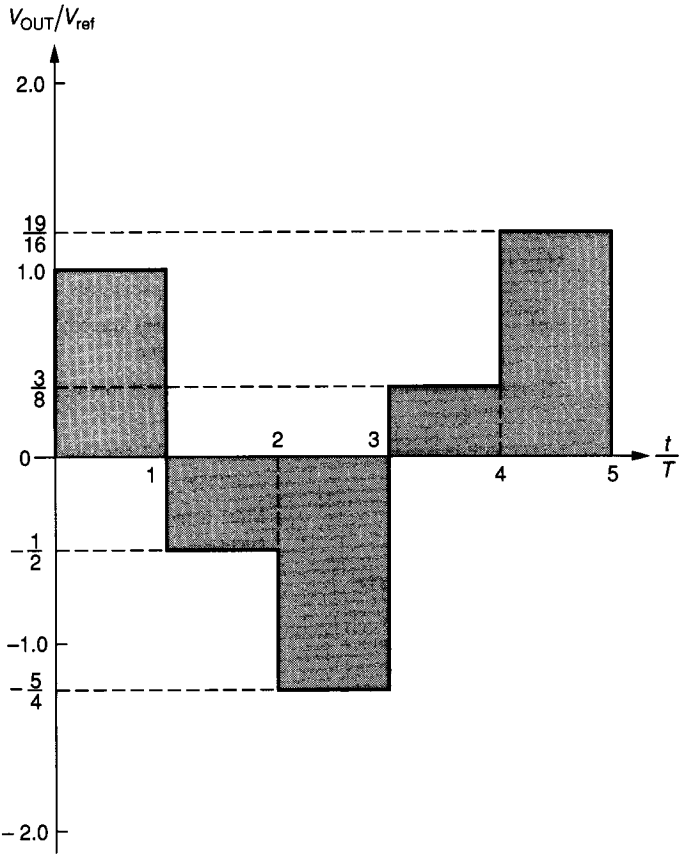


FIGURE 8.2-25
Output waveform for Fig. 8.2-24 for the conditions of Example 8.2-2.

ratios or other ratios and must have an accuracy better than ±0.5 LSB. The algorithmic converter will be presented again under the subject of serial A/D converters. The serial D/A converter is very simple but requires a longer time for conversion. In some applications, these characteristics are advantageous.

D/A converter techniques compatible with BJT and MOS technology have been presented in this section. Table 8.2-1 gives a summary of these D/A

TABLE 8.2-1
Comparison of the D/A conversion techniques compatible with BJT and MOS technology

D/A converters	Figure	Advantage	Disadvantage
Current-scaling, binary-weighted	8.2-10	Fast; insensitive to switch parasitics	Large element spread; nonmonotonic
Current-scaling, *R*-2*R* ladder	8.2-11	Fast; small element spread	Nonmonotonic; sensitive to switch parasitics

(continued)

TABLE 8.2-1
(Continued)

D/A converters	Figure	Advantage	Disadvantage
Current-scaling, cascade	8.2-13*a*	Minimum area; monotonic	R_1 must be accurate
Current-scaling, master-slave	8.2-13*b*	Minimum area; monotonic	I_1 must be accurate
Voltage-scaling	8.2-14*a*	Monotonic	Large area; sensitive to parasitic capacitances
Charge-scaling	8.2-15*a*	Fast	Large element spread; nonmonotonic
Charge-scaling, cascade	8.2-16*a*	Minimum area	Nonmonotonic; divider must be accurate
Voltage-scaling, charge-scaling	8.2-18	Monotonic in MSBs	Must trim for absolute accuracy
Charge scaling, voltage-scaling	8.2-20	Monotonic in LSBs	Must trim for absolute accuracy
Serial, charge redistribution	8.2-21	Simple; minimum area	Slow; requires complex external circuits
Serial, algorithmic	8.2-24	Simple; minimum area	Slow; requires complex external circuits

converters. In the following sections, we shall examine the complementary subject of A/D converters. Many of the A/D converters that will be discussed use the D/A converters developed and illustrated in this section.

8.3 ANALOG-TO-DIGITAL CONVERTERS

The principles and characteristics of analog-to-digital converters are examined in this section. The objective of an A/D converter is to determine the output digital word corresponding to an analog input signal. The A/D converter usually requires a sample-and-hold circuit at the input because it is not possible to convert a changing analog input signal. We shall see that A/D converters often make use of D/A converters, which is why this section follows the last. The types of A/D converters that will be considered include the serial, successive approximation, parallel (flash), and high performance A/D converters.

Figure 8.3-1 shows the block diagram of a basic parallel A/D converter. The input to the A/D is from a sample-and-hold circuit and is designated as V_{in}^*. The voltages V_0 through V_{N-1} represent reference voltages that are all proportional to a single reference voltage, V_{ref}. The input, along with a reference voltage, V_{ref}, is used to determine the digital word that best represents the sampled analog input signal. The comparator outputs, X_i, are then encoded into an output digital word. The means by which the conversion is accomplished may be different from that suggested in Fig. 8.3-1. Regardless of how the conversion is made, the A/D

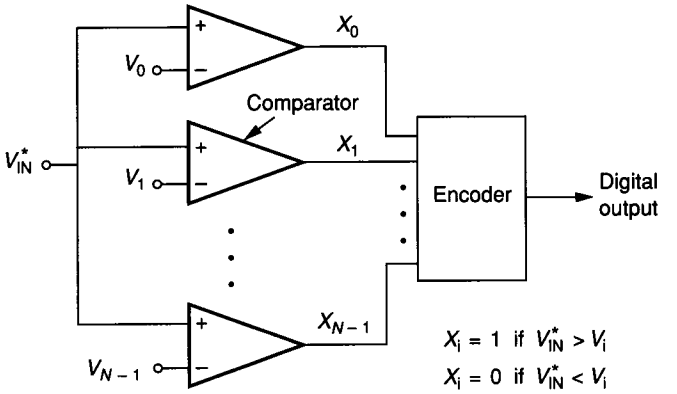


FIGURE 8.3-1
Block diagram of a general analog-to-digital converter.

converter is a device that converts a continuous range of input amplitude levels into a discrete, finite set of digital words.

The characterization of the A/D converter is almost identical to that of the D/A converter in the last section if the input and output definitions are interchanged. The static A/D converter properties will be considered first. Figure 8.3-2 shows the transfer characteristic of an ideal 3-bit A/D converter. This characteristic is analogous to Fig. 8.2-6 for the D/A converter. The analog input

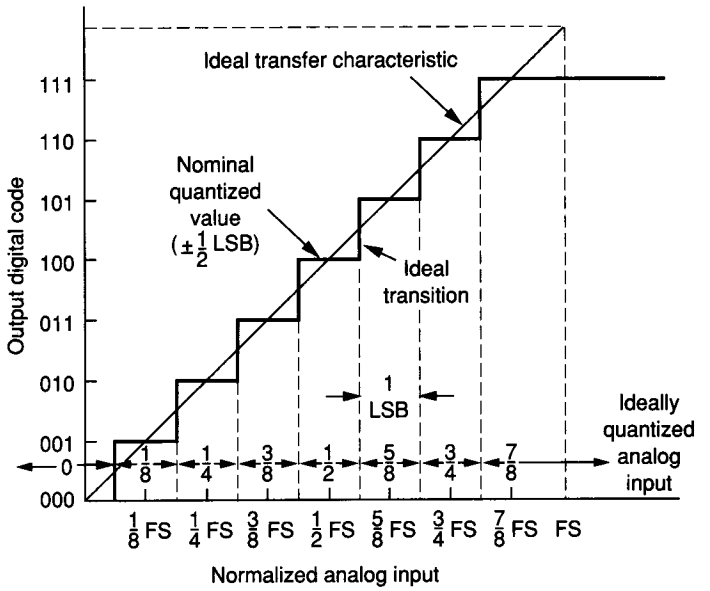


FIGURE 8.3-2
Ideal input-output characteristics for a 3-bit A/D converter.

voltage normalized to full scale (FS) is shown on the horizontal axis. The digital output code is given on the vertical axis.

The A/D converter has been designed so that the output digital word changes when the analog input is at odd multiples of FS/16. The LSB of the digital output code changes each time the analog input changes by $FS/2^n$ where n is equal to the number of digital bits. A change of $FS/2^n$ in the analog input is called an LSB in the same manner as defined for the D/A converter. In Fig. 8.3-2, an LSB is the length of the horizontal part of the stairstep, or FS/8. The ideally quantized ranges of the analog input are shown just above the horizontal axis on Fig. 8.3-2. These ranges are centered about even multiples of FS/16 except for the rightmost and leftmost, which have no right or left limits, respectively.

The definitions of resolution and quantization noise were given in Sec. 8.2 for both the A/D and D/A converter. The straight line on Fig. 8.3-2 through the midpoint of each step represents the ideal transfer characteristic of the A/D converter as the resolution approaches infinity. The full scale range, dynamic range, and the signal-to-noise ratio defined in Sec. 8.2 in terms of the analog axis of the characteristic also apply to the A/D converter.

The remaining static characteristics include offset error, gain error, nonlinearity, and monotonicity. Figure 8.3-3 illustrates each one of these characteristics for a 3-bit A/D converter. In each case, the ideal characteristic is shown by dashed lines for comparison. Because these characteristics are usually referred to the analog signal, the definitions given in Sec. 8.2 are also applicable for the A/D converter. Figure 8.3-3*a* illustrates the offset error in a 3-bit A/D converter. Figure 8.3-3*b* shows the gain error for the A/D converter and is similar to that of Fig. 8.2-7*b*. Figure 8.3-3*c* shows the nonlinearity characteristics of a 3-bit A/D converter. Integral and differential nonlinearity have the same definition as for the D/A converter. The maximum deviation from ideal occurs at the transition from 110 to 111 and is 1.5 LSB or 18.75% of FS. Figure 8.3-3*d* illustrates excessive differential nonlinearity, which causes nonmonotonic behavior in D/A converters. However, in A/D converters, nonmonotonicity typically manifests itself as missed codes. In Fig. 8.3-3*d* the digital codes 010, 011, and 110 are skipped.

The dynamic characteristics of an A/D converter have to do primarily with the speed of operation. Because either the input or the output of a converter is a digital word, sampling or discrete time signals are inherent. Therefore, the rate at which the converter can operate is of interest. The *conversion time* is the time from the application of the signal to start conversion to the availability of the completed output signal (digital or analog). Typically, a D/A converter can provide an analog output signal very soon after the digital word is applied (except for the serial converters). On the other hand, A/D converters may require one or more clock cycles following the application of the analog input signal before the output digital word is available.

Because a sample-and-hold circuit is a key aspect of the A/D converter, it is worthwhile to examine it in more detail than that of Fig. 8.2-3. Figure 8.3-4 shows the waveforms of a practical sample-and-hold circuit. The *acquisition time*, indicated by t_a, is the time during which the sample-and-hold circuit must remain in the sample mode to ensure that the subsequent hold mode output will be within a specified error band of the input level that existed at the instant of

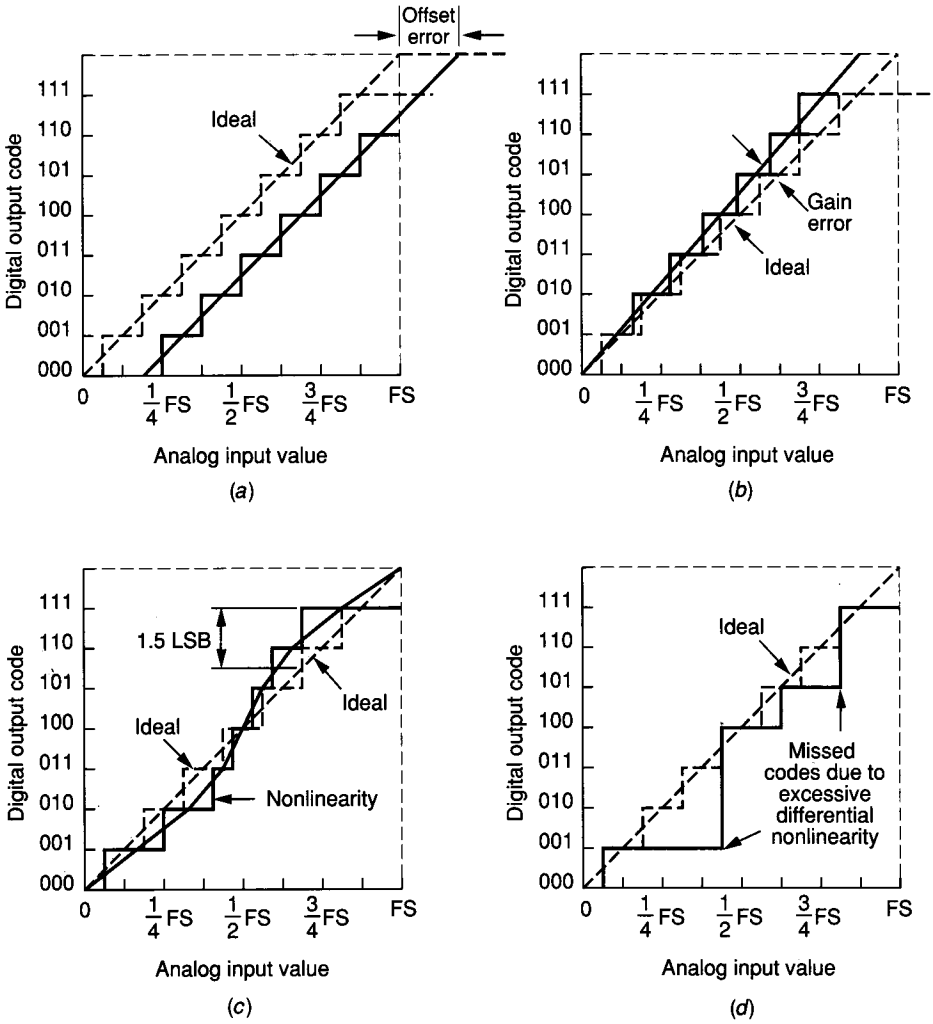


FIGURE 8.3-3
Characterization of a 3-bit A/D converter: (*a*) Offset error, (*b*) Scale factor (gain) error, (*c*) Integral linearity, (*d*) Differential linearity.

the sample-and-hold conversion. The acquisition time assumes that the gain and offset effects have been removed. The *settling time*, indicated by t_s, is the time interval between the sample-and-hold transition command and the time when the output transient and subsequent ringing have settled to within a specified error band. Thus, the minimum sample-and-hold time is equal to the sum of t_a and t_s. The minimum conversion time for an A/D converter is equal to T_{sample}, and the maximum sample rate is

$$f_{\text{sample}} = \frac{1}{T_{\text{sample}}} = \frac{1}{t_s + t_a} \tag{8.3-1}$$

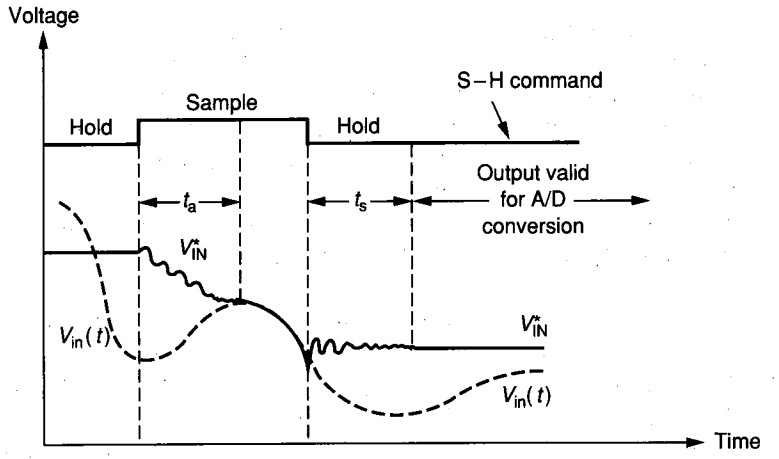


FIGURE 8.3-4
Waveforms for a sample-and-hold circuit.

The dynamic performance of the converter will depend largely on the dynamic characteristics of the op amps and comparators. Therefore, the slew rate, settling time, and overload recovery time of these circuits are of importance. It should be remembered that f_{sample} is the maximum sample rate and the effective bandwidth will be at least two times lower than f_{sample} to satisfy Nyquist criterion.

An important aspect of the conversion time is the aperture uncertainty. The *aperture uncertainty* is the time jitter in the sample point and is caused by short-term stability errors in the timebase generating the sample command to the A/D converter. The time jitter causes an amplitude uncertainty, which depends on the rate of rise of the signal at the sample point.

In addition to the dynamic characteristics of converters, there are characteristics having to do with stability of operation. These characteristics define the immunity of the converter to time, temperature, power supplies, and component aging. These characteristics are typically expressed in terms of the change of the converter performance parameter per unit change in the quantity affecting influence. Examples include the *temperature coefficient of linearity, temperature coefficient of gain,* and the *temperature coefficient of differential nonlinearity*. Also of importance to the stability of a converter is the voltage reference, which was presented in Chapter 5. The voltage reference can be supplied externally or internally to the integrated circuit converter. It is important that the reference provide the stability necessary for the proper operation of the converter.

It is of interest to consider how one can test converters. Testing is divided into static and dynamic tests for D/A and A/D converters. Most test configurations require the ability to resolve the analog signal to within ± 0.5 LSB, which can be very demanding if the number of bits is large. Techniques for testing both types of converters can be found in more detail in the literature.[6-8] Often, a computer

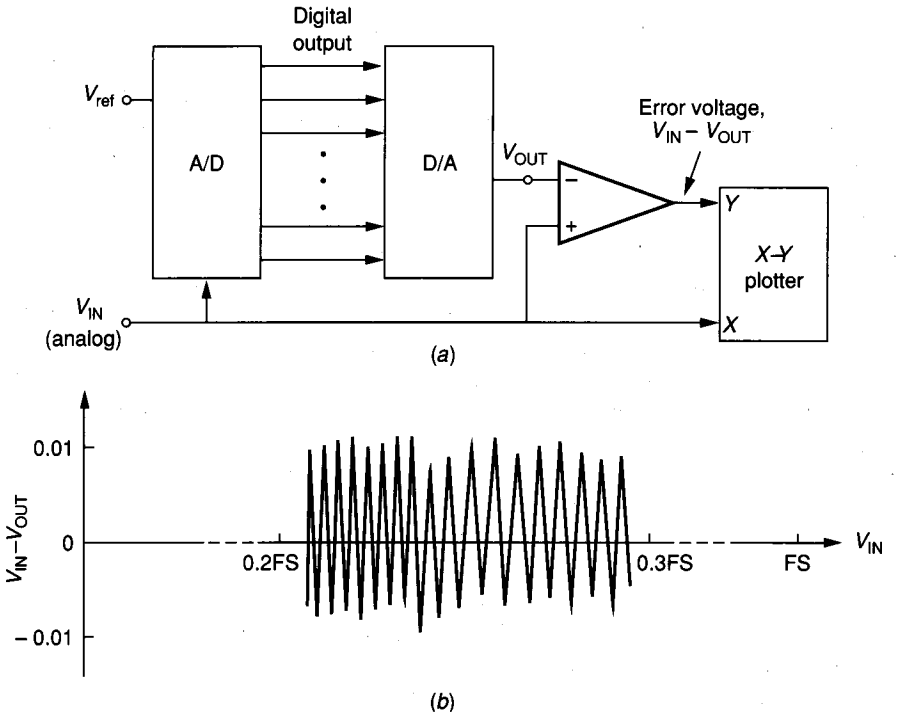


FIGURE 8.3-5
(*a*) A method of testing A/D and D/A converters, (*b*) Typical output for the error voltage of *a*.

is used to perform the tests on the converter. One simple means of testing both the D/A and A/D converters is shown in Fig. 8.3-5*a*. In this configuration, the output of an A/D converter is connected to the input of the D/A converter, resulting in an error voltage that can be plotted on an *X-Y* recorder as a function of the amplitude of the analog input signal. A typical portion of the error voltage for a 12-bit converter is shown in Fig. 8.3-5*b*. In this test either the A/D or D/A converter will be the device under test (DUT). The other converter must have higher performance and resolution than the DUT in order to be able to measure its performance without error. The order of the A/D and D/A converters in Fig. 8.3-5*a* can be interchanged so that the input and output are digital words that can be compared.

Several other approaches to testing the performance of an A/D converter will be briefly described. A high-quality sinusoid whose peak-to-peak amplitude is equal to the full scale value of the analog input can be used to test the A/D converter. Two such tests are called the *histogram test* and the *Fast Fourier Transform (FFT) test*. In the histogram test, a sinusoid of FS peak-to-peak amplitude is applied to the input of the A/D converter. The frequency is selected to avoid coherence with the sample rate of the A/D converter. A large number of samples of the digital output code are taken and expressed in the form of a histogram. A

perfect A/D converter would produce a cusp-shaped probability density function given by

$$p(V) = \left[\pi(A^2 - V^2)^{1/2}\right]^{-1} \tag{8.3-2}$$

where A is the peak amplitude of the sine wave (FS/2) and $p(V)$ is the probability of an occurrence at a voltage V. Nonlinear behavior will show up as spikes rising above the ideal probability density function, and missing codes will be gaps in the probability density function. The frequency of the sinusoid can be increased to determine the upper frequency limits for the A/D converter performance. The histogram test can also detect offset and gain errors. Offset errors cause the histogram to be asymmetrical about the A/D converter output code corresponding to midscale. Gain errors can be determined from the width of the histogram.

The FFT test can also be used to evaluate the A/D converter performance. First, a spectrally pure sinusoid of amplitude 0.5 FS is applied to the input of the A/D converter. A 2^N point record sampled at the maximum sampling rate is taken and converted to the frequency domain using an FFT algorithm. The harmonics of the input sinusoid caused by the nonlinearity of the A/D converter are aliased into the baseband spectrum and can be used to identify the nonlinear performance of the A/D converter. The frequency of the input sine wave must be selected so that harmonics aliased into the baseband do not coincide with the fundamental. If the ratio of the fundamental to the highest amplitude harmonic on an N-bit A/D converter is greater than $6N$ dB, the error contribution of the nonlinearity is insignificant compared with the quantization noise. Unfortunately, even very low levels of harmonics may be sufficient to create encoding errors by causing a voltage near a threshold level to go to the next quantization level.

The above tests are typical of those applied to complex A/D converters. Further details and other types of testing procedures can be found in the references.[6–8] We next consider the various architectures for realizing A/D converters in MOS and/or bipolar technologies.

8.3.1 Serial A/D Converters

The serial A/D converter is similar to the serial D/A converter in that it performs serial operations until the conversion is complete. We shall examine two architectures, called the *single-slope* and the *dual-slope*. Figure 8.3-6 gives the block diagram of a single-slope serial A/D converter. This type of converter consists of a ramp generator, an interval counter, a comparator, an AND gate, and a counter that generates the output digital word. At the beginning of a conversion cycle, the analog input is sampled and held and applied to the positive terminal of the comparator. The counters are reset, and a clock is applied to both the time interval counter and the AND gate. On the first clock pulse, the ramp generator begins to integrate the reference voltage, V_{ref}. If V_{IN}^* is greater than the initial output of the ramp generator, then the output of the ramp generator, which is applied to the negative terminal of the comparator, begins to rise. Because V_{IN}^* is greater than the output of the ramp generator, the output of the comparator is high and each clock pulse applied to the AND gate causes the counter at the output to

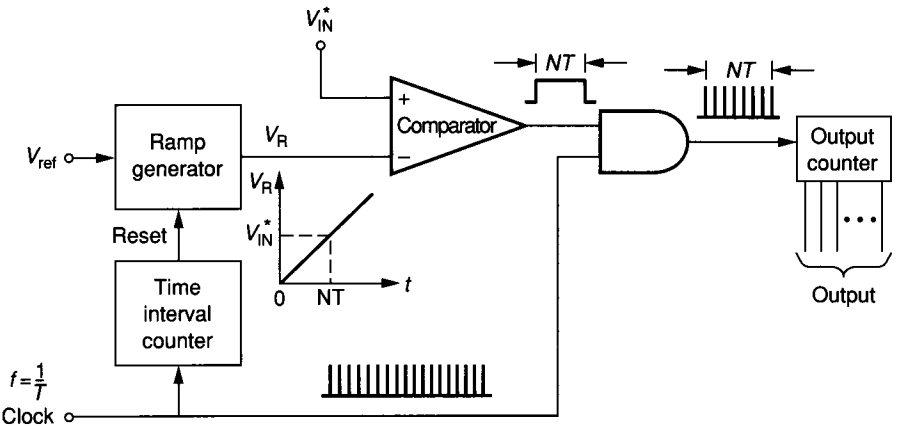


FIGURE 8.3-6
Block diagram of a single-slope serial A/D converter.

count. Finally, when the output of the ramp generator is equal to V_{IN}^*, the output of the comparator goes low, and the output counter is now inhibited. The binary number representing the state of the output counter can now be converted to the desired digital word format.

The single-slope A/D converter can have many different implementations. For example, the interval counter can be replaced by logic to detect the state of the comparator output and reset the ramp generator when its output has exceeded V_{IN}^*. The serial A/D converter has the advantage of simplicity of operation. Disadvantages of the single-slope A/D converter are that it is subject to error in the ramp generator and it is unipolar. Another disadvantage of the single-slope A/D converter is that a long conversion time ($2^N T$ in the worst case) is required if the input voltage is near the value of V_{ref}.

A block diagram of a dual-slope A/D converter is shown in Fig. 8.3-7. The basic advantage of this architecture is the elimination of the dependence of the

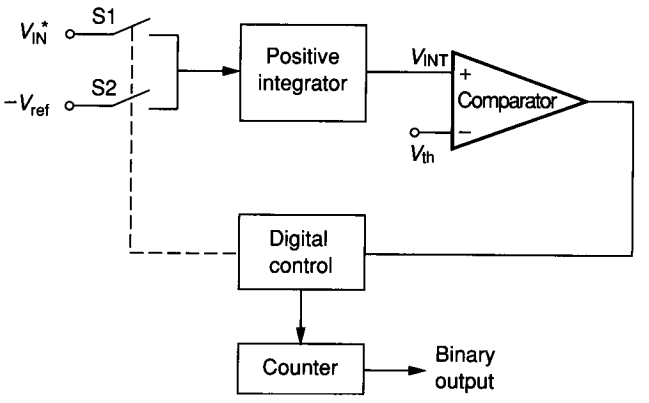


FIGURE 8.3-7
Block diagram of a dual-slope A/D converter.

conversion process on the linearity and accuracy of the ramp generator. Initially, V_{INT} is zero, and the input is sampled and held. In this scheme, it is necessary for V_{IN}^* to be positive. The conversion process begins by resetting the positive integrator until the output of the integrator is equal to the threshold, V_{th}, of the comparator. Next, S1 is closed, and V_{IN}^* is integrated for N_{ref} number of clock cycles. Figure 8.3-8 illustrates the conversion process. It is seen that the slope of the voltage at V_{INT} is proportional to the amplitude of V_{IN}^*. The voltage, $V_{int}(t)$, during this time is given as

$$V_{int}(t) = K \int_0^{N_{ref}T} V_{IN}^* dt + V_{int}(0) = K N_{ref} T V_{IN}^* + V_{th} \qquad (8.3\text{-}3)$$

where T is the clock period. At the end of N_{ref} counts, the carry output of the counter is applied to switch S2 and causes $-V_{ref}$ to be applied to the integrator. Now the integrator integrates negatively with a constant slope because V_{ref} is constant. When $V_{int}(t)$ becomes less than the value of V_{th}, the counter is stopped, and its binary count can be converted into the digital word. This is demonstrated by considering $V_{int}(t)$ during the time designated as t_2 in Fig. 8.3-8. This voltage is given as

$$V_{int}(t) = V_{int}(0) + K \int_0^{N_{out}T} (-V_{ref}) dt \qquad (8.3\text{-}4)$$

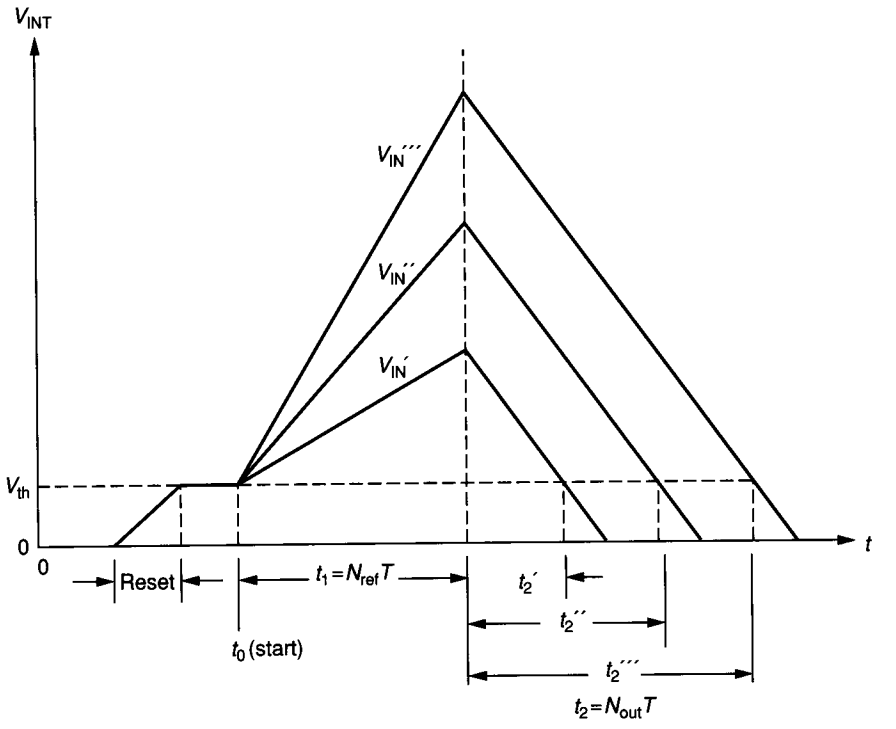


FIGURE 8.3-8
Waveforms illustrative of the dual-slope A/D converter of Fig. 8.3-7.

However, when $t = N_{out}T$, then Eq. 8.3-4 becomes

$$V_{int}(N_{out}T) = (KN_{ref}TV^*_{IN} + V_{th}) - KV_{ref}N_{out}T \tag{8.3-5}$$

Because $V_{int}(N_{out}T) = V_{th}$, then Eq. 8.3-5 can be solved for N_{out}, giving

$$N_{out} = N_{ref}\left(\frac{V^*_{IN}}{V_{ref}}\right) \tag{8.3-6}$$

It is seen that N_{out} will be some fraction of N_{ref}, where that fraction corresponds to the ratio of V^*_{IN} to V_{ref}.

The output of the serial dual-slope D/A converter (N_{out}) is not a function of the threshold of the comparator, the slope of the integrator, or the clock rate. Therefore, it is a very accurate method of conversion. The only disadvantage is that it takes a worst-case time of $2(2^N)T$ for a conversion, where N is the number of bits of the A/D converter. The positive integrator of this scheme can be replaced by a switched capacitor integrator, which will be discussed in Sec. 8.5.

The preceding two examples are representative of the architecture and resulting performance of serial A/D converters. Other forms of serial conversion exist in the literature.[9,10] The serial A/D converter can be expected to be slow but to provide a high resolution. Typical values for serial A/D converters are conversion frequencies of less than 100 Hz and greater than 12 bits of resolution.

8.3.2 Successive Approximation A/D Converters

A second category of A/D converters is called *successive approximation A/D converters*. This class of A/D converters converts an analog input into an N-bit digital word in N clock cycles. Consequently, the conversion time is less than for the serial converters without much increase in the complexity of the circuit. We will examine successive approximation converters that use a combination of voltage-scaling and charge-scaling D/A converters, serial D/A converters, and algorithmic D/A converters.

Figure 8.3-9 illustrates the architecture of a successive approximation A/D converter. This converter consists of a comparator, a D/A converter, and digital control logic. The function of the digital control logic is to determine the value of each bit in a sequential manner based upon the output of the comparator. To illustrate the conversion process, assume that the converter is unipolar (only positive analog signals can be applied). The conversion cycle begins by sampling the analog input signal to be converted. Next, the digital control circuit assumes that the MSB is 1 and all other bits are 0. This digital word is applied to the D/A converter, which generates an analog signal of $0.5V_{ref}$, which is compared to the sampled analog input, V^*_{IN}. If the comparator output is high, then the digital control logic makes the MSB 1. If the comparator output is low, the digital control logic makes the MSB 0. This completes the first step in the approximation sequence. At this point, the value of the MSB is known. The approximation process continues by once more applying a digital word to the D/A converter, with the MSB having its proven value, the second bit guessed at 1, and all

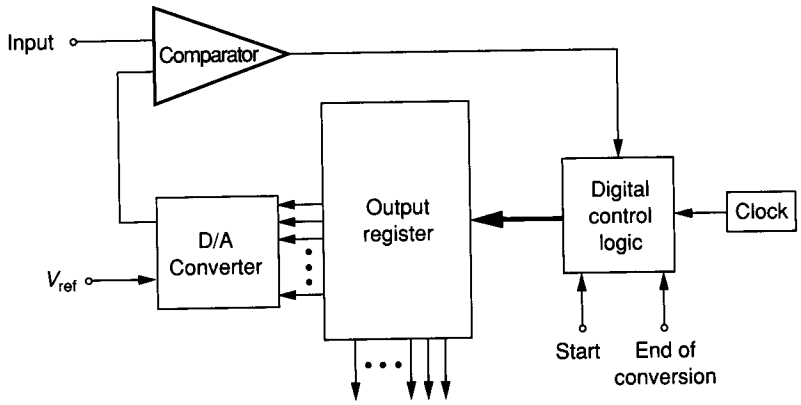


FIGURE 8.3-9
Example of a successive approximation A/D converter architecture.

remaining bits having a value of 0. Again, the sampled input is compared to the output of the D/A converter with this digital word applied. If the output of the comparator is high, the second bit is proven to be 1. If the output of the comparator is low, the second bit is 0. The process continues in this manner until all bits of the digital word have been decided by the successive approximation process.

Figure 8.3-10 shows how the successive approximation sequence works in converting the analog output of the D/A converter to the sampled analog input.

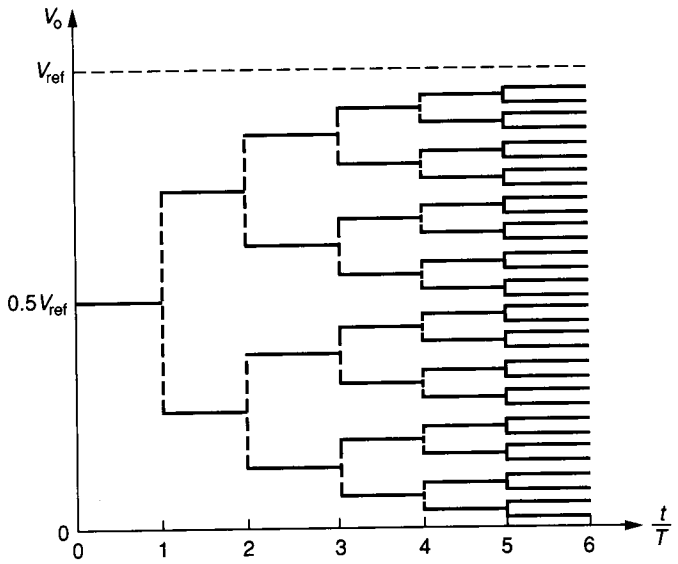


FIGURE 8.3-10
The successive approximation process.

It is seen that the number of cycles required for the conversion to an N-bit word is N. It is also observed that as N becomes large, the requirement of the comparator to distinguish between almost identical signals must increase. Bipolar A/D conversion can be achieved by using a sign bit to choose either $-V_{\text{ref}}$ or V_{ref}.

The digital control logic of Fig. 8.3-9 is often called a *successive approximation register* (SAR). An example of a 5-bit successive approximation A/D converter using a SAR is shown in Fig. 8.3-11. This SAR has the advantage of compatibility with a bit-slice approach, which makes it attractive for integrated circuit implementation. The bit-slice consists of a shift register (SR), an AND gate (G), a SR flip-flops (FF) with direct reset capability, and an analog switch (AS).

Figure 8.3-12 shows an example of a successive approximation A/D converter that uses the voltage-scaling and charge-scaling D/A converter of Fig. 8.2-18. The extra components, in addition to the D/A converter, include a comparator and a SAR. From the concepts of Sec. 6.6, we know that the comparator should have a gain greater than $(V_L 2^{M+K}/V_{\text{ref}})$, where V_L is the minimum output swing of the comparator required by the logic circuit it drives. For example, if $M + K = 12$ and $V_L = V_{\text{ref}}$, then the comparator must have a voltage gain of at least 4096.

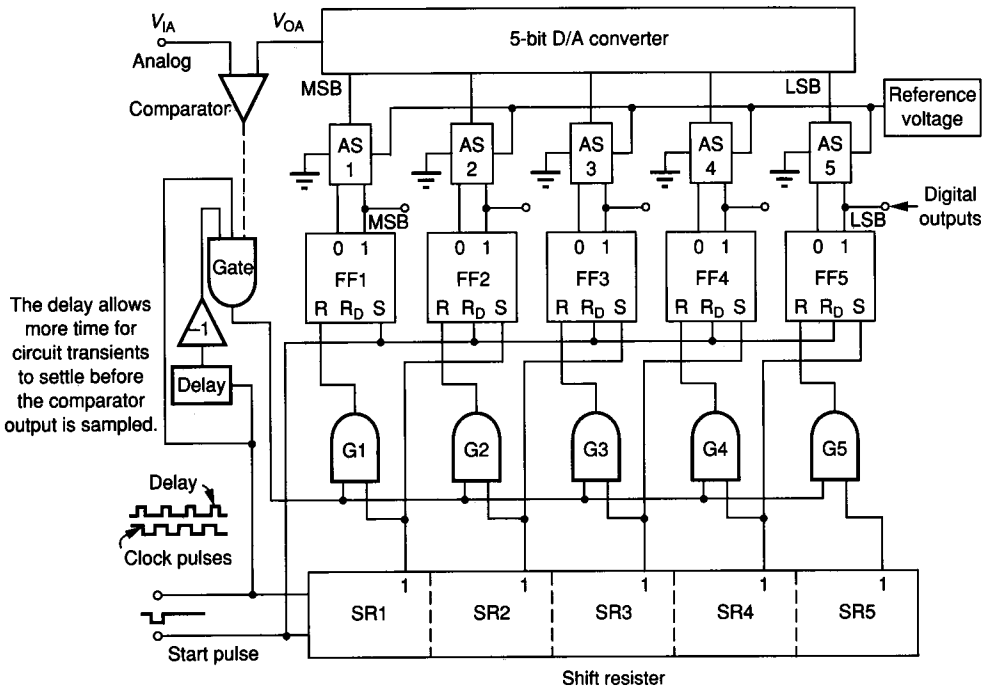


FIGURE 8.3-11
Five-bit successive approximation A/D converter with shift register control.

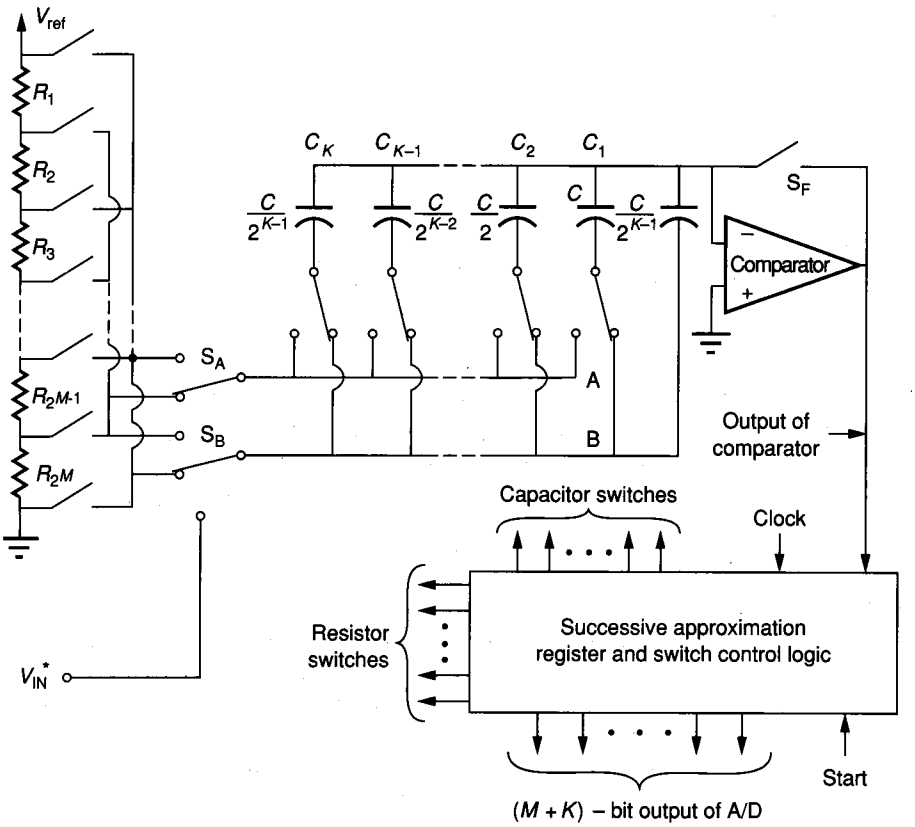


FIGURE 8.3-12
A voltage-scaling, charge-scaling, successive approximation A/D converter.

The conversion operates as follows. With S_F closed, the bottom plates of C_1 through C_K are connected through switch S_B to V_{IN}^*. The voltage stored on the capacitor array at the end of the sampling period is actually V_{IN}^* minus the threshold voltage of the comparator, which removes the threshold as a source of offset error. Because the comparator has unity feedback, it must be compensated in order to remain stable in this step. After switch S_F is opened, a successive approximation search among the resistor string taps is performed to find the segment in which the stored sample lies. Next, buses A and B are switched to the ends of the resistor defining this segment. Finally, the capacitor bottom plates are switched in a successive approximation sequence until the comparator input voltage converges back to the threshold voltage. The sequence of comparator outputs is a digital code corresponding to the unknown analog input signal. The A/D converter in Fig. 8.3-12 is capable of 12-bit monotonic conversion with a differential linearity of less than $\pm\frac{1}{2}$ LSB and a conversion time of 50 ms.[11]

A successive approximation A/D converter using the serial D/A converter of Fig. 8.2-21 is shown in Fig. 8.3-13. This converter works by converting the

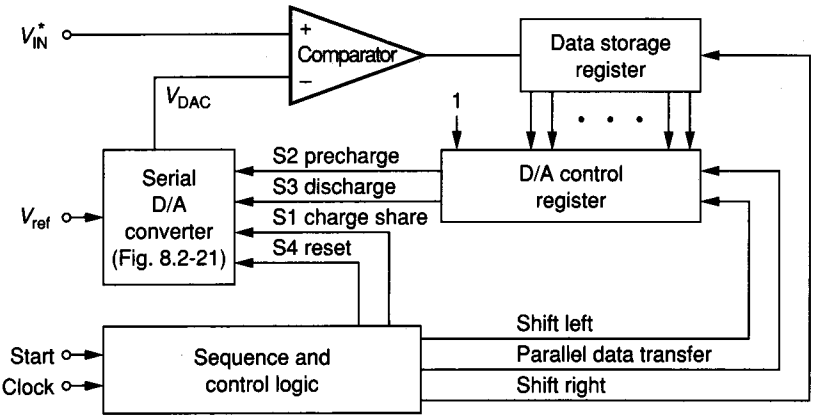


FIGURE 8.3-13
A serial A/D converter using the serial D/A converter of Fig. 8.2-21.

MSB, a_1, first. (The ith bit is denoted as d_i for D/A conversion and ith LSB is denoted as a_i for A/D conversion.) The control logic takes a very simple form because the D/A input string at any given point in the conversion is just the previously encoded word taken LSB first. For example, consider the point during the A/D conversion where the first K MSBs have been decided. To decide the $(K + 1)$th MSB, a $(K + 1)$-bit word is formed in the D/A control register by adding a 1 as the LSB to the K-bit word already encoded in the data storage register. A $(K + 1)$-bit D/A conversion then establishes the value of a_{N-K} by comparison with the unknown voltage V_{IN}^*. The bit is then stored in the data storage register, and the next serial D/A conversion is initiated. The conversion sequence is shown in detail in Table 8.3-1. Altogether, $N(N + 1)$ clock cycles are required for an N-bit A/D converter using the configuration of Fig. 8.3-13.

TABLE 8.3-1
Conversion sequence for the serial D/A converter of Fig. 8.3-13.

D/A conversion number	D/A input word						Comparator output	Number of charging steps
	d_N	d_{N-1}	d_{N-2}	⋯	d_2	d_1		
1	1	—	—		—	—	a_1	2
2	1	a_1	—		—	—	a_2	4
3	1	a_2	a_1		—	—	a_3	6
.	.	.	.		.	.	.	.
.	.	.	.		.	.	.	.
.	.	.	.		.	.	.	.
$N-1$	1	a_{N-2}	a_{N-3}		a_3	a_2	a_{N-1}	$2(N-1)$
N	1	a_{N-1}	a_{N-2}	⋯	a_2	a_1	a_N	$2N$
Total number of charging steps = $N(N + 1)$								

An algorithmic A/D converter patterned after the algorithmic D/A converter of the preceding section is shown in Fig. 8.3-14. This N-bit A/D converter consists of N stages and N comparators for determining the signs of the N outputs. Each stage takes its input, multiplies it by 2, and adds or subtracts the reference voltage depending on the sign of the previous output. The comparator outputs form an N-bit digital representation of the bipolar analog input to the first stage. The operation of the algorithmic A/D converter can be demonstrated by the following example.

Example 8.3-1. Illustration of the operation of the algorithmic A/D converter. Assume that the sampled analog input to a 4-bit algorithmic A/D converter is 1.5 V. If V_{ref} is equal to 5 V, then the conversion proceeds as follows. Since $V_{\text{IN}}^* = 1.5$ V is positive, the output of the comparator of stage 1 is high, which corresponds to a digital 1. Stage 1 then multiplies this value by 2 to get 3 V and subtracts V_{ref}, obtaining an output of -2 V. Stage 2 input sees a negative value, which causes the comparator of this stage to be low, equivalent to a digital 0. Stage 2 then multiplies -2 V by 2 and adds the 5 V reference to output a value of 1 V. Because the output of stage 2 is positive, the comparator of stage 3 is high. The 1 V signal is then multiplied by 2 and 5 V is subtracted, giving a stage 3 output of -3 V. The conversion ends when the comparator of the fourth stage goes low because of the negative input voltage from stage 3.

The digital output word is 1010 for this example. To determine whether this is correct, we use the following formula.

$$V_{\text{ANALOG}} = V_{\text{ref}}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N})$$

where b_i is $+1$ if the ith bit is 1 and -1 if the ith bit is 0. In this example, we see that

$$V_{\text{ANALOG}} = 5\left(\frac{1}{2} - \frac{1}{4} + \frac{1}{8} - \frac{1}{16}\right) = 5(0.3125) = 1.5625$$

It is seen that the value of V_{ANALOG} will eventually converge to the value 1.5.

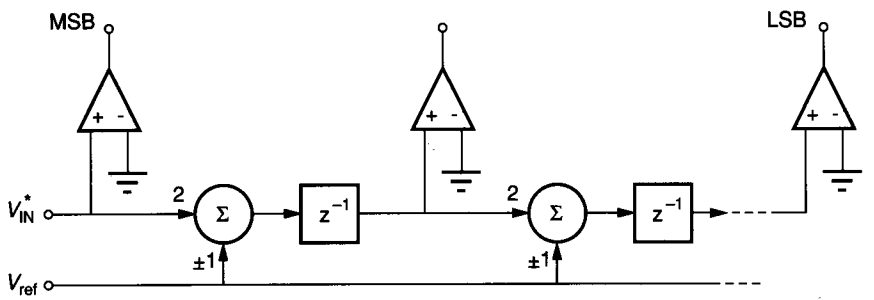


FIGURE 8.3-14
Pipeline implementation of the algorithmic A/D converter.

The algorithmic A/D converter of Fig. 8.3-14 has the disadvantage that the time to convert a sample is N clock cycles, although one complete conversion can be obtained at each clock cycle. The algorithmic A/D converter is considered to be ratio-independent because the performance does not depend on the ratio accuracy of a capacitor or resistor array. The multiplication by 2 of the first stage must be accurate to within 1 LSB, which is a distinct disadvantage of the pipeline configuration of the algorithmic A/D converter.

The iterative reduction of Fig. 8.2-23 resulting in Fig. 8.2-24 can be applied to the A/D converter of Fig. 8.3-14 in a manner similar to what was done for the algorithmic pipeline D/A converter. The analog output of the ith stage can be expressed as

$$V_{Oi} = [2V_{O,i-1} - b_i V_{ref}]z^{-1} \tag{8.3-7}$$

where b_i is $+1$ if the ith bit is 1 and -1 if the ith bit is 0. This equation can be implemented with the circuit in Fig. 8.3-15*a*. The next step is to incorporate the ability to sample the analog input voltage at the start of the conversion. This step is shown in Fig. 8.3-15*b*. In this implementation, $-V_{ref}$ has been

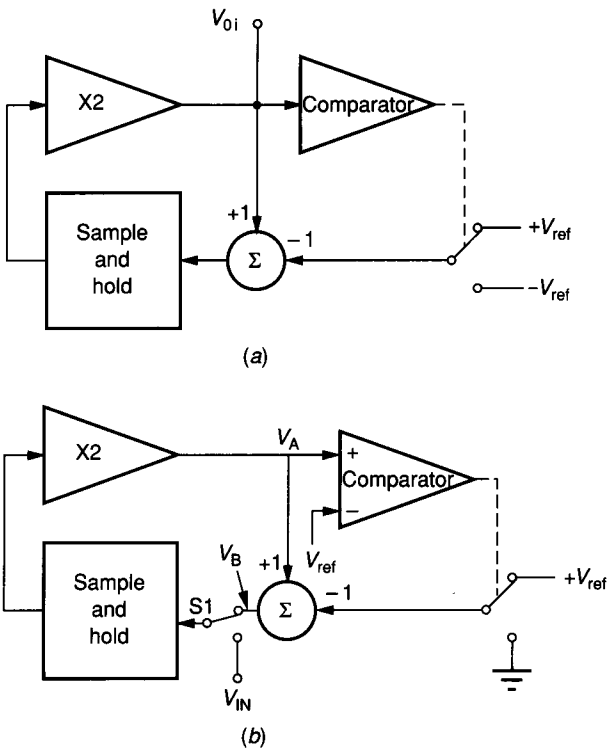


FIGURE 8.3-15
(*a*) Implementation of Eq. 8.3-7, (*b*) Implementation of the iterative algorithmic A/D converter.

replaced with ground for simplicity. The iterative version of the algorithmic A/D converter consists of a sample-and-hold circuit, a gain-of-2 amplifier, a comparator, and a reference subtraction circuit.

The operation of the converter involves first sampling the input signal by connecting switch S1 to V_{IN}. V_{IN}^{*} is then applied to the gain-of-2 amplifier. To extract the digital information from the input signal, the resultant signal, denoted as V_A, is compared to the reference voltage. If V_A is larger than V_{ref}, the corresponding bit is set to 1 and the reference voltage is then subtracted from V_A. If V_A is less than V_{ref}, the corresponding bit is set to 0 and V_A is unchanged. The resultant signal, denoted by V_B, is then transferred by means of switch S1 back into the analog loop for another iteration. This process occurs until the desired number of bits have been obtained, whereupon a new sampled value of the input signal will be processed. The digital word is processed in a serial manner with the MSB first. An example illustrates the process.

Example 8.3-2. Conversion process of an iterative algorithmic A/D converter. The iterative algorithmic A/D converter of Fig. 8.3-15*b* is to be used to convert an analog signal of $0.8V_{ref}$. Figure 8.3-16 shows the waveforms for V_A and V_B during the process. T is the time for one iteration cycle. In the first iteration, the analog input of $0.8V_{ref}$ is applied by switch S1 and results in a value for V_A of $1.6V_{ref}$, which corresponds to a V_B value of $0.6V_{ref}$ and a MSB of 1. During the next iteration, V_B is multiplied by 2 to give a V_A of $1.2V_{ref}$. Thus, the next bit is also 1, and V_B is $0.2V_{ref}$. V_A during the third iteration is $0.4V_{ref}$, resulting in the assignment of 0 for the next bit and a value of $0.4V_{ref}$ for V_B. The fourth iteration gives V_A as $0.8V_{ref}$, which gives $V_B = 0.8V_{ref}$ and the fourth bit as 0. The fifth iteration gives $V_A = 1.6V_{ref}$, $V_B = 0.6V_{ref}$, and the fifth bit as 1. This procedure continues as long as desired. The digital word after the fifth iteration is 11001 and is equivalent to an analog voltage of $0.78125V_{ref}$.

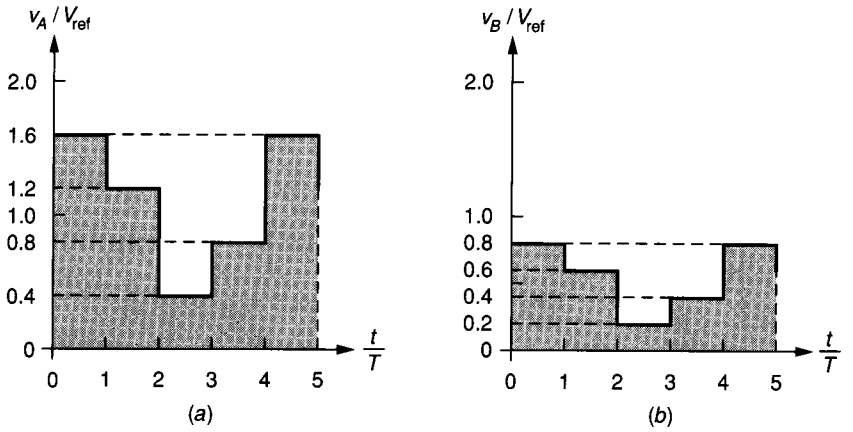


FIGURE 8.3-16
Waveforms for Example 8.3-2 and Fig. 8.3-15*b*: (*a*) V_A, (*b*) V_B.

The iterative algorithmic A/D converter can be constructed from very little precision hardware. Its implementation in a monolithic technology can therefore be area-efficient. A distinct advantage over the pipeline configuration is that all of the gain-of-2 amplifiers are identical because only one is used in an iterative manner. Sources of error for this A/D converter include low operational amplifier gain, finite input offset voltage in the operational amplifier, charge injection from the MOS switches, and capacitance voltage dependence. An integrated 12-bit A/D converter using the approach of Fig. 8.3-15*b* has exhibited an experimental performance having a differential linearity and integral linearity of 0.019% (0.8LSB) and 0.034% (1.5LSB), respectively, for a sample rate of 4 kHz. These values increased to 0.022% (0.9LSB) and 0.081% (3.2LSB) for a sample rate of 8 kHz.

The successive approximation A/D architecture is a very general one, as has been shown. It can make use of any of the D/A converters we have illustrated. If serial D/A converters are used, the conversion time is increased and the area required is decreased. In general, successive approximation A/D converters can have conversion times that fall within the range of 10^4 to 10^5 conversions/second. They are capable of 8 to 12 bits of untrimmed accuracy. The number of bits can be increased if trimming is permitted.

8.3.3 Parallel A/D Converters

In many applications, it is necessary to have a smaller conversion time than is possible with the previously defined A/D converter architectures. This has led to the development of high-speed A/D converters that use parallel techniques to achieve short conversion times. The ultimate conversion speed is one clock cycle, which typically consists of a set-up and a convert phase. Some of the high-speed architectures trade off speed with area and require more than one clock cycle but less than the N clock cycles required for the successive approximation A/D architecture. Another method of improving the speed of the converter is to increase the speed of the individual components. Typically, the comparator sample time, T_{sample} (see Eq. 8.3-1), is the limiting factor for the speed. In this presentation, we shall consider the parallel, the time-interleaved, the two-step, and the ripple approaches to implementing a high-speed A/D converter.

Figure 8.3-1 is a general block diagram of a high-speed A/D converter known as the *parallel* or *flash* A/D converter. An example of how this converter works is illustrated in Fig. 8.3-17. Figure 8.3-17 shows a 3-bit parallel A/D converter. V_{ref} is divided into eight values, as indicated in the figure. Each of these values is applied to the positive terminal of a comparator. The outputs of the comparators are taken to a digital encoding network, which determines the digital output word from the comparator outputs. For example, if V_{IN}^* is $0.6V_{\text{ref}}$, then the top three comparator outputs are 1s and the bottom four are 0s. The digital encoding network would identify 100 as the corresponding digital word. Many versions of this basic concept exist. For example, the voltage at the taps may be in multiples of $V_{\text{ref}}/16$ with $V_{\text{ref}}/8$ voltage differences between the taps. Also, the resistor string can be connected between $+V_{\text{ref}}$ and $-V_{\text{ref}}$ to achieve bipolar conversion (positive and negative analog output voltages).

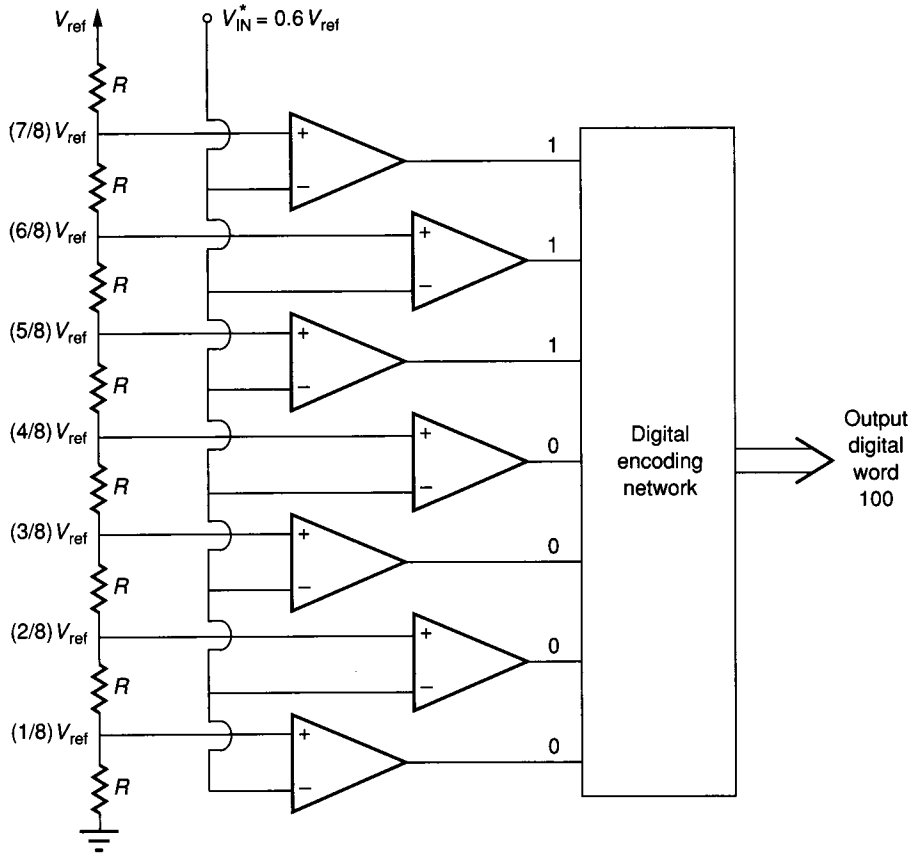


FIGURE 8.3-17
A 3-bit parallel A/D converter.

The parallel A/D converter of Fig. 8.3-17 converts the analog signal to a digital word in one clock cycle, which has two phase periods. During the first phase period, the analog input voltage is sampled and applied to the comparator inputs. During the second phase period, the digital encoding network determines the correct output digital word and stores it in a register/buffer. Thus, the conversion is limited by how fast this sequence of events can occur. Typical clock frequencies can be as high as 20 MHz for CMOS and 100 MHz for BJT technologies. This gives a theoretical conversion time of 50 ns and 10 ns, respectively. The sample-and-hold time may be larger than these values and could prevent these conversion times from being realized. Another problem is that as N increases, the number of comparators required is $2^N - 1$. For N greater than 8, too much area is required. Other methods we shall discuss give almost the same conversion times with much more efficient utilization of chip area.

One method of achieving small system conversion times is to use slower A/D converters in parallel, which is called *time-interleaving* and is shown in Fig.

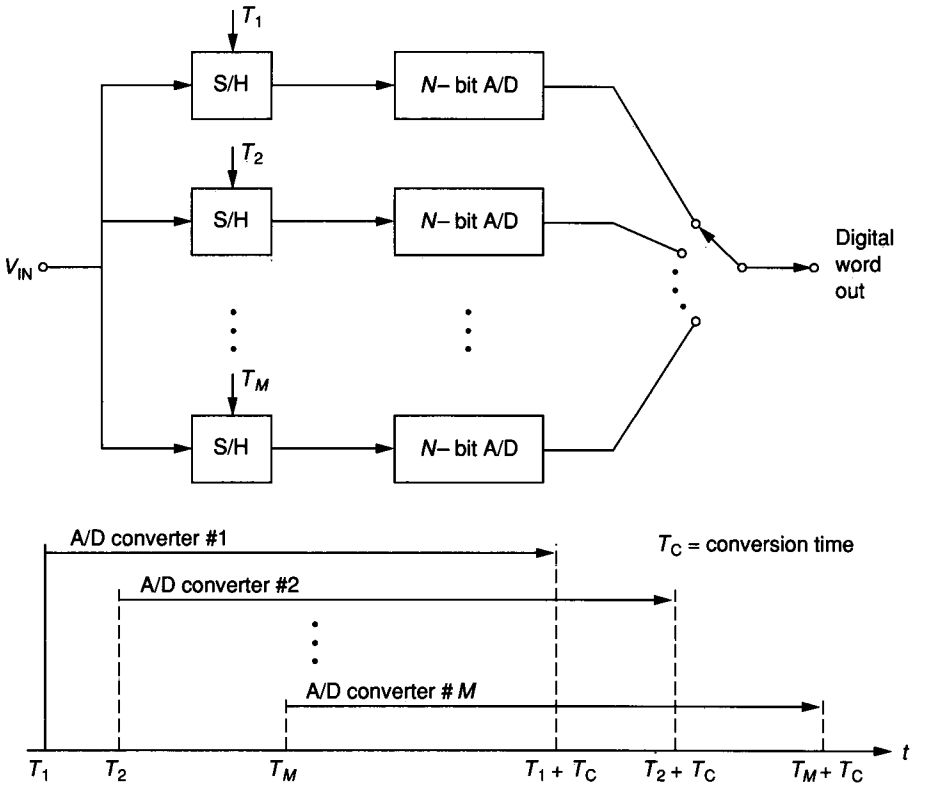


FIGURE 8.3-18
A time-interleaved A/D converter array.

8.3-18. Here M successive approximation A/D converters are used in parallel to complete the N-bit conversion of one analog signal per clock cycle. The sample-and-hold circuits consecutively sample and apply the input analog signal to their respective A/D converters. N clock cycles later, the A/D converter provides a digital word output. If $M = N$, then a digital word is output at every cycle. If one examines the chip area for an N bit A/D converter using the parallel A/D converter architecture ($M = 1$) compared with the time-interleaved architecture for M = N, the minimum area will occur for a value of M between 1 and N.

Combining the parallel approach with a series approach results in an A/D converter architecture with high speed and reasonable area. This approach is often called a pipeline A/D converter, particularly if the number of series stages is greater than two. Figure 8.3-19 shows a $2M$-bit A/D converter using two M-bit parallel A/D converters. The method first converts the M MSBs and then converts the M LSBs. Consequently, only $2^{M+1} - 2$ comparators are required to convert a $2M$-bit digital word. For the configuration of Fig. 8.3-19, the analog input is applied to the left-hand string of $2^M - 1$ comparators during the first clock phase, and the M MSBs are encoded during the second clock phase. During the

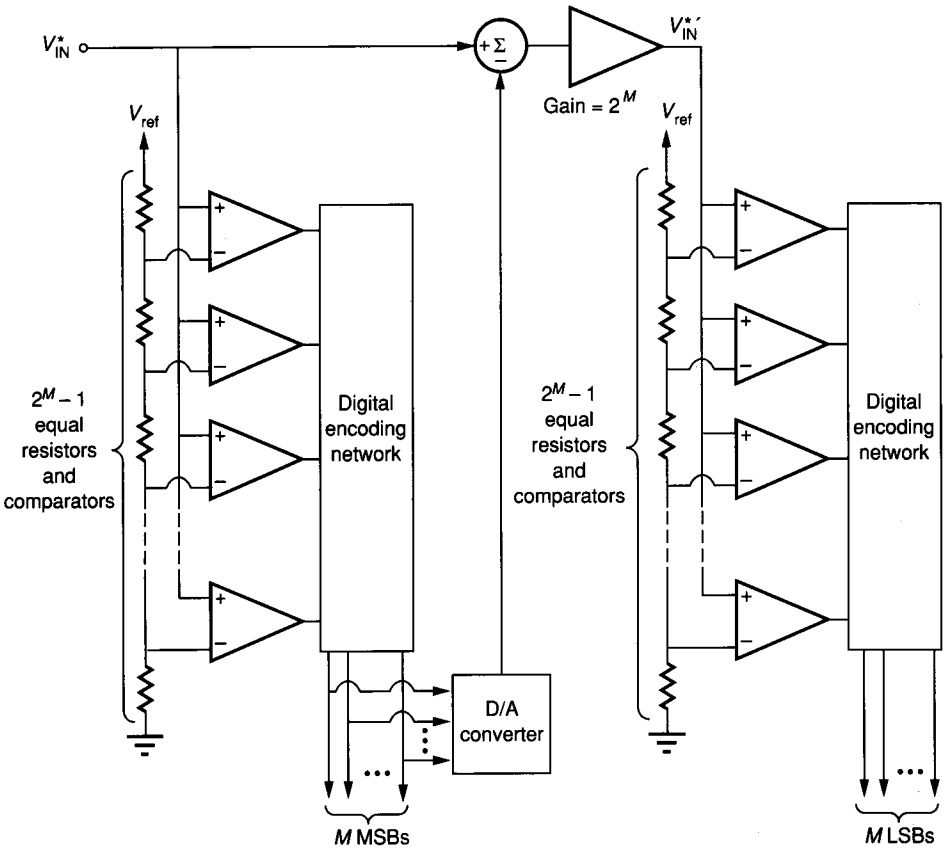


FIGURE 8.3-19
A $2M$-bit parallel-series A/D converter configuration.

third clock phase, the M MSBs are converted to an analog equivalent, which is subtracted from V_{ref}, multiplied by a gain of 2^M, and applied to the right-hand string of $2^M - 1$ comparators. Finally, during the fourth clock phase, the M LSBs are encoded. Thus, if the clock has two phases, then in two clock cycles a $2M$-bit digital word will be converted.

It is possible to make this conversion in three phases if necessary because the second and third phases can be combined into a single phase. Figure 8.3-20 shows the microphotograph of a parallel-series 8-bit A/D converter using the architecture of Fig. 8.3-19 implemented with MOS technology. The conversion time for this converter is in the range of 2 μs and is limited by the sampling time of the comparators and the settling times for the logic encoding network.

Up to this point analog-to-digital conversion techniques compatible with BJT and CMOS technology have been presented. The major categories include serial, successive approximation, and parallel A/D converters and are compared in Table 8.3-2 along with high performance A/D converters discussed next.

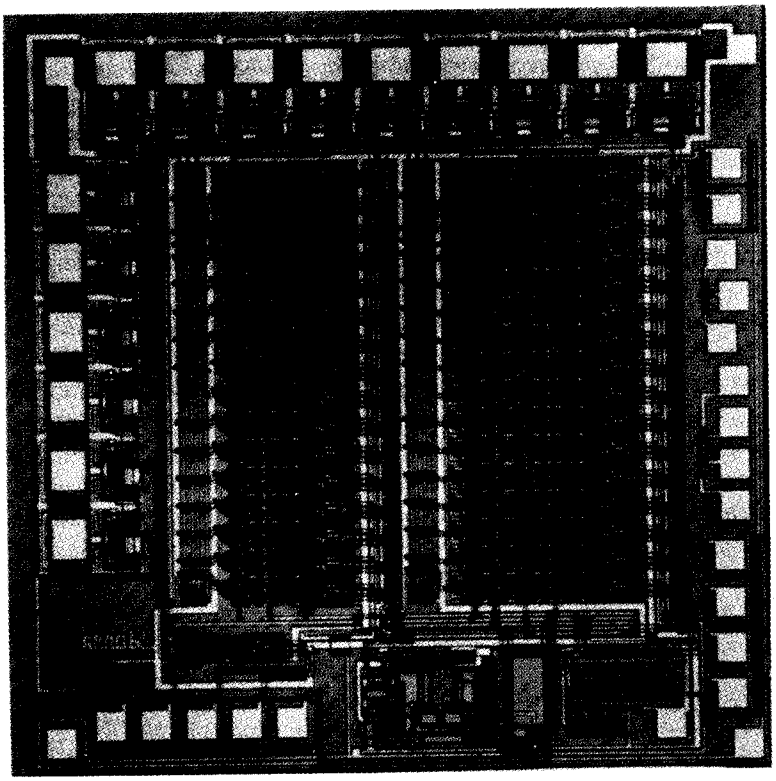


FIGURE 8.3-20
Microphotograph of the implementation of Fig. 8.3-19 for $M = 4$.

TABLE 8.3-2
Comparison of the performance of the various types of A/D converters

A/D converter type	Performance characteristics
Serial	1–100 conversions/second; 12–14-bit accuracy; requires no element-matching; a stable reference voltage is necessary
Successive approximation	10,000–100,000 conversions/second; 8–10 bits of untrimmed accuracy; 12–14 bits monotonicity; 12–14 bits trimmed accuracy
Parallel	$10^6 - 2 \times 10^7$ conversions/second; 7–8 bits of accuracy; requires large area
High performance	8000–10^6 conversion/second; 12–18 bits of accuracy

8.3.4 High-Performance A/D Converters

Recent advances in A/D converters have resulted in converters with significant improvement in performance over those considered in the previous categories. The performance improvement is typically in the areas of resolution or speed. Converters whose resolution is approaching 18 bits or sample rates of several hundred megasamples per second are now feasible. This discussion will examine three A/D converters that offer improved performance. These A/D converters include selfcalibrating A/D converters, pipeline A/D converters, and oversampled A/D converters.

A self-calibrating A/D converter is one that includes a calibration cycle to adjust its transfer characteristic to approach the ideal transfer characteristic. A block diagram of a self-calibrating A/D converter using the basic architecture of Fig. 8.3-12 is shown in Fig. 8.3-21. This circuit consists of an N-bit charge-scaling array called the main D/A converter, an M-bit voltage scaling array called the sub–D/A converter, and a voltage-scaling array called a calibration D/A converter. The calibration D/A converter must have several more bits of resolution than the sub–D/A converter. Digital control circuits govern capacitor switching during the

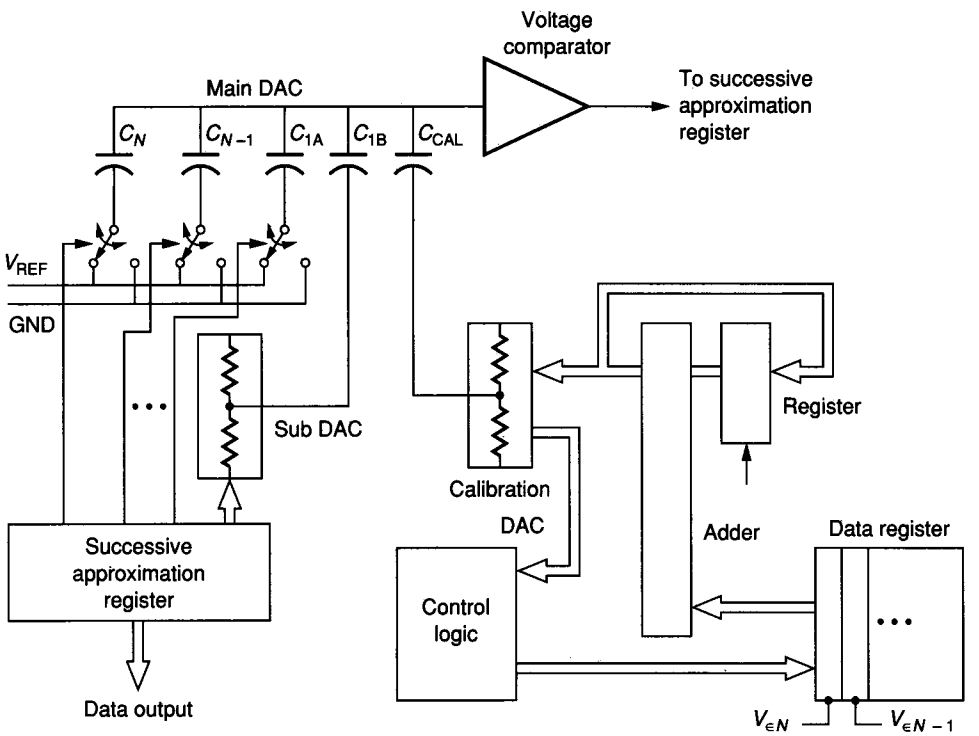


FIGURE 8.3-21
Block diagram of a self-calibrating A/D converter.

calibration cycle and store the nonlinearity correction terms in data registers. The ratio errors of the sub–D/A converter and overall quantization errors accumulate during digital computation of error voltages. To overcome these errors, at least one bit of additional resolution is needed during the calibration cycle. This extra bit is used to achieve final linearity within 1 LSB of an ideal straight line or within 0.5 LSB of an ideal staircase converter response. In practice, two extra bits are used in order to have a margin of safety. Typical performance of a self-calibrating A/D converter is 15–16 bits of resolution, an offset error of less than 1 LSB, a dynamic range of over 90 dB, a nonlinearity of less than 0.25 LSB, and a conversion time of less than 50 μs.

A pipeline converter is different from the A/D converter of Fig. 8.3-19 in that more stages are used with fewer bits per stage. This allows the designer to make tradeoffs between area and conversion time. A typical pipeline converter might have four stages with 3–4 bits per stage. A 2-bit implementation of a pipeline stage is shown in Fig. 8.3-22*a*. The input is sampled and held and applied to the comparators C_0 through C_2, where the 2-bit digital output is encoded. The digital output controls the switches on the resistor string to obtain an analog output equivalent to the 2-bit digital word. This analog voltage is subtracted from the original input and multiplied by 4, which results in the residue voltage passed on to the next stage. Figure 8.3-22*b* shows the plot of the amplified residue voltage versus the analog input voltage of the A/D converter of Fig. 8.3-22*a*.

The errors that can occur in the pipeline converter are shown in Table 8.3-3 along with their effects and possible solutions. Auto-zeroing, trimming, and calibration have been discussed previously. Digital error correcting techniques solve the problem of where one stage makes a conversion that the following stage cannot resolve. For example, consider two 2-bit cascaded stages forming a 4-bit pipeline converter. Assume that $V_{\text{in}}^* = (3/8)V_{\text{ref}}$, which corresponds to a digital output code of $D = 0110$. Because $(3/8)V_{\text{ref}}$ is greater than $(2/8)V_{\text{ref}}$, the first stage gives a digital output of $D_1 = 01$. Converting D_1 to an analog voltage gives $(4/8)V_{\text{ref}}$, which is subtracted from $(3/8)V_{\text{ref}}$ to give $-(1/8)V_{\text{ref}}$. Multiplying by 4 gives an amplified residue of $-(4/8)V_{\text{ref}}$ applied to the second stage. The second stage will output a digital code of $D_2 = 00$. When D_1 and D_2 are combined, the digital output code is 1000, which is in error. This error could be removed by increasing the number of bits by one at the second stage and using this extra bit to achieve the proper output. Unfortunately, the extra bit does not extend the resolution of the A/D converter. An alternative correction technique is to introduce an intentional offset to all the comparators so that the direction of the A/D decision error is always known. For example, if the intentional offsets are negative when the A/D subconverter makes its decision, then the residue voltage is always negative. The sign of the residue can be used to temporarily correct (decrement) the digital output code without using an extra bit.

One of the sources of nonlinearity in the pipeline A/D converter is the reference scaling nonlinearity and is illustrated in Fig. 8.3-23. When the peak

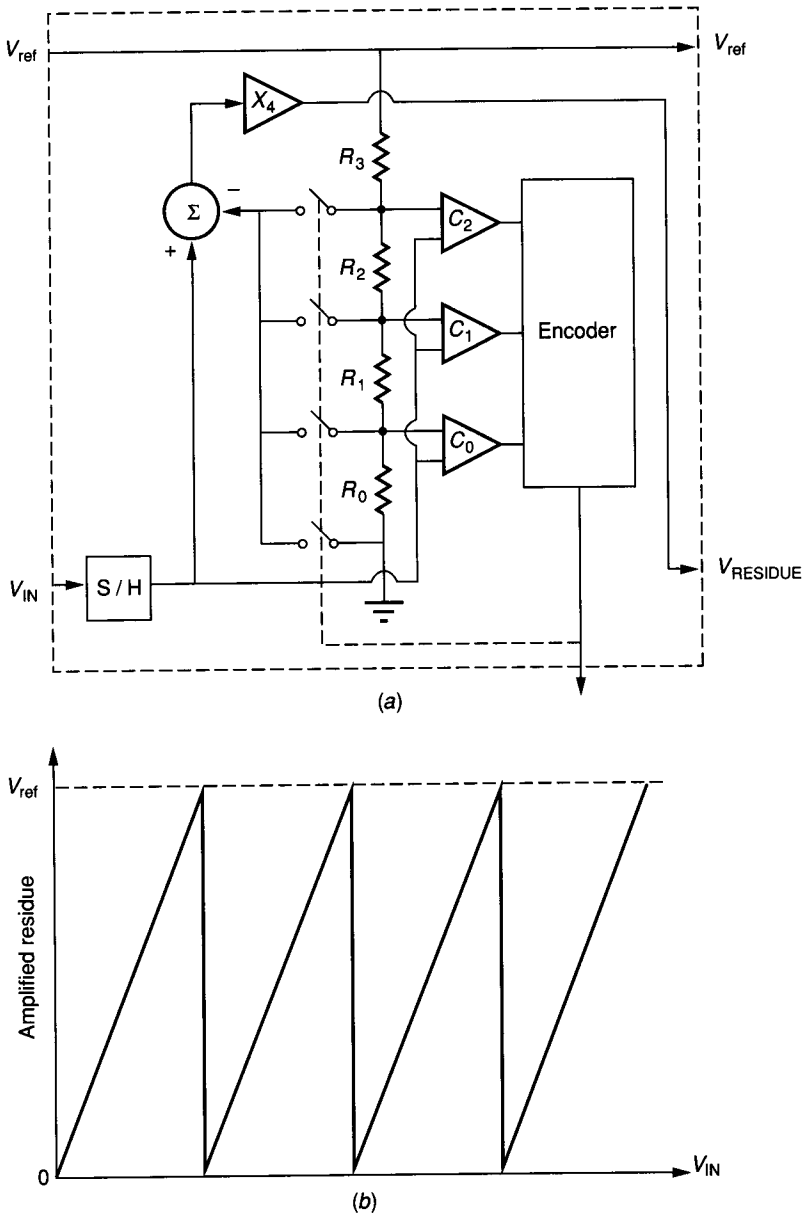


FIGURE 8.3-22
(*a*) Two-bit implementation of a pipeline stage, (*b*) Ideal plot of the amplifier residue versus the analog input.

TABLE 8.3-3
Static error analysis for a pipeline A/D converter

Element	Error(s)	Effect(s)	Solution(s)
S/H	Offset	Offset	Auto-zeroing
		Nonlinearity	Digital error correction
A/D converter	Offset	Offset	Auto-zeroing
		Nonlinearity	Digital error correction
	Nonlinearity	Nonlinearity	Digital error correction
D/A converter	Nonlinearity	Nonlinearity	Trim/calibrate
Interstage amplifier	Offset	Nonlinearity	Auto-zeroing
	Gain error	Nonlinearity	Trim/calibrate

of the amplified residual voltage is not equal to V_{ref}, plus and minus differential nonlinearity errors will be produced. For converters up to 10 bits, these errors can be sufficiently reduced by adjusting the residue so that it is always equal to the reference. Feedforward reference correction techniques have been used to extend this error minimization approach to 13 bits.[12]

Pipeline A/D converters offer a flexible approach to achieving high performance. A subranging technique has been used to further enhance the per-

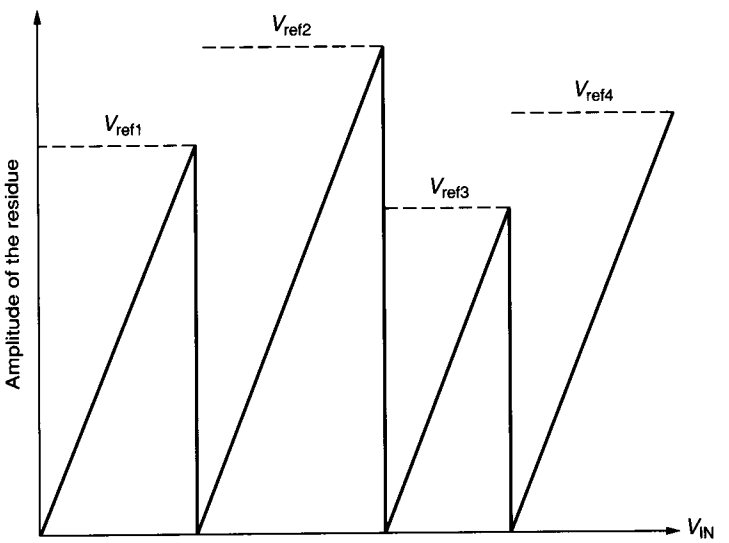


FIGURE 8.3-23
Illustration of feedforward reference correction.

formance of the pipeline A/D converter.[13] In the subranging A/D converter, the conversion is done in several cycles. In each successive cycle, the gain of the residue amplifier is increased until the full scale of the amplified residue voltage is reached. In this manner, errors can be corrected and removed on each successive cycle.

The performance of the pipeline A/D converters depends on the technology used. CMOS converters typically have 13–14 bits of resolution, 5–10 μs conversion times, and 10–30 mW of power dissipation. Bipolar pipeline converters typically have 10 bits of resolution, 200 ns conversion times, and 100–500 mW of power dissipation. The summary of this section will compare these converters with others, including those using BiCMOS technology.

Oversampled A/D converters offer a means of exchanging resolution in time for resolution in amplitude in order to circumvent the need for complex precision analog circuits. A basic oversampled A/D converter architecture is shown in Fig. 8.3-24. This architecture includes a clocked feedback loop, which produces a coarse estimate that oscillates about the true value of the input, and a digital filter, which averages this coarse estimate to obtain a finer approximation. This approximation is accurate to more bits at a lower (decimated) sampling rate. Although trading resolution in time for resolution in amplitude is a simple concept, the key to usefulness of oversampling systems based on the architecture of Fig. 8.3-24 is that the amplitude resolution is enhanced faster than the time resolution is reduced.

The feedback loop with the integrating filter $H(z)$ in Fig. 8.3-24 forces the quantization error in the N-bit estimate to have a high-frequency spectrum. When the low-pass digital filter subsequently reduces the bandwidth of the spectrum, it excludes a more-than-linear proportion of the quantization noise. Typical theoretical signal-to-noise ratio enhancement from the initial N-bit estimate is

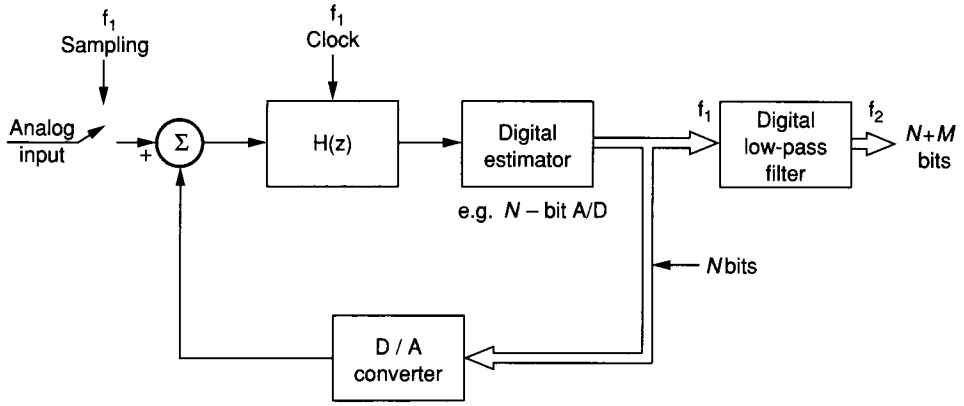


FIGURE 8.3-24
A basic oversampled A/D converter block diagram; $H(z)$ is an integrating filter.

$$\Delta S/N = 9L - 5.2 \text{ dB} \tag{8.3-8}$$

where L is the number of octaves of oversampling when $H(z)$ is first-order. If $H(z)$ is second-order, then the estimate is

$$\Delta S/N = 15L - 13 \text{ dB} \tag{8.3-9}$$

If we assume an oversampling factor of 128, the S/N enhancements for a first-order and second-order oversampling converter are 57.8 dB and 92 dB, respectively.

Of special interest is the case where $N = 1$. In this case, the coarse estimate and the D/A converter have a 1-bit resolution. When $N = 1$, the circuit of Fig. 8.2-24 is called a *delta-sigma modulator*. One advantage of delta-sigma A/D, oversampling converters is that because they obtain resolution by linearly interpolating between two states, they do not require an array of precision binary scaling elements for the D/A converter. This means that nonlinearity errors will not exist. Figure 8.3-25 shows a practical delta-sigma oversampling A/D converter with both one and two integrators in the loop [$H(z)$ first- and second-order].

The output of the delta-sigma modulator is applied to a low-pass digital filter whose function is to operate on the 1-bit signal to remove frequencies and quantization noise above the desired signal bandwidth. The output of the filter is a multibit digital representation at a lower (decimated) sampling rate. Basic delta-sigma modulator systems generate severe noise components for certain input values. In order to remove this noise, a square wave dither frequency within the stopband of the decimating filter randomizes the delta-sigma noise. The square wave dither frequency does not appear at the output of the filter or prevent arbitrary dc inputs from being passed through the filter.

The output of the delta-sigma modulator can be downsampled by a finite-impulse response digital low-pass filter. One possible architecture of the digital

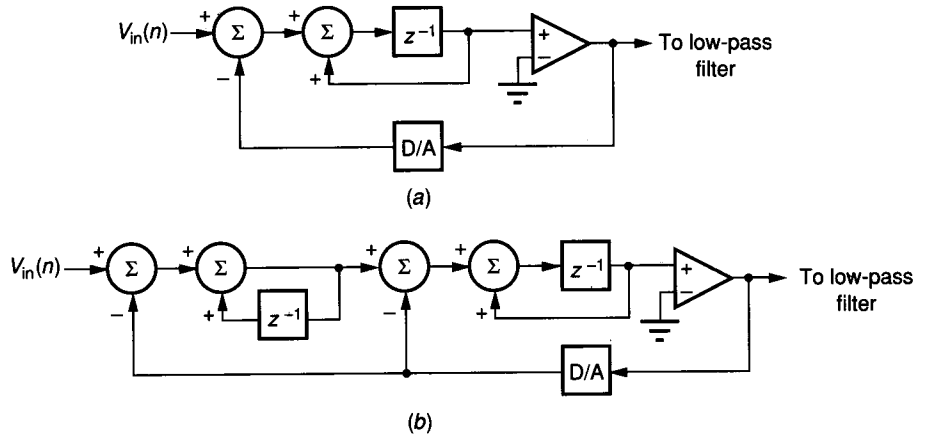


FIGURE 8.3-25
Typical delta-sigma modulators using (*a*) one and (*b*) two integrators in z-domain notation.

filter is shown in Fig. 8.3-26. This architecture uses a 256:1 decimation factor and a 1-bit digital input signal. A 1024-point impulse response, of which the symmetric half is stored in a read-only memory, is distributed to four accumulators. No explicit multiplications are necessary because of the 1-bit input signal. The impulse-response coefficients were designed to satisfy the dual objectives of quantization-noise removal and anti-alias filtering. Because the finite-impulse response low-pass filters are relatively insensitive to coefficient roundoff, 6-bit coefficients are adequate to define the impulse response.

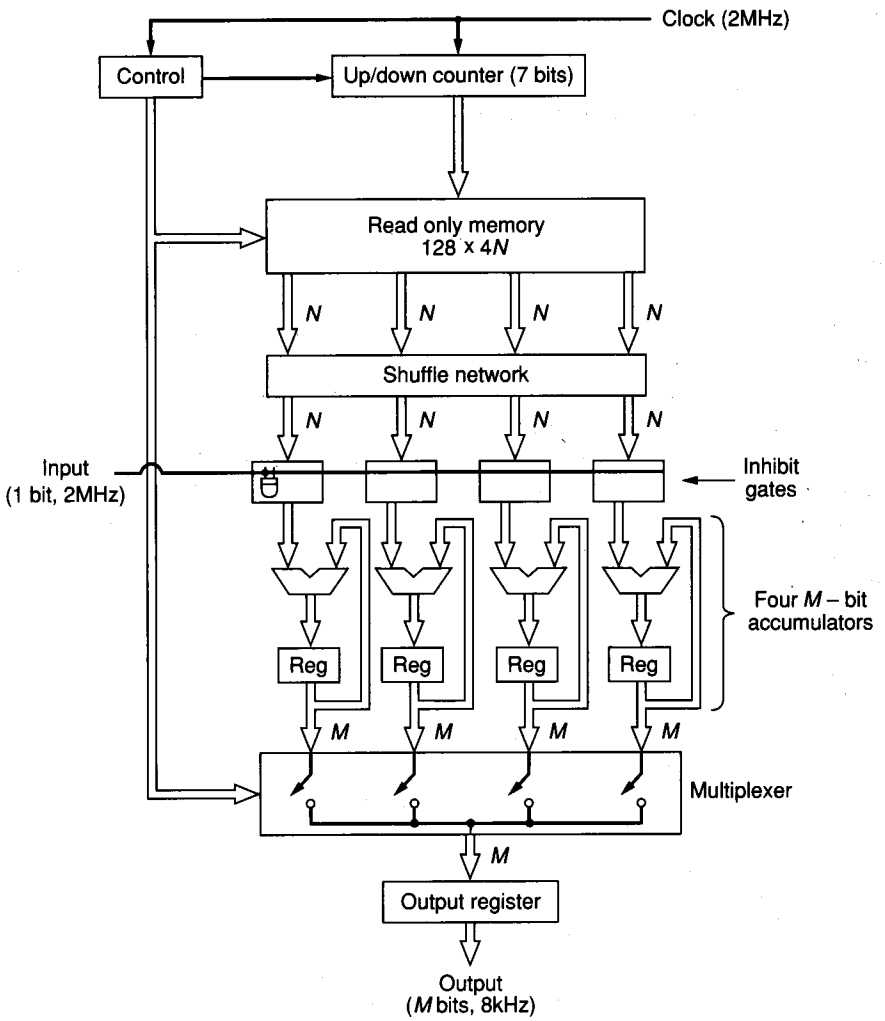


FIGURE 8.3-26
Architecture of a 1024-point finite-impulse response low-pass digital filter with values of $N = 6$ and $M = 15$.

Typical performance for a CMOS delta-sigma oversampled A/D converter is 14–16 bits at a sampling rate of 1–20 kHz, and a power dissipation of 10–30 mW. Dynamic ranges of up to 96 dB are possible, with noise being the limiting factor. The oversampling A/D converter is very suitable to applications such as digital audio.

8.3.5 Summary

A/D conversion techniques compatible with bipolar and CMOS technologies have been presented in this section. The major categories included serial, successive approximation, and parallel A/D converters. Table 8.3-2 provides a summary of these A/D converters. High-performance A/D converters offer improved accuracy (resolution) or speed (conversion time). Examples of high-performance A/D converters include self-calibration methods, pipeline converters with error correcting methods, and delta-sigma oversampled A/D converters. Some of the high-speed A/D converters are beginning to offer capabilities in the video range of frequencies.

The performance of A/D converters is steadily increasing with improvements in technology. Figure 8.3-27 shows the performance of monolithic A/D converters as of 1988.[14] This graph plots converter sampling rate on the horizontal axis and

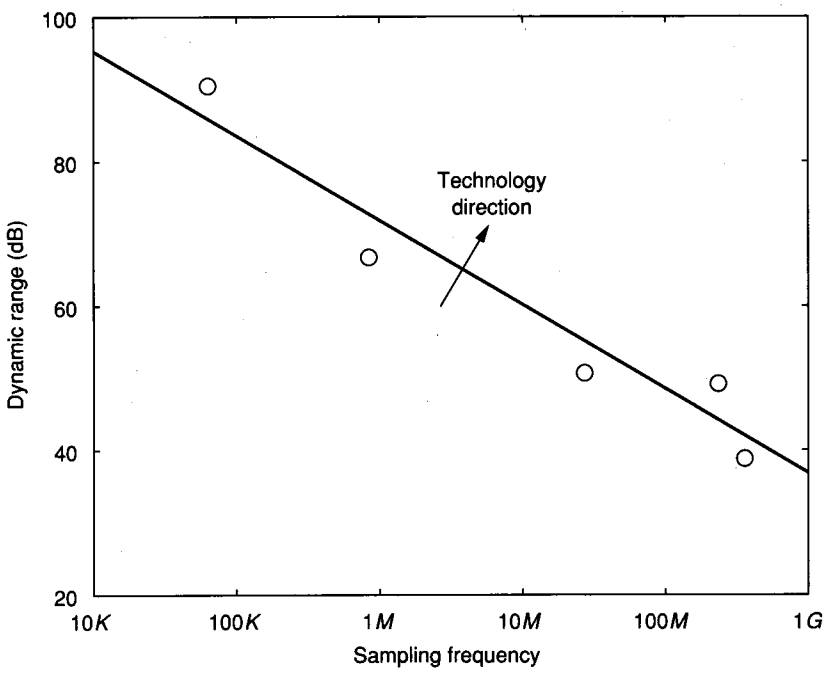


FIGURE 8.3-27
1988 monolithic A/D converter performance in terms of dynamic range versus sampling frequency.

converter dynamic range (signal-to-noise plus distortion) on the vertical axis. Each point on the graph represents the performance of the best monolithic converters. These points fall close to the line drawn on the figure. If such a figure were drawn for each year back to the mid-1970s when monolithic A/D converters first appeared, the movement of the line would be just over 2 dB per year in the vertical direction. The slope of the line is -0.6, supporting the conjecture that it is more difficult to be accurate than fast.

Flash or parallel architectures dominate at and below the 60 dB level. Self-calibrated, successive approximation architectures dominate above the 60 dB line. Self-calibrated delta-sigma oversampled A/D converters will probably provide increasing dynamic ranges.

Figure 8.3-28 is similar to Fig. 8.3-27 except that the various types of converters and types of technology are identified.[15–25] This graph shows how combined technologies such as BiMOS can be used to achieve performance beyond that obtainable with single technologies.

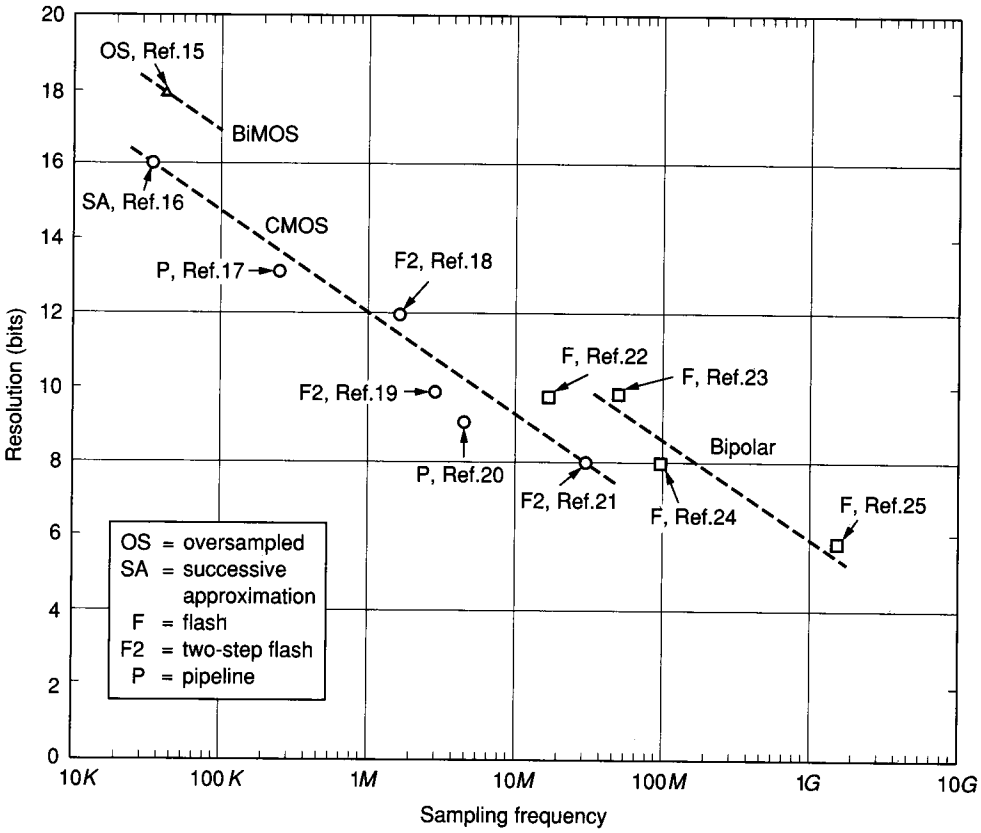


FIGURE 8.3-28
Comparison of high-performance, monolithic A/D converters in terms of resolution versus sampling frequency. Circles, squares, and triangles are CMOS, bipolar, and BiMOS technologies, respectively. The architecture and reference is indicated in the figure (Courtesy of J. P. Hwang).

8.4 CONTINUOUS-TIME FILTERS

One of the largest applications of analog signal processing circuits is in the area of frequency-domain filters. However, until the recent development of switched capacitor circuit techniques,[26] integrated circuit technology was not practical for the implementation of analog filters. The primary reasons were that RC time constants could not be defined with the accuracy necessary for filters and the area requirements for audio filters were unacceptably large. With switched capacitor circuit techniques, the time constants are proportional to capacitor ratios. In integrated circuit technology, it is possible to achieve capacitor ratios sufficiently accurate for filter requirements. In order to design switched capacitor filters, it is necessary to understand the design of continuous-time filters. The objective of this section is to prepare the reader for the following section, which concerns switched capacitor filter design.

For simplicity, we will initially consider linear filters that are classified into four different groups according to the type of gain characteristic. We will assume that the desired gain of the filter is unity in the *passband*, where frequencies are transmitted, and zero in the *stopband*, where frequencies are rejected. Furthermore, we shall assume that under ideal conditions, the passband and stopband are adjacent to each other and that ω_T is the frequency where the transition is made from one band to the other.

The magnitudes of the frequency-dependent gain of the four types of filters that will be considered are shown in Fig. 8.4-1. Figure 8.4-1*a* shows the frequency response of a *low-pass filter*, which has the ideal magnitude response of

$$|H_{LP}(j\omega)| = \begin{cases} 1 & 0 \leq \omega \leq \omega_T \\ 0 & \omega_T < \omega < \infty \end{cases} \tag{8.4-1}$$

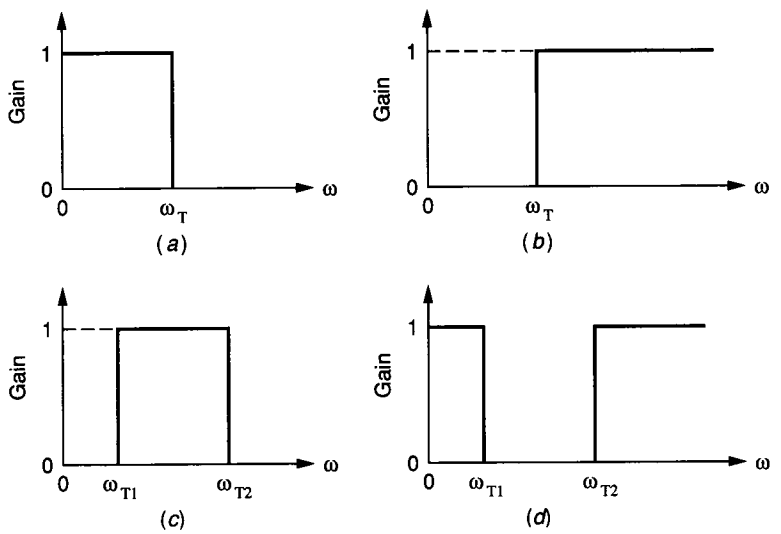


FIGURE 8.4-1
Types of filters: (*a*) Low-pass, (*b*) High-pass, (*c*) Bandpass, (*d*) Band-elimination.

Figure 8.4-1*b* illustrates the magnitude frequency response of a *high-pass filter*, described mathematically as

$$|H_{HP}(j\omega)| = \begin{cases} 0 & 0 \le \omega < \omega_T \\ 1 & \omega_T \le \omega < \infty \end{cases} \tag{8.4-2}$$

The magnitude frequency response of a *bandpass filter* is shown in Fig. 8.4-1*c*. The ideal frequency response of this type of filter is

$$|H_{BP}(j\omega)| = \begin{cases} 0 & 0 \le \omega < \omega_{T1} \\ 1 & \omega_{T1} \le \omega \le \omega_{T2} \\ 0 & \omega_{T2} < \omega < \infty \end{cases} \tag{8.4-3}$$

Finally, the frequency response of a *band-elimination filter* is shown in Fig. 8.4-1*d*. The ideal magnitude frequency response of this filter is given mathematically by

$$|H_{BE}(j\omega)| = \begin{cases} 1 & 0 \le \omega < \omega_{T1} \\ 0 & \omega_{T1} \le \omega \le \omega_{T2} \\ 1 & \omega_{T2} < \omega < \infty \end{cases} \tag{8.4-4}$$

The phase shift of each of the filters of Fig. 8.4-1 can be expressed as

$$\text{Arg } H(j\omega) = -\omega T_d, \qquad 0 \le \omega \le \infty \tag{8.4-5}$$

where T_d is the time delay of the filter. Because T_d is equal to the negative of the derivative of the phase shift, Eq. 8.4-5 defines a system that has a constant time delay of T_d seconds for each frequency transmitted through the filter.

In practice, the ideal filter characteristics of Fig. 8.4-1 cannot be realized. It is not possible to have discontinuous changes in transmission as a function of frequency or to have zero transmission over a region or band of frequencies. Consequently, we can only approximate these ideal filter characteristics. Let us consider how we can modify the ideal filter specifications of Fig. 8.4-1 so that they can be realized in practice. Our efforts will be focused on the low-pass filter. The resulting considerations can be easily extended to the other three types of filters.

8.4.1 Low-Pass Filters

Consider the low-pass filter frequency response of Fig. 8.4-2. The frequency range has been divided into three parts. From zero to the passband frequency, ω_{PB}, the gain must be between G_{PB} and unity. From the stopband frequency, ω_{SB}, to infinity, the gain must be between G_{SB} and zero. The frequency range between ω_{PB} and ω_{SB} is called the *transition region*. The gain of the filter is unspecified in this region, although a good approximation would be expected to follow closely a straight line drawn from point A to point B. Another way of interpreting Fig. 8.4-2 is to say that the filter response must fall in the shaded regions. The reasons for the transition region and a nonzero value of G_{SB} are clear from the concepts of circuit theory. However, it may not be clear why G_{PB} cannot be unity. The answer is that there is a tradeoff between how close G_{PB} is to unity and the width of the transition region. We shall see that permitting G_{PB} to be less than unity allows the value of ω_{SB}/ω_{PB} to approach unity and, thus, a smaller transition region.

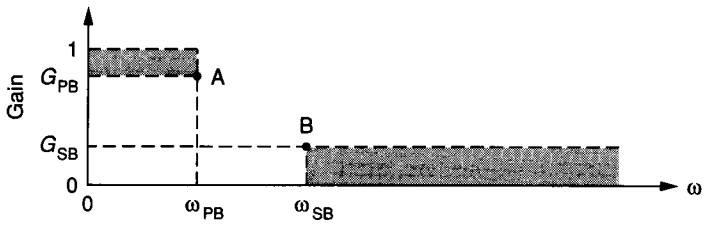


FIGURE 8.4-2
Practical specifications for a low-pass filter.

All transfer functions of active and/or passive filters with a finite number of lumped components are rational functions in s. With this observation, the filter design problem is generally partitioned into two parts: approximation and synthesis. In the approximation problem, a rational function (with real coefficients), often termed an approximating function, is derived to meet the filter requirements. The synthesis problem concerns the design of a circuit that has the approximating function as its transfer function.

There are several types of filter approximation functions that satisfy the requirements of Fig. 8.4-2. These filter types can all be expressed by the rational polynomial transfer function given as

$$H(s) = \frac{b_0 + b_1 s + b_2 s^2 + \cdots + b_{n-1} s^{n-1} + b_n s^n}{a_0 + a_1 s + a_2 s^2 + \cdots + a_{n-1} s^{n-1} + a_n s^n} \qquad (8.4\text{-}6)$$

The order of this transfer function is n. The types of filter approximations are generally classified by some aspect of their frequency response. For example, the *Butterworth filter approximation* has a magnitude response that is maximally flat in the passband and monotonically decreasing in the transition and passband regions. For the Butterworth low-pass filter approximation, $b_0 = 1$ and $b_i = 0$ for all $i \geq 1$ in Eq. 8.4-6. An example of some Butterworth filter approximations for various values of n is given in Fig. 8.4-3. It is customary to normalize the passband frequency ω_{PB} to 1 rps when using the approximation. The normalized ω_{PB} is transformed to the desired transition frequency during the synthesis phase of the

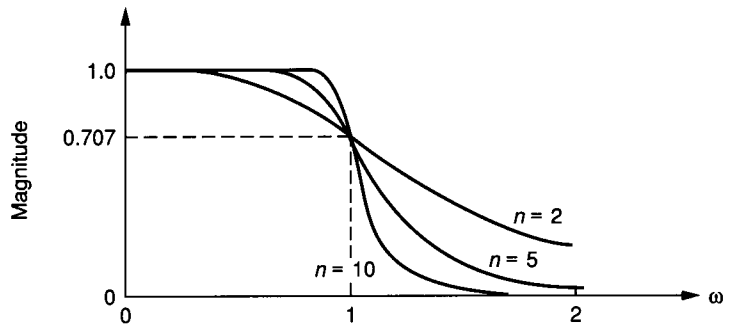


FIGURE 8.4-3
Magnitude characteristics of a Butterworth approximation for orders of $n = 2, 5$, and 10.

problem. Figure 8.4-3 shows only the magnitude characteristics of the Butterworth approximation. All approximating functions are characterized by both a magnitude and phase response although many filter specifications are based solely on the magnitude response. The phase shift of the Butterworth filter approximation may be found in other sources.[27]

Several other filter approximations are often used in filter design. One of these is called the *Chebyshev filter approximation* and is illustrated in Fig. 8.4-4 for various values of n. It is seen that the magnitude of the Chebyshev filter approximation ripples in the passband and is monotonically decreasing in the transition and stopband regions. The advantage of the Chebyshev filter approximation is that for a given n, the slope of the magnitude response in the vicinity of ω_{PB} is steeper than that of a Butterworth filter approximation, resulting in a smaller transition region if G_{PB} and G_{SB} are identical.

A third popular filter approximation is called the *elliptic filter approximation* and is shown in Fig. 8.4-5. This approximation ripples both in the stopband and the passband, but is monotonically decreasing in the transition region. The elliptic filter approximation has the narrowest transition region of any type of filter characteristics considered here, given the same values of n, G_{PB}, and G_{SB}. Other filter approximations have been tabulated and feature other frequency characteristics such as linear phase shift.

Fortunately, there is considerable tabulated information available on standard filter approximations.[27–34] The objective of the filter designer in using this tabulated information is to obtain a polynomial such as Eq. 8.4-6, its roots, or a passive RLC ladder network. Any of these three form the starting point for the design using one of many methods to arrive at an active filter realization of the filter approximation. Switched capacitor filter design can start from the active filter realization, the approximating function, or from the original information used to characterize the filter requirements.

To use the tabulated information, it is necessary to determine the order n from the filter specification. Because n determines the number of components and complexity of a filter, the minimum value of n is generally selected. Although the filter specification can be given as shown in Fig. 8.4-2, it is more customary to

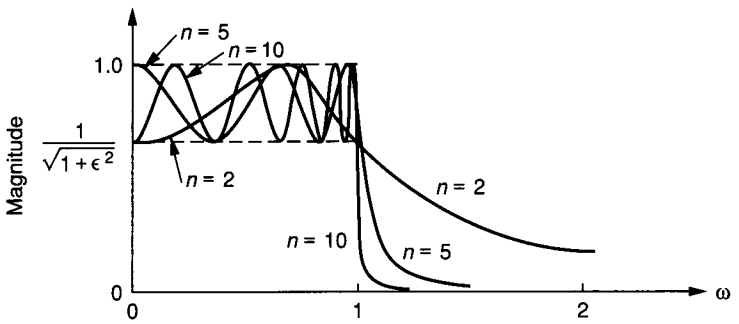


FIGURE 8.4-4
Magnitude characteristics of a Chebyshev approximation for an arbitrary ϵ and for orders n = 2, 5, and 10.

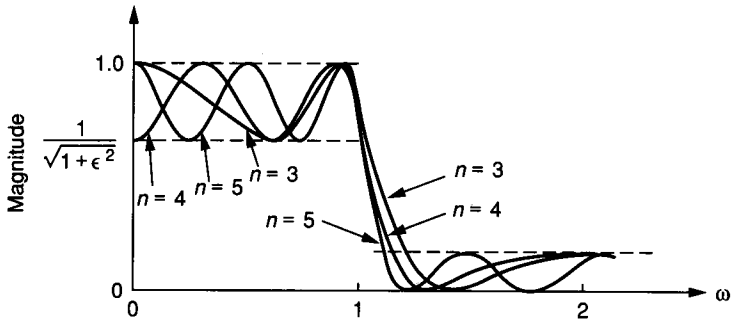


FIGURE 8.4-5
Magnitude characteristics of an elliptic approximation with arbitrary ϵ and for orders of n = 3, 4, and 5.

convert the vertical axis to a decibel range. Figure 8.4-6*a* shows the gain specifications, G, of a low-pass filter with the vertical axis specified in decibels and the frequency axis normalized to ω_{PB}. Ω is defined as ω_{SB}/ω_{PB} and G_Ω (dB) $= 20 \log_{10} G_{SB}$. Because the gains of most filters are less than unity, attenuation rather than gain is often used to describe their characteristics. Figure 8.4-6*b* shows the equivalent specification of Fig. 8.4-6*a* in terms of attenuation, $A = 1/G$, where $A_{PB} = 1/G_{PB}$ [A_{PB} (dB) $= -G_{PB}$ (dB)], and $A_\Omega = 1/G_\Omega$ [A_Ω (dB) $= -G_\Omega$ (dB)].

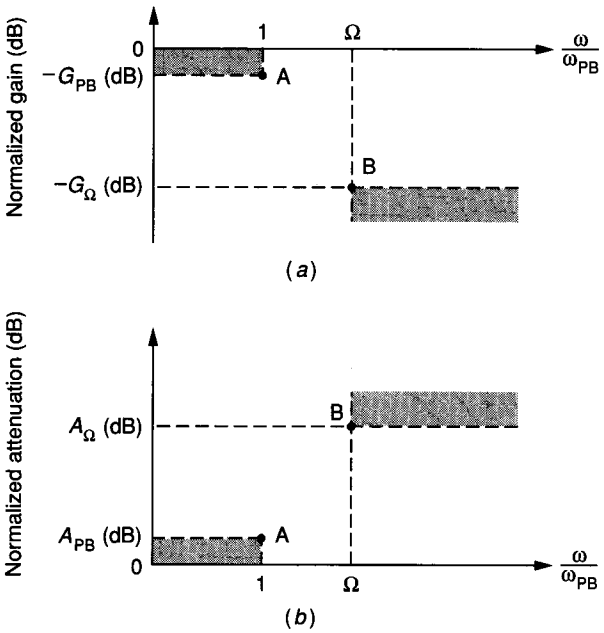


FIGURE 8.4-6
(*a*) Specifications for a low-pass filter in terms of gain, (*b*) Specifications for a low-pass filter in terms of attenuation.

From the parameters A_Ω, A_{PB}, and Ω, the order of the filter can be quickly determined using a set of nomographs.[35] Figure 8.4-7 is a nomograph for determining the order of the Butterworth filter approximation. The use of nomographs is illustrated in Fig. 8.4-8. A straight line is drawn through the specified values of A_{PB} and A_Ω, shown as points 1 and 2 in Fig. 8.4-8. The intersection with the

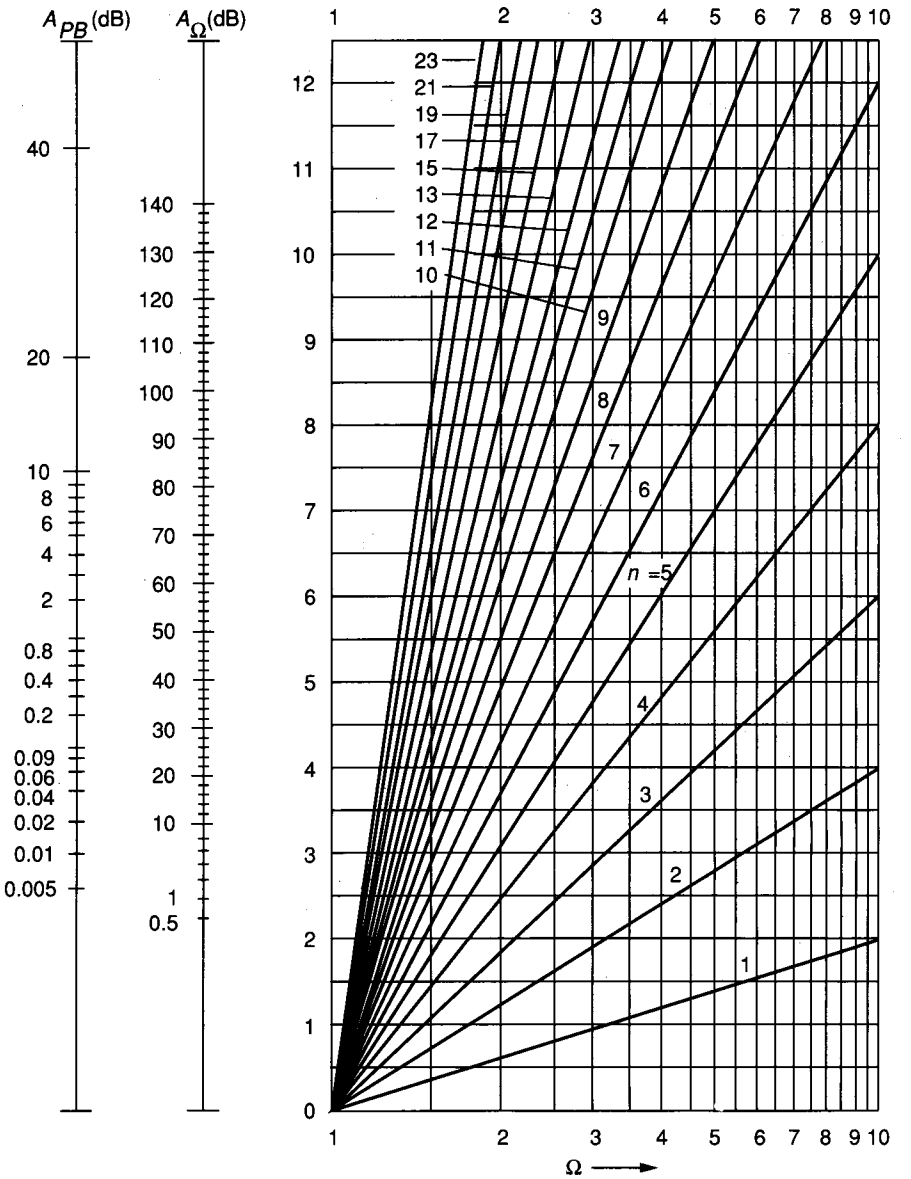


FIGURE 8.4-7
A nomograph for determining the order of a Butterworth magnitude function (Kawakami).

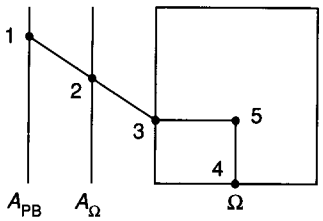


FIGURE 8.4-8
The method for using the nomograph of Fig. 8.4-7.

left side of the graph (point 3) is then extended horizontally until it meets a line drawn vertically from point 4, corresponding to the desired normalized stopband frequency, Ω. The resulting intersection at point 5 establishes the required order of the filter. If point 5 is between two of the *order loci*, the higher one must be used.

Example 8.4-1. Determination of the order of a low-pass Butterworth filter. Find the order of a Butterworth filter approximation to Fig. 8.4-6*b* where $A_{\Omega} = 40$ dB, $A_{PB} = 3$ dB, and $\Omega = 2$.

Solution. Using the nomograph of Fig. 8.4-7, we find that point 5 lies between $n = 6$ and $n = 7$. Therefore, the order of the filter approximation must be 7.

Figures 8.4-9 and 8.4-10 give the corresponding nomographs for determining the order or degree of Chebyshev and elliptic filter approximations, respectively. These nomographs are used in the same manner as the one in Fig. 8.4-7. An example will illustrate how the Chebyshev and elliptic filter approximations require lower order than the Butterworth filter approximation for the same design parameters.

Example 8.4-2. Determination of low-pass Chebyshev and elliptic filter approximations. Repeat the preceding example to find the order of the Chebyshev and elliptic filter approximations that will meet the same specifications.

Solution. From Fig. 8.4-9 we obtain $n = 4$ for the Chebyhev filter approximation, and from Fig. 8.4-10 we see that $n = 3$ is sufficient for the elliptic filter approximation to satisfy the specifications.

Once the order of the filter approximation is known, the designer must then decide how the filter is to be realized. Two approaches will be considered. The first approach starts with Eq. 8.4-6 in which the numerator and denominator polynomials are factored in the form of second-order products with real coefficients (a first-order product will be necessary if n is odd). This information can be found from the tabulations in the literature. For example, Table 8.4-1 shows the denominator coefficients of Eq. 8.4-6 with $b_0 = 1$ and gives the pole locations and quadratic functions of the denominator of Eq. 8.4-6 for the Butterworth filter approximations. The numerator polynomial of Eq. 8.4-6 for the Butterworth filter approximation is a constant. In this case the function $H(s)$ can be expressed as

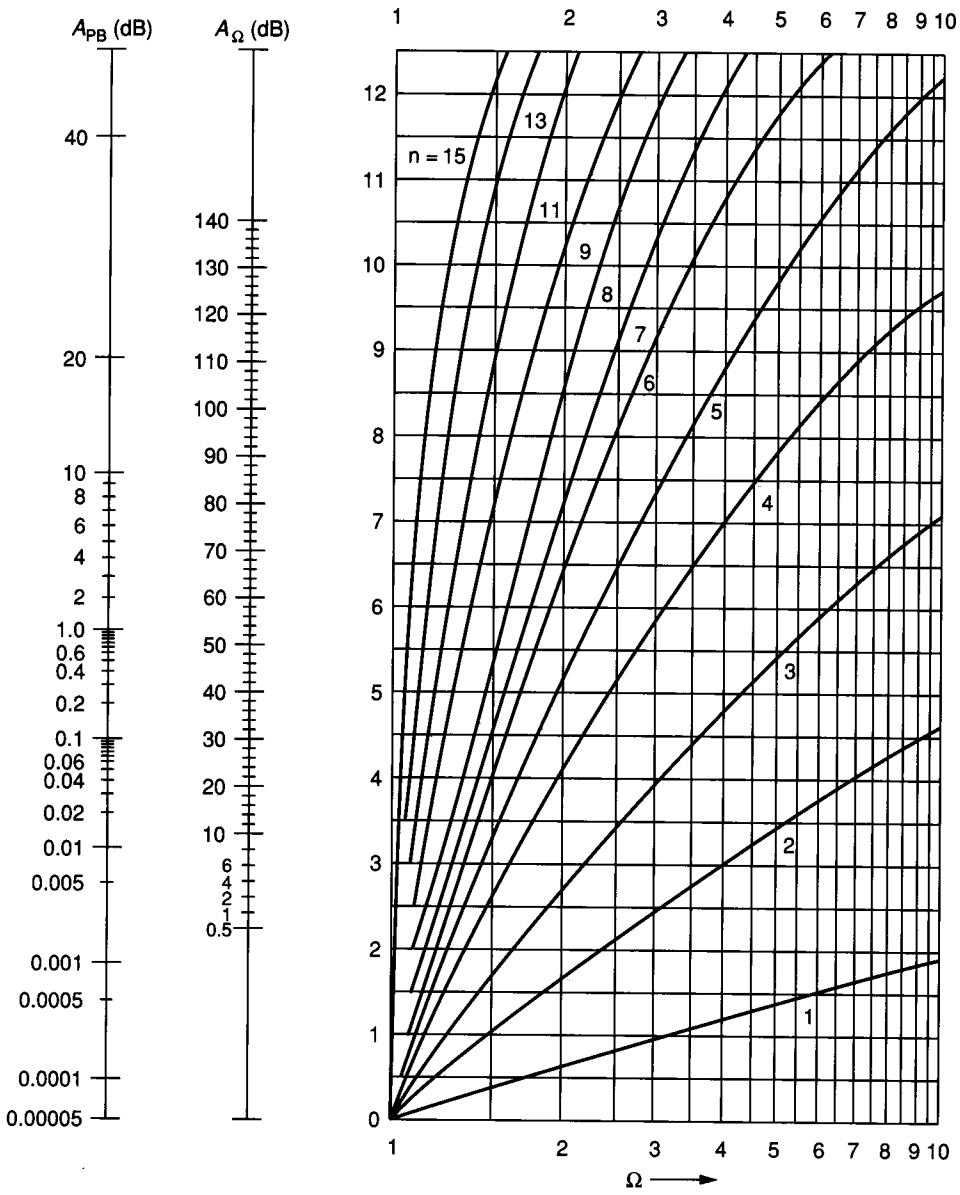


FIGURE 8.4-9
A nomograph for determining the order of a Chebyshev magnitude approximation (Kawakami).

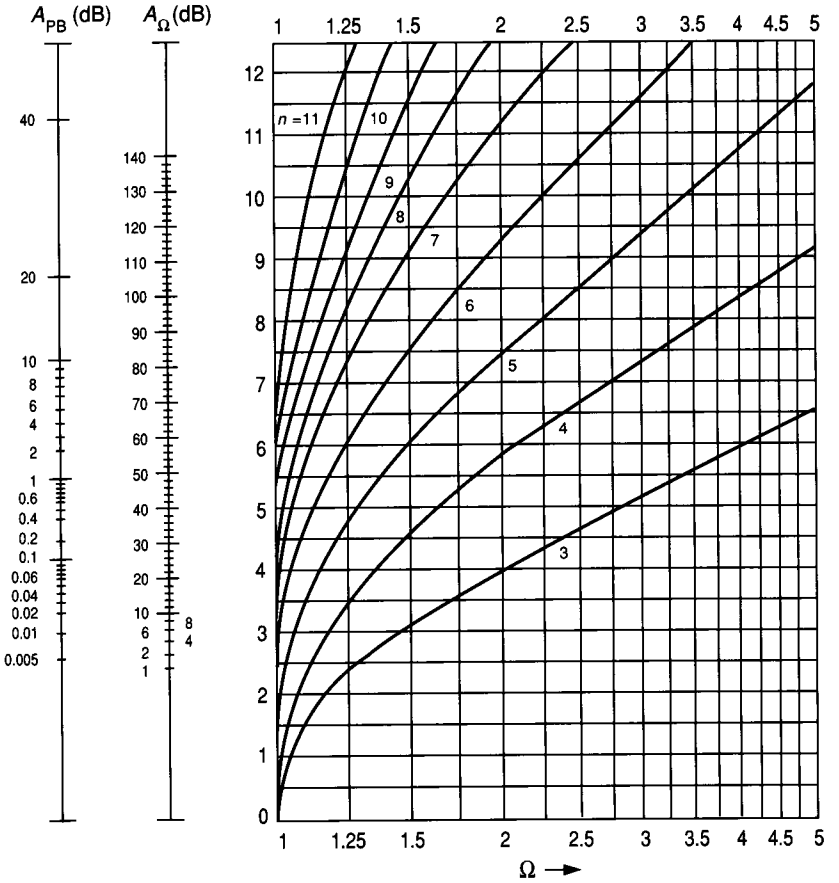


FIGURE 8.4-10
A nomograph for determining the order of an elliptic magnitude approximation (Kawakami).

TABLE 8.4-1*a*
Denominator coefficients of maximally flat magnitude (Butterworth) functions of the form: $s^n + b_{n-1}\,s^{n-1} + b_{n-2}\,s^{n-2} + \cdots b_2 s^2 + b_1 s + 1$ with passband 0 – 1 rad/s

n	b_1	b_2	b_3	b_4	b_5
2	1.414214				
3	2.000000				
4	2.613126	3.414214			
5	3.236068	5.236068			
6	3.863703	7.464102	9.141620		
7	4.493959	10.097835	14.591794		
8	5.125831	13.137071	21.846151	25.688356	
9	5.758770	16.581719	31.163437	41.986386	
10	6.392453	20.431729	42.802061	64.882396	74.233429

(By permission from L. P. Huelsman and P. E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill Book Co., New York, 1980.)

TABLE 8.4-1*b*
Pole locations and quadratic factors ($s^2 + b_1 s + 1$) of maximally flat magnitude (Butterworth) functions with passband 0 − 1 rad/s (*Note:* All odd-order functions also have a pole at $s = 1$)

n	Poles	b_1
2	$-0.70711 \pm j0.70711$	1.41421
3	$-0.50000 \pm j0.86603$	1.00000
4	$-0.38268 \pm j0.92388$	0.76536
	$-0.92388 \pm j0.38268$	1.84776
5	$-0.30902 \pm j0.95106$	0.61804
	$-0.80902 \pm j0.58779$	1.61804
6	$-0.25882 \pm j0.96593$	0.51764
	$-0.70711 \pm j0.70711$	1.41421
	$-0.96593 \pm j0.25882$	1.93186
7	$-0.22252 \pm j0.97493$	0.44504
	$-0.62349 \pm j0.78183$	1.24698
	$-0.90097 \pm j0.43388$	1.80194
8	$-0.19509 \pm j0.98079$	0.39018
	$-0.55557 \pm j0.83147$	1.11114
	$-0.83147 \pm j0.55557$	1.66294
	$-0.98079 \pm j0.19509$	1.96158
9	$-0.17365 \pm j0.98481$	0.34730
	$-0.50000 \pm j0.86603$	1.00000
	$-0.76604 \pm j0.64279$	1.53208
	$-0.93969 \pm j0.34202$	1.87938
10	$-0.15643 \pm j0.98769$	0.31286
	$-0.45399 \pm j0.89101$	0.90798
	$-0.70711 \pm j0.70711$	1.41421
	$-0.89101 \pm j0.45399$	1.78202
	$-0.98769 \pm j0.15643$	1.97538

(By permission from L. P. Huelsman and P. E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill Book Co., New York, 1980.)

a product of biquadratic functions, $H_i(s)$, where the general form of the second-order (quadratic) function will be

$$H(s) = \frac{\pm H_{0i}\omega_{pi}^2}{s^2 + (\omega_{pi}/Q_i)s + \omega_{pi}^2} = \frac{\pm H_{0i}p_{1i}p_{2i}}{(s + p_{1i})(s + p_{2i})} \tag{8.4-7}$$

where H_{0i} is the gain at $\omega = 0$, ω_{pi} is the undamped natural frequency, and Q_i is the quality factor of the pole p_i and p_{2i} is the complex conjugate of p_{1i} if p_{1i} is not real.

Typically, the information tabulated on filter design is normalized so that ω_{PB} is unity. However, the actual filter specifications are usually in the neighborhood of thousands of cycles per second. To convert the *normalized frequency* values of the design tables to the actual filter frequency requires a *frequency denormalization*. This denormalization involves a change of the complex frequency variable. If we consider p as the normalized complex frequency variable and s as the denormalized (actual) one, then the frequency denormalization is defined as

$$s = \Omega_n p \tag{8.4-8}$$

where Ω_n is a dimensionless frequency denormalization constant. This denormalization is generally used at the synthesis stage of the design. Following this approach, a filter is initially synthesized to realize the normalized transfer function. The denormalization then entails a subsequent scaling of the component values in the filter. Table 8.4-2 shows how this denormalization acts on the normalized values of R, L, and C.

A second type of denormalization that is often used is called *impedance denormalization*. It permits an arbitrary scaling to be applied simultaneously to all the passive elements of a filter in order to get more practical component values. A normalized impedance $Z_n(s)$ can be denormalized to the impedance $Z(s)$ by the relation

$$Z(s) = z_n Z_n(s) \tag{8.4-9}$$

where z_n is a dimensionless impedance denormalization constant. Table 8.4-2 shows how this denormalization affects the passive elements. The combined effects of the denormalizations of Eqs. 8.4-8 and 8.4-9 are illustrated in this table. *This impedance denormalization does not affect the voltage or current gain of the filter.*

Figure 8.4-11 shows three possible active filter realizations of Eq. 8.4-7. Figure 8.4-11*a* uses a finite-gain amplifier and an RC feedback network. This circuit was originally proposed by Sallen and Key in 1955[36] and was one of the first active RC filter structures. This circuit does not have flexibility in realizing Eq. 8.4-7 if H_{oi} is also specified because H_{oi} is fixed and equal to $3 - (1/Q_i)$.

TABLE 8.4-2
Effect of frequency and impedance denormalization on network elements

Denormalized	R	C	L
$s = \Omega_n p$	R	$\frac{C}{\Omega_n}$	$\frac{L}{\Omega_n}$
$Z = z_n Z_n$	$z_n R$	$\frac{C}{z_n}$	$z_n L$
$Z(s) = z_n Z_n(p)$	$z_n R$	$\frac{C}{\Omega_n z_n}$	$\frac{z_n}{\Omega_n} L$

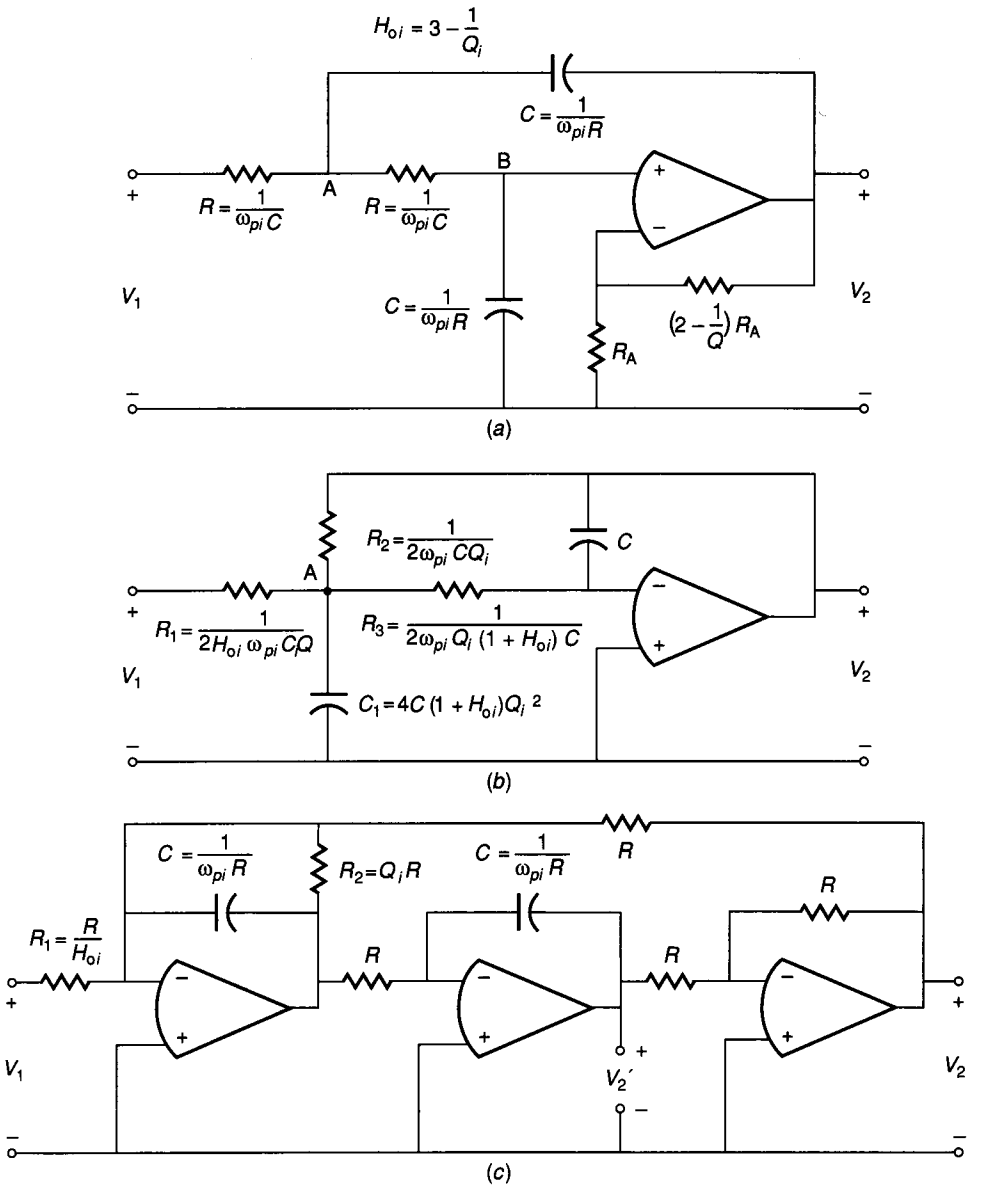


FIGURE 8.4-11
Three possible realizations of Eq. 8.4-7 (second-order, low-pass): (*a*) Sallen and Key (finite-gain) structure, (*b*) Infinite-gain structure, (*c*) Tow-Thomas (resonator) structure.

This is not considered a major limitation because the overall gain can be realized by adding a cascaded gain stage. In Fig. 8.4-11*a*, one may choose a suitable value for R; ω_{pi} and Q_i define the rest of the elements. Alternatively, one may choose a suitable value for the capacitors; then the resistors are defined as $(\omega_{pi}C)^{-1}$. The circuit of Figure 8.4-11*a* realizes Eq. 8.4-7 with a positive sign.

The circuit of Figure 8.4-11*b* is called an *infinite-gain realization*. It has the ability to realize simultaneously H_{oi}, ω_{pi}, and Q_i and realizes Eq. 8.4-7 with a negative sign. The circuit of Figure 8.4-11*c* is called the Tow-Thomas circuit[37,38] and consists of the cascade of a damped inverting integrator, an inverting integrator, and an inverter. This circuit has a great deal of flexibility and is very easy to tune. If the output is taken at V_2, then it realizes Eq. 8.4-7 with a negative sign. If the output is taken at V_2', then the circuit of Fig. 8.4-11*c* realizes Eq. 8.4-7 with a positive sign. In these circuits, a suitable value for either R or C is chosen and the remaining component values are calculated from the equations given in the figure. Many other realizations of Eq. 8.4-7 exist; however, the circuits of Fig. 8.4-11 are representative.

Example 8.4-3. Design of a low-pass Butterworth filter. A low-pass Butterworth filter is to be designed for the specifications of $A_\Omega = 30$ dB, $\omega_{PB} = 2000\pi$, and $\omega_{SB} = 4000\pi$.

Solution. If we normalize ω_{PB} to unity, we get $\Omega = 2$. From Fig. 8.4-7 we see that $n = 5$ will satisfy the filter specification. From Table 8.4-1, we conclude that this function can be realized with two second-order stages cascaded with one first-order stage. The realization is shown in Fig. 8.4-12*a*. The stage order is arbitrary, although one typically chooses the high-Q stages as the last stages. The normalized transfer function for each of the stages is shown, as well as Q_i and ω_{pi}. Note that stage 1 is a simple, first-order circuit so that Q is not defined. Stage 1 may be realized by a simple damped integrator, whereas one of the circuits in Fig. 8.4-11 can be used for stages 2 and 3. Selecting the circuit of Fig. 8.4-11*b* results in the realization of Fig. 8.4-12*b*, where the formulas of Fig. 8.4-12*a* have been used with $\omega_{pi} = 1$ for $i = 1, 2$ and 3, $Q_2 = 0.61804$, and $Q_3 = 1.61804$. The last step is to frequency-denormalize the realization using Eq. 8.4-8. To denormalize from a frequency of 1 rad/s to 2000π rad/s requires $\Omega_n = 2000\pi$. To avoid 1 Ω resistors, an impedance normalization of $z_n = 10^4$ will also be used. The resulting realization is shown in Fig. 8.4-12*c*. If a Butterworth filter approximation had been used for any value of A_{PB} other than -3 dB, then the normalized passband would not be unity. This must be taken into account when finding the proper Ω_n.

Note that the same circuit structure used in Fig. 8.4-12 could also be used to realize the Chebyshev function. In this case the quadratic functions would be obtained from tabulated data in the literature. Only the component values in Fig. 8.4-12*b* and *c* would vary in changing this realization from a Butterworth to a Chebyshev filter.

8.4.2 High-Pass Filters

Filters other than the low-pass type can be designed through the use of frequency transformations. These allow one to take the tabulated low-pass filter information

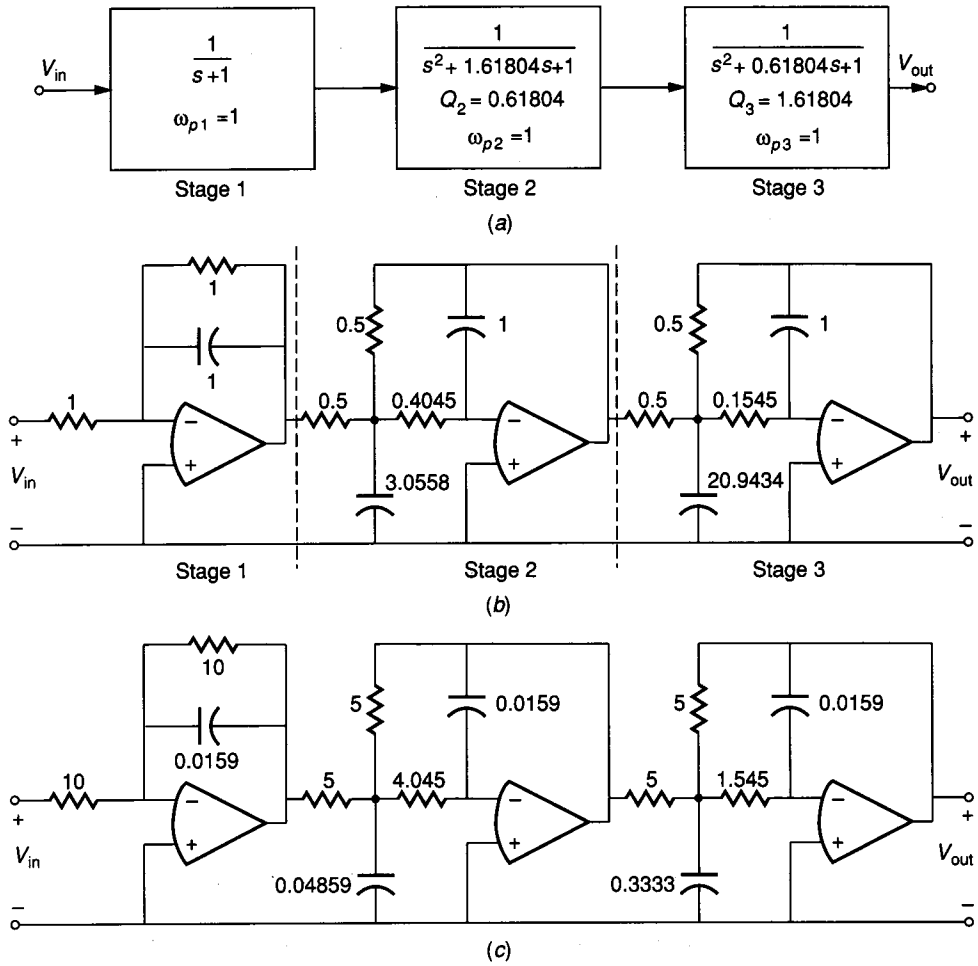


FIGURE 8.4-12
Realization for Example 8.4-3: (*a*) Stage ordering, (*b*) Normalized realization (all values in ohms or farads), (*c*) Frequency and impedance denormalized realization (all values in kilohms and microfarads).

and transform it to apply to high-pass, bandpass, or band-elimination filters. The transformed filter information can then be realized in a cascaded manner using the appropriate RC active stages. A low-pass to high-pass transformation can be defined as

$$s = \frac{1}{p} \tag{8.4-10}$$

where s is the low-pass complex frequency variable. Figure 8.4-13 illustrates how Eq. 8.4-10 transforms an ideal low-pass filter to an ideal high-pass filter. The poles of a high-pass filter can be found by substituting the low-pass poles for s in Eq. 8.4-10. One must also remember that a high-pass realization of order n

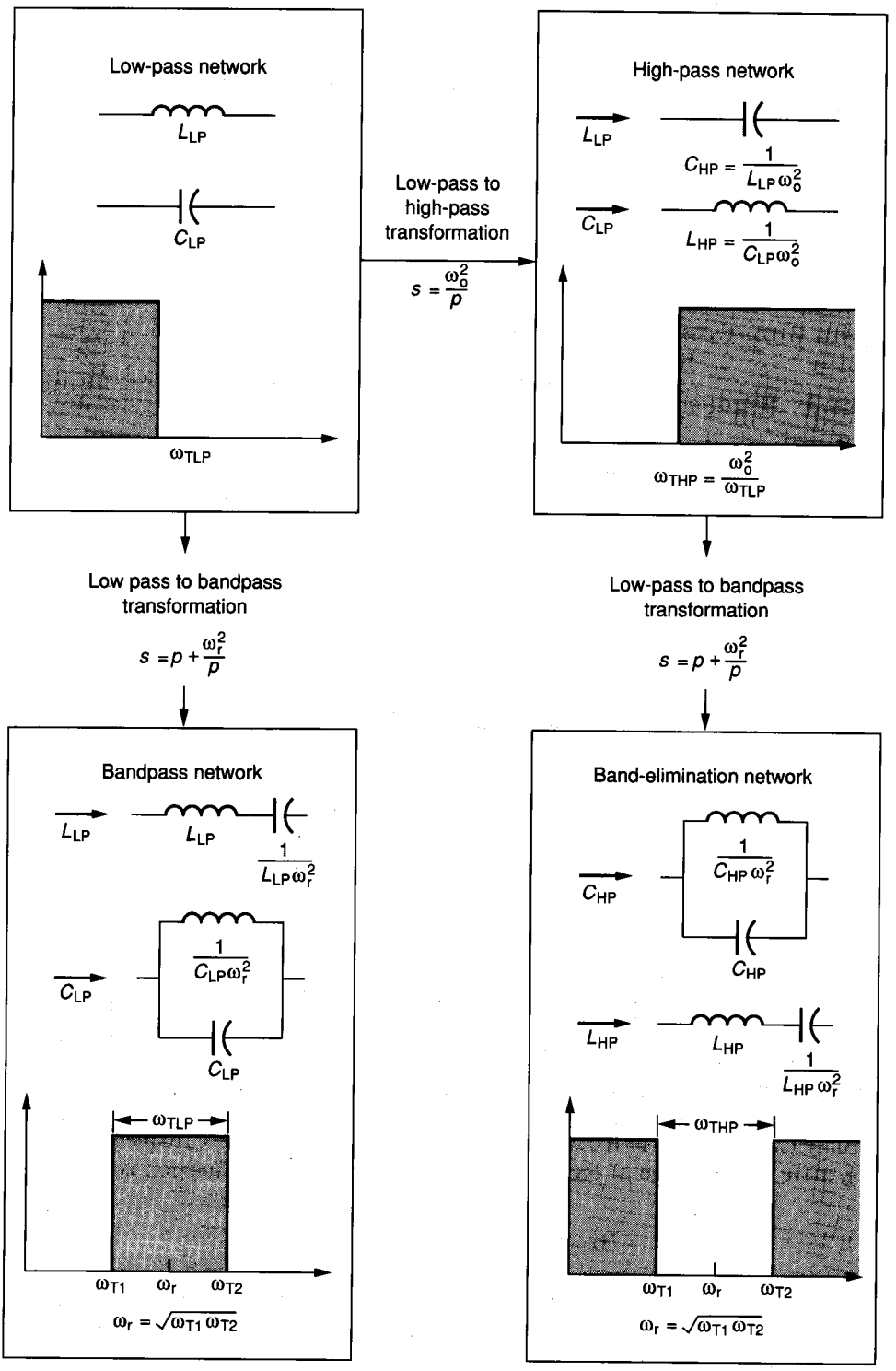


FIGURE 8.4-13
Changes of network elements under frequency transformations. (By permission of L. P. Huelsman and P. E. Allen, *Introduction to the Theory and Design of Active Filters,* McGraw-Hill Book Co., New York, 1980.)

has n zeros at the origin. Alternatively, one can use Eq. 8.4-10 to replace s in expressions such as Eq. 8.4-7 to get

$$H_{HPi}(p) = \frac{\pm H_{oi}p^2}{p^2 + (\omega_{pi}/Q_i)p + \omega_{pi}^2} \tag{8.4-11}$$

which is a high-pass quadratic form of Eq. 8.4-7. Second-order RC active realizations of Eq. 8.4-11 similar to those shown in Fig. 8.4-11 can be found in the literature on RC active filters. Figure 8.4-14 gives three realizations using the same types of structures as were used in Fig. 8.4-11.

8.4.3 Bandpass Filters

A low-pass to bandpass transformation can be defined as

$$s = p + \frac{\omega_r^2}{p} \tag{8.4-12}$$

where s is the low-frequency complex variable, p is the bandpass complex variable, and ω_r is defined in Fig. 8.4-13 as the geometric center frequency of the bandpass filter, given as

$$\omega_r = \sqrt{\omega_{T1}\omega_{T2}} \tag{8.4-13}$$

where ω_{T1} and ω_{T2} are defined in Fig. 8.4-13. The bandwidth is defined as $\omega_{T2} - \omega_{T1}$ and is equal to the original passband of the low-pass filter, ω_{TIP} (or ω_{PB}). The transformation of Eq. 8.4-12 is used in the same manner as the transformation of Eq. 8.4-10 to get either the new bandpass roots or the bandpass transfer function. The transformation of Eq. 8.4-12 doubles the order of the low-pass filter. For example, if a low-pass filter is given as

$$H_{LPi}(s) = \frac{H_{oi}(\omega_1/Q)}{s + (\omega_1/Q)} \tag{8.4-14}$$

then application of the low-pass to bandpass transformation of Eq. 8.4-12 gives

$$H_{BPi}(p) = \frac{\pm H_{oi}(\omega_1/Q)p}{p^2 + (\omega_1/Q)p + \omega_r^2} \tag{8.4-15}$$

It is seen that the second-order bandpass structure has two poles which are often complex and a zero at the origin and at infinity in the complex frequency plane. A more general form of the second-order bandpass transfer function is

$$H_{BPi}(s) = \frac{\pm H_{oi}(\omega_{pi}/Q_i)s}{s^2 + (\omega_{pi}/Q_i)s + \omega_{pi}^2} \tag{8.4-16}$$

where we have reverted to the notation of s for the complex frequency variable. Figure 8.4-15 shows three realizations of Eq. 8.4-16 using the same basic structures illustrated in Figs. 8.4-11 and 8.4-14.

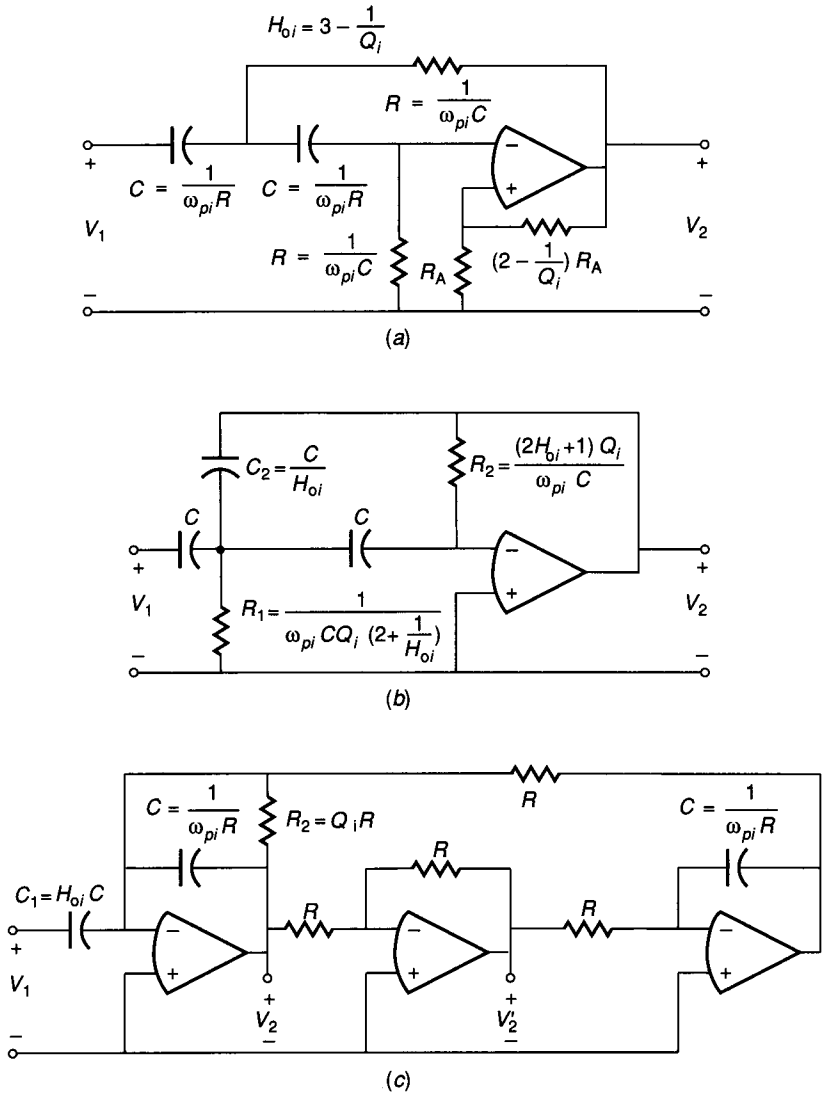


FIGURE 8.4-14
Three realizations of Eq. 8.4-11 (second-order, high-pass): (*a*) Finite-gain or Sallen and Key structure, (*b*) Infinite-gain structure, (*c*) Tow-Thomas or resonator structure.

A second major approach to active filter design, once the order of the filter is known, is to go directly to a passive realization. Passive RLC realizations for normalized low-pass filter approximations have also been tabulated and can be found in the literature.[26,27,28,34,39] To illustrate this approach, we repeat Example 8.4-3.

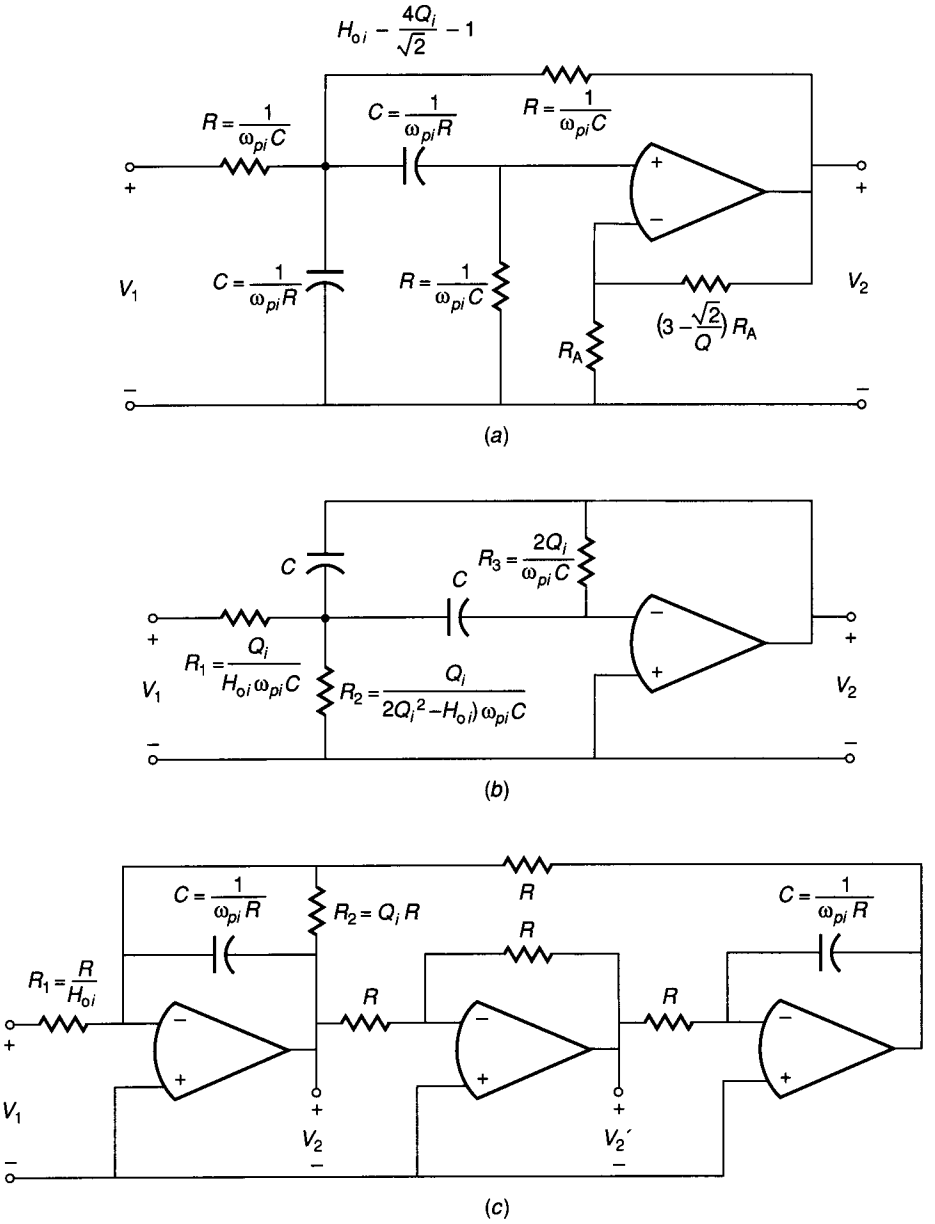


FIGURE 8.4-15
Three realizations of Eq. 8.4-16 (second-order, bandpass structure): (*a*) Finite-gain or Sallen and Key structure, (*b*) Infinite-gain, (*c*) Tow-Thomas or resonator structure.

Example 8.4-4. Realization of a passive RLC filter. Design a passive RLC filter that will satisfy the specifications of Example 8.4-3. This filter is to be driven from a voltage source having zero resistance and will be terminated in a 1000 Ω load.

Solution. From Example 8.4-3, we know that $n = 5$. From the tabulation found in the literature, we obtain the realization shown in Fig. 8.4-16. This realization has been normalized so that $\omega_{PB} = 1$ rps and $R_L = 1\ \Omega$. It is now necessary to denormalize using Eqs. 8.4-8 and 8.4-9. Because ω_{PB} of Fig. 8.4-16*a* is unity and we desire ω_{PB} of 2000π, then $\Omega_n = 2000\pi$. Because R_L of Fig. 8.4-16*a* is 1 Ω and we want $R_L = 1000\ \Omega$, then $z_n = 1000$. Applying the equations of Table 8.4-2 to the components of Fig. 8.4-16*a* results in the final realization shown in Fig. 8.4-16*b*, which has a transfer function equivalent to that of Fig. 8.4-12*c*.

The passive RLC low-pass realizations may be easily converted to high-pass, bandpass, or band-elimination using the transformations of Fig. 8.4-13. The passive RLC realizations are also used as the starting point in certain types of active filter design.

Figure 8.4-17 summarizes this section. The design of active RC filters starts with the filter specification, which is converted into a filter approximation. Sometimes, the classical approximations presented here are not adequate, and computer-generated approximations are used instead. The filter approximation will take the form of a rational polynomial transfer function. If the roots of the rational polynomial are factored into first- and second-order products, then the cascade realization approach illustrated here can be used. Methods also exist

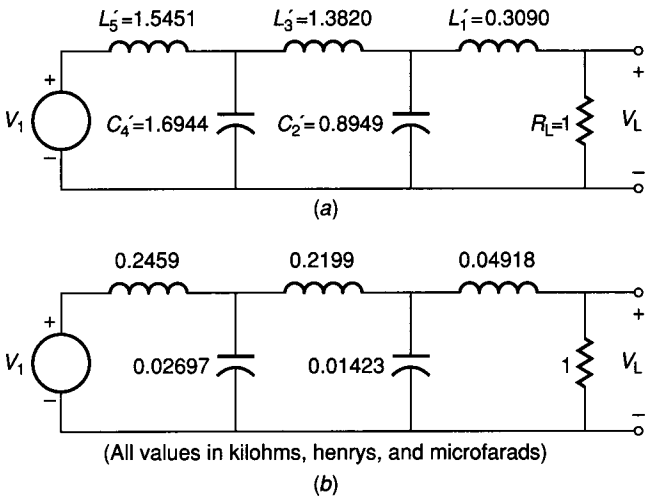


FIGURE 8.4-16
(*a*) Passive RLC normalized prototype for Example 8.4-4, (*b*) Denormalized realization of *a*.

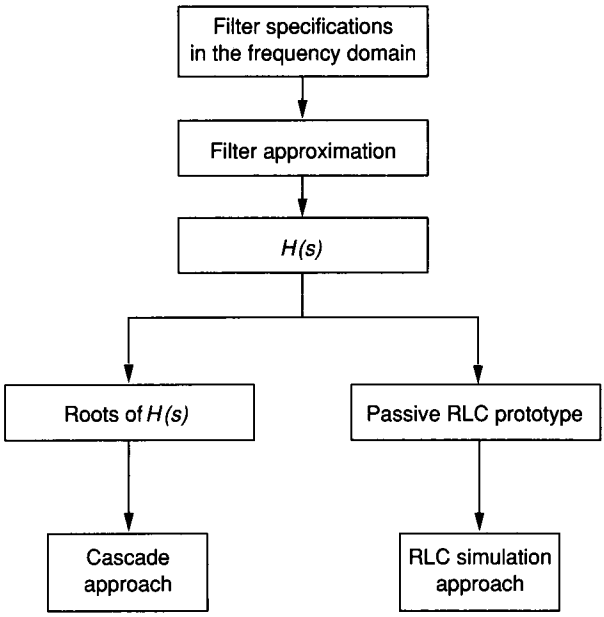


FIGURE 8.4-17
Summary of continuous-time filter design approaches.

for synthesizing a circuit directly from the rational polynomial without obtaining the roots, but they have not been discussed here. Tabulations of a passive RLC prototype circuit that implement the standard approximating functions are also widely available in the literature. The switched capacitor filters, which will be presented in the next section, start from the roots of the rational function, the rational function, or the passive RLC prototype.

8.5 SWITCHED CAPACITOR FILTERS

The use of switched capacitor methodology to design and implement analog filters using integrated circuit technology is illustrated in this section. It is necessary that the technology be capable of providing a good switch, a well-defined capacitor, and an op amp. Because all of these aspects are found in MOS technology, it has become the predominant technology for switched capacitor filters. Switched capacitor methods are not new and, in fact, were employed by James Clerk Maxwell in his discussion on the equivalent resistance of a periodically switched capacitor.[40] The key development that led to the rapid evolution of practical switched capacitor methods was the realization that switched capacitor concepts could be implemented in MOS technology.[41] This realization was followed by a rapid development and implementation of analog signal processing techniques in MOS technology. Today, many switched capacitor circuits, including filters, are found in various products, including telecommunications products.[42]

The material presented in this section is a brief description of how to design switched capacitor filters. Three basic methods will be described. The first is resistor substitution and replaces the resistors in an RC active circuit with a switched capacitor realization. The second uses switched capacitor integrators to simulate the passive RLC prototype circuit for a desired filter realization. The last uses a direct building block approach in the z-domain. The filter requirements are transformed from the continuous-time frequency domain to the discrete-time frequency domain (z-domain). These approaches are representative of the methods used in switched capacitor filter design. More information can be found in the references.

8.5.1 Resistor Realization

One of the simplest approaches in switched capacitor design is to replace the resistors of a continuous-time, active RC filter realization with a switched capacitor realization of each resistor. Resistor realizations contain capacitors and switches and simulate the continuous-time resistor very well as long as the rate at which the switches are opened and closed is much higher than the frequencies of interest in the analog signal. Figure 8.5-1*a* shows the configuration of a *parallel* switched capacitor realization of a resistor, R, connected between two voltage sources, V_1 and V_2, illustrated in Fig. 8.5-1*b*. The switches, ϕ_1 and ϕ_2, are controlled by the nonoverlapping clocks of period T_c, as shown in Fig. 8.5-1*c*.

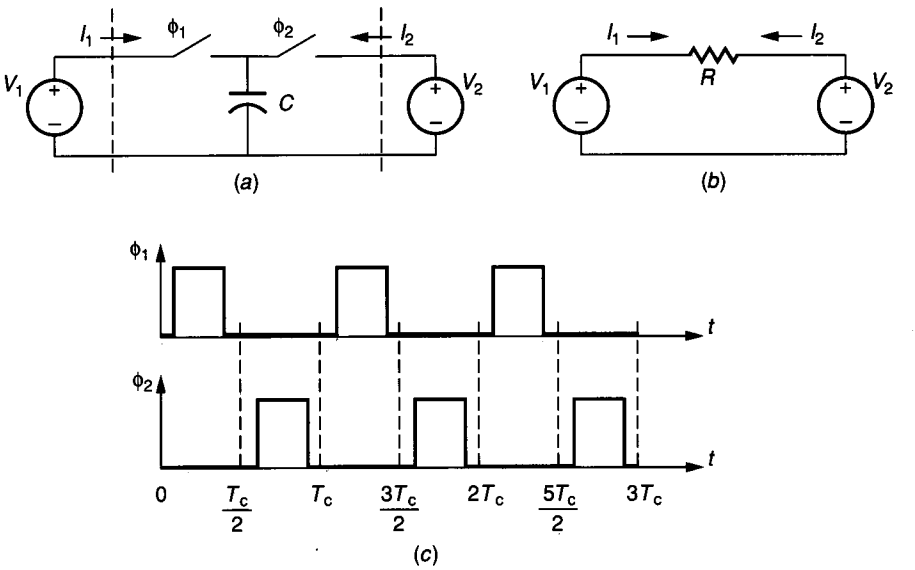


FIGURE 8.5-1
(*a*) Parallel switched capacitor realization of a resistor, (*b*) A continuous resistor, (*c*) Clock waveforms for the switched capacitor realization.

When the clock waveform in Fig. 8.5-1*c* is high, the switch designated by that waveform is closed.

To demonstrate the equivalence between the switched capacitor circuit in Fig. 8.5-1*a* and the resistor in Fig. 8.5-1*b*, assume that $V_1(t)$ and $V_2(t)$ are unchanged for several clock cycles. We shall designate these constant voltages as V_1 and V_2, respectively. During the time between 0 and $T_c/2$, switch ϕ_1 closes. If the switch resistance is small or the clock period large enough, the capacitor C will be charged to V_1. At $t = T_c/2$, we can define the total charge flow between 0 and $T_c/2$ past the left-hand vertical dashed line as $Q_1(T_c/2)$, which is given as

$$Q_1(T_c/2) = CV_1 \tag{8.5-1}$$

where C is initially uncharged. Next, consider the time interval between $T_c/2$ and T_c. Switch ϕ_2 closes and connects the charged capacitor to V_2. At time T_c, we can define the charge flow past the right-hand vertical dashed line as $Q_2(T_c)$ for $0 < t < T_c$, which is given as

$$Q_2(T_c) = C(V_2 - V_1) \tag{8.5-2}$$

Note that the flow of charge past the left-hand vertical dashed line during this period is

$$Q_1(T_c) = 0 \tag{8.5-3}$$

During the interval from T_c to $3T_c/2$, switch ϕ_1 closes again, resulting in the following charge flow during this interval.

$$Q_1\left(\frac{3T_c}{2}\right) = C(V_1 - V_2) \tag{8.5-4}$$

and

$$Q_2\left(\frac{3T_c}{2}\right) = 0 \tag{8.5-5}$$

As long as $V_1(t)$ and $V_2(t)$ remain constant, these equations hold for the charge flow into the capacitor C during the various switch closures.

The charge flows, Q_1 and Q_2, can be expressed in terms of the current that flows during the switch closure. This expression for Q_1 during the period from $T_c/2$ to $3T_c/2$ can be written as

$$Q_1 = Q_1(T_c) + Q_1\left(\frac{3T_c}{2}\right) = 0 + C(V_1 - V_2) = \int_{T_c/2}^{3T_c/2} I_1(t)\,dt \tag{8.5-6}$$

If we divide Eq. 8.5-6 by T_c, then the integral over the period T_c (in this case, from $T_c/2$ to $3T_c/2$) is equal to the average value of $I_1(t)$, designated as $I_1(\text{aver})$. Thus, from Eq. 8.5-6 we may write the following expression.

$$I_1(\text{aver}) = \frac{C}{T_c}(V_1 - V_2) \tag{8.5-7}$$

The average current flowing through the resistor R in the same time interval of length T_c is proportional to $V_1 - V_2$ and is expressed as

$$I_{1R}(\text{aver}) = \frac{V_1 - V_2}{R} \tag{8.5-8}$$

If V_1 and V_2 remain constant, then we can equate $I_1(\text{aver})$ and $I_{1R}(\text{aver})$ to obtain the equivalent resistance of the switched capacitor circuit. From Eq. 8.5-7 and Eq. 8.5-8 this is

$$R \cong \frac{T_c}{C} = \frac{1}{f_c C} \tag{8.5-9}$$

Equation 8.5-9 is a key result! It states that as long as V_1 and V_2 are approximately constant, the switched capacitor circuit of Fig. 8.5-1*a* realizes the resistor of Fig. 8.5-1*b*.

In reality, $V_1(t)$ and $V_2(t)$ are not constants but time-varying voltages. However, if the clock period is small enough, the values of $V_1(t + T_c)$ and $V_2(t + T_c)$ are not much different from $V_1(t)$ and $V_2(t)$. This can be stated in a different manner, assuming that the $V_1(t)$ and $V_2(t)$ waveforms are sinusoidal with a frequency of f_s. If f_s is much less than f_c, then T_s is much greater than T_c and Eq. 8.5-9 is valid. This condition is called the *high sampling approximation.*

Three other configurations of switched capacitor realizations of resistance along with the parallel switched capacitor configuration are shown in Fig. 8.5-2. The parallel switched capacitor resistance realization we have just discussed is shown in the first row. A second configuration, called the *series* switched capacitor realization, consists of two switches and one capacitor. If one repeats the preceding charge flow analysis, it can be shown that the equivalent resistance of the series switched capacitor realization is also given by Eq. 8.5-9. A third configuration, called the *series-parallel* switched capacitor realization, is shown in the third row of Fig. 8.5-2. The value of the resistor realization is shown in the last column and can be found in exactly the same manner as was done for the previous two configurations. Finally, the *bilinear* switched capacitor realization is shown. It uses four switches and one capacitor. If the high sampling frequency approximation is valid, all resistors of continuous-time RC active networks can be replaced on a one-for-one basis to obtain a switched capacitor realization.

The advantage of the switched capacitor methodology can be illustrated by comparing the RC product of a resistance designated as R_1 and a capacitance designated as C_2. Let us assume that the product of R_1 and C_2 forms the time constant τ, given as

$$\tau = R_1 C_2 \tag{8.5-10}$$

The dependence of the accuracy of τ on R_1 and C_2 can be written as

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \tag{8.5-11}$$

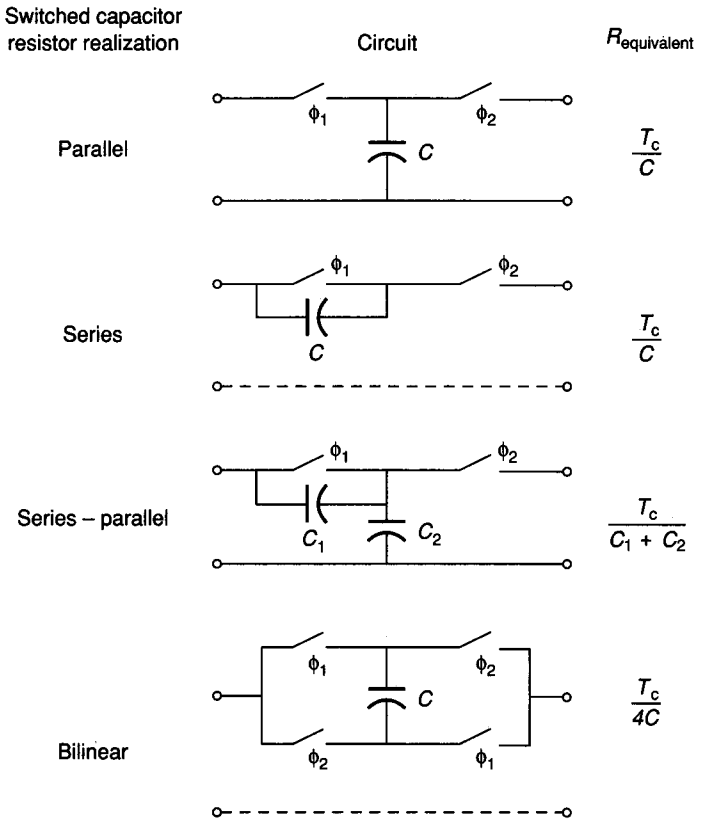


FIGURE 8.5-2
Summary of switched capacitor resistor simulations where $f << f_e$.

where dx/x is interpreted as the accuracy of x. The worst-case accuracy of τ will be the sum of the absolute accuracies of R_1 and C_2, which will be very poor if R_1 and C_2 are directly implemented by integrated circuit technology.

If R_1 is replaced by a switched capacitor resistance realization with a capacitor of value C_1 having an equivalent resistance given by Eq. 8.5-9, the time constant τ now becomes

$$\tau = \frac{1}{f_c}\frac{C_2}{C_1} = T_c\frac{C_2}{C_1} \tag{8.5-12}$$

The accuracy of the time constant, τ, in Eq. 8.5-12 can be expressed as

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \tag{8.5-13}$$

If the clock frequency is assumed to be constant, then Eq. 8.5-13 reduces to

$$\frac{d\tau}{\tau} \cong \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \tag{8.5-14}$$

We know from our previous studies that the relative accuracy of two capacitors fabricated on the same integrated circuit can be quite good. As a result, the value of Eq. 8.5-14 can be as low as 0.1%, which represents a tremendous improvement over Eq. 8.5-11 and is one of the key factors contributing to the success of integrated switch capacitor filters.

Unfortunately, the concept of a one-for-one replacement of resistors by switched capacitor resistor realizations breaks down if the high sampling frequency assumption is not valid. Although this does impact how switched capacitor circuits must be designed, it does not affect the accuracy or the small area achievable with switched capacitor circuits. The degree to which f_c must be larger than f_s for Eq. 8.5-9 to be valid depends on both the realization chosen and the circuit in which it is used. For a demonstration of some of these ideas, consider the first-order continuous-time RC circuit of Fig. 8.5-3. The continuous-time frequency-domain voltage transfer function can be written as

$$H(s) = \frac{1}{s\tau_1 + 1} = \frac{1}{s/\omega_1 + 1} \tag{8.5-15}$$

where $\tau_1 = 1/\omega_1 = R_1C_2$. The frequency response can be found by replacing s by $j\omega$ to get

$$H(j\omega) = \frac{1}{j(\omega/\omega_1) + 1} \tag{8.5-16}$$

The magnitude of Eq. 8.5-16 is

$$|H(j\omega)| = \frac{1}{[1 + (\omega R_1C_2)^2]^{1/2}} \tag{8.5-17}$$

and the argument, or phase shift, is

$$\text{Arg } H(j\omega) = -\tan^{-1}(\omega R_1C_2) \tag{8.5-18}$$

The frequency response of the circuit of Fig. 8.5-3 is shown in Fig. 8.5-4*a* and *b*. It is seen that this circuit is a first-order low-pass filter. The root of this filter is given in Fig. 8.5-4*c*.

A realization of the filter of Fig. 8.5-3 can be obtained by replacing the resistor, R_1, with any of the switched capacitor resistor realizations of Fig. 8.5-2. Figure 8.5-5*a* shows a switched capacitor realization using the parallel switched capacitor resistor realization. To analyze this circuit, the clock sequence must be specified. Figure 8.5-5*b* shows a shorthand method of illustrating the clock sequence for this circuit. ϕ_1 and ϕ_2 specify the phase periods during which the switches ϕ_1 and ϕ_2 close and will be denoted as the *odd* and *even* phase clocks, respectively. The odd phase periods (ϕ_1) will be designated by a superscript o, and the even phase periods (ϕ_2) will be designated by a superscript e.

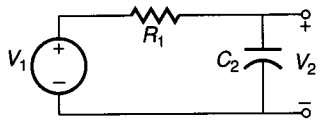


FIGURE 8.5-3
Continuous-time RC network.

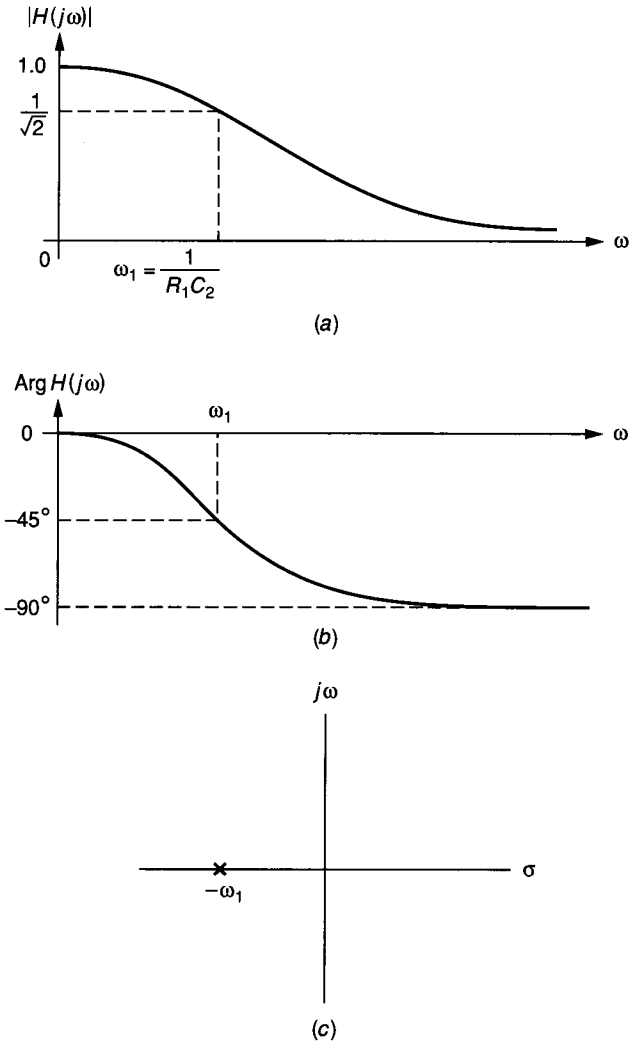


FIGURE 8.5-4
Frequency response of Fig. 8.5-3: (*a*) Magnitude, (*b*) Phase response, (*c*) Root locations of Fig. 8.5-3.

In the analysis of the circuit of Fig. 8.5-5*a* we assume that $V_1(t)$ is constant during the phase periods (which can be achieved by a sample-and-hold circuit). T will be used to denote T_c when there is no possible confusion. Consider the first odd phase period, where $(n-1) \leq (t/T) < (n-\frac{1}{2})$, when switch ϕ_1 is closed. In this analysis, we assume that switch ϕ_1 closes immediately after $t = (n-1)T$ and that C_1 is charged instantaneously to $V_1^{\circ}[(n-1)T]$. In practice, the time required for V_1 to charge C_1 to this value should be small compared with

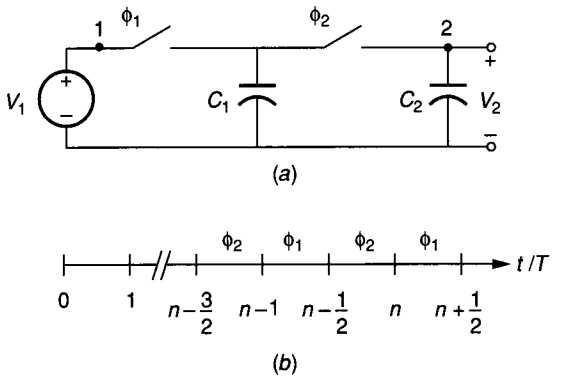


FIGURE 8.5-5
(*a*) Switched capacitor realization of Fig. 8.5-3, (*b*) Clock phasing.

$T/2$. During the odd phase period, we may redraw the circuit of Fig. 8.5-5*a* as shown in Fig. 8.5-6*a*. From this figure, we see that

$$V_{C1}(t) = V_1^o[(n-1)T] = V_1^o(n-1) \tag{8.5-19}$$

and

$$V_{C2}(t) = V_2^o[(n-1)T] = V_2^o(n-1) \tag{8.5-20}$$

The clock period T in Eqs. 8.5-19 and 8.5-20 has been dropped because it adds no useful information, thus simplifying the notation. This convention will be followed where no misinterpretation is likely.

In the next even phase period, $(n-\frac{1}{2}) \leq (t/T) < n$, switch ϕ_1 is open and switch ϕ_2 closes. Figure 8.5-6*b* represents Fig. 8.5-5*a* during this phase period. During this time, C_1 and C_2 are paralleled, resulting in a new value of V_2. The circuit of Fig. 8.5-6*b* may be converted to the equivalent circuit of Fig. 8.5-6*c* with uncharged capacitors. The voltage sources representing the initial voltages on the capacitors are assumed to be multiplied by a unit step function that starts at $t = (n-\frac{1}{2})T$ but whose value was established at $t = (n-1)T$. After closing switch ϕ_2, the charges on C_1 and C_2 must be redistributed to reestablish equilibrium. Using superposition techniques, V_2 can be expressed as

$$V_2(t) = \frac{C_1}{C_1+C_2}V_1^o(n-1) + \frac{C_2}{C_1+C_2}V_2^o(n-1) \tag{8.5-21}$$

Evaluating $V_2(t)$ at $t = (n-\frac{1}{2})T$, we obtain

$$V_2^e(n-\frac{1}{2}) = \frac{C_1}{C_1+C_2}V_1^o(n-1) + \frac{C_2}{C_1+C_2}V_2^o(n-1) \tag{8.5-22}$$

At the beginning of the next phase period $n \leq t/T < (n+\frac{1}{2})$, the voltage at V_2 can be written as

$$V_2^o(n) = V_2^e(n-\frac{1}{2}) \tag{8.5-23}$$

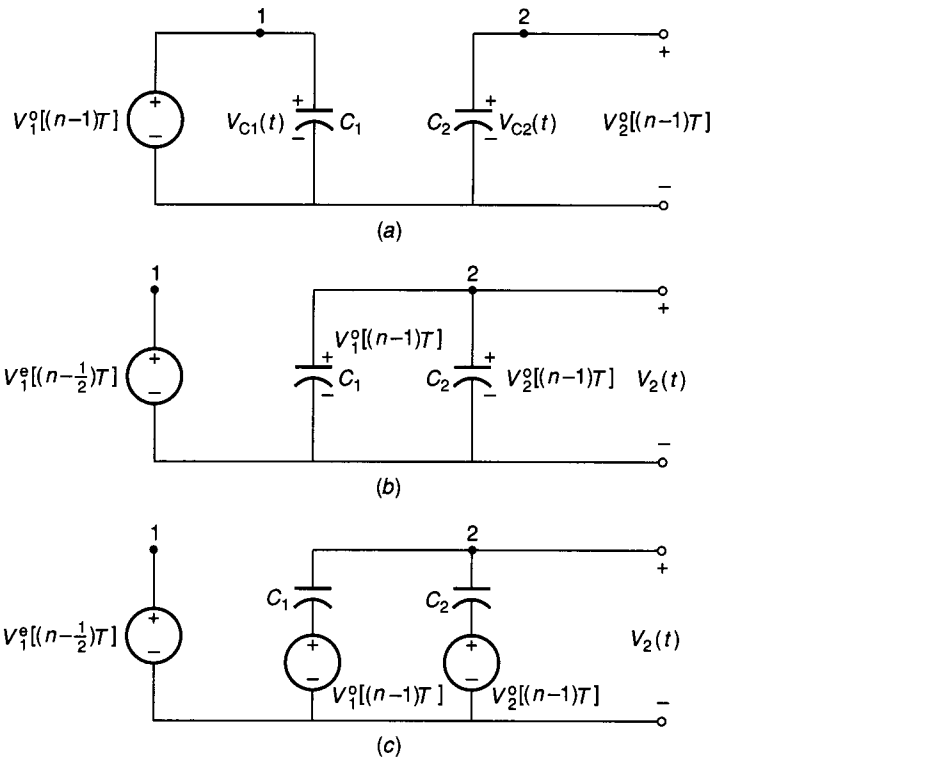


FIGURE 8.5-6
(*a*) Equivalent circuit of Fig. 8.5-5*a* when switch ϕ_1 is closed, (*b*) Equivalent circuit of Fig. 8.5-5*a* when switch ϕ_2 is closed, (*c*) Alternate form of *b*.

because the voltage V_2 has not changed from its value at $t = (n - \frac{1}{2})T$. Using Eq. 8.5-23 allows us to write

$$V_2^o(n) = \frac{C_1}{C_1 + C_2} V_1^o(n-1) + \frac{C_2}{C_1 + C_2} V_2^o(n-1) \tag{8.5-24}$$

Equation 8.5-24 recursively defines a sequence that can be transformed from the discrete-time domain to the z-domain by taking the z-transform characterized by

$$V(n) \rightarrow z^{-n} V(z) \tag{8.5-25}$$

Using this transformation on Eq. 8.5-24 results in

$$V_2^o(z) = \frac{C_1 z^{-1}}{C_1 + C_2} V_1^o(z) + \frac{C_2 z^{-1}}{C_1 + C_2} V_2^o(z) \tag{8.5-26}$$

Solving for $V_2^o(z)/V_1^o(z)$ results in the z-domain transfer function of the circuit of Fig. 8.5-5*a* sampled at the odd output phase.

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = \left(\frac{1}{1 + \alpha}\right) \frac{z^{-1}}{1 - [\alpha/(1 + \alpha)]z^{-1}} \tag{8.5-27}$$

where $\alpha = C_2/C_1$. Applying Eq. 8.5-25 to Eq. 8.5-23 results in $V_2^o(z) = z^{-1/2}V_2^e(z)$. Thus, Eq. 8.5-27 can be written as

$$H^{oe}(z) = \frac{V_2^e(z)}{V_1^o(z)} = \left(\frac{1}{1+\alpha}\right)\frac{z^{-1/2}}{1-[\alpha/(1+\alpha)]z^{-1}} \tag{8.5-28}$$

Thus,

$$H^{oo}(z) = z^{-1/2}H^{oe}(z) \tag{8.5-29}$$

The basic concepts of the z-transform have been used in an algorithmic manner in order to keep the presentation simple. The z-transform is rigorously developed elsewhere.[43]

The discrete-time frequency response can be found by replacing z by $e^{j\omega T}$, which is analogous to replacing s by $j\omega$ in the continuous-time frequency domain. Making this replacement in Eq. 8.5-27 gives the following expression, which is equivalent to the discrete-time frequency response of the circuit of Fig. 8.5-5*a*.

$$H^{oo}(e^{j\omega T}) = \frac{V_2^o(e^{j\omega T})}{V_1^o(e^{j\omega T})} = \frac{1}{(1+\alpha)\cos\omega T - \alpha + j(1+\alpha)\sin\omega T} \tag{8.5-30}$$

where Euler's formula ($e^{j\omega T} = \cos\omega T + j\sin\omega T$) has been used to remove $e^{j\omega T}$. The magnitude of Eq. 8.5-30 is

$$|H^{oo}(e^{j\omega T})| = \frac{1}{[1+2\alpha(1+\alpha)(1-\cos\omega T)]^{1/2}} \tag{8.5-31}$$

and the phase shift is

$$\text{Arg}\,[H^{oo}(e^{j\omega T})] = -\tan^{-1}\left[\frac{\sin\omega T}{\cos\omega T - \alpha/(1+\alpha)}\right] \tag{8.5-32}$$

In order to compare the performance of the circuit of Fig. 8.5-5 with the circuit of Fig. 8.5-3, we must appropriately choose the values of α and T_c. One of several methods used for making this comparison is to assume that ω_1 of Eq. 8.5-15 is much less than $\omega_c = 1/(2\pi T_c)$. In this case, z of Eq. 8.5-27 can be replaced by

$$z = e^{j\omega T} \simeq 1 + j\omega T \tag{8.5-33}$$

to get

$$H^{oo}(e^{j\omega T}) \simeq \frac{1}{j\omega(1+\alpha)T + 1} \tag{8.5-34}$$

Comparing Eq. 8.5-16 with Eq. 8.5-34 gives

$$\frac{1}{\omega_1} = T(1+\alpha) \tag{8.5-35}$$

The frequency response of Eq. 8.5-30 is plotted in Fig. 8.5-7 for the value of $\omega_c/\omega_1 = 10$, which from Eq. 8.5-35 corresponds to $\alpha = 0.5915$. Also plotted is the frequency response of Eq. 8.5-16 from the circuit of Fig. 8.5-3. For frequencies of ω less than $0.02\omega_c$, the switched capacitor circuit of Fig. 8.5-5*a* is a good approximation of the frequency response of the circuit of Fig. 8.5-3. However, as the frequency increases, the switched capacitor circuit is a very poor approximation. At $\omega/\omega_c = 0.5$, the greatest attenuation of the switched capacitor circuit occurs; and at $\omega = \omega_c$, the magnitude is at the starting value, with a phase shift of $-360°$. The roots of the circuit of as determined from Eq. 8.5-27 are shown in Fig. 8.5-8 and consist of a pole located at $\alpha/(1 + \alpha)$ on the positive real axis. To improve the switched capacitor realization of the circuit of Fig. 8.5-3, it is necessary to increase ω_c or, alternatively, reduce ω_1.

At this point, one can begin to use the resistor realization method to replace the resistances of an RC active network. This method has been applied to the filters of Figs. 8.4-11, 8.4-14, and 8.4-15. The disadvantages of this method are that the circuits are very difficult to analyze and they contain floating nodes. *Floating*

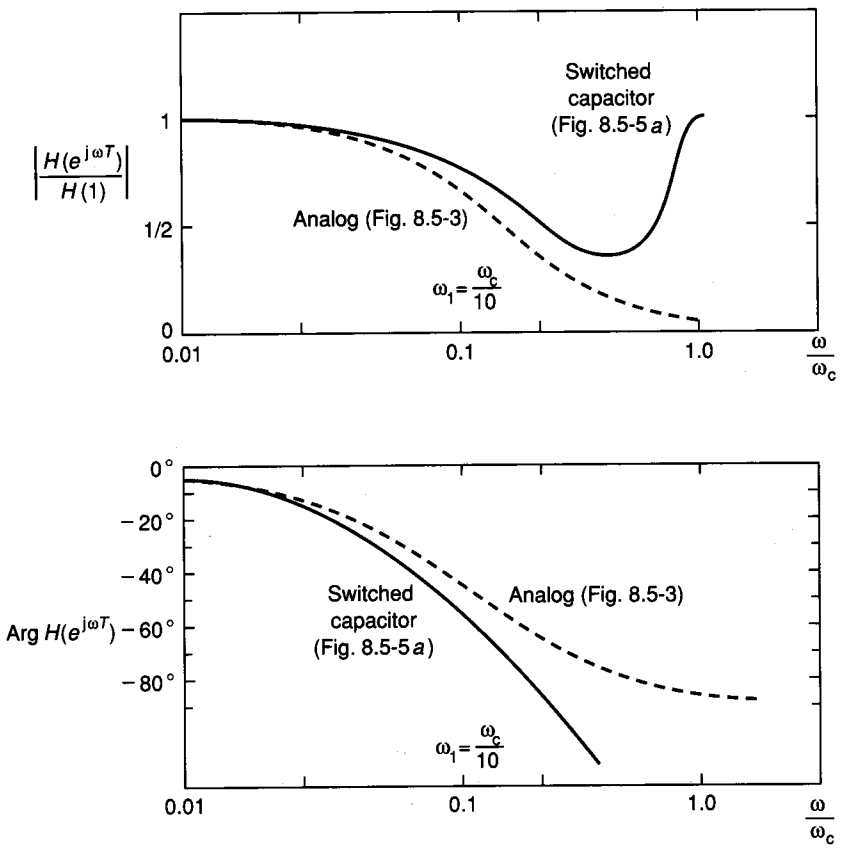


FIGURE 8.5-7
Frequency response of Fig. 8.5-5*a* compared with the frequency response of Fig. 8.5-3.

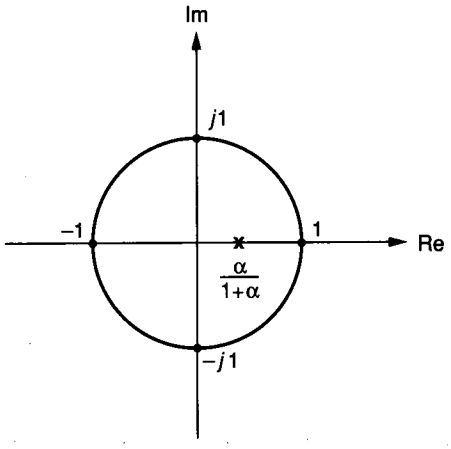


FIGURE 8.5-8
Roots of Fig. 8.5-5*a*.

nodes are nodes that are not connected to a voltage source or a virtual ground. Floating nodes cause a susceptibility to parasitic capacitance as well as complicate the analysis. Examples of floating nodes are nodes A and B in Fig. 8.4-11*a* and node A in Fig. 8.4-11*b*. Figure 8.4-11*c* has no floating nodes and thus is suitable for the resistor simulation approach. Because of these reasons, the resistor simulation method is restricted to simple configurations. The following two methods provide better and easier methods of realizing switched capacitor filters.

8.5.2 Passive RLC Prototype Switched Capacitor Filters

One of the more useful methods of synthesizing filters using switched capacitor networks is based on the realization of RLC ladder networks. Since the integrator is an important part of this method, we shall consider the implementation of switched capacitor integrators first. An inverting analog integrator is shown in Fig. 8.5-9. The transfer function can be found as

$$H(s) = \frac{V_2(s)}{V_1(s)} = \frac{-1}{sR_1C_2} = \frac{-1}{s\tau_0} = \frac{-\omega_0}{s} \tag{8.5-36}$$

where τ_0 is the time constant of the integrator. The transfer function magnitude of the inverting integrator is given as

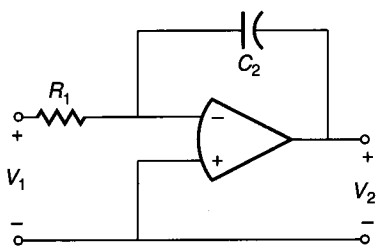


FIGURE 8.5-9
An inverting continuous-time integrator.

$$|H(j\omega)| = \frac{\omega_0}{\omega} \tag{8.5-37}$$

and the phase shift is

$$\text{Arg } H(j\omega) = \frac{\pi}{2} \tag{8.5-38}$$

A noninverting integrator has the same magnitude as the inverting integrator. The phase shift of the noninverting integrator is equal to $-\pi/2$.

A logical approach to a switched capacitor integrator realization is to replace the resistor R_1 of Fig. 8.5-9 by the parallel switched capacitor realization of Fig. 8.5-1*a*. The result is shown in Fig. 8.5-10*a* and is called the parallel switched capacitor integrator. Figure 8.5-10*b* shows the clock sequence for the switched capacitor integrator. During the odd phase periods, the charge on C_2 is constant. An equivalent circuit to Fig. 8.5-10*a* is shown in Fig. 8.5-10*c* for the even phase period. The charge left on C_2 at $t = (n - \frac{1}{2})T$, Q_L, is

$$Q_L^e(n - \frac{1}{2}) = C_2 V_2^e(n - \frac{1}{2}) \tag{8.5-39}$$

The charge on C_2 during the odd period, Q_M, is

$$Q_M^o(n - 1) = C_2 V_2^o(n - 1) \tag{8.5-40}$$

The charge that will be contributed to C_2 from C_1 during the even phase period, Q_C, is

$$Q_C^o(n - 1) = -C_1 V_1^o(n - 1) \tag{8.5-41}$$

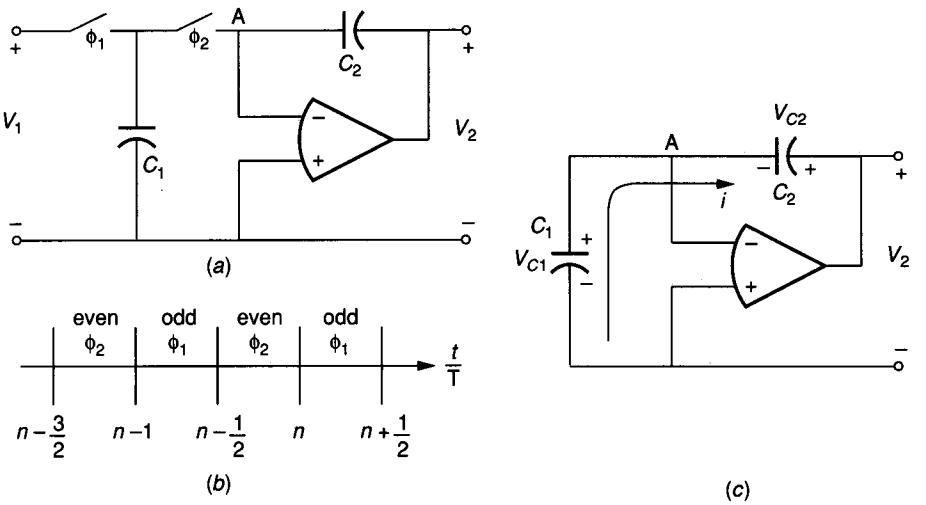


FIGURE 8.5-10
(*a*) Parallel switched capacitor inverting integrator, (*b*) Clock sequence, (*c*) Equivalent circuit during the ϕ_2 phase period.

Charge conservation techniques applied to node A of Fig. 8.5-10*c* result in

$$Q_L^e(n - \frac{1}{2}) = Q_M^o(n - 1) + Q_C^o(n - 1) \tag{8.5-42}$$

Making the substitutions of Eqs. 8.5-39 through 8.5-41 into Eq. 8.5-42 results in

$$C_2 V_2^e(n - \frac{1}{2}) = C_2 V_2^o(n - 1) - C_1 V_1^o(n - 1) \tag{8.5-43}$$

During the odd phase, the charge on C_2 does not change, so that

$$V_2^o(n) = V_2^e(n - \frac{1}{2}) \tag{8.5-44}$$

Combining Eqs. 8.5-43 and 8.5-44 results in

$$C_2 V_2^o(n) = C_2 V_2^o(n - 1) - C_1 V_1^o(n - 1) \tag{8.5-45}$$

Applying the transformation of Eq. 8.5-25 to Eq. 8.5-45 results in the desired z-domain transfer function

$$C_2 V_2(z) = C_2 z^{-1} V_2^o(z) - C_1 z^{-1} V_1^o(z) \tag{8.5-46}$$

This can be expressed as

$$H^{oo}(z) = \frac{V_2^0(z)}{V_1^0(z)} = -\frac{C_1}{C_2}\left(\frac{z^{-1}}{1 - z^{-1}}\right) \tag{8.5-47}$$

$H^{oe}(z)$ can be found by multiplying Eq. 8.5-47 by $z^{-1/2}$. $H^{oo}(z)$ of Eq. 8.5-47 and the corresponding $H^{oe}(z)$ are sometimes called the type *I* direct-transform discrete integrator and the type *I* lossless integrator, respectively.[43–45]

The frequency response of the circuit of Fig. 8.5-10*a* can be found by replacing z by $e^{j\omega T}$ in Eq. 8.5-47 to get

$$H^{oo}(e^{j\omega T}) = -\frac{C_1}{C_2}\left(\frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\right) \tag{8.5-48}$$

If we define $\omega_o = C_1/(TC_2)$, then Eq. 8.5-48 can be expressed as

$$H^{oo}(e^{j\omega T}) = -\frac{\omega_o}{j\omega}\left[\frac{\omega T/2}{\sin(\omega T/2)}\right]\exp(-j\omega T/2) \tag{8.5-49}$$

Thus, the magnitude and phase response of Eq. 8.5-49 can be expressed as

$$|H^{oo}(e^{j\omega T})| = \frac{\omega_o}{\omega}\left[\frac{\omega T/2}{\sin(\omega T/2)}\right] \tag{8.5-50}$$

and

$$\text{Arg } H^{oo}(e^{j\omega T}) = \frac{\pi}{2} - \left[\frac{\omega T}{2}\right] \tag{8.5-51}$$

We observe from Eqs. 8.5-50 and 8.5-51 that as ωT approaches zero, these equations approach Eqs. 8.5-37 and 8.5-38, respectively. Consequently, the terms

TABLE 8.5-1
Magnitude and phase (delay) errors in switched capacitor integrators versus normalized frequency

Normalized frequency f/f_c	Error in gain constant magnitude	Error in phase from ideal 90°
0.00	0.00%	0°
0.05	0.41%	9°
0.10	1.66%	18°
0.15	3.80%	27°
0.20	6.90%	36°
0.25	11.07%	45°
0.30	16.50%	54°
0.35	23.41%	63°
0.40	32.13%	72°
0.45	43.13%	81°
0.50	57.08%	90°

in the bracketed portions of Eqs. 8.5-50 and 8.5-51 can be considered magnitude and phase error terms. The effects of these error terms are shown in Table 8.5-1.

A noninverting switched capacitor integrator is shown in Fig. 8.5-11. It can be observed that C_1 is charged by V_1 in one direction and then reversed before it is discharged into C_2. The result is exactly the same transfer function as Eq. 8.5-47 except there is no minus sign. The phase shift is given as

$$\text{Arg } H^{oo}(e^{j\omega T}) = -\frac{\pi}{2} - \left[\frac{\omega T}{2}\right] \tag{8.5-52}$$

Consequently, the magnitude and phase errors given in Table 8.5-1 are also appropriate for the noninverting switched capacitor integrator.

Figure 8.5-11 has a very important property not found in any of the switched capacitor circuits previously considered in this section. This property is called *stray insensitivity*. In reality, every node in a circuit has some stray capacitance to ground. These capacitances are represented by C_A and C_B in Fig. 8.5-11. During the ϕ_1 phase, C_B is discharged and C_A is charged by the voltage source, V_1.

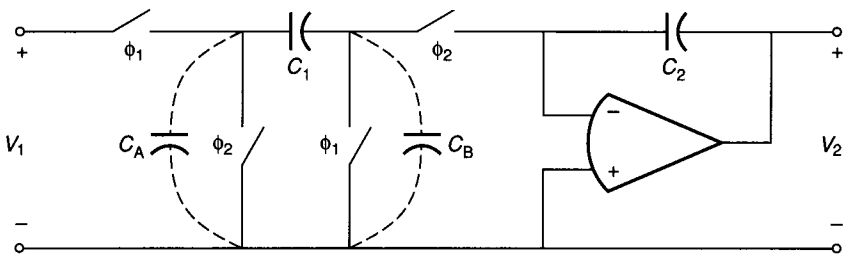


FIGURE 8.5-11
A stray-insensitive, noninverting switched capacitor integrator.

During the ϕ_2 phase, an uncharged C_B is paralleled with a virtual ground, and C_A is discharged to ground. Neither C_A nor C_B has any direct influence on the charge on C_1, which is transferred to C_2 during the ϕ_2 phase period. Consequently, Fig. 8.5-11 is insensitive to stray capacitances. Repeating this procedure with a stray capacitance in Fig. 8.5-10*a* will show that the charge transferred from C_1 to C_2 during the ϕ_2 phase period will be influenced by stray capacitances. Most commercial switched capacitor circuits use building blocks that are stray insensitive.

The stray-insensitive, inverting switched capacitor integrator of Fig. 8.5-12 will complete our repertoire of switched capacitor integrators. Although there are many other possible integrators, these will be sufficient for our purposes in this section. The transfer function of this integrator can be found by writing the expressions for the various charges that are being transferred. The clock phasing of Fig. 8.5-10*b* will be used for Fig. 8.5-12. The charge left on C_2 at the end of the even phase period is

$$Q_L^e\left(n - \frac{1}{2}\right) = C_2 V_2^e\left(n - \frac{1}{2}\right) \tag{8.5-53}$$

The charge on C_2 during the previous odd phase is

$$Q_M^o(n - 1) = C_2 V_2^o(n - 1) \tag{8.5-54}$$

The charge transferred to C_2 by the charging of C_1 to $V_1(n - \frac{1}{2})$ during the even phase is

$$Q_C^e\left(n - \frac{1}{2}\right) = -C_1 V_1^e\left(n - \frac{1}{2}\right) \tag{8.5-55}$$

Using charge conservation techniques gives

$$Q_L^e\left(n - \frac{1}{2}\right) = Q_M^o(n - 1) + Q_C^e\left(n - \frac{1}{2}\right) \tag{8.5-56}$$

Substituting Eqs. 8.5-53 through 8.5-55 into Eq. 8.5-56 results in

$$C_2 V_2^e\left(n - \frac{1}{2}\right) = C_2 V_2^o(n - 1) - C_1 V_1^e\left(n - \frac{1}{2}\right) \tag{8.5-57}$$

If we assume the input is from a sample-and-hold circuit, then $V_1^e(n - \frac{1}{2}) = V_1^o(n)$.

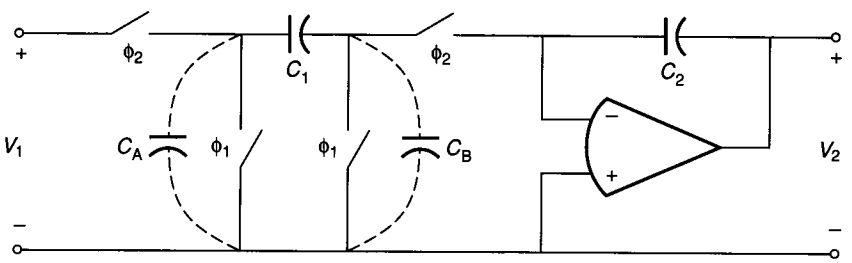


FIGURE 8.5-12
A stray-insensitive, inverting switched capacitor integrator.

During ϕ_1, $V_2^e(n-\frac{1}{2}) = V_2^o(n)$. Substituting these relations into Eq. 8.5-57 gives

$$C_2V_2^o(n) = C_2V_2^o(n-1) - C_1V_1^o(n) \tag{8.5-58}$$

Using Eq. 8.5-25 we obtain the desired transfer function for the circuit of Fig. 8.5-12 as

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = -\frac{C_1}{C_2}\left(\frac{1}{1-z^{-1}}\right) \tag{8.5-59}$$

We see that for the inverting, stray-insensitive switched capacitor integrator, there is no delay in the forward path from the input to the output.

The frequency response of the circuit of Fig. 8.5-12 can be found by replacing z by $e^{j\omega T}$. Making this replacement and multiplying through the numerator and denominator by $e^{j\omega T}$ gives

$$H^{oo}(e^{j\omega T}) = -\frac{C_1}{C_2}\left(\frac{e^{j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\right) \tag{8.5-60}$$

We note that Eq. 8.5-60 is identical to Eq. 8.5-48 except for the minus sign in the numerator exponential. This means that the magnitude response of the circuit of Fig. 8.5-12 is given by Eq. 8.5-50 and the phase shift by Eq. 8.5-51, except that the phase error term is positive. The integrator error terms given in Table 8.5-1 are also applicable to the integrator of Fig. 8.5-12. The frequency response of various types of integrators is illustrated in Fig. 8.5-13 for a ratio of ω_o to ω_c of 0.1. The integrators we have just discussed are sufficient to implement practical switched capacitor filters. A more complete presentation, concerning other realizations and details, can be found in the literature.

Next we shall use the switched capacitor integrator to realize the passive RLC prototype ladder filter. Consider the fifth-order low-pass filter shown in Fig. 8.5-14. This filter is similar to the type that was considered in Sec. 8.4. The subscript n on the components indicates prototype or normalized values. The first step is to select the electrical variables that will be used to describe the circuit. Each component is characterized by a current, I_i, and a voltage, V_i, one of which can be expressed as the integration of the other variable. The integrand variable is current for an inductor and voltage for a capacitor. The integrand variables I_1, V_2, I_3, V_4, and I_5 are shown in Fig. 8.5-14.

The next step is to use these integrand variables to write a set of s-domain equations that describe the circuit. The selection of the integrand variables allows the realization using integrators. For the variable I_1, we may write the loop equation:

$$V_{in} - I_1(R_{0n} + sL_{1n}) - V_2 = 0 \tag{8.5-61}$$

Using the concept of a "voltage analog" of current, we express Eq. 8.5-61 as

$$V_{in} - \frac{V_1'}{R}(R_{0n} + sL_{1n}) - V_2 = 0 \tag{8.5-62}$$

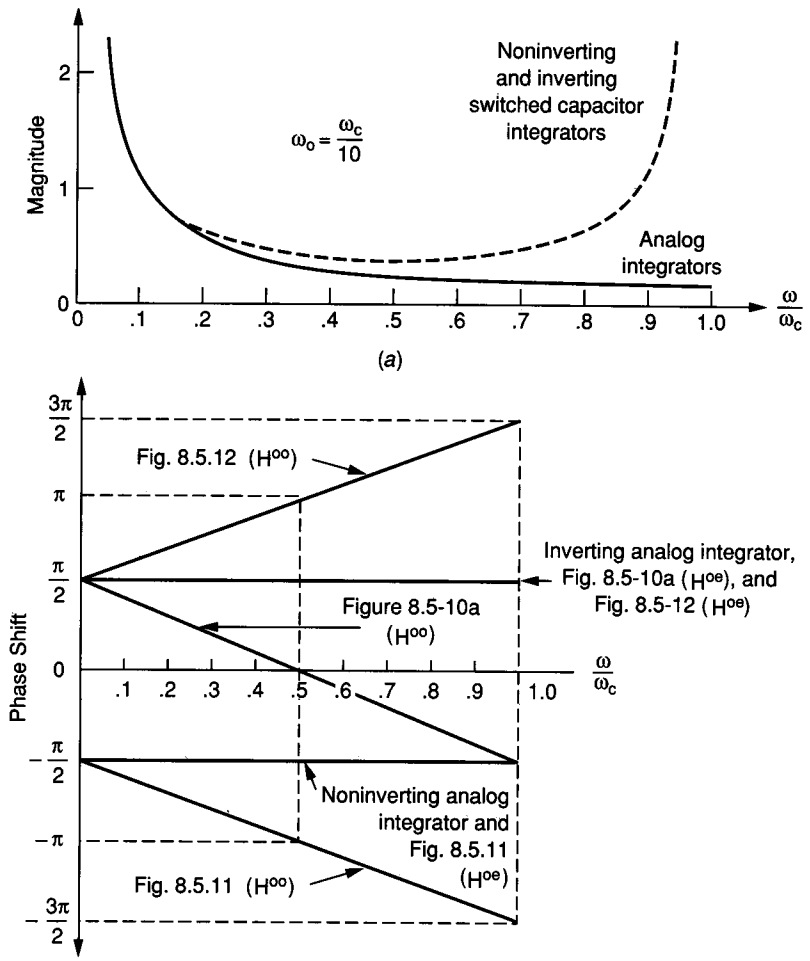


FIGURE 8.5-13
(*a*) Magnitude response of various switched capacitor integrators compared with a continuous-time integrator when $\omega_0/\omega_c = 1/10$, (*b*) Phase response of various switched capacitor and continuous-time integrators.

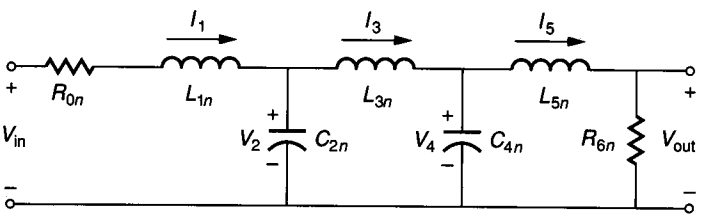


FIGURE 8.5-14
A fifth-order, low-pass, passive prototype filter.

where the voltage analog of I_1 is designated as V_1' and is defined as

$$V_1' = RI_1 \tag{8.5-63}$$

where R is an arbitrary scaling resistance (normally unity). Solving for V_1' of Eq. 8.5-62 results in

$$V_1' = \frac{R}{sL_{1n}}\left[V_{in} - V_2 - \left(\frac{R_{0n}}{R}\right)V_1'\right] \tag{8.5-64}$$

This expression can be implemented by an integrator that sums V_{in}, $-V_2$, and $-(R_{0n}/R)V_1'$. The fact that the output is in part equal to the integral of itself indicates nothing more than a damped integrator. Moving on to the next variable, V_2, we sum currents to get

$$I_1 - I_3 - sC_{2n}V_2 = 0 \tag{8.5-65}$$

Solving for the variable V_2 using voltage analogs of I_1 and I_2, we get

$$V_2 = \frac{1}{sRC_{2n}}[V_1' - V_3'] \tag{8.5-66}$$

The equation describing the variable I_3 can be written from the loop consisting of C_{2n}, L_{3n}, and C_{4n} as

$$V_2 - sL_{3n}I_3 - V_4 = 0 \tag{8.5-67}$$

Solving for the voltage analog of I_3 gives

$$V_3' = \frac{R}{sL_{3n}}(V_2 - V_4) \tag{8.5-68}$$

Next, the equation involving V_4 can be found by a nodal equation written as

$$I_3 - sC_{4n}V_4 - I_5 = 0 \tag{8.5-69}$$

Again using voltage analogs for I_3 and I_5 gives,

$$V_4 = \frac{1}{sRC_{4n}}(V_3' - V_5') \tag{8.5-70}$$

Finally, a loop equation involving C_{4n}, L_{5n}, and R_{6n} will be used to describe the variable I_5:

$$V_4 - sL_{5n}I_5 - I_5R_{6n} = 0 \tag{8.5-71}$$

which can be expressed in terms of voltage analogs as

$$V_5' = \frac{R}{sL_{5n}}\left(V_4 - \frac{R_{6n}}{R}V_5'\right) \tag{8.5-72}$$

However, we would prefer to have the variable V_{out} rather than V_5'. Because $V_{out} = (R_{6n}/R)V_5'$, we express Eq. 8.5-72 as

$$V_{out} = \frac{R_{6n}}{sL_{5n}}(V_4 - V_{out}) \tag{8.5-73}$$

The method of generating these equations should be obvious. Starting with Eq. 8.5-61, the equations are a succession of loop equations followed by a node equation. The substitution of V_{out} for V_5' was simply by application of Ohm's law. This method can be used for practically all low-pass ladder RLC filters.

The next step is the realization of Eqs. 8.5-64, 8.5-66, 8.5-68, 8.5-70, and 8.5-73. Equation 8.5-64 represents a summing integrator with inputs of V_{in}, V_2, and V_1' and output V_1'. It can be realized by switched capacitor circuits by combining the ideas of Figs. 8.5-11 and 8.5-12. The circuit of Fig. 8.5-15*a* results as a proposed realization of Eq. 8.5-64. Note that the right-hand switches have been combined to reduce the number of switches. Using the results of Eqs. 8.5-47 and 8.5-59, we write

$$V_1'(z) = \left(\frac{1}{1 - z^{-1}}\right)[\alpha_{11}z^{-1}V_{in}(z) - \alpha_{21}V_2(z) - \alpha_{31}V_1'(z)] \quad (8.5\text{-}74)$$

Next the high sampling approximation is made so that $1 - z^{-1}$ is approximately sT and z^{-1} is approximately $1 - sT \simeq 1$. Thus, Eq. 8.5-74 becomes

$$V_1'(s) \simeq \frac{1}{sT}[\alpha_{11}V_{in}(s) - \alpha_{21}V_2(s) - \alpha_{31}V_1'(s)] \quad (8.5\text{-}75)$$

Before Eq. 8.5-75 can be equated with Eq. 8.5-64, it must be frequency-denormalized. This is because Eq. 8.5-64 is based on a low-pass normalized prototype, having a cutoff frequency of 1 rps. This denormalization is accomplished by replacing the clock period, T, in Eq. 8.5-75 by

$$T = \frac{T_n}{\Omega_n} \quad (8.5\text{-}76)$$

where T_n is the normalized clock period and Ω_n is defined as

$$\Omega_n = \frac{\text{Actual cutoff frequency in rps}}{\text{Normalized cutoff frequency rps}} \quad (8.5\text{-}77)$$

Therefore, Eq. 8.5-75 can be written as

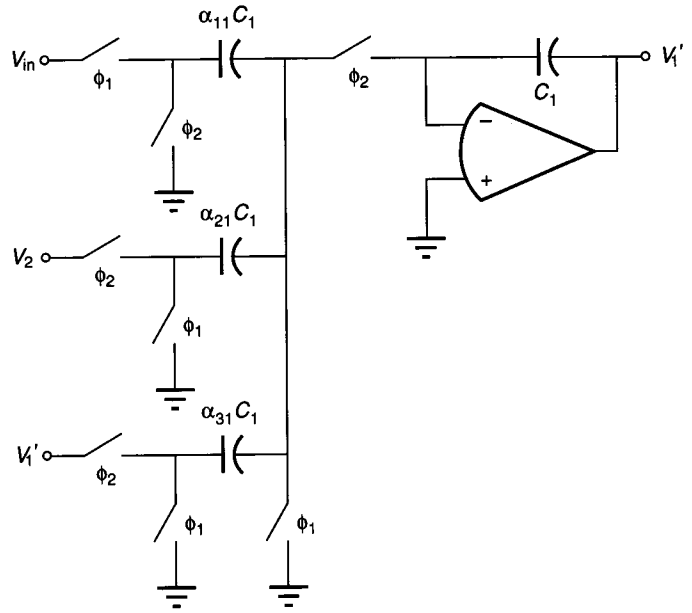
$$V_1'(s) \simeq \frac{1}{sT_n}[\alpha_{11}V_{in}(s) - \alpha_{21}V_2(s) - \alpha_{31}V_1'(s)] \quad (8.5\text{-}78)$$

Equating Eq. 8.5-78 and Eq. 8.5-64 results in the design of the first integrator of Fig. 8.5-15. These results are

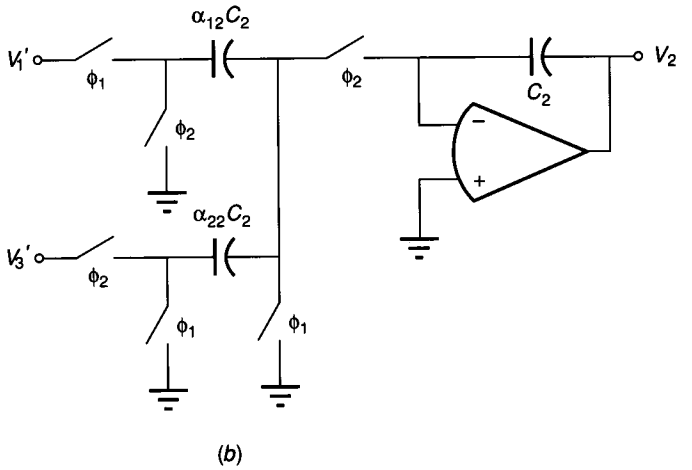
$$\alpha_{11} = \alpha_{21} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n T}{L_{1n}} = \frac{R\Omega_n}{L_{1n}f_c} \quad (8.5\text{-}79)$$

and

$$\alpha_{31} = \frac{R_{0n}T_n}{L_{1n}} = \frac{R_{0n}\Omega_n T}{L_{1n}} = \frac{R_{0n}\Omega_n}{L_{1n}f_c} \quad (8.5\text{-}80)$$

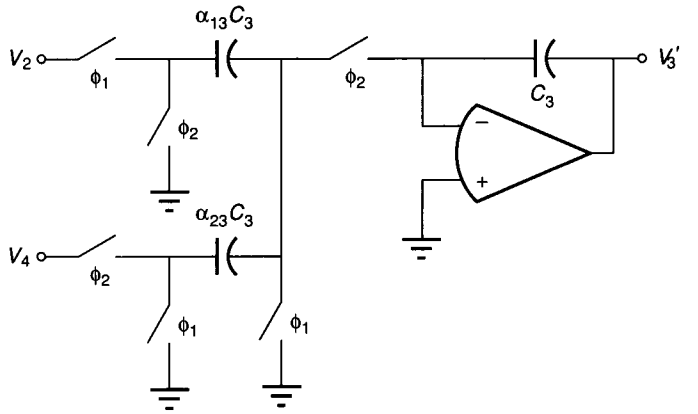


(*a*)

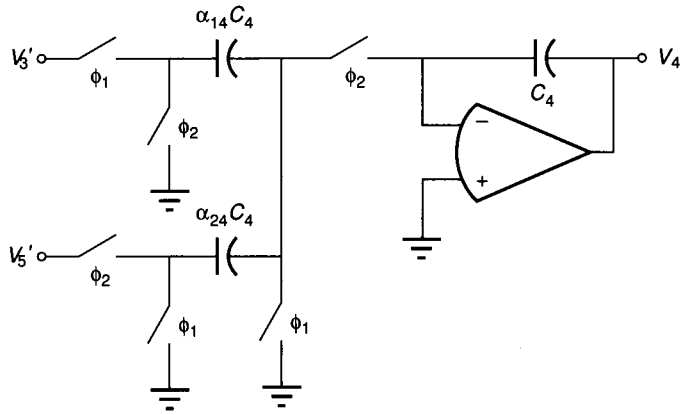


(*b*)

FIGURE 8.5-15
Stage-by-stage realization of Fig. 8.5-14: (*a*) Input stage, (*b*) Second stage, (*c*) Third stage, (*d*) Fourth stage, (*e*) Output stage.



(c)



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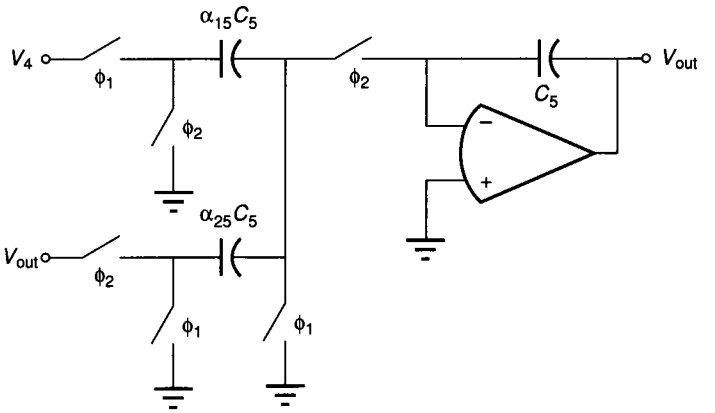

(e)

FIGURE 8.5-15
(*Continued*)

Next we repeat this process for the variable V_2 of Eq. 8.5-66. Figure 8.5-15*b* is a realization of Eq. 8.5-66. Using the high sampling approximation allows us to write the output of this circuit as

$$V_2(s) \simeq \frac{1}{sT_n}[\alpha_{12}V_1'(s) - \alpha_{22}V_3'(s)] \tag{8.5-81}$$

employing the same approach that was used to get Eq. 8.5-78. Equating Eq. 8.5-66 with Eq. 8.5-81 results in

$$\alpha_{12} = \alpha_{22} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n T}{RC_{2n}} = \frac{\Omega_n}{RC_{2n}f_c} \tag{8.5-82}$$

The realizations for Eqs. 8.5-68, 8.5-70, and 8.5-73 are identical in concept to that of Eq. 8.5-66. Figure 8.5-15 shows the switched capacitor realizations of these equations. Using the same approach as before, we may express the design equations of Fig. 8.5-15*c* as

$$\alpha_{13} = \alpha_{23} = \frac{RT_n}{L_{3n}} = \frac{R\Omega_n T}{L_{3n}} = \frac{R\Omega_n}{f_c L_{3n}} \tag{8.5-83}$$

and Fig. 8.5-15*d* as

$$\alpha_{14} = \alpha_{24} = \frac{T_n}{RC_{4n}} = \frac{\Omega_n T}{RC_{4n}} = \frac{\Omega_n}{RC_{4n}f_c} \tag{8.5-84}$$

and Fig. 8.5-15*e* as

$$\alpha_{15} = \alpha_{25} = \frac{R_{6n}T_n}{L_{5n}} = \frac{R_{6n}\Omega_n}{L_{5n}f_c} \tag{8.5-85}$$

Equations 8.5-79, 8.5-80, and 8.5-82 through 8.5-85 permit the design of the filter in Fig. 8.5-14 according to a given set of specifications. When the various integrators of Fig. 8.5-15 are combined, the filter realization is that shown in Fig. 8.5-16. The filter structure consists of coupled internal feedback loops containing two integrators each. In order to achieve minimum delay around each loop, it is necessary that each integrator be sampled by the next integrator as soon as the new sample is available. Therefore, in one clock period, the signal circulates around the internal feedback loop. The clock scheme indicated will avoid a $T/2$ delay, which would create a difference between the actual realization and that desired. The following example illustrates the application of the preceding approach to the switched capacitor realization of a low-pass filter.

Example 8.5-1. A switched capacitor realization of a fifth-order low-pass Chebyshev filter. A fifth-order low-pass Chebyshev filter with a 1 dB ripple in the passband is to be designed for a cutoff frequency of 1000 Hz. The structure of Fig. 8.5-16 based upon the passive prototype of Fig. 8.5-14 is to be used. Find the switched capacitor realization for this filter if the clock frequency is 100 kHz.

Solution. The normalized values of the RLC passive prototype that satisfies the specifications are $R_{0n} = 1\ \Omega, L_{1n} = 2.1349$ H, $C_{2n} = 1.0911$ F, $L_{3n} = 3.009$ H,

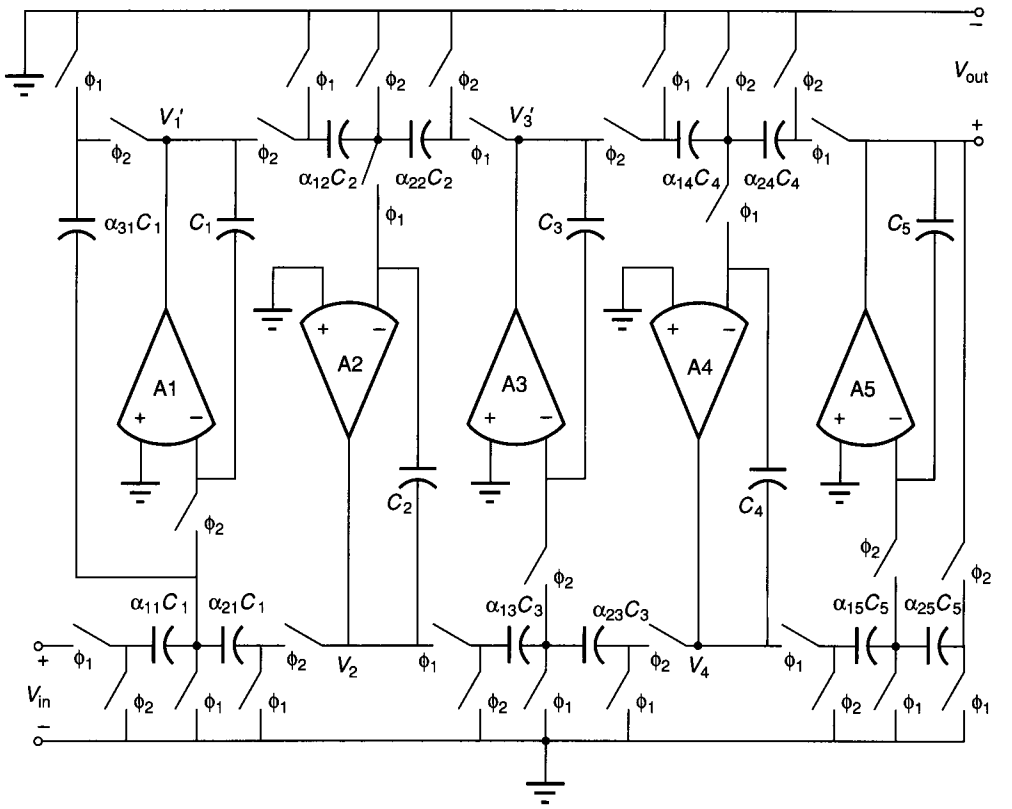

FIGURE 8.5-16
Switched capacitor realization of Fig. 8.5-14.

$C_{4n} = 1.0911$ F, $L_{5n} = 2.1349$ H, and $R_{6n} = 1\ \Omega$. These values are found from tabulations in the literature.[26,31] Using the preceding equations with $\Omega_n = 2000\pi$, we get

$$\alpha_{11} = \alpha_{21} = \alpha_{31} = 0.02943$$

$$\alpha_{12} = \alpha_{22} = 0.05759$$

$$\alpha_{13} = \alpha_{23} = 0.02094$$

$$\alpha_{14} = \alpha_{24} = 0.05759$$

$$\alpha_{15} = \alpha_{25} = 0.2943$$

One item of concern in switched capacitor filters is the total capacitance required in the realization. Large capacitor ratios are undesirable because of the loss of relative accuracy and increased area. If α_{ij} of the jth stage is less than unity, then $\alpha_{ij} C_j$ will be less than C_j. If we equate the smallest capacitor, $\alpha_{ij} C_j$, to a unity capacitance C_{uj}, then we may find the total relative capacitance of a stage by summing C_{uj} with all other capacitors being divided by α_{ij}. In the

preceding example if we let $C_{u1} = C_{u2} = C_{u3} = C_{u4} = C_{u5} = C_u$, then the total capacitance is $155.596C_u$. If C_u is selected as 1 pF, then 155.596 pF of capacitance is required for the filter. It is important to keep this number as small as possible if the filter is to be integrated. Reduction of the clock frequency will always reduce this number, but at the expense of not satisfying the high sampling approximation at the higher signal frequencies.

This design method starting from the low-pass, passive RLC prototype is general and can be applied to all types of symmetrical filters. Elliptic filters can also be synthesized by replacing the L cutsets or C loops with controlled sources.[26] The result requires a nonintegrated input to the integrator, which can be accomplished by an unswitched capacitor. Bandpass, high-pass, and band-elimination filters can be synthesized using the transformations of Fig. 8.4-13 applied to the low-pass, passive RLC prototype. The bandpass is realized by a second-order bandpass structure with the ability to sum multiple inputs. Such a structure could be derived from the circuit of Fig. 8.4-15*c* if the integrators are replaced by the appropriate combinations of the integrators of Fig. 8.5-11 and Fig. 8.5-12 with summing inputs.

The high-pass switched capacitor filter realizations present more of a challenge, although they use the same approach as that used for low-pass switched capacitor filters. The reason for the additional complexity is that the low-pass to high-pass transformation applied to the low-pass, passive RLC prototype will result in differentiators if the same integrand variables used for low-pass filters are selected. It is necessary to reselect the variables so that the equations can be realized with integrators.

Band-elimination filters are also possible using this approach. One first transforms the low-pass, passive RLC prototype to a band-elimination form. The switched capacitor realization will require a second-order structure with the ability to sum both integrated and nonintegrated inputs. For more information on the design of switched capacitor circuits from general symmetrical filters, the reader should consult Chapter 4 of the text *Switched Capacitor Circuits*.[26]

8.5.3 *Z*-Domain Synthesis Techniques

In many cases, the designer is given the filter approximation in the z-domain rather than the s-domain. In this case, the realization of the filter takes place directly in the z-domain. Various methods of arriving at $H(z)$ given $H(s)$ are well developed and can be found elsewhere. Irrespective of how the tranformation is made, the starting point of z-domain synthesis techniques is

$$H(z) = \frac{a_0 + a_1 z + a_2 z^2 + \ldots + a_{m-1} z^{m-1} + a_m z^m}{b_0 + b_1 z + b_2 z^2 + \ldots + b_{n-1} z^{n-1} + b_n z^n} \tag{8.5-86}$$

One approach is to convert Eq. 8.5-86 into a signal flow diagram consisting of amplifiers, delays, and summers.[43] Another approach is to break Eq. 8.5-86 into products of first- and second-order terms. An example of how the first approach works is illustrated by Fig. 8.5-17*a*. This is a general building block that consists of a combination of a stray-insensitive noninverting and inverting

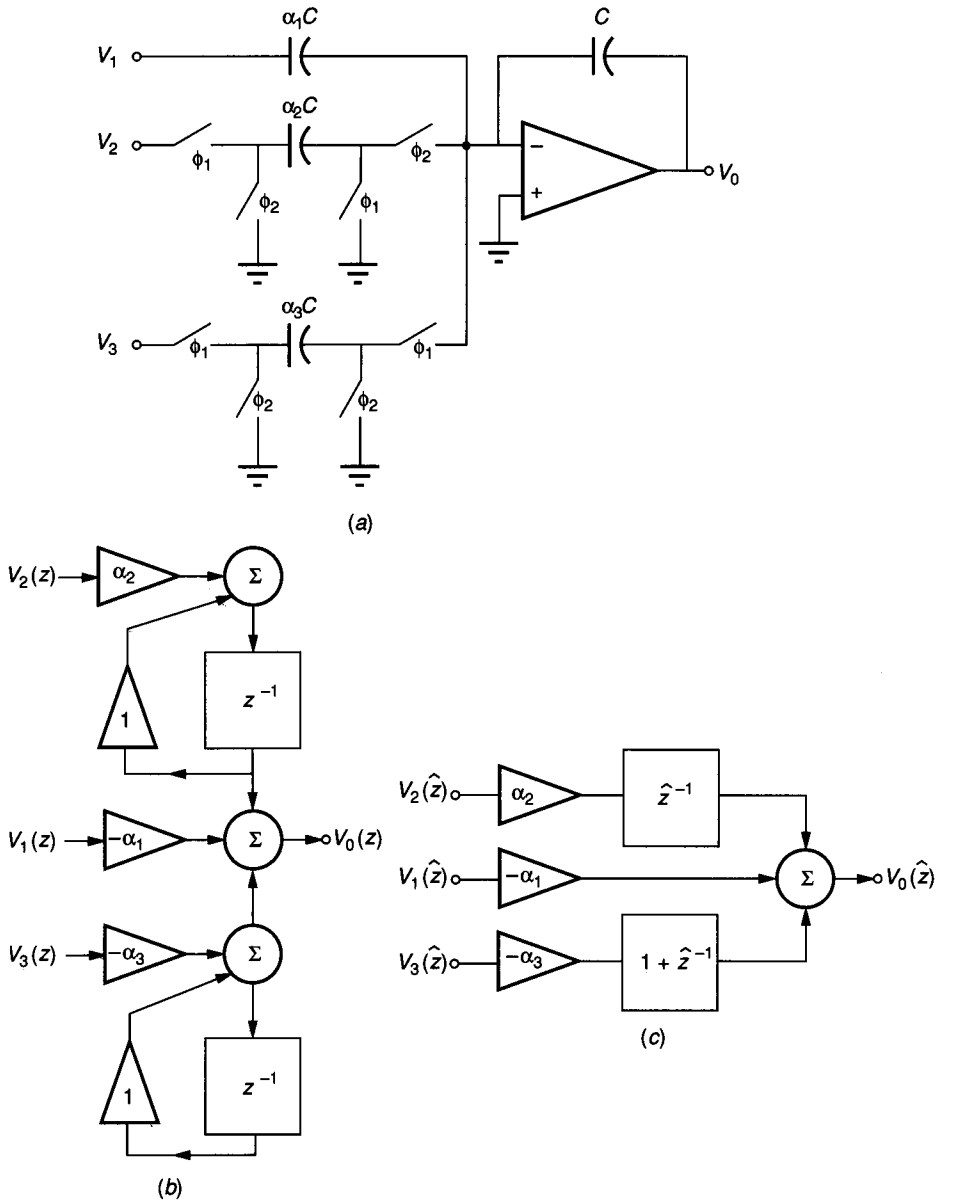

FIGURE 8.5-17
General building block: (*a*) SC circuit, (*b*) z-domain block diagram, (*c*) $\hat{z}$-domain block diagram.

integrators and an inverting amplifier. Note that V_1, V_2, and V_3 can be connected at arbitrarily different points or to the same node to provide more flexibility for different structures. This general building block can provide different paths, including local feedback, overall feedback, and feedforward. Figure 8.5-17*b* shows the flow diagram of Fig. 8.5-17*a* in terms of z^{-1} delay elements. A change of the z-domain variable is introduced, which simplifies the flow diagram and improves the sensitivity performance of the various realizations.[46] This transformation is

$$\hat{z} = z - 1 \tag{8.5-87}$$

Figure 8.5-17*c* gives the $\hat{z}$ flow diagram of the circuit of Fig. 8.5-17*a*. The output of the circuit of Fig. 8.5-17*c*, $V_o(\hat{z})$, is given by

$$V_o(\hat{z}) = \alpha_2 \hat{z}^{-1} V_2(\hat{z}) - \alpha_1 V_1(\hat{z}) - \alpha_3(1 + \hat{z}^{-1}) V_3(\hat{z}) \tag{8.5-88}$$

The transformation used in Eq. 8.5-87 is arbitrary. The design procedure outlined in the following could equally well be applied to $H(z)$. Note that Eq. 8.5-88 may be simplified if $V_2(\hat{z}) = V_3(\hat{z})$. Combinations of this general building block can be used to realize various z-domain transfer functions when the transformation of Eq. 8.5-87 is made to Eq. 8.5-86 to get $H(\hat{z})$. When $H(\hat{z})$ is converted to a signal flow diagram, then the synthesis becomes a straightforward procedure. These ideas will be demonstrated for second- and third-order structures, which can be cascaded to obtain a filter of any order in the z-domain.

One popular method of designing higher-order filters is the cascade of first-, second-, and third-order sections.[47,48] Because Fig. 8.5-17*a* represents a first-order filter, we will consider only the second-order (biquad) and third-order (triquad) realizations. The biquad is a fundamental building block for higher-order switched capacitor filters. The biquad flow diagram shown in Fig. 8.5-18 is a versatile structure and is one of many that could be considered. The properties of this structure are (1) the capability of realizing all stable z-domain biquadratic transfer functions, (2) sufficient flexibility to permit small total capacitance with low sensitivity, and (3) freedom from parasitic capacitances.

The general biquad structure is formed by the interconnection of the general building block of Fig. 8.5-17*a*. The biquadratic transfer function of the circuit of Fig. 8.5-18 is given as

$$H(\hat{z}) = \frac{V_{oz}(\hat{z})}{V_i(\hat{z})} = \frac{A_0 + A_1 \hat{z}^{-1} + A_2 \hat{z}^{-2}}{1 + C_1 \hat{z}^{-1} + C_2 \hat{z}^{-2}} \tag{8.5-89}$$

where

$$\begin{aligned} A_0 &= D_0 B_3 - D_3 \\ A_1 &= D_1 - D_3 + D_3 B_0 - D_0 B_1 - D_2 B_3 + D_0 B_3 \\ A_2 &= D_3 B_0 + D_2 B_1 - D_2 B_3 - D_1 B_0 \\ C_1 &= B_2 B_3 - B_0 \\ C_2 &= B_2 B_3 - B_1 B_2 \end{aligned} \tag{8.5-90}$$

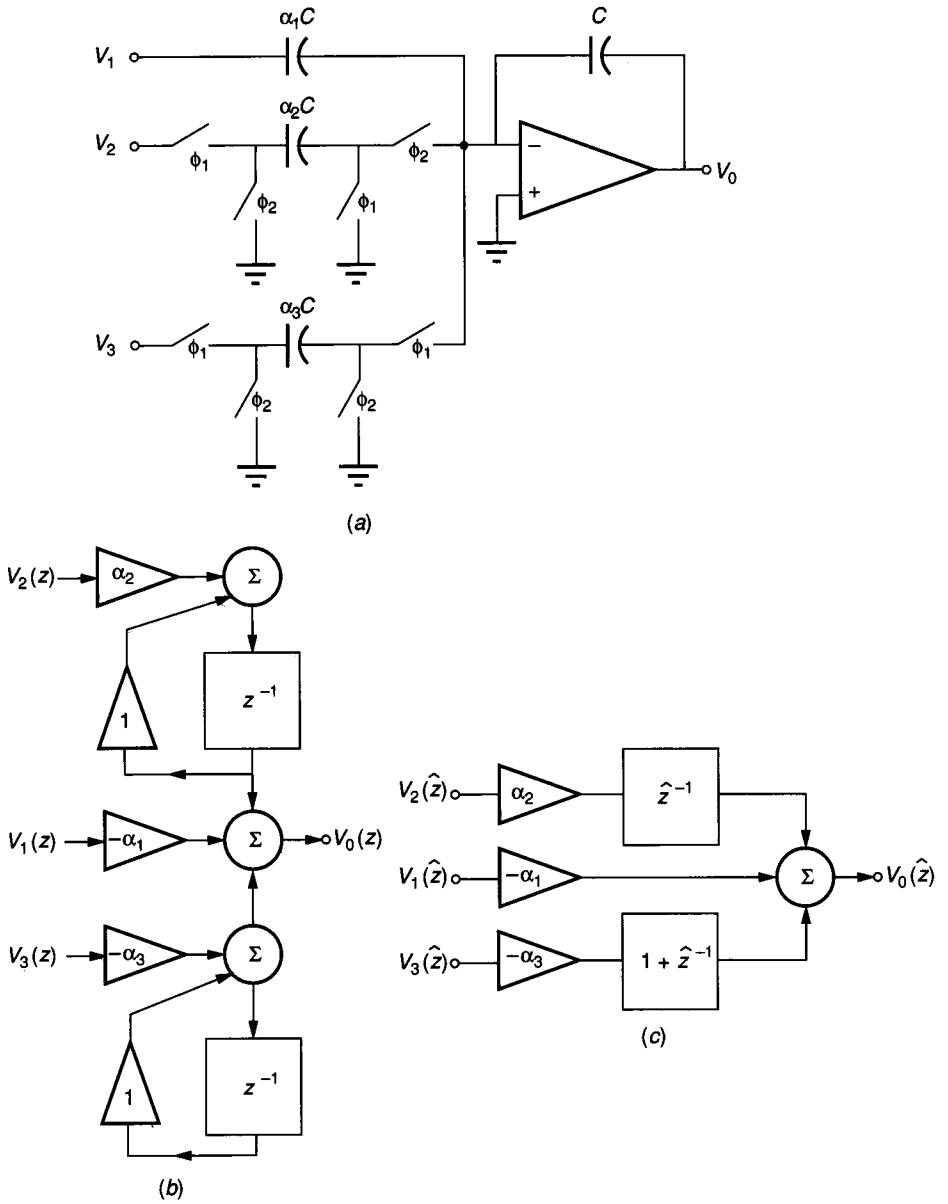

FIGURE 8.5-17
General building block: (*a*) SC circuit, (*b*) z-domain block diagram, (*c*) $\hat{z}$-domain block diagram.

integrators and an inverting amplifier. Note that V_1, V_2, and V_3 can be connected at arbitrarily different points or to the same node to provide more flexibility for different structures. This general building block can provide different paths, including local feedback, overall feedback, and feedforward. Figure 8.5-17*b* shows the flow diagram of Fig. 8.5-17*a* in terms of z^{-1} delay elements. A change of the z-domain variable is introduced, which simplifies the flow diagram and improves the sensitivity performance of the various realizations.[46] This transformation is

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where

$$\begin{aligned} A_0 &= D_0 B_3 - D_3 \\ A_1 &= D_1 - D_3 + D_3 B_0 - D_0 B_1 - D_2 B_3 + D_0 B_3 \\ A_2 &= D_3 B_0 + D_2 B_1 - D_2 B_3 - D_1 B_0 \\ C_1 &= B_2 B_3 - B_0 \\ C_2 &= B_2 B_3 - B_1 B_2 \end{aligned} \tag{8.5-90}$$

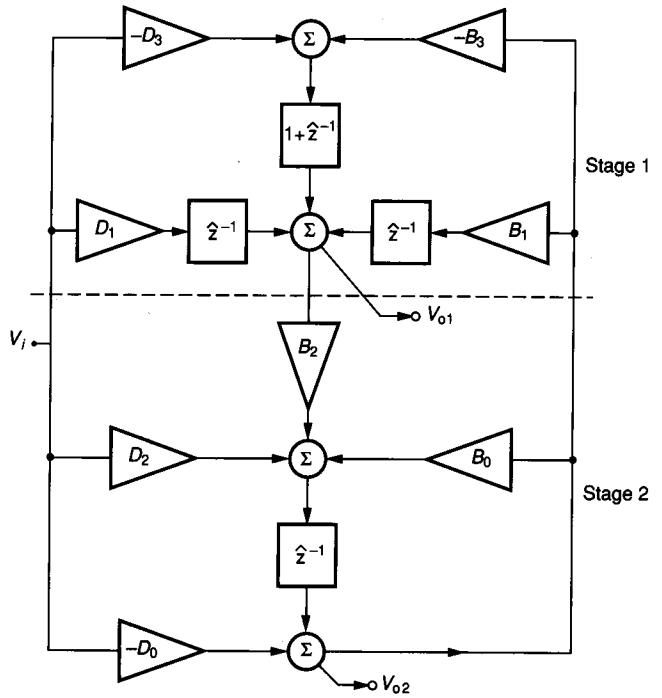


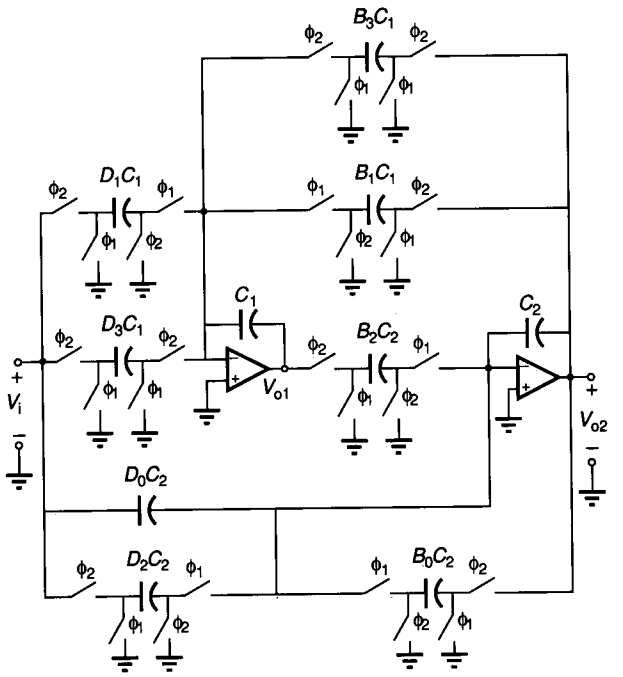
FIGURE 8.5-18
Signal flow diagram of a biquad.

It is observed in Fig. 8.5-18 that B_0 and B_1 are positive-feedback components. If B_0 and B_1 are zero, the filter will be stable from an ideal viewpoint. For nonzero values of B_0 and B_1, the filter will remain stable if B_3 is greater than B_1 and B_0 is less than B_2B_3.

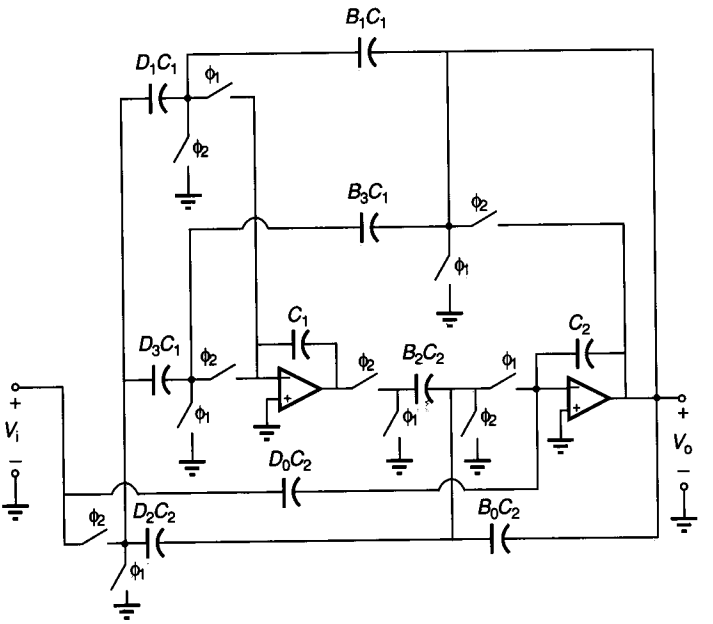
Figure 8.5-19*a* shows a switched capacitor implementation of the flow diagram of Fig. 8.5-18. The two outputs are designated as V_{o1} and V_{o2}. The most general output of this realization is at V_{o2} because each coefficient can be realized independently of the other. The transfer function at V_{o2} is

$$H(\hat{z}) = \frac{V_{o2}(\hat{z})}{V_i(\hat{z})} = \frac{D_0 + (D_3B_2 - D_2)\hat{z}^{-1} + (D_3B_2 - D_1B_2)\hat{z}^{-2}}{1 + (B_2B_3 - B_0)\hat{z}^{-1} + (B_2B_3 - B_1B_2)\hat{z}^{-2}} \tag{8.5-91}$$

Note that the individual Bs and Ds represent a ratio of two capacitors. The circuit can be simplified in a number of ways depending on the actual transfer function required. For instance, if there is a zero at $\hat{z} = -2$ (i.e., $z = 1$), the "bilinearly" equivalent analog-domain zero frequency is at $s = \infty$; and if the zero is neglected, then D_0 becomes zero. The switched capacitor implementation of Fig. 8.5-19*a* with the minimum number of switches is shown in Fig. 8.5-19*b*.



(*a*)



(*b*)

FIGURE 8.5-19
(*a*) Switched capacitor implementation of Fig. 8.5-18, (*b*) Switched capacitor biquad with a minimum number of switches.

Generally, the second-order z-domain transfer function is given in terms of its z-domain roots. A general expression for Eq. 8.5-91 in terms of the roots is

$$H(\hat{z}) = \frac{1 + (2 - 2r_o \cos\theta_o)\hat{z}^{-1} + (1 + r_o^2 - 2r_o \cos\theta_o)\hat{z}^{-2}}{1 + (2 - 2r\cos\theta)\hat{z}^{-1} + (1 + r^2 - 2r\cos\theta)\hat{z}^{-2}} \tag{8.5-92}$$

where the locations of the poles and zeros in the z-plane are at $re^{\pm j\theta}$ and $r_o e^{\pm j\theta_o}$, respectively. Expressions for the root locations in terms of the coefficients are

$$r = [1 - B_1 B_2 + B_0]^{1/2} \tag{8.5-93}$$

$$\cos\theta = \frac{2 - B_2 B_3 + B_0}{2r} \tag{8.5-94}$$

$$r_o = [1 + (D_2 - D_1 B_2)/D_0]^{1/2} \tag{8.5-95}$$

and

$$\cos\theta_o = \frac{2 + (D_2 - D_3 B_2)/D_0}{2r_o} \tag{8.5-96}$$

A possible set of design equations is developed next. The root locations described by r, r_o, θ, and θ_o are assumed to be given. Because there are several extra degrees of freedom, we can arbitrarily choose B_2, B_3, D_2, and D_3. Therefore, the rest of the components can be calculated from

$$B_0 = 2r\cos\theta - 2 + B_2 B_3 \tag{8.5-97}$$

$$B_1 = 0.5[2 - B_2 B_3 + B_0] \tag{8.5-98}$$

$$D_0 = \frac{D_2 - D_3 B_2}{2(r_o \cos\theta_o - 1)} \tag{8.5-99}$$

and

$$D_1 = \frac{D_2 + (1 - r_o^2)D_0}{B_2} \tag{8.5-100}$$

It is observed that the general biquad can be simplified by choosing as many of the capacitor values as possible to be equal to zero. The coefficients of Eq. 8.5-91 are a result of the multiplication and subtraction of several individual capacitor ratios. Thus, the biquad is capable of realizing very small coefficients. However, we must keep in mind that the sensitivity might be inversely proportional to that small difference. Typically, a tradeoff between sensitivities and total capacitance is possible and will be illustrated shortly.

Next, a third-order realization is developed. This structure is useful when the filter has an odd order. Figure 8.5-20*a* shows a general third-order structure in its signal flow diagram form. The transfer function of this structure is

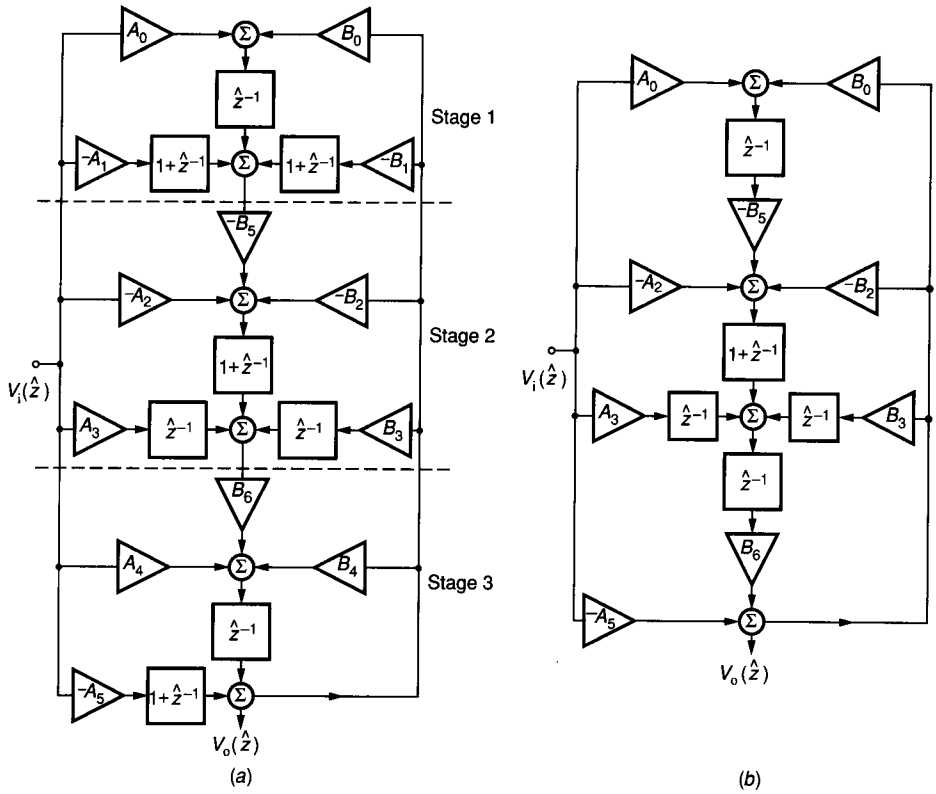


FIGURE 8.5-20
(*a*) General third-order block diagram, (*b*) Simplified third-order block diagram (signal flow graph).

$$H(\hat{z}) = \frac{V_o(\hat{z})}{V_i(\hat{z})} = \frac{\alpha_0 + \alpha_1\hat{z}^{-1} + \alpha_2\hat{z}^{-2} + \alpha_3\hat{z}^{-3}}{1 + \beta_1\hat{z}^{-1} + \beta_2\hat{z}^{-2} + \beta_3\hat{z}^{-3}} \tag{8.5-101}$$

where

$$\alpha_0 = -A_5 \tag{8.5-102}$$

$$\alpha_1 = A_1B_5B_6 - A_2B_6 + A_4 - A_5 \tag{8.5-103}$$

$$\alpha_2 = 2A_1B_5B_6 - A_0B_5B_6 + A_3B_6 - A_2B_6 \tag{8.5-104}$$

$$\alpha_3 = B_5B_6(A_1 - A_0) \tag{8.5-105}$$

$$\beta_1 = B_2B_6 - B_1B_5B_6 - B_4 \tag{8.5-106}$$

$$\beta_2 = B_0B_5B_6 - 2B_1B_5B_6 - B_3B_6 + B_2B_6 \tag{8.5-107}$$

and

$$\beta_3 = B_5B_6(B_0 - B_1) \tag{8.5-108}$$

Besides the transfer function of Eq. 8.5-101, two other transfer functions for each op amp output can be obtained. Equation 8.5-101 is chosen for its flexibility. A simplified yet versatile structure is considered next.

If $B_1 = B_4 = A_1 = A_4 = 0$, and if we omit the $1 + \hat{z}^{-1}$ following A_5, then the flow diagram Fig. 8.5-20*b* results. The coefficients of Eq. 8.5-101 become

$$-\alpha_0 = A_5 \tag{8.5-109}$$

$$-\alpha_1 = A_2 B_6 \tag{8.5-110}$$

$$-\alpha_2 = B_6(A_0 B_5 - A_3 + A_2) \tag{8.5-111}$$

$$-\alpha_3 = A_0 B_5 B_6 \tag{8.5-112}$$

$$\beta_1 = B_2 B_6 \tag{8.5-113}$$

$$\beta_2 = B_6(B_0 B_5 - B_3 + B_2) \tag{8.5-114}$$

and

$$\beta_3 = B_0 B_5 B_6 \tag{8.5-115}$$

A switched capacitor implementation of Fig. 8.5-20*b* is shown in Fig. 8.5-21. Table 8.5-2 shows the generality of the third-order building block in designing the transmission zeros. This table gives the values of the α coefficients and the capacitor ratios required for several conventional types of filters. In addition to the tradeoff between sensitivity and total capacitance mentioned before, we have added the constraint that the largest-to-smallest capacitor ratio be less than 10. More details regarding the tradeoff between sensitivity, output voltage swing, and total capacitance are given elsewhere.[49]

If the third-order specifications are given in terms of root locations, then it is necessary to relate the coefficients to the root locations. The root locations include one real pole at r_1, two complex poles at $r e^{\pm j\theta}$, and two complex zeros at $r_0 e^{\pm j\theta_0}$. These expressions are

$$\alpha_0 = 0 \tag{8.5-116}$$

$$\alpha_1 = 1 \tag{8.5-117}$$

$$\alpha_2 = 2 - 2r_0 \cos\theta_0 \tag{8.5-118}$$

$$\alpha_3 = 1 + r_0^2 - 2r_0 \cos\theta_0 \tag{8.5-119}$$

$$\beta_1 = 3 - r_1 - 2r\cos\theta \tag{8.5-120}$$

$$\beta_2 = 3 - 2r_1 + r^2 - 4r\cos\theta + 2rr_1\cos\theta \tag{8.5-121}$$

and

$$\beta_3 = 1 - r_1 + r^2 - r_1 r^2 - 2r\cos\theta + 2rr_1\cos\theta \tag{8.5-122}$$

To illustrate the synthesis procedure, the second-order and third-order blocks are used to design a fifth-order low-pass filter. The specifications of the filter are a 0.125 dB passband ripple, a cutoff frequency of 3.4 kHz, a stopband minimum attenuation of 32 dB above 4.6 kHz and a clock frequency of 128 kHz. The design begins with the roots of the s-domain rational polynomial approximation, $H(s)$. These roots are mapped to the $\hat{z}$-domain through the bilinear transformation.[26]

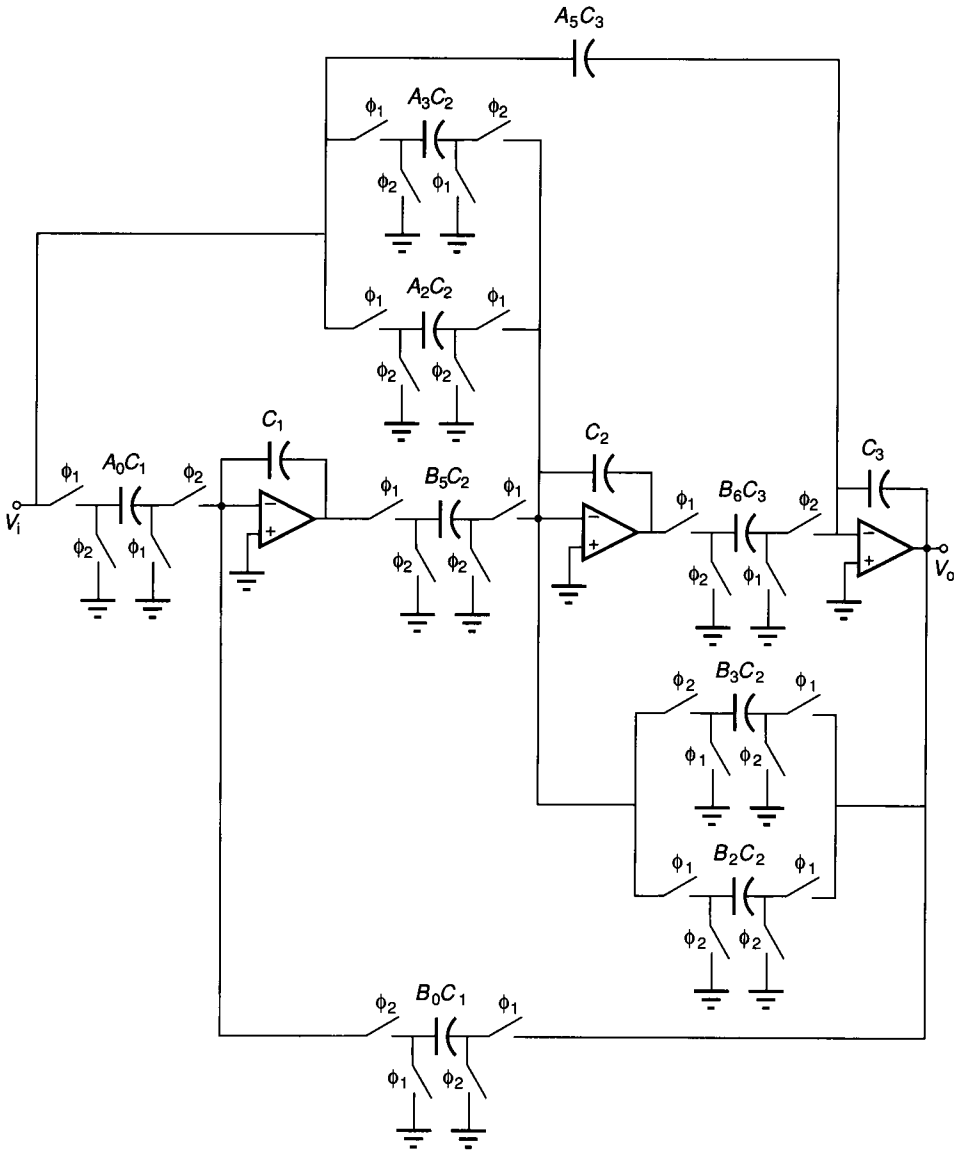


FIGURE 8.5-21
Switched capacitor implementation of Fig. 8.5-20*b*.

TABLE 8.5-2
Values of coefficients of zeros of the third-order filter

Filter type	Zeros in z-plane	Coefficient of $H(\hat{z})$				Corresponding capacitor ratios			
		α_0	α_1	α_2	α_3	A_0	A_2	A_3	A_5
Low-pass	$z_1 = -1$	0	0	0	1	B_0[a]	0	A_0B_5	0
Band-pass	$z_1 = -1$ $z_2 = 1$	0	0	1	0	0	0	A_3[b]	0
High-pass	$z_1 = 1$	1	0	0	0	0	0	0	A_5[b]
Notch	$z_1 = e^{j\theta_0}$ $z_2 = e^{-j\theta_0}$	0	1	$2(1 - \cos\theta_0)$	$2(1 - \cos\theta_0)$	$\frac{\alpha_2}{B_5B_6}$	$\frac{1}{B_6}$	$\frac{1}{B_6}$[c]	0

[a] $A_0 = B_0$ to obtain a 0 dB dc gain.

[b] A_3 and A_5 to be chosen to give the required center (cutoff) frequency gain.

[c] A_0, A_2, and A_3 can be scaled to obtain the desired dc gain.

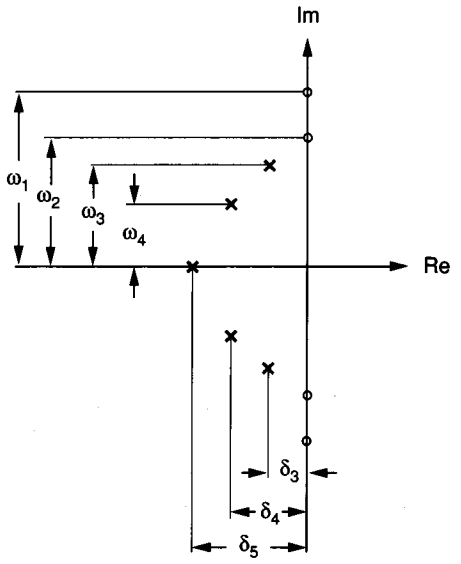


FIGURE 8.5-22
Root locations in the s-plane of the fifth-order filter: ○ = zeros, × = poles; $\omega_1 = 40.792 \times 10^3, \omega_2 = 28.367 \times 10^3, \omega_3 = 22.604 \times 10^3, \omega_4 = 17.83 \times 10^3, \delta_3 = 1.938 \times 10^3, \delta_4 = 8.514 \times 10^3, \delta_5 = 15.474 \times 10^3$.

The s-domain zero at infinity that maps to $\hat{z} = -2$ is ignored. The location of the roots in the s-domain are illustrated in Fig. 8.5-22. The second-order realization has two zeros and two poles, $\pm j\omega_2$ and $\delta_4 \pm j\omega_4$, respectively. The corresponding root locations in the $\hat{z}$-domain are $r = 0.92838, \theta = \pm 7.722°$, and $r_0 = 1.0, \theta_0 = \pm 12.928°$ for the poles and zeros, respectively. The third-order stage realizes two zeros and three poles: $\pm j\omega_1, \delta_5$, and $\delta_3 \pm j\omega_3$, respectively. The corresponding root locations in the z-domain are $r = 0.938, \theta = \pm 9.88°$, $r_1 = 0.878, r_0 = 1.0$, and $\theta_0 = \pm 18.9°$ for the poles and zeros, respectively.

It should be noted that in obtaining the coefficients in both filters, the dc gain of each stage was adjusted to be near unity. For the specified values of r and θ, the capacitor ratios of the biquad can be calculated by setting $B_2 = 0.1, B_3 = 1.6, D_2 = 0.0$, and $D_3 \simeq 0.22$. The final results are summarized in Table 8.5-3. The total capacitance for the biquad is 28.172 C_u. The capacitor ratios for the third-order building block are given in Table 8.5-4. The total capacitance for the third-order building block is $39.481C_u$. After simplifications,[49] the total capacitance is $33.28C_u$. The total filter capacitance is $C_T = 61.452C_u$. It has been shown that there is a tradeoff between sensitivity, total capacitance, and dynamic range.[26] Figure 8.5-23 shows the resulting fifth-order low-pass filter realization.

TABLE 8.5-3
Capacitor values in units of C_μ for the biquad circuit

Capacitor	B_2C_2 B_3C_1	B_1C_1	B_0C_2 D_2C_2	D_3C_1	D_0C_2	D_1C_1	C_1	C_2
Value	1	6.2863	0	1	4.3336	0	4.5517	10

TABLE 8.5-4
Capacitor values in units of C_μ for the triquad circuit

Capacitor	A_0C_1 B_0C_1	C_1 C_3	B_6C_3 A_2C_2	A_3C_2	B_2C_2	B_3C_2	C_2	B_5C_2
Value	1	10	1	1	5.684	4.657	3.057	1.083

The performance of this filter is shown in Fig. 8.5-24. The simulated results and the experimental results agree quite closely.[50]

A brief overview of the methods of designing switched capacitor filters has been shown. The three approaches selected were resistor replacement or simulation by switched capacitor equivalents, the use of integrators to realize passive RLC prototype ladder filters, and the direct synthesis of the z-domain transfer function. Many more approaches exist, and they should be considered if the above approaches do not provide the required performance.

Because of the lack of space, topics such as the prewarping of the s-domain specifications to account for the $(\sin x)/x$ effect of the sample-and-hold circuit on the filter performance have not been discussed. Also, the influence of the switches and the op amp performance (gain and bandwidth) have not been considered. Another problem the designer is faced with when designing switched capacitor circuits is a method of analysis. Because the switched capacitor circuit is an analog sampled-data system, aliasing can occur, and it is often necessary to use an antialiasing filter, which must be a continuous-time filter. Fortunately, the accuracy requirement of the continuous-time, antialiasing filter is not severe, and RC active filter techniques can be used.

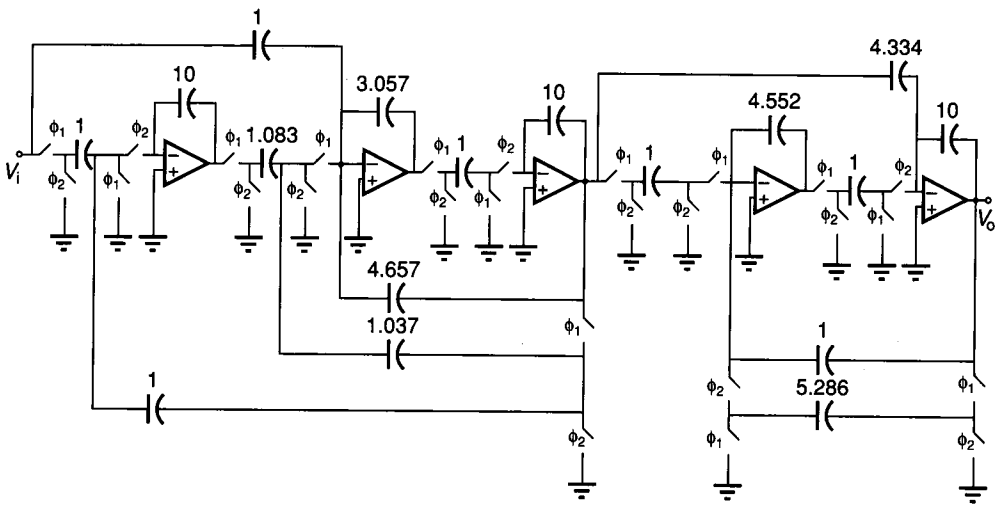


FIGURE 8.5-23
SC circuit diagram of the fifth-order filter, capacitor values in C_u units.

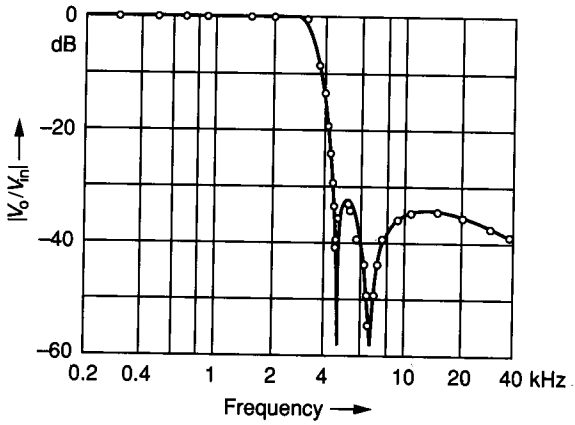


FIGURE 8.5-24
Experimental and theoretical frequency response of the filter of Fig. 8.5-23: O = experiment, — = theory.

The success of switched capacitor filters has created the demand for increased performance in the area of dynamic range and frequency. The influence of the feedthrough of the switches has been found to be a serious factor in limiting dynamic range. Besides using small switches and other methods previously discussed to reduce feedthrough, it is important to keep the summing nodes of switched capacitor circuits physically away from the clock lines. In fact, any analog input line should be isolated from lines that carry digital signals. Another factor limiting the dynamic range is noise. The noise can come from the op amp or from switched capacitors (kT/C noise). Of particular concern is the folding of high-frequency noise into the baseband of the switched capacitor circuit.

The frequency limits of switched capacitor circuits are primarily due to the op amp frequency limitations. Design methods exist that allow the signal bandwidth to approach half the sampling frequency. One of the benefits of these methods is that the capacitor ratios are reduced and the area required for capacitors is minimum. The finite gain bandwidth of the op amp will cause the actual switched capacitor filter performance to deviate from the desired performance.

Careful layout, the use of high-frequency op amps, and a fully differential signal path have resulted in switched capacitor filters with very good dynamic range and with high-frequency performance. Of the three approaches presented, the RLC ladder approach using fully differential integrators or the cascaded biquad are typically used. The designer generally tries to minimize the area and power dissipation in addition to achieving the filter performance requirements.

Switched capacitor techniques are also useful for nonfilter applications. Many of the circuits covered in the next section can be implemented using switched capacitor circuit methods. The full application of switched capacitor circuit techniques has yet to be investigated with respect to analog signal processing circuits.

8.6 ANALOG SIGNAL PROCESSING CIRCUITS

One of the largest areas of application of analog signal processing circuits is filtering. This has been the subject of the last two sections. In this section, we consider nonfilter applications of analog signal processing circuits. These applications include precision breakpoint circuits, multipliers and modulators, oscillators, and phase-locked loops. Many other circuits and systems could be included, but these are representative of the concepts and principles.

8.6.1 Precision Breakpoint Circuits

In many applications it is necessary to realize a voltage transfer characteristic similar to those given in Fig. 8.6-1. In these transfer characteristics, the breakpoint is the point where two straight-line segments join, which is at the origin for each

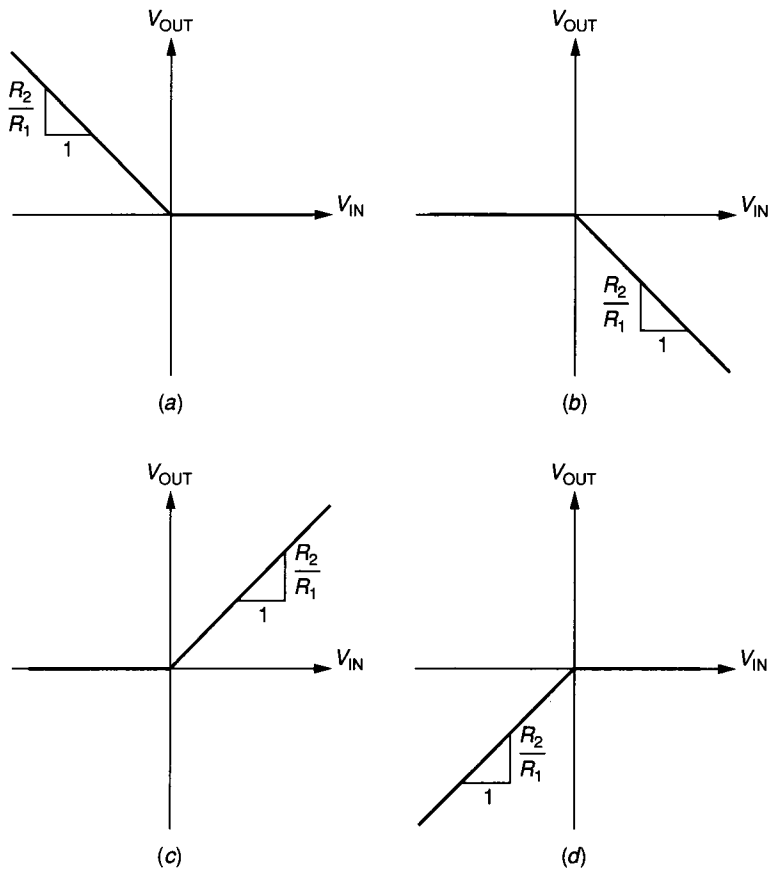


FIGURE 8.6-1
Four possible types of nonlinear voltage transfer characteristics having the breakpoint at $V_{IN} = 0$.

of these cases. If the technology used can implement a diode, a resistor, and an op amp, then Fig. 8.6-2 shows a realization of each of the respective voltage transfer characteristics of Fig. 8.6-1. The slopes of the realizations will be determined by the ratio of R_2 and R_1. Because the diodes are in the feedback path, they behave as ideal diodes. This permits the drain-gate connected MOSFET to function in place of the diodes in Fig. 8.6-2.

In every diode circuit, it is necessary to first find the breakpoints of the circuits related to either the input or output variable. In Fig. 8.6-2, the current

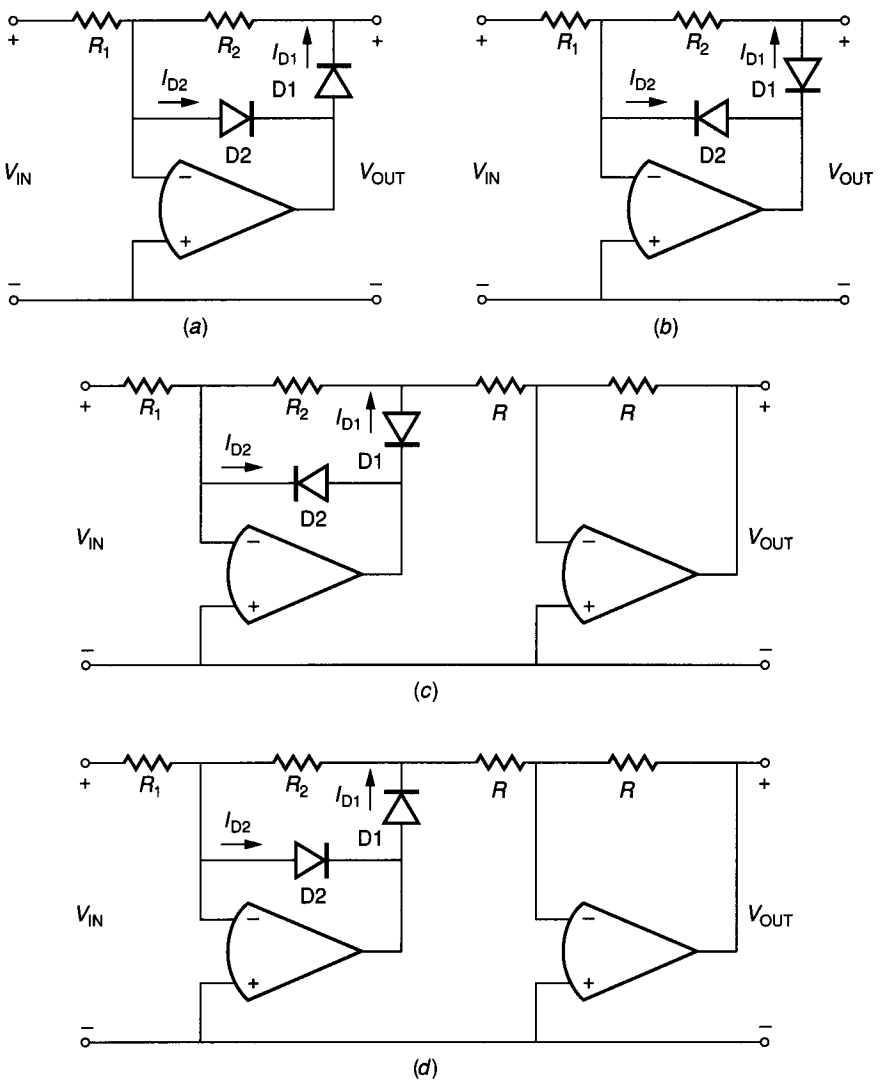


FIGURE 8.6-2
Realizations of the characteristics of Fig. 8.6-1: (*a*) Fig. 8.6-1*a* with slope $-R_2/R_1$, (*b*) Fig. 8.6-1*b* with slope $-R_2/R_1$, (*c*) Fig. 8.6-1*c* with slope R_2/R_1, (*d*) Fig. 8.6-1*d* with slope R_2/R_1.

flow in or out of the op amp can flow only through D1 or D2 but not both at the same time. Therefore, the only possible states of D1 and D2 are D1 on–D2 off or D1 off–D2 on. The breakpoint in the circuits of Fig. 8.6-2 will occur when both diode currents are zero. The direction of I_{D1} and I_{D2} is not important because they will be equated to zero to find the breakpoint. For example, consider Fig. 8.6-2*a*. The currents I_{D1} and I_{D2} can be expressed as

$$I_{D1} = \frac{V_{IN}}{R_1} + \frac{V_{OUT}}{R_2} \qquad I_{D2} = \frac{V_{OUT}}{R_2} \tag{8.6-1}$$

Setting I_{D1} and I_{D2} to zero gives the breakpoints as $V_{OUT}(BP) = 0$ and $V_{IN}(BP) = 0$.

In many cases, the breakpoint is to be shifted away from zero. This can be accomplished for the circuit of Fig. 8.6-2*b* as illustrated in Fig. 8.6-3*a*. A dc voltage, E_r, has been connected to the inverting input through a resistor, R_3. Using the principles just explained, we solve for I_{D1} and I_{D2} as

$$I_{D1} = \frac{V_{IN}}{R_1} + \frac{E_r}{R_3} + \frac{V_{OUT}}{R_2} \qquad I_{D2} = \frac{V_{OUT}}{R_2} \tag{8.6-2}$$

Setting I_{D1} and I_{D2} to zero in Eq. 8.6-2 gives the breakpoint as

$$V_{IN}(BP) = -\frac{E_r R_1}{R_3} \qquad V_{OUT}(BP) = 0 \tag{8.6-3}$$

Figure 8.6-3*b* shows the voltage transfer characteristics of the circuit of Fig. 8.6-3*a*.

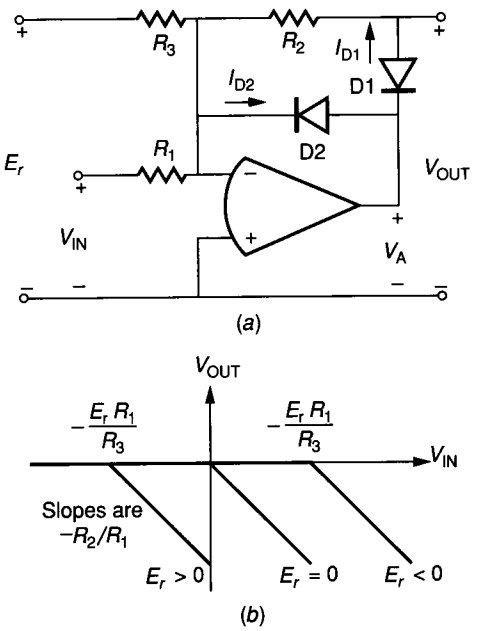


FIGURE 8.6-3
(*a*) Method of shifting the breakpoint of Fig. 8.6-1*b*, (*b*) Transfer characteristics of (*a*).

Mathematically, we may express the output voltage of Fig. 8.6-3*a* as

$$V_{OUT} = \begin{cases} -R_2 v_{IN}/R_1 + R_2 E_r/R_1 & V_{IN} \geq -R_1 E_r/R_3 \\ 0 & V_{IN} < -R_1 E_r/R_3 \end{cases} \quad (8.6\text{-}4)$$

We note that E_R can be positive or negative, which will shift the breakpoint to the left or right, respectively. The same principle can be applied to the other circuits of Fig. 8.6-2 to develop a general capability of establishing a breakpoint at any value of V_{IN}.

These concepts can be extended to synthesize a voltage transfer function by using piecewise linear segments. Figure 8.6-4*a* shows a number of circuits similar to the circuit of Fig. 8.6-3*a* summed into a summing amplifier. The resulting

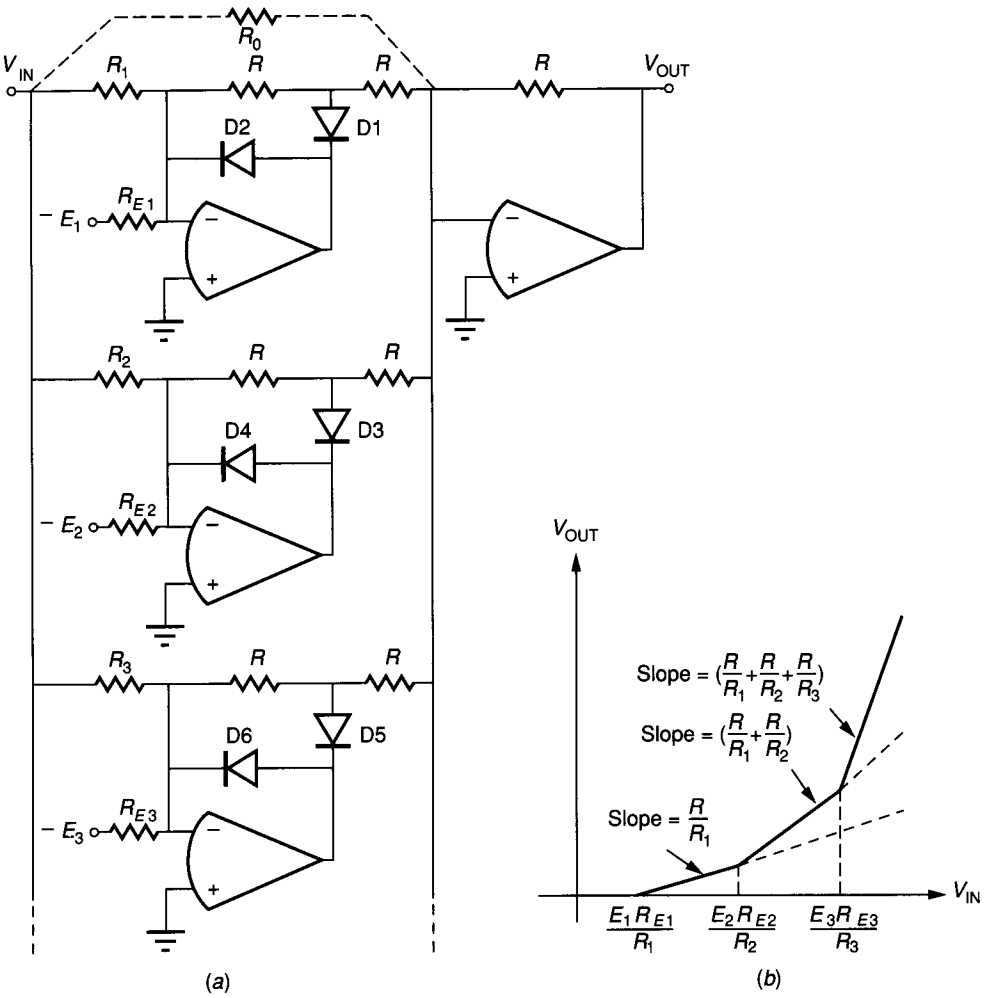


FIGURE 8.6-4
(*a*) Summation of individual segments to form a piecewise linear approximation, (*b*) Voltage transfer characteristics of (*a*).

transfer characteristic is shown in Fig. 8.6-4*b*. Each of the individual outputs implements one line segment. We note that all E_is can be identical, and the R_{Ei} resistors can be used to design the breakpoints. On the other hand, all R_{Ei}s can be identical and the E_i voltage sources used to design the breakpoints. The slopes of the line segments become increasingly larger and are indicated on the curve. If the diodes are all reversed and the polarities of E_i changed, the piecewise linear curve moves to the third quadrant. R_0 shown in Fig. 8.6-4*a* can be added to allow a line segment with a nonzero slope to go through the origin of Fig. 8.6-4*b*.

The curve of Fig. 8.6-4*b* is monotonically increasing in slope. If the slope is to decrease, then one could place an inverter in with each breakpoint circuit of Fig. 8.6-4*a* before summing its output. All possible monotonically increasing and decreasing slopes are realizable in any of the four quadrants using these ideas.

Although the diodes and op amps of the above circuits can easily be implemented in BJT or MOS technology, the resistors are not practical. Resistors are not sufficiently accurate for most applications and require too much area. A method of eliminating the resistors in MOS technology using switched capacitor methods will be presented next.

Consider the switched capacitor implementation of a noninverting amplifier shown in Fig. 8.6-5. This circuit is similar to the noninverting stray-insensitive integrator of Fig. 8.5-11 except for the switch added to discharge C_2 during the ϕ_1 phase. This switch essentially removes the memory of the integrator, resulting in an amplifier. It can be shown that the z-domain transfer function of the circuit of Fig. 8.6-5 is

$$H^{\text{oe}}(z) = \frac{V_{\text{OUT}}(z)}{V_{\text{IN}}(z)} = \frac{C_1}{C_2} z^{-1/2} \tag{8.6-5}$$

Equation 8.6-5 represents a noninverting gain function that is valid during the ϕ_2 phase and is delayed by a half clock period from the input. A sample and hold circuit can be added to hold the output for the entire clock period. If the output is sampled and held, then Eq. 8.6-5 is multiplied by $z^{-1/2}$ to get a full delay of $H^{\text{oo}}(z)$. One of the disadvantages of the circuit of Fig. 8.6-5 is that the op amp output is slewed to zero during each ϕ_1 phase and back to the desired output during each ϕ_2 phase. This is unnecessary and can be prevented by the introduction of more capacitors and switches as will be shown later.

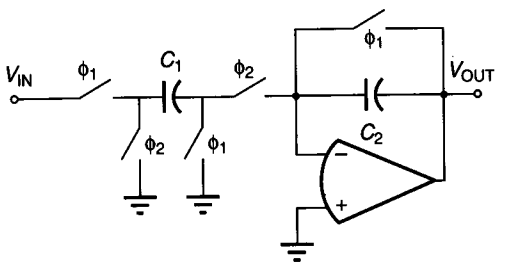


FIGURE 8.6-5
Noninverting switched capacitor amplifier realization.

If the leftmost pair of switches has the phasing reversed, then the amplifier is inverting, and the transfer function is given as

$$H(z) = \frac{V_{OUT}(z)}{V_{IN}(z)} = -\frac{C_1}{C_2} \tag{8.6-6}$$

where the output is valid only at the ϕ_2 phase. If we assume that the high sampling approximation is valid, then Fig. 8.6-5 can be considered as a simple noninverting or inverting amplifier depending upon the phasing of the leftmost switch pair.

The voltage transfer characteristics of Fig. 8.6-1 can be realized using MOS technology if we combine a comparator with the amplifier of Fig. 8.6-5, as shown in Fig. 8.6-6*a*. Note that the comparator output controls the switch that couples C_1 into the inverting input of the op amp (called the transfer switch). If this switch is open during the ϕ_2 phase period, the output of the op amp will be zero. If the transfer switch is closed during the ϕ_2 phase period, the output will be given by Eq. 8.6-5 or 8.6-6, depending on the phasing of the leftmost switch pair. To see how the circuit works, consider the circuit of Fig. 8.6-6*a* with a positive value of V_{IN}. The comparator output will be high, causing the transfer switch to be closed. Thus, the output is given by Eq. 8.6-5. If V_{IN} is less than zero, the comparator output is low, causing the transfer switch to be open. Therefore, the circuit of Fig. 8.6-6*a* realizes the voltage transfer curve of Fig. 8.6-1*c* with outputs valid during the ϕ_2 clock phase. If the comparator inputs are reversed, Fig. 8.6-6*a* realizes the voltage transfer curve of Fig. 8.6-1*d*. If the phases of the leftmost switches (input switches) are reversed, the circuit of Fig. 8.6-6*b* results. With the inputs to the comparator as shown, this circuit realizes the voltage transfer curve of Fig. 8.6-1*b*. If the comparator inputs are reversed, the voltage transfer curve of Fig. 8.6-1*a* is realized.

The switched capacitor breakpoint realizations can be implemented by alternate configurations, but all will utilize a comparator controlling one or more switches. It is easy to shift the breakpoint of the realization by connecting the

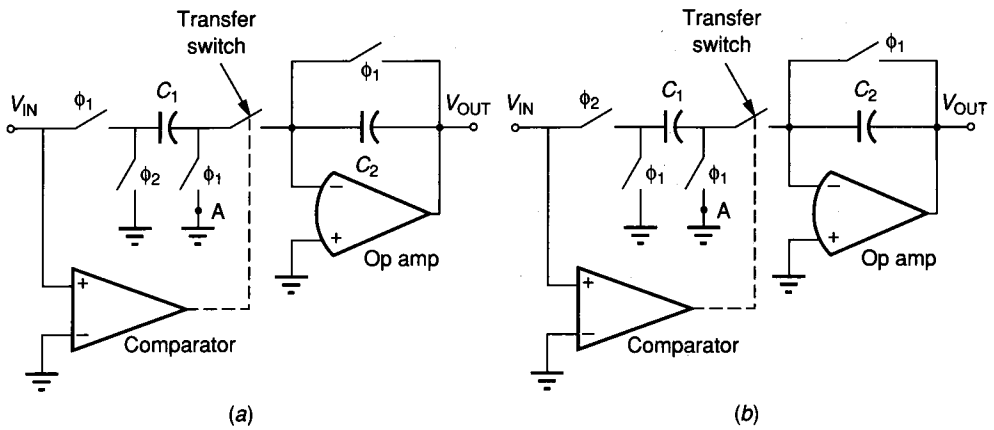


FIGURE 8.6-6
(*a*) Switched capacitor realization of Fig. 8.6-1*c*, (*b*) Switched capacitor realization of Fig. 8.6-1*b*.

grounded input terminal of the comparators of Fig. 8.6-6*a* and *b* to the voltage E_r. It is also necessary to remove point A from ground and connect it to the voltage E_r. A positive value of E_r applied to the inverting input of the comparator of Fig. 8.6-6*a* will cause the breakpoint to occur at $V_{IN} = E_r$. The outputs of several shifted breakpoint realizations can be summed in a manner similar to Fig. 8.6-4 to obtain a piecewise linear approximation of a voltage transfer function.[51] The switched capacitor realizations of the precision breakpoint circuits are compatible with MOS technology and have been employed in many commercial applications.

8.6.2 Modulators and Multipliers

Modulators include a class of circuits with multiple inputs where one input can modify or control the signal flow from the other input to the output. Figure 8.6-7 illustrates the modulator on a block diagram basis. $V_1(t)$ and $V_2(t)$ are input signals. The modulator output signal can be expressed in general as

$$V_{OUT}(t) = f_A[V_1(t)]f_B[V_2(t)] \tag{8.6-7}$$

where f_A and f_B are two arbitrary functions of the respective inputs. If $f_A[V_1(t)]$ and $f_B[V_2(t)]$ are linearly dependent upon $V_1(t)$ and $V_2(t)$, respectively, the modulator is called a *multiplier*. Thus, Eq. 8.6-7 becomes

$$V_{OUT}(t) = K_1 V_1(t) V_2(t) \tag{8.6-8}$$

where K_1 is the combination of the individual constants for $V_1(t)$ and $V_2(t)$.

Figure 8.6-8 shows a BJT modulator using the differential amplifier configuration of Fig. 6.4-7 with resistor loads and a current sink implemented by a current mirror. The output voltage can be expressed as

$$V_{OUT} = R_c(I_{C1} - I_{C2}) = \alpha_F I_{EE} R_c \left[\frac{1}{1 + e^{-V_1/V_t}} - \frac{1}{1 + e^{V_1/V_t}} \right] \tag{8.6-9}$$

using Eqs. 6.3-52 and 6.3-53. Equation 8.6-9 can be rewritten as

$$V_{OUT} = \alpha_F I_{EE} R_c \tanh\left(\frac{V_1}{2V_t}\right) \simeq I_{EE} R_c \left(\frac{V_1}{2V_t}\right) \tag{8.6-10}$$

if V_1 is much less than 50 mV. Because I_{EE} is equal to $[V_2 - V_{BE}(on)]/R$, we may express Eq. 8.6-10 as

$$V_{OUT} = \frac{R_c}{2V_t R} V_1 \cdot [V_2 - V_{BE}(on)] = K_1 V_1 [V_2 - V_{BE}(on)] \tag{8.6-11}$$

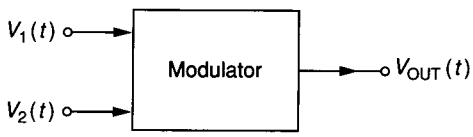


FIGURE 8.6-7
Block diagram for a modulator.

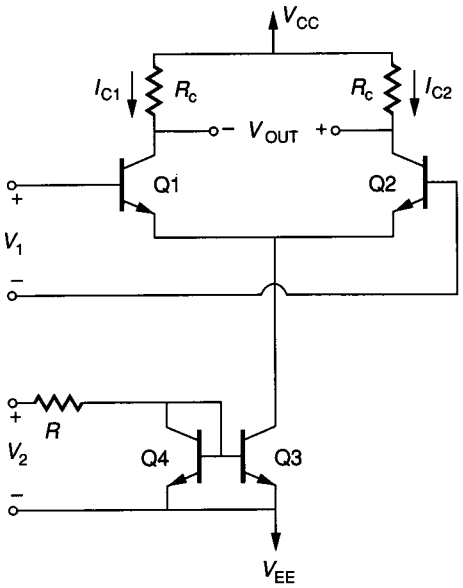


FIGURE 8.6-8
A simple BJT modulator using a differential amplifier.

The multiplier of Fig. 8.6-8 has several problems. The first is that V_2 is offset by $V_{BE}(\text{on})$. The second is that V_2 must always be positive, resulting in a two-quadrant multiplier. A third problem is that the dynamic range is limited because of the approximation necessary to replace $\tanh x$ by x where $x = V_1/2V_t$ in Eq. 8.6-10.

The first two problems can be solved by the Gilbert cell[52] shown in Fig. 8.6-9. The Gilbert cell allows four-quadrant operation and is the basis for most integrated circuit balanced multipliers. The operation of this key cell is as follows. The collector currents of Q3 and Q4 are

$$I_{C3} = \frac{I_{C1}}{1 + \exp(-V_1/V_t)} \tag{8.6-12}$$

and

$$I_{C4} = \frac{I_{C1}}{1 + \exp(V_1/V_t)} \tag{8.6-13}$$

Similarly the collector currents for Q5 and Q6 are

$$I_{C5} = \frac{I_{C2}}{1 + \exp(V_1/V_t)} \tag{8.6-14}$$

and

$$I_{C6} = \frac{I_{C2}}{1 + \exp(-V_1/V_t)} \tag{8.6-15}$$

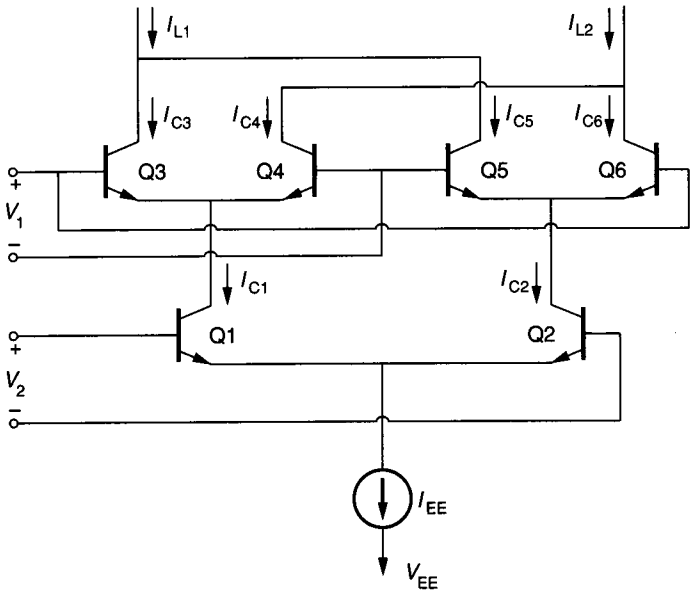


FIGURE 8.6-9
The Gilbert multiplier cell.

The two collector currents I_{C1} and I_{C2} can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + \exp(-V_2/V_t)} \tag{8.6-16}$$

and

$$I_{C2} = \frac{I_{EE}}{1 + \exp(V_2/V_t)} \tag{8.6-17}$$

Substituting Eqs. 8.6-16 and 8.6-17 into Eqs. 8.6-12 through 8.6-15 results in

$$I_{C3} = \frac{I_{EE}}{[1 + \exp(-V_1/V_t)][1 + \exp(-V_2/V_t)]} \tag{8.6-18}$$

$$I_{C4} = \frac{I_{EE}}{[1 + \exp(V_1/V_t)][1 + \exp(-V_2/V_t)]} \tag{8.6-19}$$

$$I_{C5} = \frac{I_{EE}}{[1 + \exp(V_1/V_t)][1 + \exp(V_2/V_t)]} \tag{8.6-20}$$

and

$$I_{C6} = \frac{I_{EE}}{[1 + \exp(-V_1/V_t)][1 + \exp(V_2/V_t)]} \tag{8.6-21}$$

Next we define the differential output current, ΔI, as

$$\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6}) = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5}) \tag{8.6-22}$$

Substituting Eqs. 8.6-18 through 8.6-21 into Eq. 8.6-22 and using the exponential formulaes for hyperbolic functions results in the differential output current being expressed as

$$\Delta I = I_{EE}\left[\tanh\left(\frac{V_1}{2V_t}\right)\right]\left[\tanh\left(\frac{V_2}{2V_t}\right)\right] \tag{8.6-23}$$

If the input signals V_1 and V_2 are small enough, the Gilbert cell of Fig. 8.6-9 functions as a four-quadrant analog multiplier. The output voltage, V_{OUT}, can be generated from ΔI by using two equal-valued resistors connected to V_{CC} with current $I_{L1}(=I_{C3} + I_{C5})$ flowing through one and current $I_{L2}(=I_{C4} + I_{C6})$ flowing through the other.

The circuit of Fig. 8.6-9 can be used as a modulator when one of the inputs is very large and the other sufficiently small so that tanh x is approximately equal to x. The large input will cause the transistors to which it is applied to act like switches. This effectively multiplies the small signal by a square wave. Such modulators are called *synchronous modulators* and have many applications in signal processing, including demodulation and phase detection. The amplitude range of V_2 can be extended considerably by placing resistors between the emitters and the I_{EE} current source of the Gilbert cell.

The amplitude constraints on the inputs of the Gilbert cell can be removed using a predistortion technique that results in a linear relationship between V_1 and V_{OUT} and V_2 and V_{OUT}. Figure 8.6-10 illustrates the complete four-quadrant multiplier. The three boxes, which are voltage-to-current converters or current-to-voltage converters, will be considered shortly. The predistortion is implemented by the emitters of Q7 and Q8. The currents I_9 and I_{10} create a voltage between the emitters of Q7 and Q8 that is proportional to the inverse hyperbolic tangent of V_1. This will remove the hyperbolic tangent expressions in Eq. 8.6-23.

The analysis of the circuit of Fig. 8.6-10 can be accomplished as follows. It can be shown that the currents through base-emitter junctions that are connected in series, such as Q7, Q3, Q4, and Q8, can be expressed as

$$I_9 I_3 = I_4 I_{10} \tag{8.6-24}$$

where $I_7 = I_9$ and $I_8 = I_{10}$. Similarly, for the series connection of Q7, Q6, Q5, and Q8, we have

$$I_9 I_6 = I_5 I_{10} \tag{8.6-25}$$

Next we note that

$$I_1 = I_3 + I_4 \tag{8.6-26}$$

$$I_2 = I_5 + I_6 \tag{8.6-27}$$

$$I_{L1} = I_3 + I_5 \tag{8.6-28}$$

$$I_{L2} = I_4 + I_6 \tag{8.6-29}$$

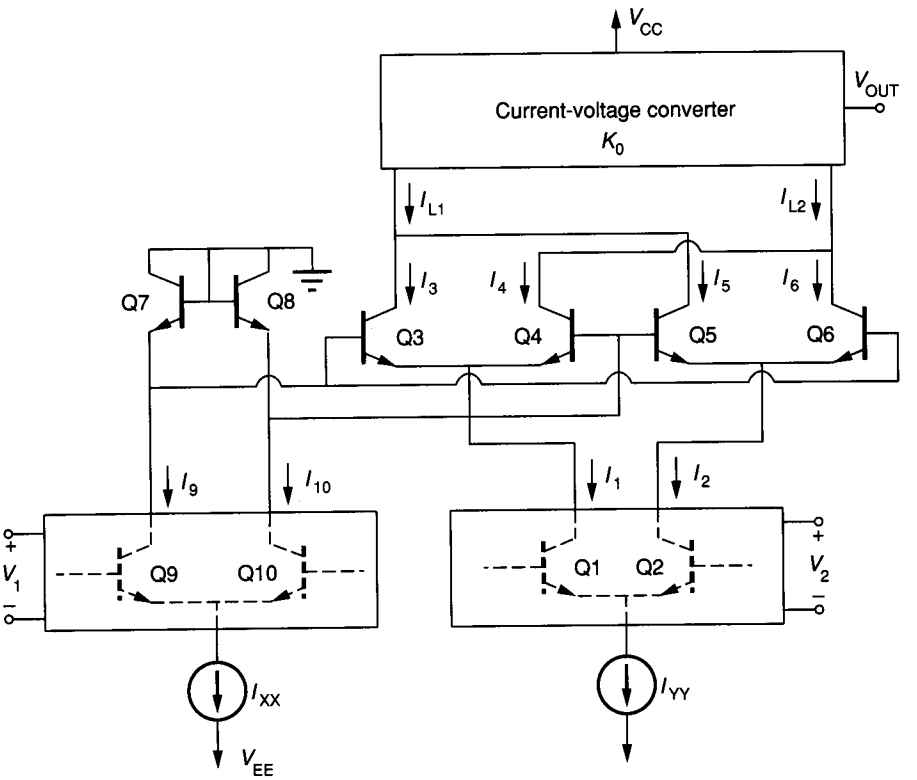


FIGURE 8.6-10
Complete four-quadrant analog multiplier.

and

$$I_{XX} = I_9 + I_{10} \tag{8.6-30}$$

Let us assume that the transfer characteristics of the rectangular blocks of Fig. 8.6-10 are given by

$$I_9 - I_{10} = V_1/K_1 \tag{8.6-31}$$

$$I_1 - I_2 = V_2/K_2 \tag{8.6-32}$$

and

$$V_{OUT} = K_o(I_{L2} - I_{L1}) \tag{8.6-33}$$

where K_o, K_1, and K_2 are constants depending on the implementation. Replacing I_{L2} and I_{L1} by Eqs. 8.6-28 and 8.6-29 results in

$$V_{OUT} = K_o[(I_4 + I_6) - (I_3 + I_5)] = K_o\left[\left(I_4 + I_5\frac{I_{10}}{I_9}\right) - \left(I_4\frac{I_{10}}{I_9} + I_5\right)\right] \tag{8.6-34}$$

Rearranging Eq. 8.6-34 results in

$$V_{OUT} = K_o\left(\frac{I_9 - I_{10}}{I_9}\right)(I_4 - I_5) \tag{8.6-35}$$

We desire to replace $(I_4 - I_5)$ by $(I_1 - I_2)$, which can be accomplished as follows.

$$I_1 - I_2 = (I_3 + I_4) - (I_5 + I_6) = \left(I_4\frac{I_{10}}{I_9} + I_4\right) - \left(I_5 + I_5\frac{I_{10}}{I_9}\right) \tag{8.6-36}$$

Combining terms and solving for $(I_4 - I_5)$ gives

$$(I_4 - I_5) = \left(\frac{I_9}{I_9 + I_{10}}\right)(I_1 - I_2) \tag{8.6-37}$$

Substituting Eq. 8.6-37 into Eq. 8.6-35 provides the desired result.

$$V_{OUT} = K_o\left(\frac{I_9 - I_{10}}{I_9 + I_{10}}\right)(I_1 - I_2) = \frac{K_o V_1 V_2}{I_{XX} K_1 K_2} = K_m V_1 V_2 \tag{8.6-38}$$

where the definitions of Eqs. 8.6-30 through 8.6-32 have been used to obtain Eq. 8.6-38. Because no approximations were used in the derivation of Eq. 8.6-38, the input signal amplitudes are not constrained.

Figure 8.6-11 shows a practical implementation of the four-quadrant analog multiplier of Fig. 8.6-10. It can be seen that

$$I_1 - I_2 = \frac{2V_2}{R_Y} \tag{8.6-39}$$

and

$$I_9 - I_{10} = \frac{2V_1}{R_X} \tag{8.6-40}$$

where it has been assumed that the part of V_1 and V_2 across the base-emitter of $Q9$, $Q10$, and $Q1$, $Q2$ are small compared to the drop across the resistors. Substituting Eqs. 8.6-39 and 8.6-40 into Eq. 8.6-38 results in

$$V_{OUT} = \frac{4K_o R_c V_1 V_2}{I_{XX} R_X R_Y} = K_m V_1 V_2 \tag{8.6-41}$$

where R is much greater than R_c. These concepts have been used to implement high-performance four-quadrant analog multipliers having good performance. One of the problems with the integrated circuit implementation is the need to be able to trim the various errors due to offsets and mismatches.

Four-quadrant multipliers have also been implemented in MOS technology.[53–56] Most of the realizations use a linearized Gilbert cell approach similar to the bipolar implementation above. A somewhat different approach is based on the cascade of two differential amplifier pairs has been found to give good results.[53] The principle of operation is illustrated in Fig. 8.6-12. If we assume

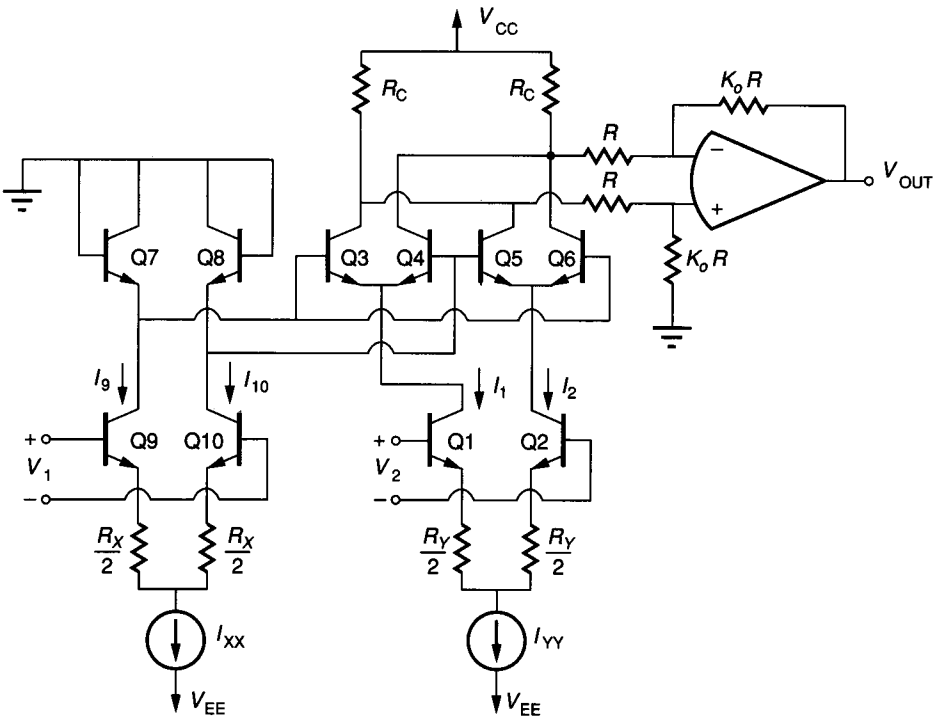


FIGURE 8.6-11
Practical implementation of Fig. 8.6-10.

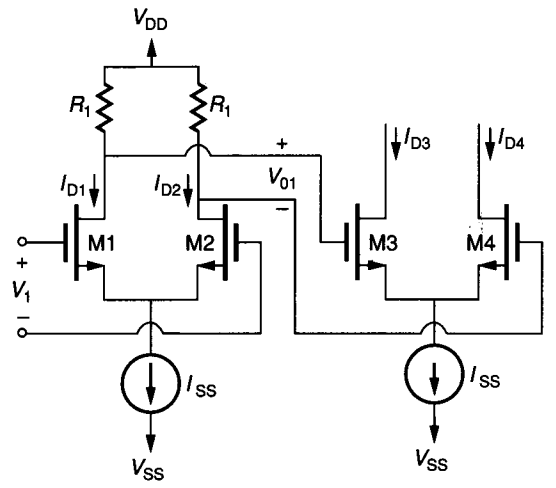


FIGURE 8.6-12
Cascaded MOS differential amplifiers.

that M1 and M2 are in the saturation region, then using Eqs. 6.3-7 and 6.3-8, we may write

$$I_{D1} - I_{D2} = I_{SS}\left[\frac{\beta_1 V_1^2}{I_{SS}} - \frac{\beta_1^2 V_1^4}{4I_{SS}^2}\right]^{1/2} = \beta_1 V_1\left[\frac{I_{SS}}{\beta_1} - \frac{V_1^2}{4}\right]^{1/2} \tag{8.6-42}$$

whre $\beta_1 = KW_1/L1$. It is seen that $I_{D1} - I_{D2}$ depends nonlinearly on V_1 and I_{SS}. Let us define V_{O1} as

$$V_{O1} = -R_1(I_{D1} - I_{D2}) \tag{8.6-43}$$

We can find a similar expression to Eq. 8.6-42 for $I_{D3} - I_{D4}$, which is

$$I_{D3} - I_{D4} = \beta_3 V_{O1}\left[\frac{I_{SS}}{\beta_3} - \frac{V_{O1}^2}{4}\right]^{1/2} \tag{8.6-44}$$

where $\beta_3 = kW_3/L3$. If we restrict V_1 to less than $0.3(I_{SS}/\beta_1)^{1/2}$, then we can approximate Eq. 8.6-42 as

$$I_{D1} - I_{D2} \simeq \beta_1 V_1[I_{SS}/\beta_1]^{1/2} \tag{8.6-45}$$

It has been shown that this assumption results in less than 0.2% total harmonic distortion in $I_{D1} - I_{D2}$. Substituting Eqs. 8.6-43 and 8.6-45 into Eq. 8.6-44 results in

$$I_{D3} - I_{D4} = V_1[-R_1 I_{SS}(\beta_1\beta_3)^{1/2}][1 - (\beta_1\beta_3 R_1^2 V_1^2/4)]^{1/2} \tag{8.6-46}$$

It is seen that $I_{D3} - I_{D4}$ depends linearly on I_{SS}. However, there is still a nonlinear dependence upon V_1. This dependence could be removed by restricting the amplitude of $I_{D3} - I_{D4}$. An alternative approach is to use the predistortion circuit of Fig. 8.6-13. In this circuit, V_1 is created by the difference in two currents, $I_{X1} - I_{X2}$. This difference, designated as I_X, can be expressed as

$$I_X = I_{X1} - I_{X2} = V_1(I_{DX}\beta_5)^{1/2}[1 - (\beta_5/4I_{DX})V_1^2]^{1/2} \tag{8.6-47}$$

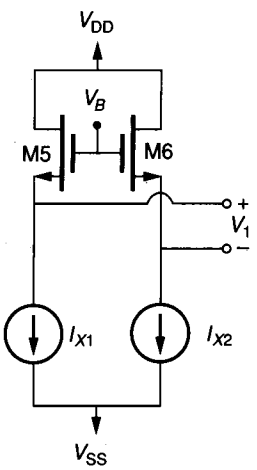


FIGURE 8.6-13
Predistortion circuit for the cascade MOS differential multiplier of Fig. 8.6-12.

where $I_{DX} = I_{X1} + I_{X2}$. Since the bracketed terms of Eqs. 8.6-46 and 8.6-47 have the same form, we can achieve predistortion by equating these two terms to get

$$\beta_5 = \beta_1\beta_3 R_1^2 I_{DX} \tag{8.6-48}$$

Therefore, Eq. 8.6-46 can be reduced to

$$I_O = I_{D3} - I_{D4} = -R_1\left[\frac{\beta_1\beta_3}{I_{DX}\beta_5}\right]^{1/2} I_{SS} I_X \tag{8.6-49}$$

Equation 8.6-49 is the form of an ideal current multiplier. I_{SS} and I_X will be generated by voltage-to-differential current amplifiers, and the output voltage will be derived from I_O.

In order to get four-quadrant operation, I_{SS} must be able to be negative. This can be accomplished by taking the difference of two of the preceding circuits. The resulting MOS realization using only n-channel transistors is shown in Fig. 8.6-14. Several practical modifications can be made to improve the performance of the multiplier with regard to temperature and linearity. This MOS four-quadrant analog multiplier is capable of linearity better than 0.3% at 75% of full scale. It has a bandwidth of dc to 1.5 MHz and an output noise 77 dB below full scale.

Other techniques exist that allow the implementation of multipliers compatible with CMOS technology. A straightforward approach using an A/D and a D/A converter is shown in Fig. 8.6-15. The input to the A/D converter is one of the multiplier inputs designated as V_1. The reference voltage for an n-bit, A/D converter is provided by another analog input, V_2, to the multiplier. The digital output word of the A/D converter is given as

$$D = \frac{V_1}{V_2} = b_1 2^{-1} + b_2 b^{-2} + \cdots + b_{n-1}2^{-n+1} + b_n 2^{-n} \tag{8.6-50}$$

where D is digital word for the value of V_1 scaled by V_2. This digital word is then applied to an n-bit, D/A converter that has an analog input, V_3, applied as its reference voltage. The analog output of the D/A converter is given as

$$V_O = DV_3 = b_1 2^{-2} + b_2 2^{-2} + \cdots + b_{n-1}2^{n-1} + b_n 2^{-n} \tag{8.6-51}$$

Substituting Eq. 8.6-50 into Eq. 8.6-51 results in the following multiplier/divider with n-bit resolution.

$$V_O = \frac{V_1 V_3}{V_2} \tag{8.6-52}$$

Any of the D/A and A/D converters of Sec. 8.2 and 8.3 can be used to implement a multiplier by this principle.

In the preceding results, we notice that the V_2 input of Fig. 8.6-15 is a dividing input. Obviously, V_2 cannot be zero. Another method of implementing a divider circuit is shown in Fig. 8.6-16. Figure 8.6-16*a* shows the block diagram

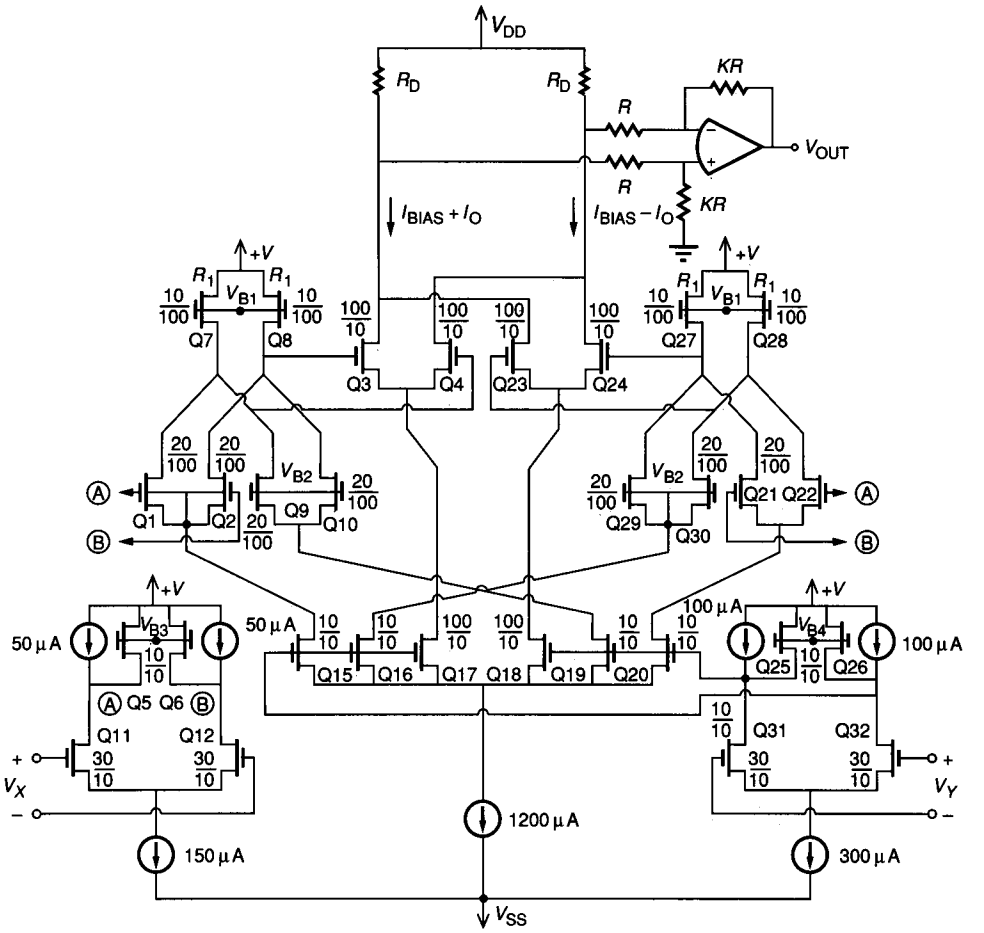


FIGURE 8.6-14
MOS four-quadrant analog current multiplier simplified schematic (values shown are W/L in microns/microns).

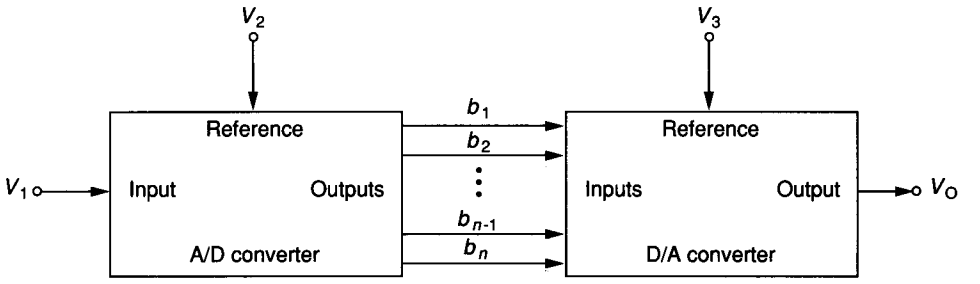


FIGURE 8.6-15
A/D–D/A converter analog multiplier.

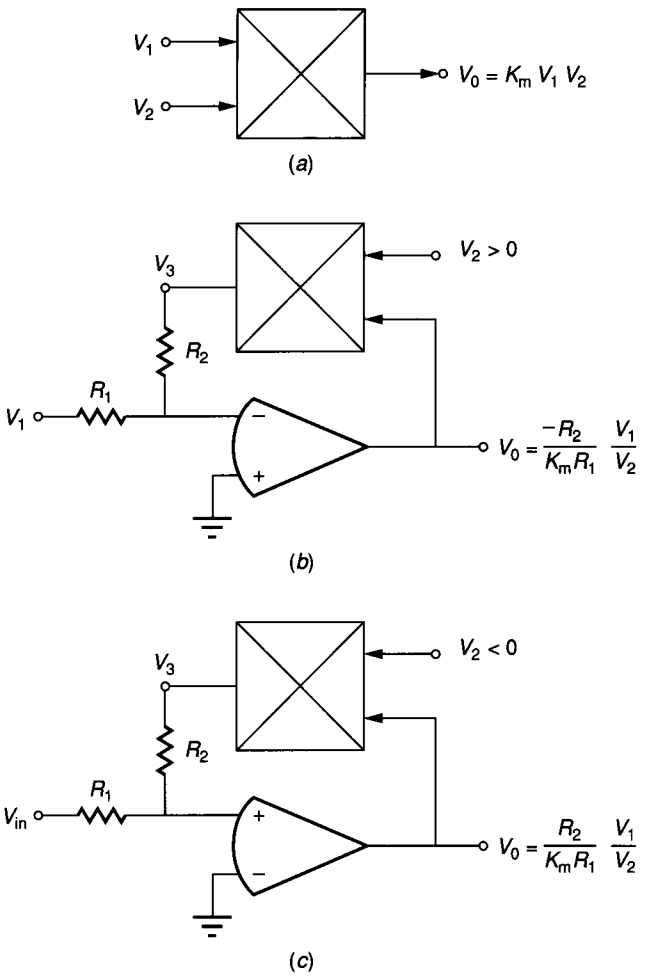


FIGURE 8.6-16
a) Block diagram symbol for a multiplier, (*b*) Negative divider, (*c*) Positive divider.

symbol for a multiplier. If the multiplier is placed in the feedback path of an inverting amplifier, as shown in Fig. 8.6-16*b*, then the output can be written as

$$V_O = \frac{-R_1}{K_m R_2}\left(\frac{V_1}{V_2}\right) \tag{8.6-53}$$

where $V_2 > 0$. If $V_2 < 0$ and the input terminals of the op amp are reversed, as indicated in Fig. 8.6-16*c*, a positive divider circuit is obtained. The phase margin of the op amp in Fig. 8.6-16 will be reduced because of the presence of the multiplier in the feedback path.

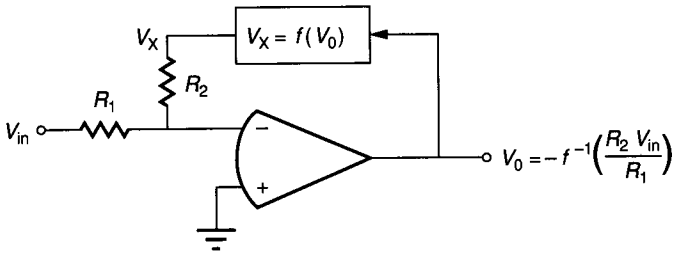


FIGURE 8.6-17
Illustration of the principle of creating the inverse function.

The principle used to develop the dividers of Fig. 8.6-16 can be generalized. This principle, illustrated in Fig. 8.6-17, is that if a functional block is placed in the feedback path of a circuit, the closed-loop response is the inverse of that function. In the previous case, division is the inverse of multiplication. If a circuit that generates the sine of an input is placed in the feedback path, the closed-loop transfer characteristic would be the inverse sine of the input.

A simple modulator compatible with MOS technology is shown in Fig. 8.6-18. If V_2 is greater than zero, then switches S2 and S3 are on and switches S1 and S4 are off. We see that the amplifier of Fig. 8.6-5 results, with the

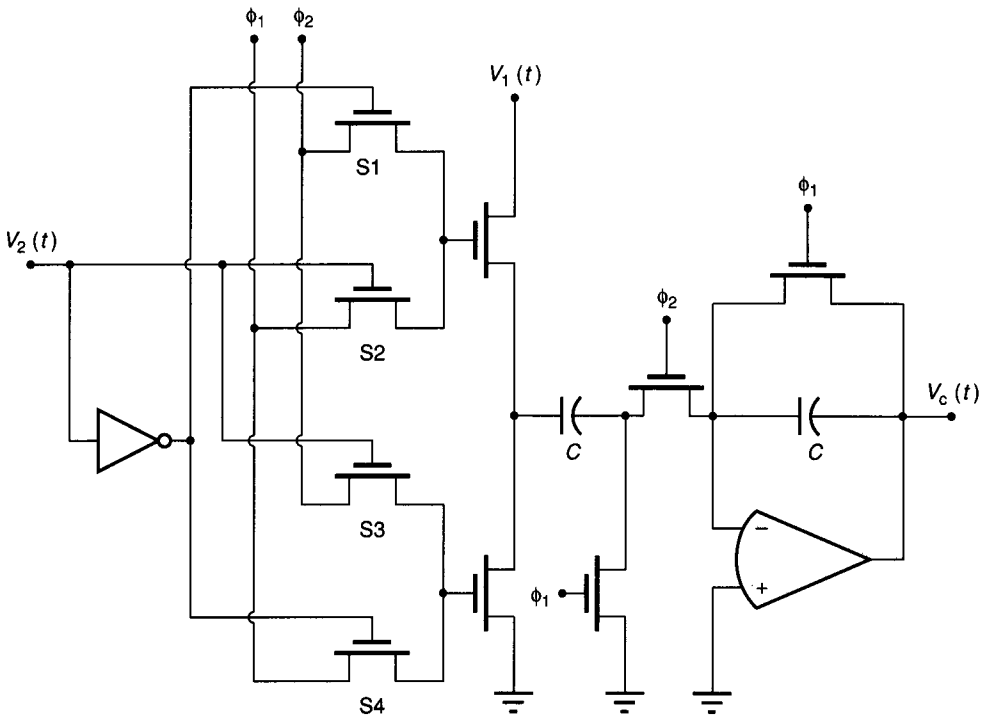


FIGURE 8.6-18
A modulator compatible with MOS technology.

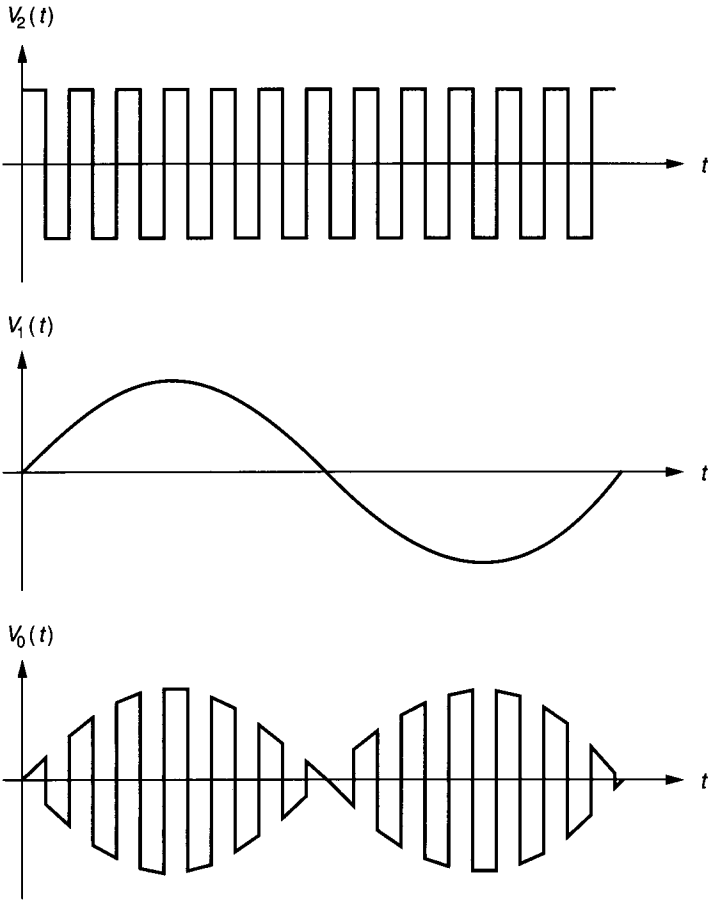


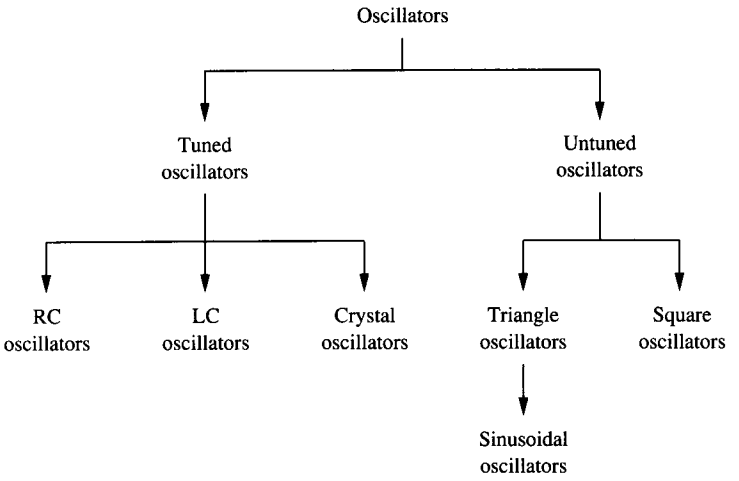
FIGURE 8.6-19
Illustration of the waveforms of Fig. 8.6-18 used as a modulator.

corresponding transfer function of Eq. 8.6-5. If V_2 is less than zero, then switches S1 and S4 are on and switches S2 and S3 are off. The phasing is reversed on the input switches, resulting in the inverting transfer function of Eq. 8.6-6. If the output is sampled and held, or if the high sampling approximation is valid, the effect of V_2 is to multiply V_1 by $+1$ when $V_2 > 0$ and by -1 when $V_2 < 0$. Figure 8.6-19 shows the waveforms of the modulator of Fig. 8.6-18 when V_1 is a sinusoid and V_2 is a square wave whose frequency is greater than that of the sinusoid but much less than the clock frequency of ϕ_1 and ϕ_2.

8.6.3 Oscillators

Oscillators are circuits that convert dc power into a periodic waveform or signal. Oscillators can be classified as shown in Table 8.6-1. The two general classes are tuned and untuned oscillators. Tuned oscillators produce nearly sinusoidal

TABLE 8.6-1
Classification of oscillators



outputs, whereas untuned oscillators produce square and/or triangle waveforms. Tuned oscillators can be further divided into RC, LC, and crystal oscillators. We shall only consider RC oscillators since these are most suitable for integrated circuit technology, although crystal oscillators are often employed with the crystal external to the integrated circuit. The outputs of the untuned oscillator are typically square waves and triangle waves. The untuned oscillator can create a sinusoid by applying the triangle wave to a sine-shaping circuit, such as the one considered in Prob. 8.40 or one made up from a sufficient number of piecewise linear line segments. The untuned oscillators are compatible with integrated circuit technology, which in part accounts for their widespread use. They are also capable of implementing a voltage-controlled oscillator (VCO), which has many uses in signal processing circuits. Due to lack of space, the considerations of oscillators will be limited. Much more information can be found in the references.[57–61]

The following discussion will consider both tuned and untuned oscillators. The principles of operation and an example will be given. Only oscillators that use op amps, capacitors, and resistors or resistor equivalents will be considered. Figure 8.6-20 shows a block diagram of a single-loop feedback system. This diagram consists of an amplifier (A), a feedback network (β), and a summing junction. The variables shown are V_S, V_F, V_I, and V_O which are the source, feedback, input, and output voltages, respectively. The + sign next to the feedback input to the summing junction indicates that the feedback is positive. If the circuit of Fig. 8.6-20 is assumed to be linear, the *loop gain*, G, is the voltage gain around the loop when $V_S = 0$ and is expressed as

$$G\big|_{V_S=0} = A\beta \tag{8.6-54}$$

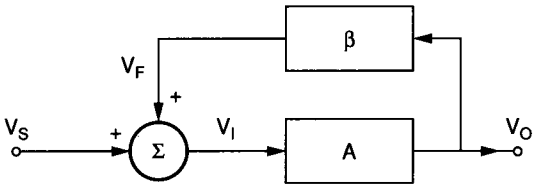


FIGURE 8.6-20
Block diagram of a single-loop feedback system.

The *closed-loop gain*, A_f, is equal to V_O/V_S and is given as

$$A_f = \frac{V_O}{V_S} = \frac{A}{1 - A\beta} = \frac{A}{1 - G} \tag{8.6-55}$$

The principle of a tuned oscillator can be seen from Eq. 8.6-55. If there is no input, $V_S = 0$, then for a finite output, V_O, Eq. 8.6-55 must be equal to infinity. This can only happen if $G = 1$. Thus, the criterion for oscillation in a tuned oscillator is

$$\text{Loop gain} = G(j\omega_0) = A(j\omega_0)\beta(j\omega_0) = 1 \tag{8.6-56}$$

where ω_0 is called the *radian frequency of oscillation*. An alternative form of Eq. 8.6-56 is

$$\text{Re}\,[G(j\omega_0)] + j\,\text{Im}\,[G(j\omega_0)] = 1 + j\,0 \tag{8.6-57}$$

or

$$|\,G(j\omega_0)\,|\,\angle\text{Arg}\,[G(j\omega_0)] = 1\angle 0° \tag{8.6-58}$$

In order to satisfy this criterion, the oscillator must be able to achieve a phase shift of 360° at some frequency, ω_0, where the loop gain is exactly unity. The analysis of oscillators is simple and consists of calculating the loop gain and using Eq. 8.6-56, 8.6-57, or 8.6-58 to find the frequency of oscillation, ω_0, and the magnitude of the amplifier gain, A, necessary for oscillation. Figure 8.6-21*a* shows an *RC* oscillator called the *Wien bridge oscillator*. This oscillator consists of an amplifier, whose gain is K, and a feedback network consisting of R_1, C_1, R_2, and C_2. Figure 8.6-21*b* shows how to open the feedback loop in order to calculate the loop gain, G. The key principle in opening the feedback loop is to do so at a point in the loop where the resistance looking forward in the loop is much greater than the resistance looking backward in the loop. In this case, the op amp in the noninverting configuration offers infinite resistance looking into the noninverting terminal. Note that the loop could also be broken at point A because resistance looking back into the op amp with negative feedback approaches zero. Assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the loop gain can be written as

$$G(s) = \frac{K(s/RC)}{s^2 + (3/RC)s + (1/RC)^2} \tag{8.6-59}$$

Substituting for s by $j\omega$ and equating to $1 + j\,0$ results in

$$G(j\omega_0) = \frac{jK\omega_0/RC}{[(1/RC)^2 - \omega_0^2] + j3\omega_0/RC} = 1 + j0 \tag{8.6-60}$$

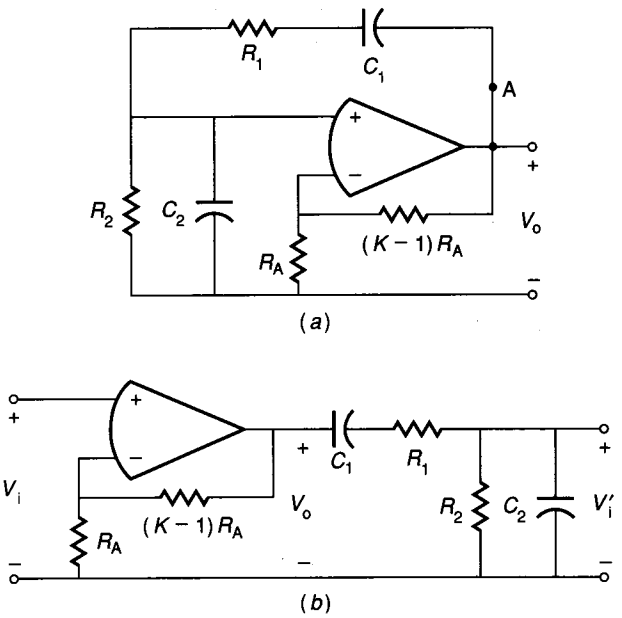


FIGURE 8.6-21
(*a*) Wien bridge *RC* oscillator, (*b*) Open-loop version of (*a*).

Equation 8.6-60 is satisfied if $K = 3$ at $\omega_0 = 1/RC$, which are precisely the conditions for oscillation of the oscillator of Fig. 8.6-21*a*. To obtain a 1 kHz oscillator, we could choose $C = 0.01$ μF, which gives $R = 15.9$ kΩ. Unfortunately, Fig. 8.6-21 is not practical for IC technologies unless the resistors were replaced with switched capacitors.

The amplitude of oscillation is indeterminate in the linear tuned oscillator. In practice, the amplitude of the oscillation is determined by a limiting nonlinearity. Figure 8.6-22 shows a possible nonlinear voltage transfer characteristic for the amplifier with gain K in Fig. 8.6-21*a*. For small values of V_O, the gain of the amplifier is designed to be greater than K (3 in the preceding example). When the gain is greater than 3, the amplitude of the sinusoidal oscillation grows. As the amplitude grows, the average gain over one cycle becomes smaller. The oscillator stabilizes at the amplitude where the time average gain is approximately equal to 3. If the amplitude should increase above this level for some reason, the oscillation will begin to decay because the effective gain is less than K. The amplitude stabilization is an important part of the oscillator. If the harmonic content of the sinusoid can be large, then the limiting effects of the power supplies can be used, although the waveform will no longer be sinusoidal. Many different schemes have been successfully used to achieve a stable oscillator amplitude. These include piecewise limiting circuits, thermistors, and the large signal transfer characteristics of differential amplifiers.

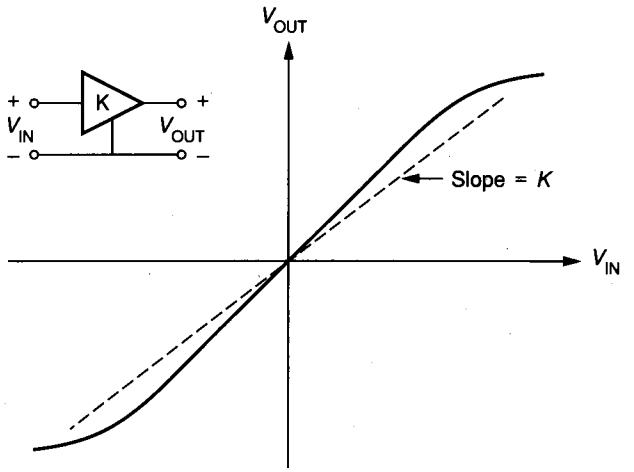


FIGURE 8.6-22
Nonlinear amplifier transfer function necessary for amplitude stabilization.

Because the RC products determine the oscillator frequency, the accuracy of an untrimmed integrated RC oscillator may not be sufficient. Switched capacitor techniques can be used to replace the resistors of the RC oscillators with resistor equivalents. Figure 8.6-23 shows a switched capacitor realization of the circuit of Fig. 8.6-21*a*. The resistor ratio, R_A/R_B, is assumed to be sufficiently accurate for this realization. If the high sampling assumption holds, then we may simply replace the resistor R with a switched capacitor equivalent resistance of T/C_R to get

$$\omega_0 \simeq \frac{C_R}{CT} = \frac{C_R}{C} f_c \tag{8.6-61}$$

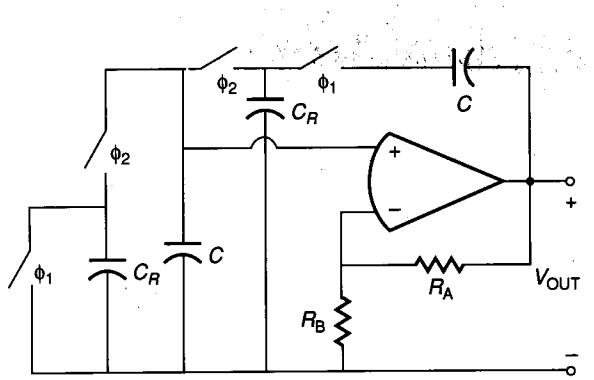


FIGURE 8.6-23
A switched capacitor realization of the Wien bridge RC oscillator of Fig. 8.6-21*a*.

We see that a switched capacitor implementation of an oscillator is really a circuit that scales the clock frequency to the oscillator frequency. The success of this implementation depends on the availability of a stable higher-frequency oscillator, f_c. The switched capacitor implementation also requires amplitude limiting.

The quadrature oscillator (see Prob. 8.42) is one in which switched capacitor techniques are suitable. The quadrature oscillator is essentially the Tow-Thomas realization of Fig. 8.4-11*c* with the $Q_i R$ resistor equal to infinity and the R/H_{oi} resistor removed. The result is a noninverting integrator and inverting integrator cascaded in a loop. The integrators of Sec. 8.5 could be used to achieve a switched capacitor implementation of the quadrature oscillator.

In general, the tuned oscillator is not widely used in integrated circuits for several reasons. The requirement for accurate RC products or an accurate clock is difficult to accomplish without using external components. The untuned oscillator or relaxation oscillator is more compatible with integrated circuit technology. The principle of operation can be seen from the block diagram of Fig. 8.6-24. This block diagram consists of an integrator cascaded with a bistable circuit. Although we have not yet discussed the realization of the bistable circuit, let us first consider the operation of Fig. 8.6-24. During the time interval from 0 to T_1, the integrator integrates the voltage L_+ provided by the bistable circuit. If K is the constant of integration, we find that the value of V_T at $t = T_1$ is given as

$$V_T(T_1) = S_- + K\int_0^{T_1} L_+ dt = S_- + KL_+T_1 = S_+ \qquad (8.6\text{-}62)$$

From Eq. 8.6-62, we may solve for the time, T_1, to get

$$T_1 = \frac{S_+ - S_-}{KL_+} \qquad (8.6\text{-}63)$$

We may solve for $V_T(T_2)$ using the same methods to get

$$V_T(T_2) = V_T(T_1) + K\int_{T_1}^{T_2} L_- dt = S_- + KT_2L_- = S_- \qquad (8.6\text{-}64)$$

Solving for T_2 gives

$$T_2 = \frac{S_- - S_+}{KL_-} \qquad (8.6\text{-}65)$$

The sum of T_1 and T_2 gives the period T and is written as

$$T = \frac{1}{f_o} = T_1 + T_2 = \left[\frac{S_+ - S_-}{K}\right]\left[\frac{1}{L_+} - \frac{1}{L_-}\right] = \frac{4S}{KL} \qquad (8.6\text{-}66)$$

if $L_+ = -L_- = L$ and $S_+ = -S_- = S$.

The above equations show that the bistable is a key element in the untuned oscillator. The bistable is a circuit that has two stable output states and exhibits

hysteresis when switching between the two states. Bistables may be clockwise or counterclockwise and can be shifted from the origin. Figure 8.6-25 shows the two possible generalized bistable characteristics. In this case, $L_+ = V_Y + V_L, L_- = V_Y - V_L, S_+ = V_X + V_H$, and $S_- = V_X - V_H$. Generally, $L_+ = L_-$ and $S_+ = S_-$. Figure 8.6-26*a* shows a realization of a clockwise (CW) bistable. If the output, V_S, is equal to V_{HH} (the positive power supply for the op amp), then the voltage at the noninverting input of the op amp is $V_{HH}R_3/(R_2 + R_3)$. If the input, V_T, is less than this value, then the output is in fact equal to V_{HH}. However, if V_T

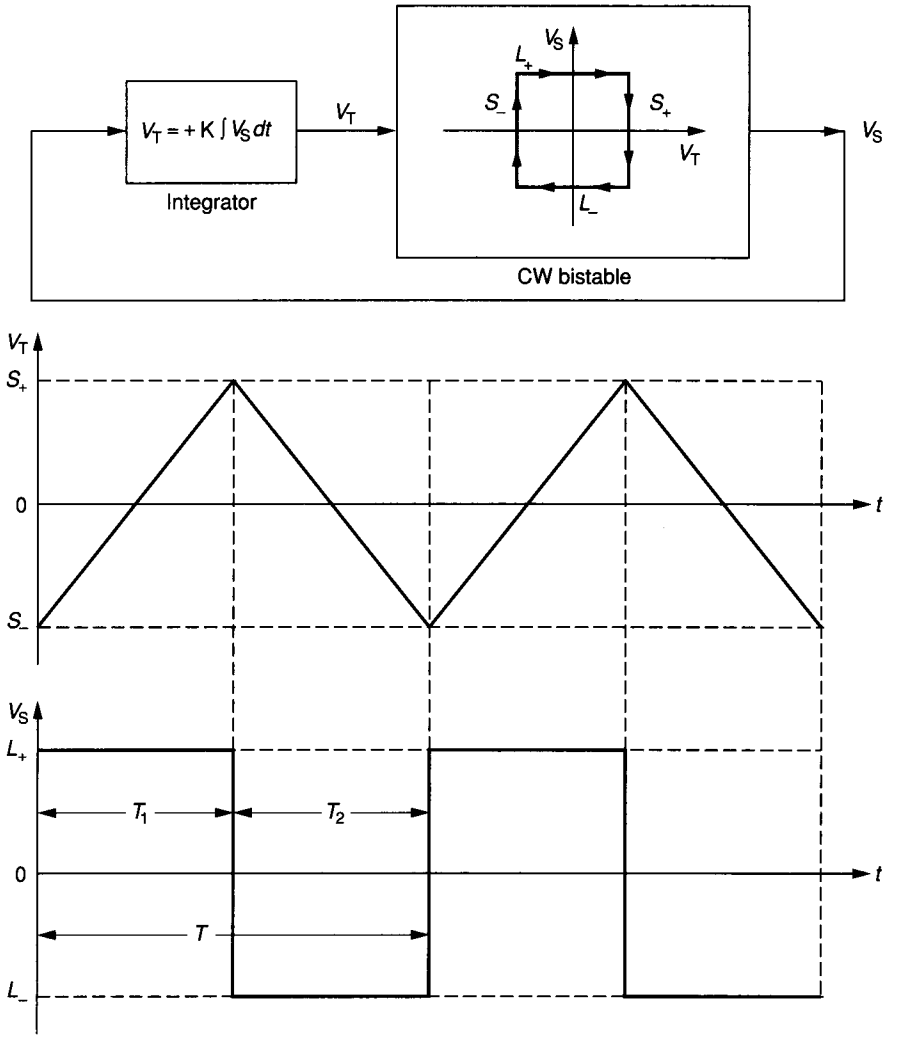


FIGURE 8.6-24
Block diagram of an untuned oscillator and the resulting waveforms.

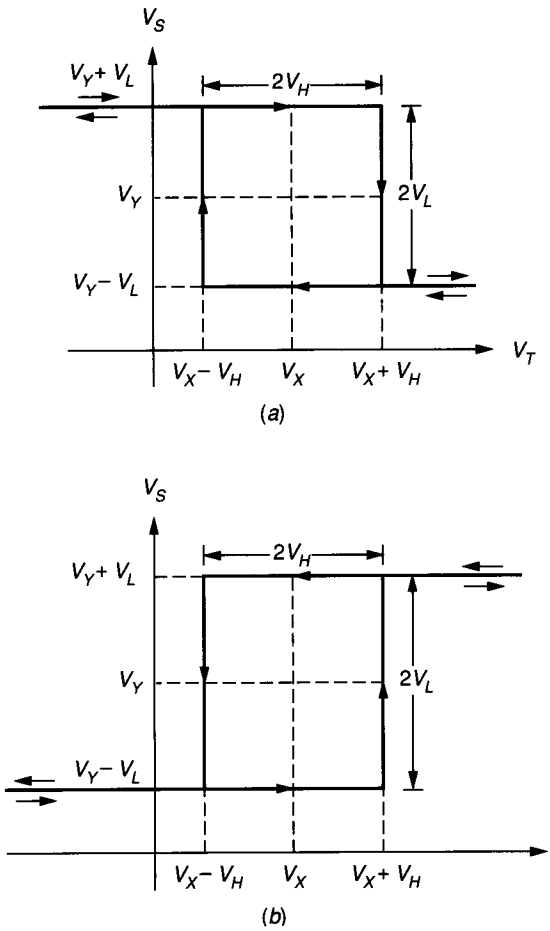


FIGURE 8.6-25
(*a*) CW bistable characteristic, (*b*) CCW bistable characteristic.

increases above this value from below, then the output voltage switches to V_{LL} (the negative power supply of the op amp) and voltage at the noninverting input changes to $V_{LL}R_3/(R_2 + R_3)$. From this discussion we see that $L_+ = V_{HH}, L_- = V_{LL}, S_+ = V_{HH}R_3/(R_2 + R_3)$, and $S_- = V_{LL}R_3/(R_2 + R_3)$. If possible, it is desirable to limit the output of the op amp to a voltage less than the power supplies.

The inverting input of the circuit of Fig. 8.6-26*a* could be grounded and the voltage V_T applied to the grounded end of R_3 to realize a counterclockwise (CCW) bistable. However, consider Fig. 8.6-26*b*, which shows a CCW bistable that limits the op amp swings to less than the power supplies. It can be shown that $L_+ = -R_6V_{LL}/R_7, L_- = -R_5V_{HH}/R_4, S_+ = -R_2(L_-)/R_3$, and $S_- = -R_2(L_+)/R_3$. Diodes D1 and D2 serve to keep the output of op amp A1 from swinging from V_{HH} to V_{LL}, thus permitting quick transition of states.

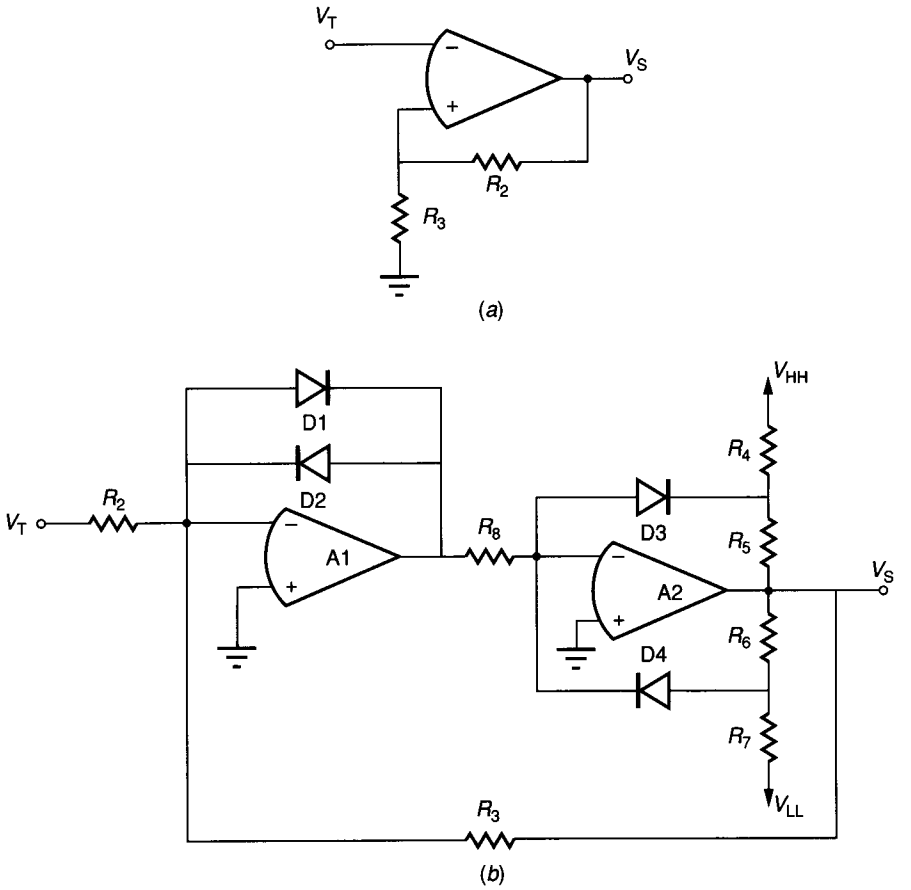


FIGURE 8.6-26
(*a*) Simple CW bistable, (*b*) CCW bistable with internal limiting.

A bistable circuit can also be implemented using switched capacitor techniques. Figure 8.6-27 shows a realization of the bistable characteristics of Fig. 8.6-25. The upper circuit, consisting of op amps 1 and 2, implements a switched capacitor amplifier with a sample-and-hold at the output and the ability to change the sign of the gain of the upper input, depending upon the output of comparator 3. The inputs to the comparator are the bistable input, V_T, and the output of the amplifier above, V_{TH}. The lower amplifier is similar to the upper amplifier. C_1 and C_2 are equivalent to the series switched capacitor simulations for a resistor. The discrete time voltages V_{TH}, V_C, and V_S are given as follows using the notation of Fig. 8.6-25.

$$V_{TH}(z) = \left\{ \frac{C_{12}}{C_1} V_{HH} + [\operatorname{sgn} V_C(z)] \left(\frac{C_{11}}{C_1} \right) V_{HH} \right\} z^{-1}$$

$$= \{ V_X + [\operatorname{sgn} V_C(z)] V_H \} z^{-1} \quad (8.6\text{-}67)$$

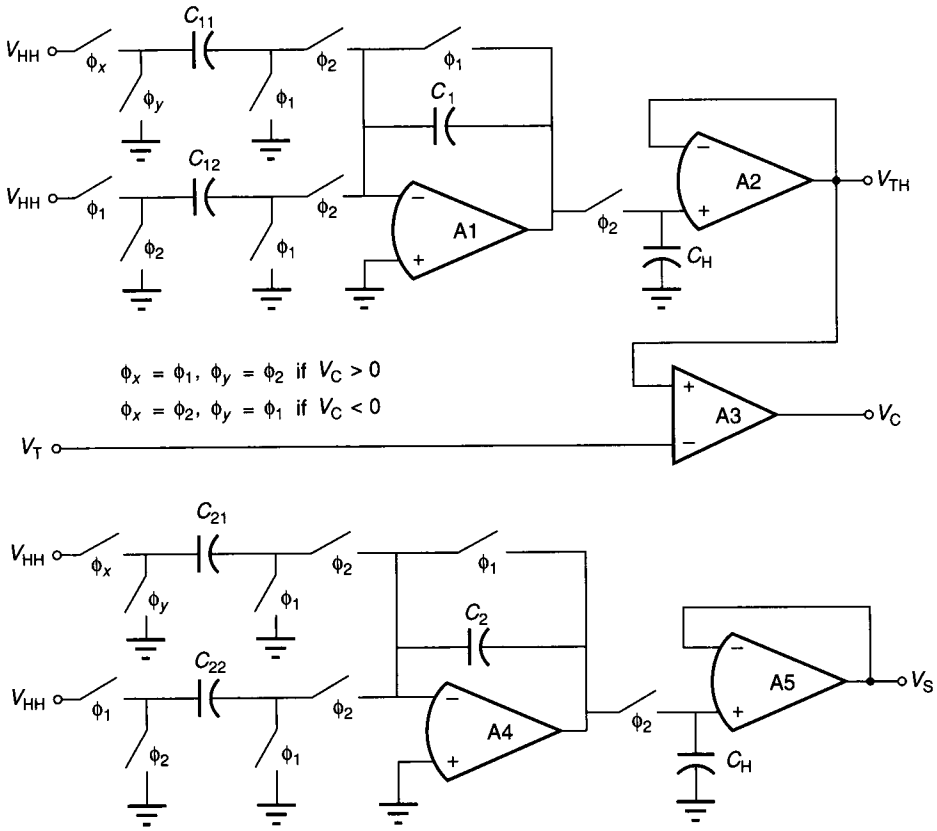


FIGURE 8.6-27
A switched capacitor implementation of the bistables of Fig. 8.6-25.

$$V_C(z) = \text{sgn}\{[V_{TH}(z) - V_T(z)]\} V_{HH} \tag{8.6-68}$$

and

$$V_S(z) = \left\{ \frac{C_{22}}{C_2} V_{HH} + [\text{sgn } V_C(z)] \left(\frac{C_{21}}{C_2} \right) V_{HH} \right\} z^{-1}$$

$$= \{ V_Y + [\text{sgn } V_C(z)] V_L \} z^{-1} \tag{8.6-69}$$

where sgn x is 1 if $x > 0$ and -1 if $x < 0$. A CW bistable characteristic is obtained when the ϕ_X and ϕ_Y of the C_{21} switched capacitor are as shown in Fig. 8.6-27 where V_T is the input and V_S is the output. If ϕ_X and ϕ_Y are reversed, then a CCW bistable is obtained. It is observed that the bistable characteristics are completely general and can be shifted as desired by varying the appropriate V_{HH}, by adjusting the capacitor ratios, and/or by changing ϕ_X and ϕ_Y of C_{21}.

The solid portion of Fig. 8.6-28 shows a simplified implementation of a CW bistable circuit based on the concepts of Fig. 8.6-27. It can be shown that the second amplifier is not needed for a CW bistable characteristic with V_X and

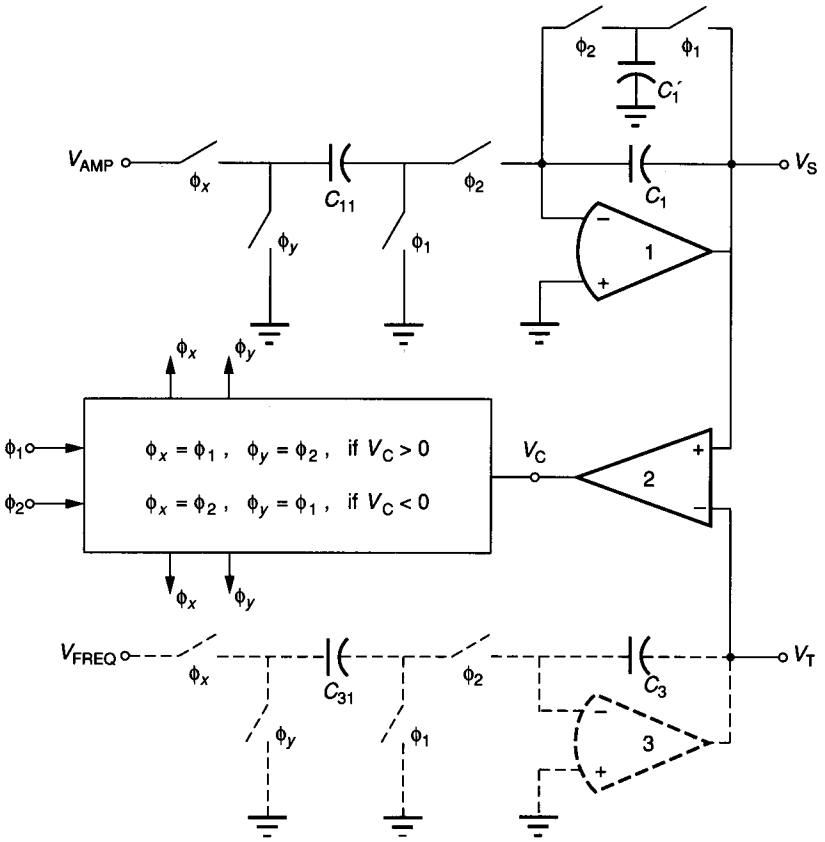


FIGURE 8.6-28
Simplified CW bistable circuit. The dotted portion is required for the waveform generator implementation.

V_Y of Fig. 8.6-25 equal to zero. The output is taken at V_S and the input is applied at V_T. The notation ϕ_X and ϕ_Y implies that these clocks are reversed depending upon the sign of V_C. For the case of Fig. 8.6-28, $\phi_X = \phi_1$ and $\phi_Y = \phi_2$ will give a noninverting gain. The phase reversal circuit can be implemented using the ideas represented in Fig. 8.6-18.

The bistable can now be combined with the proper type of integrator (noninverting or inverting) to achieve an implementation of the untuned oscillator block diagram of Fig. 8.6-24. An untuned oscillator using the CCW bistable of Fig. 8.6-26*b* and an inverting integrator is shown in Fig. 8.6-29. The integrating constant K is equal to $1/(R_1C_1)$, and the various limits of the bistable have already been shown to be $L_+ = -R_6V_{LL}/R_7, L_- = -R_5V_{HH}/R_4, S_+ = -R_2L/R_3$, and $S_- = -R_2L_+/R_3$. For example, if $V_{HH} = -V_{LL} = 15$ V, $R_1 = 100$ kΩ, $C_1 = 1$ nF, $R_2 = R_3 = 100$ kΩ, $R_4 = R_7 = 30$ kΩ, and $R_5 = R_6 = 20$ kΩ, then $L_+ = -L_- = S_+ = -S_- = 10$ V. From Eq. 8.6-66 we find that the frequency of

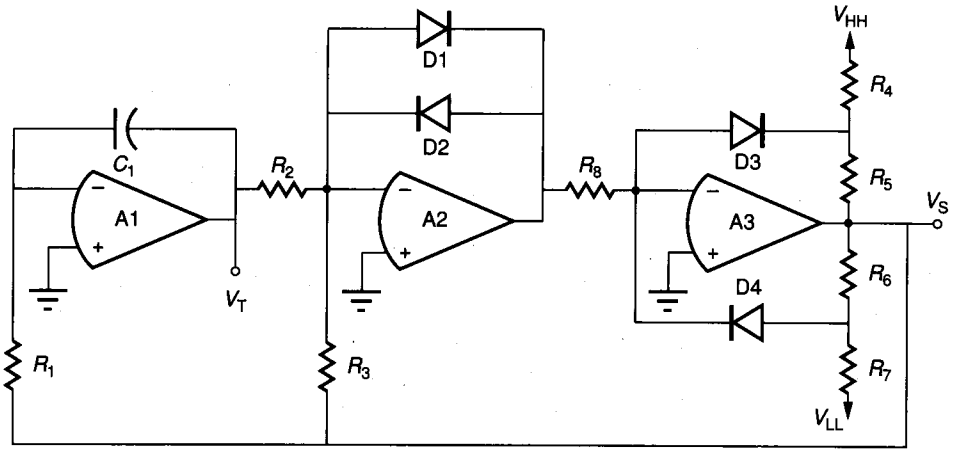


FIGURE 8.6-29
Untuned oscillator using the bistable of Fig. 8.6-26*b*.

oscillation, f_o, is 2500 Hz. Although the circuit of Fig. 8.6-29 is presented to illustrate concepts and is not practical for integration, the reader should be able to convert it to a form suitable for integration.

One of the advantages of an untuned oscillator is that the frequency can be easily controlled by a voltage. Figure 8.6-30 shows an example of how this might be accomplished. The output voltage, V_S, is used to connect the inverting integrator to a positive or negative value of a voltage called V_M. The limits of V_S effectively become $L_+ = -L_- = V_M$. Thus, the frequency of the untuned oscillator as developed in Eq. 8.6-66 becomes

$$f_o = \frac{V_M}{2R_1C_1(S_+ - S_-)} = \frac{V_M}{4R_1C_1S} \tag{8.6-70}$$

where $S = S_+ = -S_-$. The range of the control or modulating voltage, V_M, will be from the power supplies to the point at which op amp offsets become significant. Consequently, this voltage-controlled oscillator (VCO) should have two to three decades of frequency range. Other methods of controlling the oscillator frequency include a diode bridge[62] and current-controlled multivibrators.[63]

Many of the components of Fig. 8.6-29 can be removed, at the expense of some deterioration of the performance. Figure 8.6-31*a* shows an example of an untuned oscillator using only a single op amp. The analysis of this oscillator starts by assuming that the output is at L_+. Consequently, the voltage at the positive input terminal of the op amp is $R_3L_+/(R_2 + R_3) = \alpha L_+$. If V_1 is less than this voltage, then C_1 will begin to charge to L_+ through R_1. However, when V_1 is equal to αL_+, the output of the op amp switches to L_-. Now the voltage at the positive input terminal of the op amp is αL_-. Since this voltage is less than V_1, C_1 begins to discharge toward L_- through R_1. From

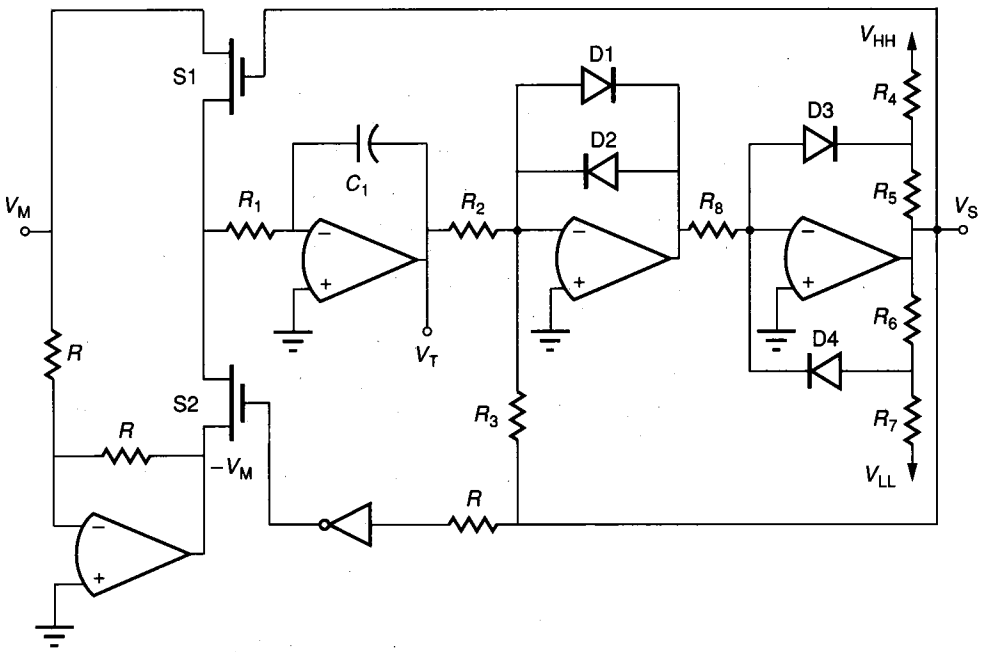


FIGURE 8.6-30
Voltage-controlled oscillator using the untuned oscillator of Fig. 8.6-29.

this analysis we see that $S_+ = \alpha L_+$ and $S_- = \alpha L_-$. The waveform at V_1 is no longer triangular but is exponential. It can be shown that the frequency of oscillation is

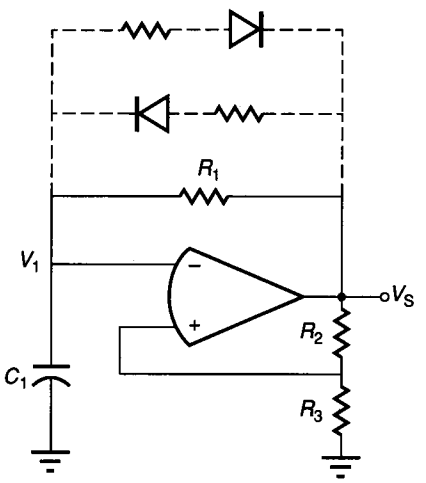
$$f_o = \frac{1}{2R_1C_1 \ln [(1 + \alpha)/(1 - \alpha)]} \tag{8.6-71}$$

where $\alpha = R_3/(R_2 + R_3)$. The square wave can be made asymmetrical through the use of diodes and resistors, as indicated in Fig. 8.6-31 in the dotted portion of the figure.

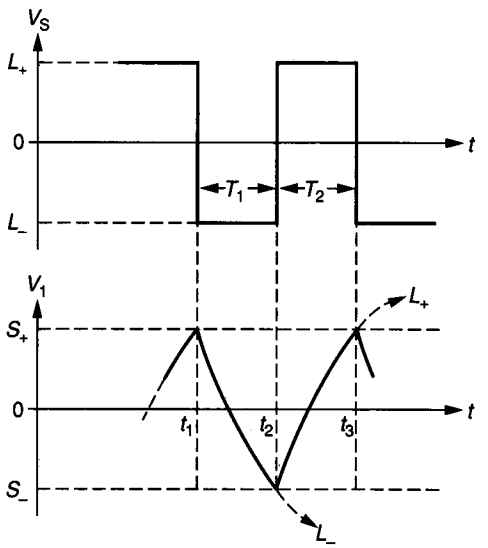
The switched capacitor bistable can also be used to implement an untuned oscillator that can be controlled by a voltage. This untuned oscillator is shown in Fig. 8.6-28 if the dotted portion is included. The amplifier of this realization uses a scheme to avoid requiring the op amp output to be zeroed during each clock cycle. The use of a parallel switched capacitor resistor realization in shunt with C_1 gives the following discrete time transfer function from V_{AMP} to V_S.

$$\frac{V_S(z)}{V_{AMP}(z)} = \frac{[\text{sgn } V_C(z)](C_{11}/C_1)z^{-1}}{1 - z^{-1}(1 - C'_1/C_1)} = [\text{sgn } V_C(z)]\left(\frac{C_{11}}{C_1}\right)z^{-1} \tag{8.6-72}$$

if $C_1 = C'_1$. C'_1 opposes the charge being transferred from C_{11} to C_1. Only the charge difference on C_{11} between consecutive samples is transferred. As a



(a)



(b)

FIGURE 8.6-31
(*a*) Simple untuned oscillator, (*b*) Waveforms of *a*.

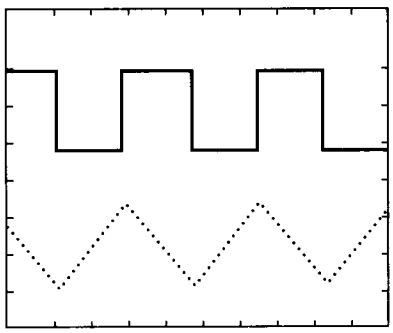
result, the op amp output voltage changes only by the difference in the input voltage multiplied by the gain factor of the amplifier. The circuit of Fig. 8.6-28 functions as a VCO where the amplitude and frequency of the square and triangle waveforms are given as

$$\text{Amplitude} = \left(\frac{C_{11}}{C_1}\right) V_{\text{AMP}}(t) \tag{8.6-73}$$

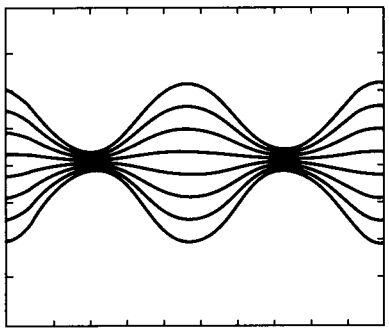
and

$$f_o = \left(\frac{C_1 C_{31} f_c}{4 C_3 C_{11}}\right) \frac{V_{\text{FREQ}}(t)}{V_{\text{AMP}}(t)} \tag{8.6-74}$$

It is seen that the switched capacitor VCO of Fig. 8.6-28 is capable of both amplitude and frequency modulation. Amplitude modulation is accomplished by connecting both $V_{FREQ}(t)$ and $V_{AMP}(t)$ to the source of modulation. Frequency modulation is accomplished by connecting only $V_{FREQ}(t)$ to the source of modulation and keeping $V_{AMP}(t)$ constant. Figure 8.6-32 shows the waveforms of the circuit of Fig. 8.6-28 used as an unmodulated, untuned oscillator, an amplitude-modulated oscillator, and a frequency-modulated oscillator (VCO).[64]



(*a*)



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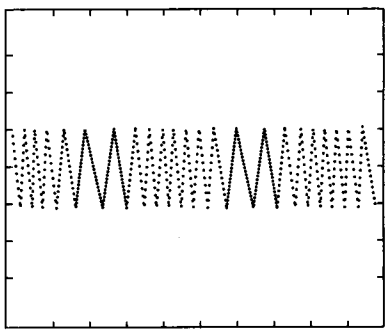


(*c*)

FIGURE 8.6-32
Drawings of actual oscilloscope waveforms. (*a*) Square and triangle waveforms, (*b*) Use of the circuit of Fig. 8.6-28 for amplitude modulation, (*c*) Use of the circuit of Fig. 8.6-28 for frequency modulation.

There are many other oscillators compatible with integrated circuit technology that have not been presented here. They include ring oscillators, constant-current oscillators, and multivibrators, including collector (drain) or emitter (source) coupled multivibrators. Other performance aspects of oscillators, including their temperature and power supply stability, has not been covered. These subjects are addressed in the technical literature.

8.6.4 Phased-Locked Loops

The last circuit we will consider in this section is the phase-locked loop (PLL). The phase-locked loop consists of a voltage controlled oscillator (VCO) whose frequency is equal to the frequency of the PLL input. The voltage controlling the VCO should vary monotonically with the frequency of the input to the PLL. A block diagram of a phase-locked loop is shown in Fig. 8.6-33. It is seen that a phase-locked loop consists of a negative feedback loop in which the output of a phase detector is applied to the control input of a VCO. The VCO applies a periodic waveform to the phase detector, the phase of which is compared with the phase of the input signal. The phase-locked loop has many applications, such as FM demodulation, frequency synchronization, signal conditioning, frequency multiplication and division, frequency translation, and AM detection.

A more detailed block diagram of the phase-locked loop is shown in Fig. 8.6-34. In the following analysis, the phase-locked loop is assumed to be locked. The input signal is assumed to be a sinusoid given as

$$V_{IN}(t) = V_p \sin(\omega t + \theta_i) \tag{8.6-75}$$

If the phase shift of the signal at the output of the VCO is θ_{osc}, then the average value of the output of the phase detector is

$$V_B = K_d(\theta_i - \theta_{osc}) \tag{8.6-76}$$

where θ_i and θ_{osc} are phase shifts with respect to an arbitrary reference. The phase of the signal at the output of the VCO as a function of time is equal to

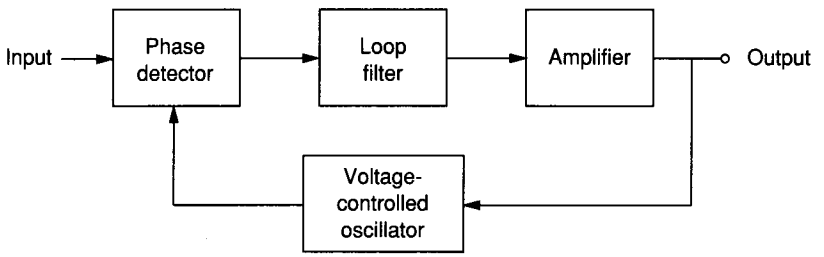


FIGURE 8.6-33
Block diagram of a phase-locked loop.

the integral of the frequency of the VCO, which can be expressed in differential form as

$$\omega_{osc}(t) = \frac{d\theta_{osc}(t)}{dt} \tag{8.6-77}$$

Thus, in the block diagram of Fig. 8.6-34, this integration is represented in the VCO block as $1/s$. If we assume that the oscillator frequency is given as

$$\omega_{osc} = \omega_o + K_o V_O \tag{8.6-78}$$

where ω_o is the free-running frequency of the oscillator when $V_O = 0$, then the transfer function of the phase-locked loop becomes

$$\frac{V_O(s)}{\theta_i(s)} = \frac{sK_dF(s)A}{s + K_dK_oAF(s)} \tag{8.6-79}$$

or

$$\frac{V_O(s)}{\omega_i(s)} = \frac{V_O(s)}{s\theta_i(s)} = \frac{K_dF(s)A}{s + K_dK_oAF(s)} \tag{8.6-80}$$

If $F(s) = 1$, then the loop inherently has a first-order, low-pass transfer response. The loop bandwidth is defined as $K_v = K_oK_dA$. Various types of filters have been used to achieve different dynamic performances for the phase-locked loop.[65]

The loop lock range is defined as the range of frequencies about ω_o for which the phase-locked loop maintains the relationship:

$$\omega_i = \omega_{osc} \tag{8.6-81}$$

If the phase detector can determine the phase difference between θ_i and θ_{osc} over a $\pm\pi/2$ range, then the loop lock range is expressed as

$$\omega_L = \pm\Delta\omega_{osc} = K_dAK_o(\pm\pi/2) = \pm K_v(\pi/2) \tag{8.6-82}$$

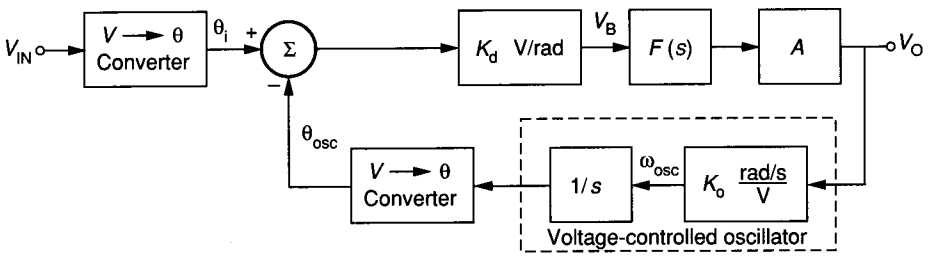


FIGURE 8.6-34
More detailed block diagram of a phased-locked loop.

The capture range is the range of input frequencies for which an initially unlocked loop will lock on an input signal. If $F(s) = 1$, then the capture range is equal to the lock range. If $F(s) = (1 + s/\omega_1)^{-1}$, then the capture range is less than the lock range. If the capture range is designated as $2\omega_C$, then Fig. 8.6-35 illustrates the relationships between the loop and capture ranges of a phase-locked loop with $F(s) = (1 + s/\omega_1)^{-1}$. The loop and capture ranges are very dependent on the loop bandwidth, K_v. If K_v decreases, the capture time increases, the capture range decreases, and the interference rejection properties of the phase-locked loop improve. The blocks shown in Fig. 8.6-34 can be implemented by circuits that we have examined previously in this chapter or in Chapter 6 for both MOS and BJT technologies.

Circuits that are representative of analog processing circuits have been introduced in this section. These circuits included the precision breakpoint circuit, multipliers and modulators, oscillators, and phase-locked loops. At this point the reader has a sufficient repertoire of circuits to undertake the design of systems using analog processing circuits or to undertake the design of a different type of analog signal processing circuit.

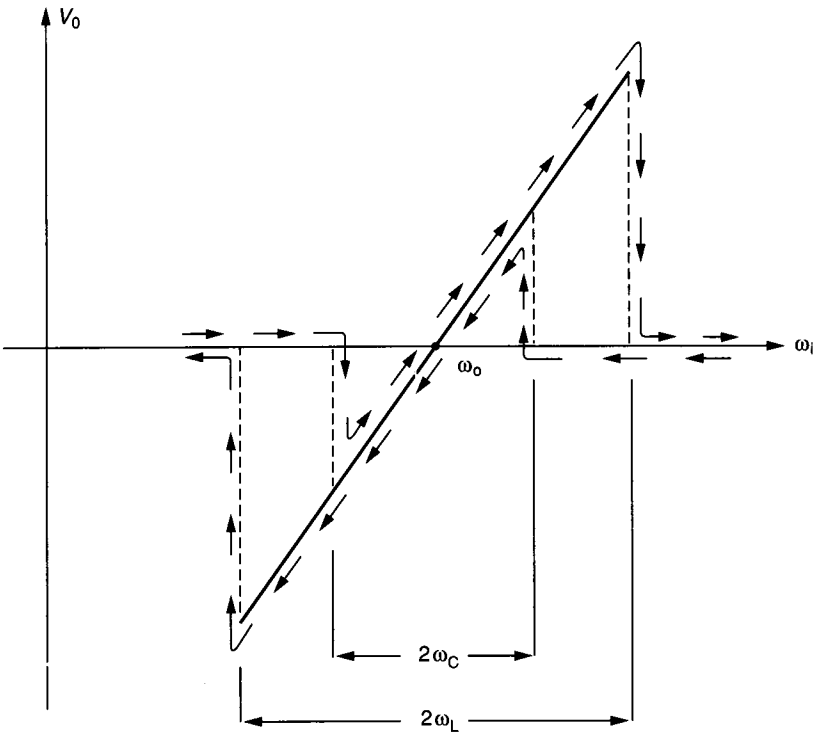


FIGURE 8.6-35
Illustration of the loop and capture ranges for a phase-locked loop.

8.7 SUMMARY

This chapter has introduced the elements of analog systems. An introduction to analog signal processing showed the important relationships between digital circuits, analog circuits, BJT technology, and MOS technology. It was seen that there is likely to be a mixture of digital and analog circuit techniques to implement signal processing systems. The selection of the appropriate technique is decided by many factors, including space, performance, and technology compatibility. The existence of technologies combining both BJT and MOS technologies offers some exciting advantages to the circuit and system designer.

Next, techniques of interfacing analog and digital circuits were presented. This subject was divided into digital-to-analog converters and analog-to-digital converters. The performance of the various types of converters was reviewed, followed by a consideration of current-scaling, voltage-scaling, charge-scaling, combination-scaling, and serial digital-to-analog converters. Analog-to-digital converters were presented, with the serial, successive approximation, parallel, and high performance analog-to-digital architectures considered.

One of the largest applications of analog circuits at the present is linear filtering. A review of continuous-time filters was presented, followed by a discussion of switched capacitor filters. The switched capacitor circuit technique is a practical adaptation of circuit design methods to match the technology, once again demonstrating the important influence of technology upon circuits and systems design. The key aspect of switched capacitor circuits is that equivalent RC products become equal to the product of capacitor ratios and an external clock frequency. This results in time constant accuracies as good as 0.1%. Three switched capacitor filter design approaches were presented; resistor replacement or substitution, passive RLC prototype based ladder synthesis, and direct realization of the filter in the z-domain.

The chapter concluded with a section on analog signal processing circuits. A number of nonfilter circuits were examined. These included waveshaping or precision breakpoint circuits; multipliers and modulators; oscillators, including tuned and untuned oscillators; and phase-locked loops. These are examples of circuits that might be used to implement a signal processing system. The boundary between a circuit and a system is very fuzzy. The topics presented in this chapter could be considered circuits from one viewpoint and systems from another. We have chosen to emphasize the circuit viewpoint over the application.

In closing, we will consider a signal processing system and examine how the design of such a system is hierarchically organized. Figure 8.7-1 shows a block diagram of an integrated circuit modem. A modem is a system that converts outgoing data in the form of a serial bit string to a form suitable for transmission over telephone lines and also converts the incoming data back to a serial bit string. This is a challenging problem because of the limited bandwidth of the telephone system and the desire to transmit data at as high a bit rate as possible. The particular modem considered is a 1200 bits/second, full-duplex, voice-band modem.[66] This system represents a reasonably complex design in terms of man-months of effort.

The details of the design of the modem will not be considered. Rather, the emphasis here will be on how the system is broken into smaller blocks that

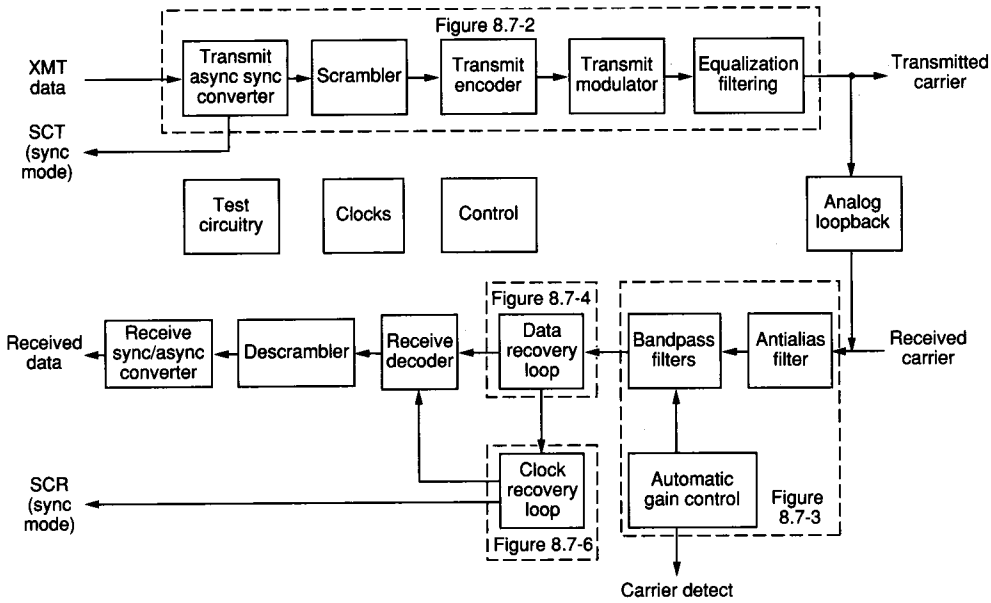


FIGURE 8.7-1
Integrated modem block diagram.

ultimately are recognizable as circuits we have considered in our study. For example, the transmitter is shown in more detail in Fig. 8.7-2. Here some of the blocks are recognizable, such as the filters, the mixers, and the summer. The asynchronous-to-synchronous converter, the scrambler, and the phase encoder are implemented by digital techniques such as those discussed in Chapters 7 and 9. The first part of the receiver channel is the automatic gain control circuit shown in Fig. 8.7-3. The analog blocks in this figure include filters, a full-wave rectifier (see Probs. 8.32 and 8.34), and a comparator.

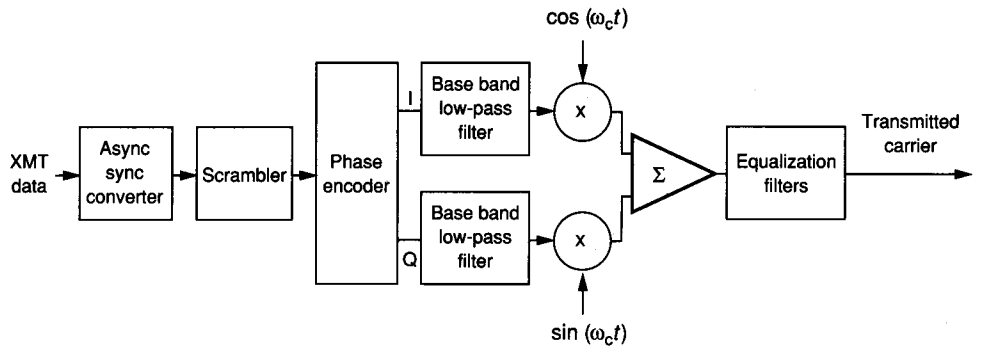


FIGURE 8.7-2
Differential QPSK transmitter.

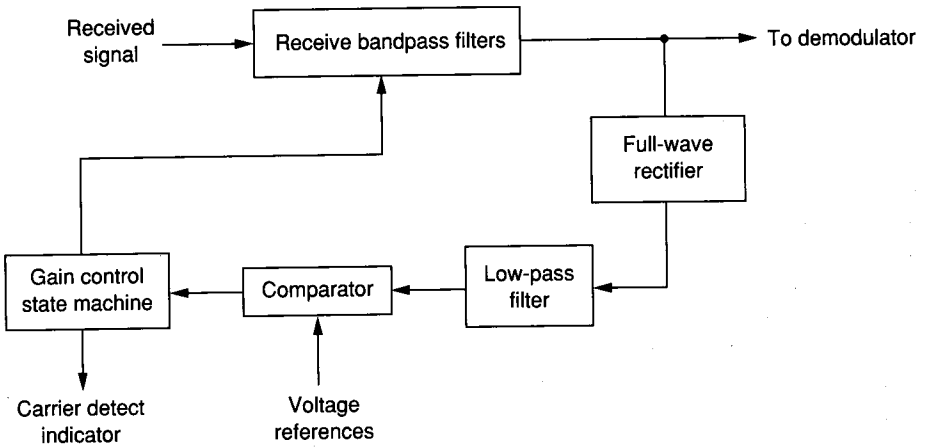


FIGURE 8.7-3
Automatic gain control circuit.

The next part of the receiver channel is called the data recovery loop and is implemented by a Costas phase-locked loop that preprocesses the received signals through Hilbert filters, as shown in Fig. 8.7-4. The Hilbert filters consist of two parallel filters, one shifted by 90° compared to the other. The data recovery loop consists of many analog circuits that have been previously considered, including

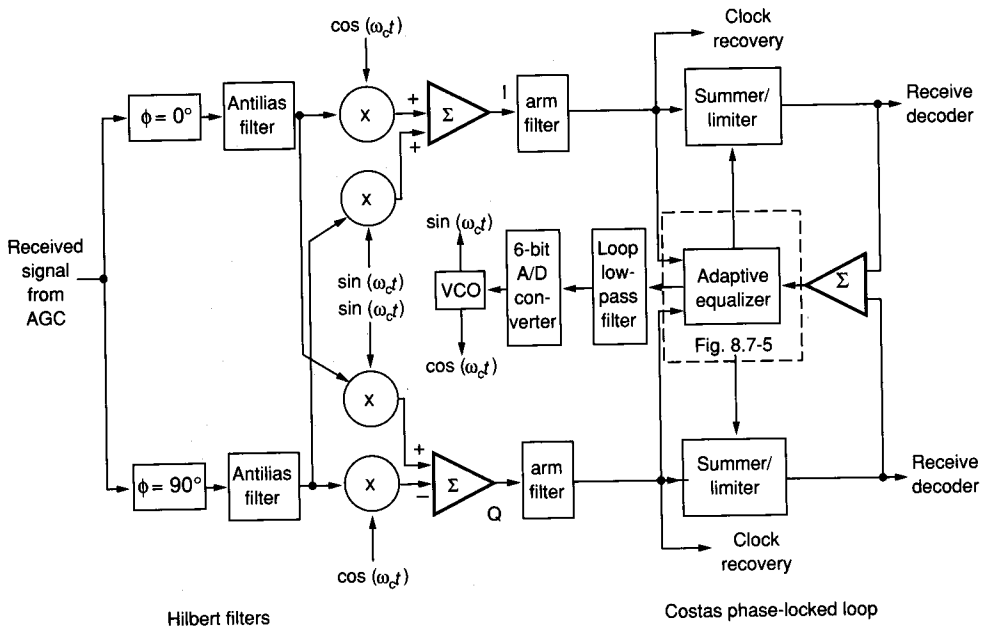
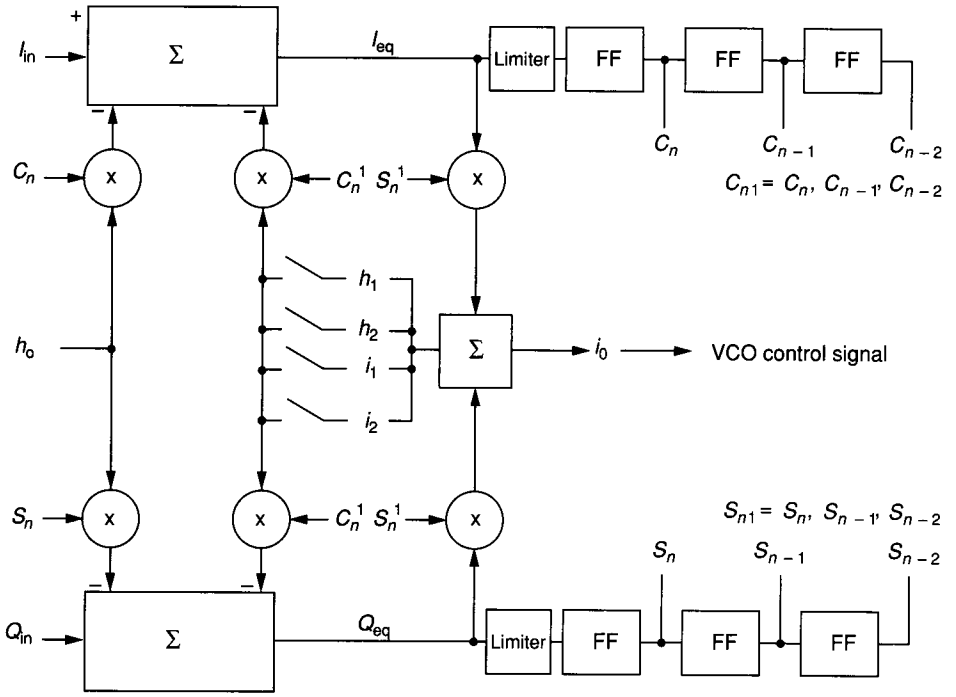


FIGURE 8.7-4
Coherent QPSK demodulation.

a 6-bit A/D converter. The adaptive equalizer of the data recovery loop is shown in more detail in Fig. 8.7-5, where we see a combination of analog and digital circuits. Another part of the receiver channel containing analog circuits is the clock recovery loop, shown in Fig. 8.7-6. The switched capacitor implementation of a part of this loop is illustrated in Fig. 8.7-7.

Figure 8.7-8 shows a photograph of the integrated circuit modem. This modem was implemented in an NMOS technology and used about 11,000 transistors. The modem used approximately 60 op amps and had a power dissipation of 750 mW. A CMOS version has reduced the power consumption significantly.

This example illustrates the hierarchy and decomposition of a system into circuits and similar components. Many other examples exist, such as speech processing circuits, other telecommunications circuits, and automotive control systems. One of the difficult problems facing the system designer is the simultaneous simulation of both the digital and analog parts of the system. In many cases, only partial simulation is possible.



$$I_{eq} = I_{in} - C_{n-2}h_2 - C_{n-1}h_1 - S_{n-2}i_2 - S_{n-1}i_1$$

$$Q_{eq} = Q_{in} - S_{n-2}h_2 - S_{n-1}h_1 + C_{n-2}i_2 - C_{n-1}i_1$$

$$\Delta i_o = K((I_{eq} - C_n h_o)S_n - (Q_{eq} - S_n h_o)C_n)$$

Where $h(t)$ = in phase impulse response

$i(t)$ = cross channel impulse response

FIGURE 8.7-5
Adaptive equalizer.

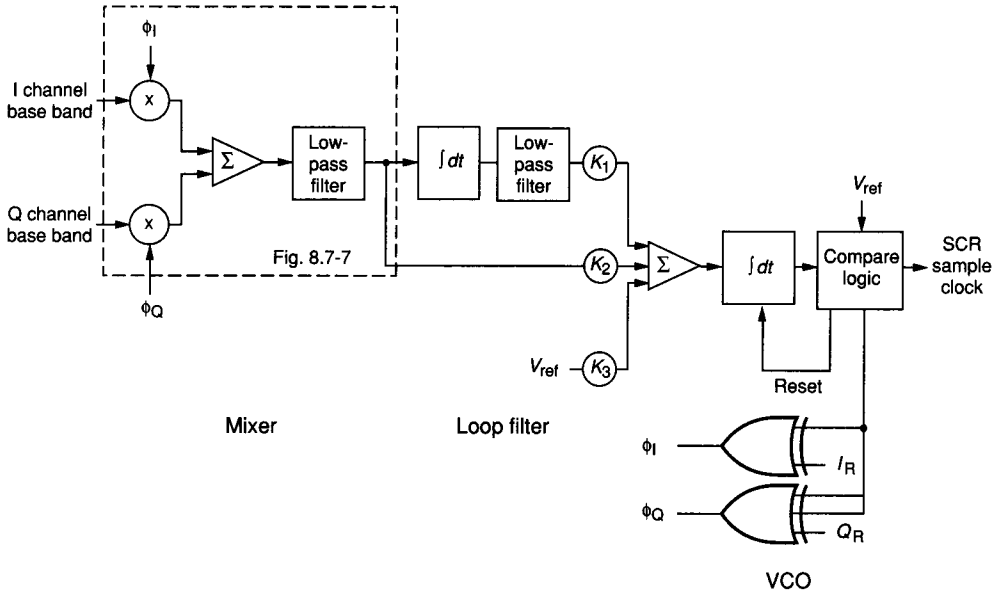


FIGURE 8.7-6
Clock recovery phase-locked loop.

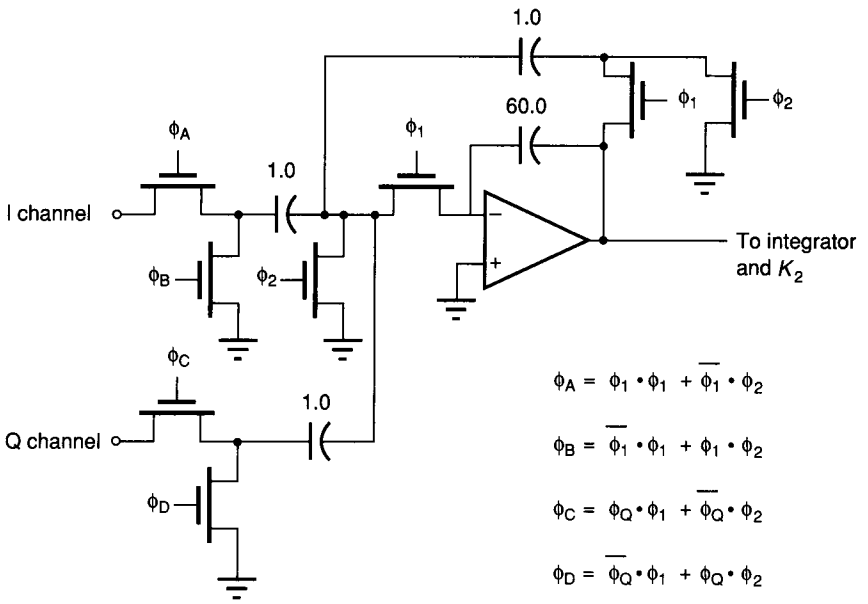


FIGURE 8.7-7
Clock PLL input.

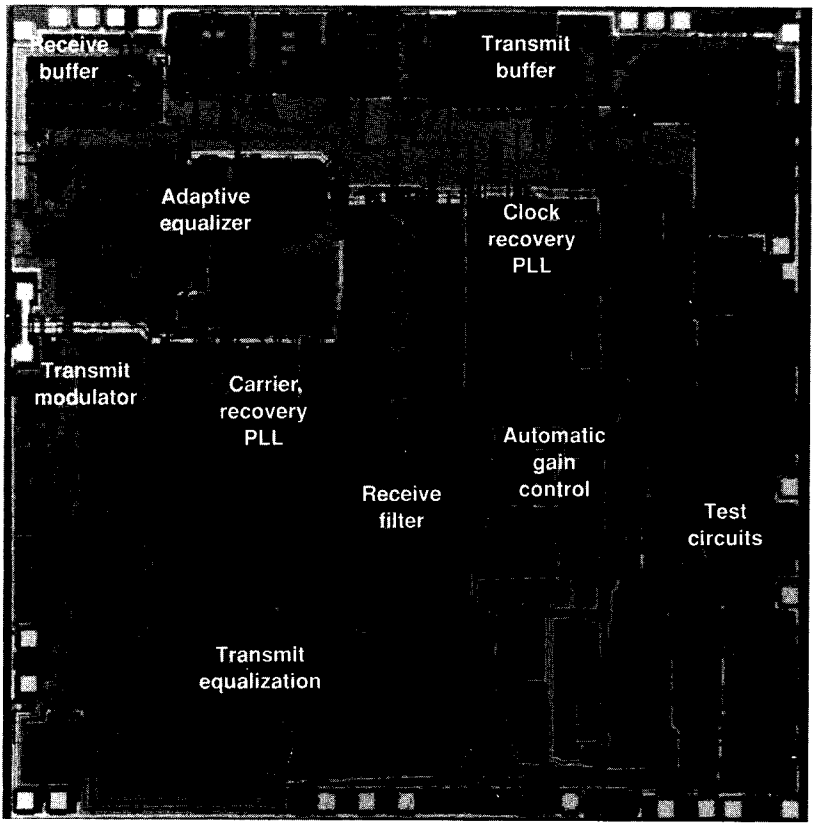


FIGURE 8.7-8
Integrated modem photograph (Courtesy of Texas Instruments).

The thrust of Chapters 5, 6, and 8 has been to present a hierarchically oriented introduction to the design of analog integrated circuits. Referring to Table 5.0-1, we have studied the design of analog circuits from the building block level in Chapter 5, through the basic circuit level in Chapter 6, up to the systems and complex circuit level of this chapter. The intent has been to give the reader an overview and the ability to know where and how to begin his or her design. The reader who faces the design of an analog circuit or system is encouraged to review the literature carefully in order to pick up some of the practical aspects and the circuit ideas and techniques that were not discussed here.

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PROBLEMS

Section 8.2

8.1. Compare the sample-and-hold circuit of Fig. 8.2-3*a* with that of Fig. 8.2-4 and discuss why the circuit of Fig. 8.2-4 can have faster sample times. Assume that ϕ and $\overline{\phi}$ are nonoverlapping clock signals.

8.2. Draw a transfer characteristic of a 3-bit D/A converter that has the largest possible integral nonlinearity when the differential nonlinearity is limited to ± 0.5 LSB. What is this maximum value of integral nonlinearity?

8.3. Express the output voltage of the binary-weighted resistor D/A converter shown in Fig. P8.3. Assume that the switches are connected to V_{ref} if the ith bit is 0, and to $-V_{\text{ref}}$ if the ith bit is 1.

8.4. Demonstrate that Fig. 8.2-12*b* will implement the function $V_{\text{OUT}} = -R_F I\,[b_1 + 2^{-1}b_2 + \cdots + 2^{-N+1}b_N]$ by considering a 4-bit example.

8.5. Find the accuracy required for R_{MSB} of a 12-bit D/A converter that uses the binary-weighted resistor approach in order to achieve monotonicity.

8.6. What is the maximum percentage tolerance of the current source (I_1) for the slave ladder of Fig. 8.2-13*b* if monotonicity is to be achieved for a 10-bit D/A converter?

8.7. Show how to modify the circuit of Fig. 8.2-15*a* to implement the bipolar operation of Eq. 8.2-13.

8.8. If an approximate formula for the ratio accuracy of capacitors is

$$\text{Ratio accuracy} \simeq 0.01 \times (\text{Capacitor ratio})^{0.25}$$

find the maximum number of bits that a charge-scaling D/A, such as in Fig. 8.2-15*a*, can have.

8.9. If A_R is the area of the resistors and A_C is the area of the capacitors of the D/A converter of Fig. 8.2-18, show that for minimum area

$$K - M = \frac{\ln\,(A_R/A_C)}{\ln 2}$$

where K is the number of bits that are charge-scaled and M is the number of bits that are voltage-scaled.

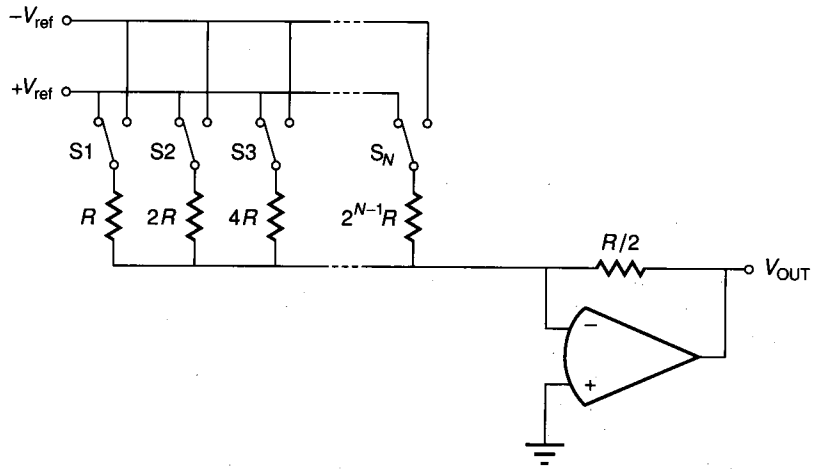

FIGURE P8.3

8.10. Determine the value of V_{C1} in Fig. 8.2-21 following the sequence of switch closing and openings: S4, S3, S1, S2, S1, S3, S1, S2, and S1. Assume that $C_1 = C_2$.

8.11. Repeat Prob. 8.10 if $C_1 = 1.05C_2$.

8.12. Show how Eq. 8.2-25 can be derived from Eq. 8.2-24. Give a realization of Fig. 8.2-24 using op amps, switches, and passive components.

8.13. Repeat Example 8.2-2 for the digital word 10101.

8.14. Assume that the amplifier with a gain of 0.5 in Fig. 8.2-24 has a gain error of ΔA. What is the maximum value ΔA can have in Example 8.2-2 without causing the conversion to be incorrect?

Section 8.3

8.15. Plot the transfer characteristic of a 3-bit A/D converter that has the largest possible differential nonlinearity when the integral nonlinearity is limited to ± 1 LSB. What is the maximum value of differential nonlinearity?

8.16. Find the 8-bit digital word if the input to Ex. 8.3-1 is 0.3215 V_{ref}.

8.17. Continue Example 8.3-2 out to the 10th bit and find the equivalent analog voltage.

8.18. Repeat Example 8.3-1 for the case where the gain-of-2 amplifiers actually have a gain of 2.1.

8.19. How many bits will an A/D converter with a sampling frequency of 10 MHz have in 1998? What technology will this converter use?

Section 8.4

8.20. Use the three circuits of Fig. 8.4-11 to obtain a realization of a second-order, low-pass Butterworth filter with a −3 dB frequency of 1000 Hz and a gain of 1 at dc. In Fig. 8.4-11*a*, additional stages may be necessary to achieve a gain of 1 at dc.

8.21. Repeat Example 8.4-3 using Fig. 8.4-11*c*, for stage 2 and stage 3.

8.22. Use the transformations of Fig. 8.4-13 to convert the result of Example 8.4-4 to a bandpass filter having a bandwidth of 500 Hz centered at 1000 Hz.

Section 8.5

8.23. Prove that the equivalent resistance given in Fig. 8.5-2 for the series switched capacitor resistance simulation is valid.

8.24. Repeat Prob. 8.23 for the series-parallel switched capacitor resistance simulation.

8.25. Repeat Prob. 8.23 for the bilinear switched capacitor resistance simulation.

8.26. Replot the frequency response of the circuit of Fig. 8.5-5*a* if $\omega_1 = 0.02\omega_c$. Compare with the frequency response (magnitude and phase) of Fig. 8.5-2.

8.27. Replace the parallel switched capacitor resistor simulation in Fig. 8.5-5*a* with the series switched capacitor resistor simulation of Fig. 8.5-2 and find the discrete-time frequency response similar to Eq. 8.5-27. Develop an expression for the magnitude and phase response and compare it with the results of Fig. 8.5-5*a*.

8.28. Obtain the exact frequency response at ϕ_1 of the switched capacitor circuit shown in Fig. P8.28. Define $\alpha = C_1/C_2$, and solve for the -3 dB frequency, in hertz, when $\alpha = 3$ and the clock frequency is (*a*) 64 kHz and (*b*) 128 kHz. The clock phases are nonoverlapping, and V_1 is from a sample-and-hold circuit.

8.29. Develop an expression for the discrete-time magnitude and phase response for H^{oe} of the noninverting switched capacitor integrator of Fig. 8.5-10*a*. Plot the magnitude and phase for frequencies from 0 to ω_c if $\omega_0/\omega_c = 0.1$.

8.30. Repeat Prob. 8.29 for the inverting switched capacitor integrator of Fig. 8.5-12.

8.31. Find the actual magnitude and phase of the noninverting switched capacitor integrator of Fig. 8.5-10*a* for H^{oo} if the frequency applied to the integrator is 10 kHz, the clock frequency is 100 kHz, and ω_0 is 20π krps.

Section 8.6

8.32. Develop a realization of $V_{OUT} = |V_{IN}|$ using resistors, diodes, and two op amps.

8.33. Develop a realization of $V_{OUT} = -|V_{IN} - 1|$ using resistors, diodes, and the minimum number of op amps.

8.34. Repeat Prob. 8.32 using capacitors, switches, one comparator, and the minimum number of op amps.

8.35. Repeat Prob. 8.33 using capacitors, switches, one comparator, and the minimum number of op amps.

8.36. (*a*) Design a circuit that realizes the transfer characteristic of Fig. P8.36 using resistors, diodes, and op amps.
(*b*) Repeat using capacitors, switches, comparators, and op amps.

8.37. (*a*) Design a circuit that realizes the transfer characteristic of Fig. P8.37 using resistors, diodes, and op amps.
(*b*) Repeat using capacitors, switches, comparators, and op amps.

8.38. Derive Eqs. 8.6-24 and 8.6-25 from Fig. 8.6-10.

8.39. Use a four-quadrant analog multiplier, op amps, and resistors to develop a circuit that produces an output voltage of $-K(V_1)^{1/2}$ when $V_1 > 0$.

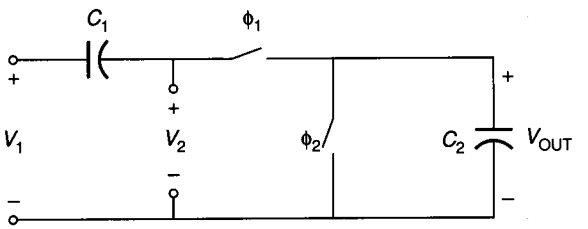

FIGURE P8.28

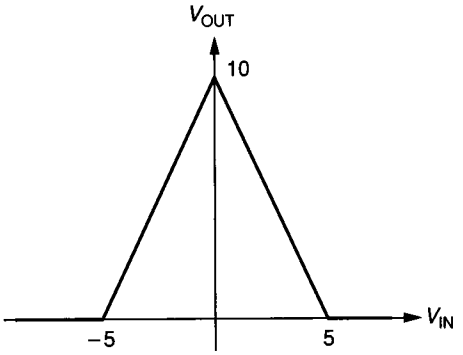

FIGURE P8.36

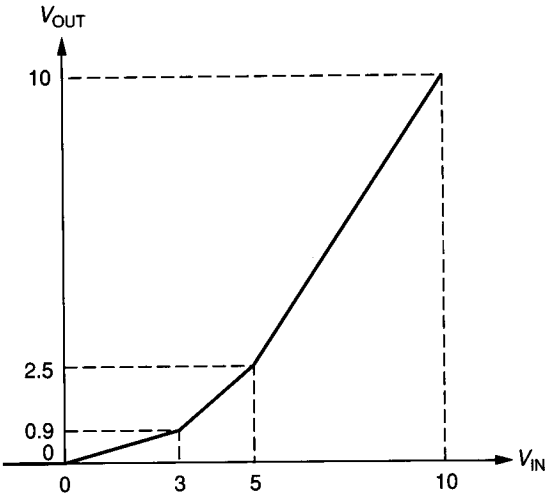

FIGURE P8.37

8.40. The sine of an input voltage V_1 can be approximated by the formula, $\sin V_1 \simeq 1.155V_1 - 0.33V_1^2$, to within $\pm 2\%$ over the range of $0 < V_1 < \pi/2$. Use multipliers and op amps to find a realization of $\sin V_1$ using this formula.

8.41. Find the frequency of oscillation, in hertz, and the value of R_f necessary for oscillation of the *RC* phase shift oscillator shown in Fig. P8.41.

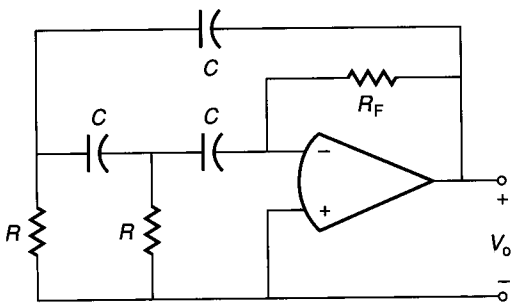

FIGURE P8.41

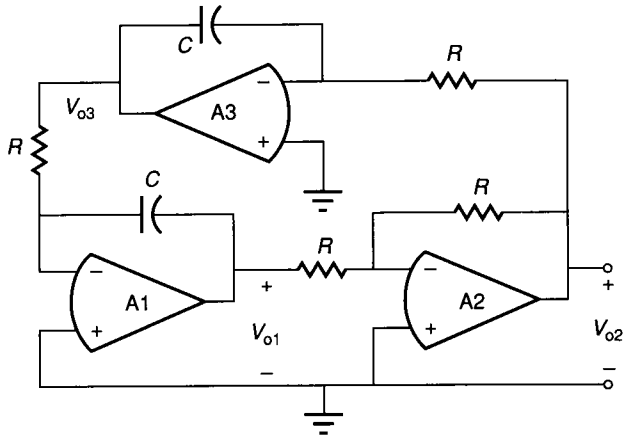

FIGURE P8.42

8.42. Find the frequency of oscillation, in hertz, of the quadrature oscillator of Fig. P8.42. Give expressions for the voltages V_{o1}, V_{o2}, and V_{o3} if the amplitude of the sinusoid at V_{o1} is 1 V peak.

8.43. Determine the values for the resistors not given in the bistable circuit of Fig. P8.43 and determine whether to connect R_q to $+15$ V or -15 V in order to realize the output-input transfer characteristic shown.

8.44. Show how to use a CW bistable to implement an untuned oscillator, and design the oscillator to produce a ± 10 V square wave at 3000 Hz.

8.45. Develop the expression for the frequency of oscillation of the circuit in Fig. 8.6-31 given in Eq. 8.6-71. What is the frequency of oscillation, in hertz, if $R_2 = R_3, R_1 = 100$ kΩ, and $C_1 = 1$ nF?

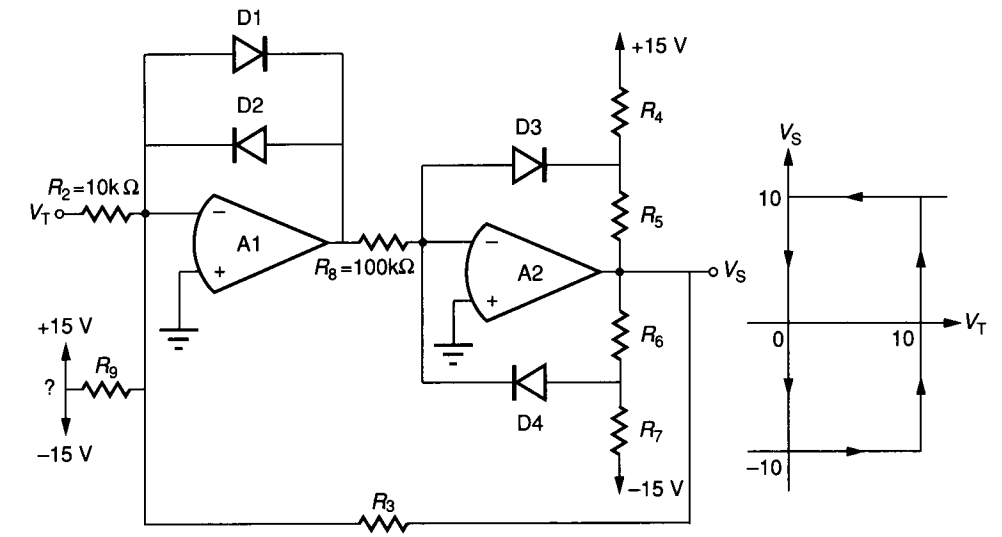

FIGURE P8.43