CHAPTER 8

ANALOG SYSTEMS

8.0 INTRODUCTION

The systems viewpoint of microelectronic design for analog integrated circuits is presented in this chapter. This material represents the highest level in the design hierarchy illustrated in Table 5.0-1. It is built on the circuits of Chapter 6, which are in turn built on the blocks and components of Chapter 5. A parallel hierarchy is presented in Chapters 7 and 9 for digital integrated circuit design. The subject matter in this chapter deals with the design of systems rather than the design of circuits. In this sense, the designer moves to a higher plateau of design. For example, rather than the design of op amps, the subject will include design *with* op amps.

The material presented in this chapter has been selected to be representative of the concepts and techniques in analog signal processing. In this chapter, we will discuss digital-to-analog and analog-to-digital conversion; review the concepts of continuous-time filter theory; and present switched capacitor filters, modulators and multipliers, waveshaping circuits, and oscillators. Although these subjects may be classified as either subsystems or systems, they are representative of analog design concepts applied at a system level. A microelectronic system often contains both digital and analog circuits and systems, so that in this sense, the material in Chapters 8 and 9 should be treated as a subsystem.

8.1 ANALOG SIGNAL PROCESSING

Figure 8.1-1 shows a simple block diagram of a typical signal processing system. As IC technology begins to exploit VLSI techniques and capabilities, many systems with this format will be built on a single chip. An example of this approach is the analog signal processor.[1] The advent of analog sampled data techniques and MOS technology has made the design of a general signal processor a viable

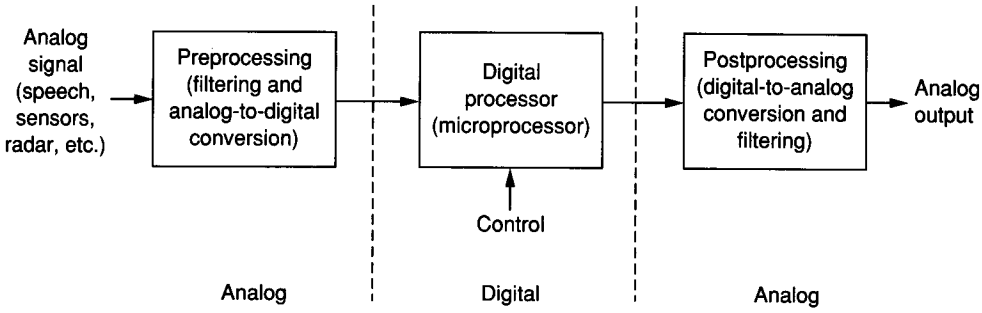

FIGURE 8.1-1
A block diagram of a typical signal processing system.

approach. At the present, CMOS technology is more suitable for combining analog and digital techniques. The primary reason for this situation is that digital VLSI circuits are typically implemented in CMOS. For this reason we will emphasize CMOS over BJT technology in this chapter. Recently, BJT and CMOS technologies have been combined to produce a new technology called BiMOS. BiMOS technology gives the designer an additional degree of freedom to select the most suitable devices for a given application.

The first step in the design of an analog signal processing system is to examine the specifications and to partition the system into the analog part and the digital part. In most cases, the input signal is analog. It could be a speech signal, a sensor output, a radar return, etc. The first block of Fig. 8.1-1 is a preprocessing block. Typically, this block will consist of filters and an analog-to-digital converter. Often, there are very strict speed and accuracy requirements on the components in this block. The next block of the analog signal processor is essentially a microprocessor. An obvious advantage of this approach is that the function of the processor can easily be controlled and changed. Finally, it is often necessary to provide an analog output. In this case, a postprocessing block is necessary. It will typically contain a digital-to-analog converter and some filtering. An interesting decision for the system designer is deciding where to place the interfaces indicated by the dotted lines.

For signal processing, probably the most important system consideration is the bandwidth of the signal to be processed. A graph of the bandwidths of a variety of signals is given in Fig. 8.1-2. The bandwidths in this figure cover the enormous range of 10 orders of magnitude in frequency. At the low end are the seismic signals, which do not extend much below 1 Hz because of the absorption characteristics of the earth. At the other extreme are the microwave signals, which are not used much above 30 GHz because of the difficulties in performing even the simplest forms of signal processing at higher frequencies.

To perform signal processing over this range of frequencies, a variety of techniques have been developed that are almost exclusively analog above 10 MHz and digital below 100 Hz, as shown in Fig. 8.1-3. In the overlap region, a tradeoff must be made between the accuracy and flexibility of a digital approach

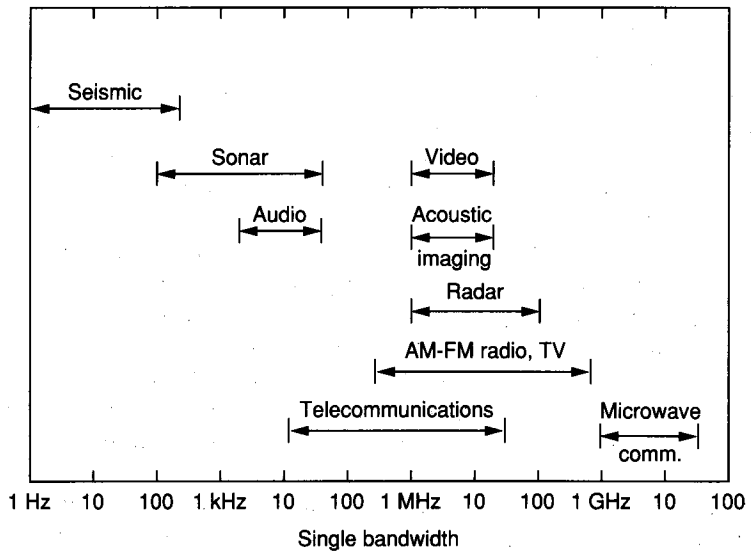

FIGURE 8.1-2
Bandwidths of signals used in signal processing applications.

and the low cost, power, and size of analog techniques. These considerations illustrate some of the advantages of a combined MOS-BJT technology.

By assuming the continuing development of MOS and bipolar technology, it is possible to extrapolate the trends of the past 10 years to obtain predictions about the capability of IC technology in the next 10 years. Some of the implications of these predictions have been considered and show that even at the limits of scaling, the processing bandwidth of MOS technology will have improved only to the point where it is equivalent to today's advanced bipolar technologies.

The ranges indicated in Fig. 8.1-3 are due to technology and are constantly increasing. One of the fastest-moving boundaries in Fig. 8.1-3 is the upper limit of the MOS digital logic, which, as the technology progresses to VLSI, should be able to process signals by the year 1992 at bandwidths of 50–100 MHz. This will be accomplished by using greatly increased density along with moderately increased device speeds. However, as can be seen in Fig. 8.1-3, bipolar digital techniques are already able to process at these rates. Therefore, VLSI will not make possible increased processing rates over what can now be achieved with processors built with bipolar technology, but rather will offer the primary advantages of reduced cost, size, and power requirements of the MOS VLSI signal processors. This will make it possible for signal processing techniques to make an impact in such cost-sensitive areas as consumer products that until now have been unable to afford the costs of using more sophisticated techniques. The combination of BJT and MOS technology offers the best promise of high performance, VLSI signal processing capability.

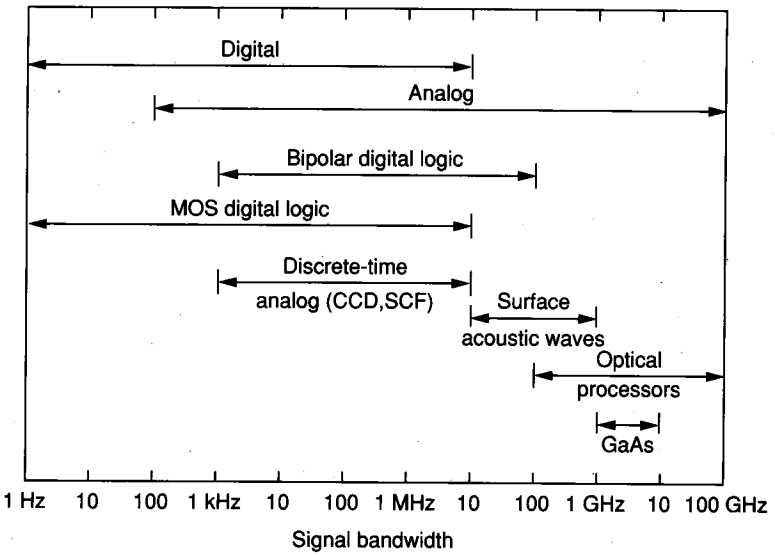

FIGURE 8.1-3
Signal bandwidths that can be processed by present-day (1989) technologies.

8.2 DIGITAL-TO-ANALOG CONVERTERS

The ability to convert digital signals to analog and vice versa is very important in signal processing. This section will examine the digital-to-analog conversion aspect of this important interface. Analog-to-digital conversion will be discussed in the next section. Most of the discussion in these two sections will be independent of whether the technology is BJT or MOS. The op amps and comparators used can be of either type. The switches will be MOS. The resistors and capacitors can be implemented by either technology, depending on the performance requirements.

Figure 8.2-1 illustrates how analog-to-digital (A/D) and digital-to-analog (D/A) converters are used in data systems.[2] In general, an A/D conversion process will convert a sampled and held analog signal to a digital word that is a representation of the analog sampled signal. Often, many analog inputs are multiplexed to the A/D converter. The D/A conversion process is essentially the inverse of the A/D process. Digital words are applied to the input of the D/A converter to create from a reference voltage an analog output signal that is a representation of the digital word.

This section will introduce the principles of D/A converters and will then discuss the performance characterization of D/A converters. The various types of linear D/A converters that will be examined include current-scaling, voltage-scaling, charge-scaling, combinations of the preceding types, and serial D/A converters. In the next section, we will see that D/A converters have an important role in the design and implementation of some A/D converters.

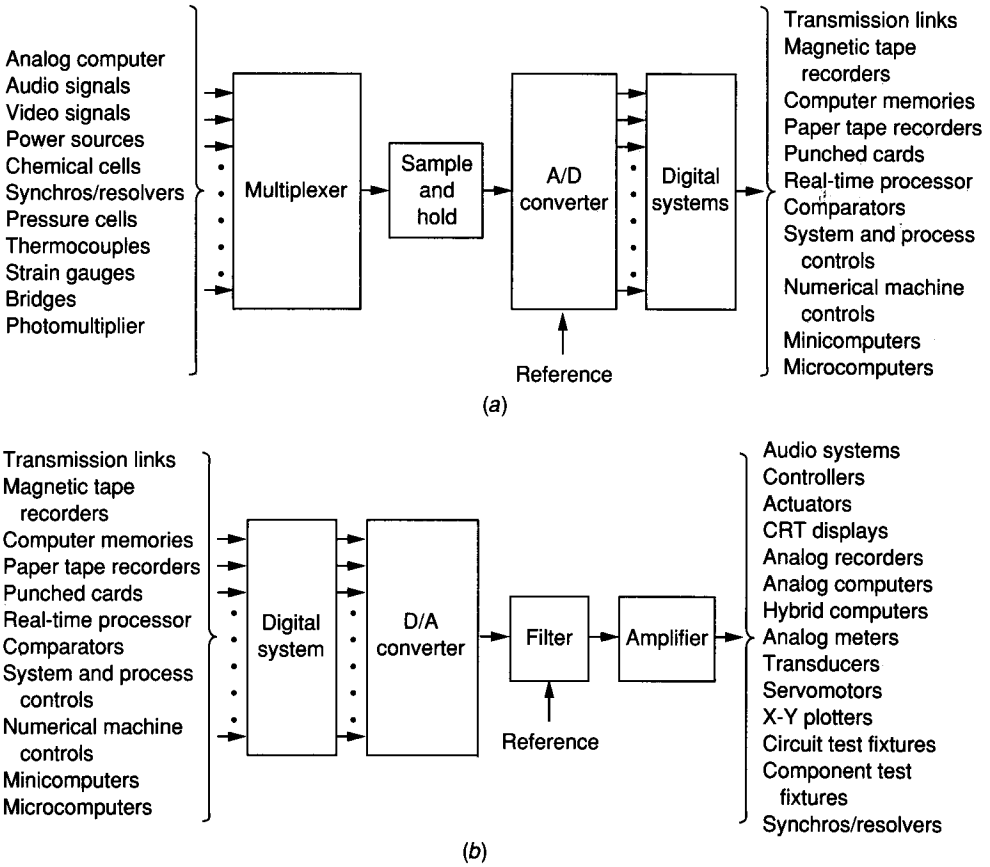

FIGURE 8.2-1
Converters in signal processing systems: (*a*) A/D, (*b*) D/A.

Figure 8.2-2*a* shows a conceptual block diagram of a D/A converter. The inputs are a digital word of N bits ($b_1, b_2, b_3, \ldots, b_N$) and a reference voltage, V_{ref}. The voltage output, V_{OUT}, can be expressed as

$$V_{\text{OUT}} = K V_{\text{ref}} D \tag{8.2-1}$$

where K is a scaling factor and the digital word D is given as

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} \tag{8.2-2}$$

N is the total number of bits of the digital word, and b_i is the ith bit coefficient and is either 0 or 1. Thus, the output of a D/A converter can be expressed by combining Eqs. 8.2-1 and 8.2-2 to get

$$V_{\text{OUT}} = K V_{\text{ref}} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} \right) \tag{8.2-3}$$

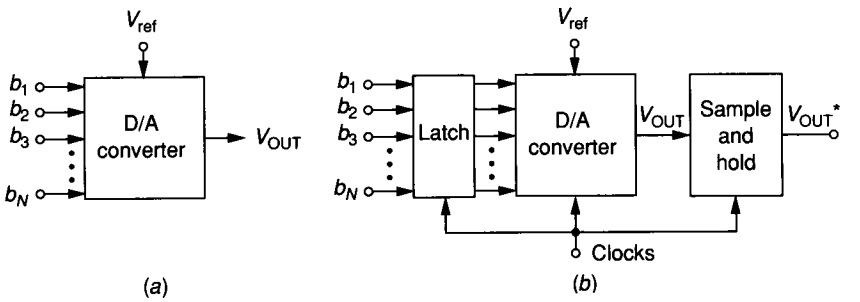

FIGURE 8.2-2
(*a*) Conceptual block diagram of a D/A converter, (*b*) Clocked D/A converter.

or

$$V_{OUT} = K V_{ref}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N})$$
$$= K V_{ref} \sum_{j=1}^{N} b_j 2^{-j} \tag{8.2-4}$$

In many cases, the digital word is synchronously clocked. In this case it is necessary to use latches to hold the word for conversion and to provide a sample-and-hold circuit at the output, as shown in Fig. 8.2-2*b*. A voltage that has been sampled and held is denoted by an asterisk. The sample-and-hold circuit consists of a circuit such as that shown in Fig. 8.2-3, where the analog signal is sampled

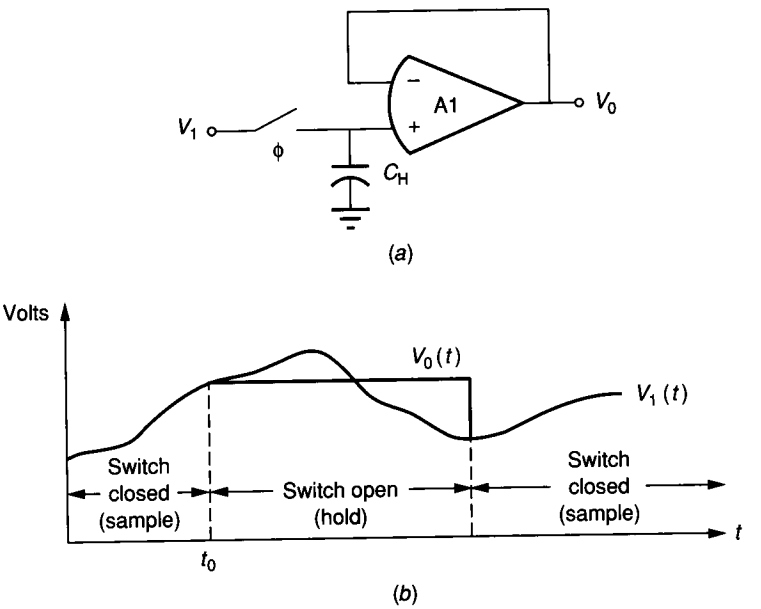

FIGURE 8.2-3
(*a*) Simple sample-and-hold circuit, (*b*) Waveforms illustrating the operation of the sample-and-hold.

on a capacitor, C_H, when the switch is closed; this is called the *sample mode*. During the time that the switch is open, or the *hold mode*, the voltage at time t_0 remains available at the output. An alternate version of the sample-and-hold circuit with higher performance is shown in Fig. 8.2-4. It is important that the sample-and-hold circuit be able to rapidly track changes in the input voltage when in the sample mode and not discharge the capacitor when in the hold mode.

The basic architecture of the D/A converter without an output sample-and-hold circuit is shown in Fig. 8.2-5. The various blocks are a voltage reference, which can be externally supplied, binary switches, a scaling network, and an output amplifier. The voltage reference, binary switches, and scaling network convert the digital word as either a voltage or current signal, and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of the conversion.

The characterization of the D/A converter is very important in understanding its use and design. The characteristics of the D/A converter can be divided into static and dynamic properties. The static properties are independent of time and include the converter transfer characteristic, quantization noise, dynamic range, gain, offset, and nonlinearity.[3]

Figure 8.2-6 shows the transfer characteristic of an ideal D/A converter. This D/A converter has been designed so that the analog output occurs at odd multiples of the full scale signal (FS) divided by 16. The right-most bit of the digital input code is called the *least significant bit* (LSB). Each time the LSB changes, the analog output changes by $FS/2^N$, where N is equal to the number of digital bits. Although this change is an analog quantity, it is often called an LSB change and should be interpreted as the analog change due to a change in the LSB of the digital input code.

The *resolution* of a converter is the smallest analog change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of FS, but is commonly expressed in number of bits, N, where the converter has 2^N possible states. The finite resolution of converters causes an inherent uncertainty in digitizing an analog value. This uncertainty is called the *quantization noise* and has a value of up to ± 0.5 LSB. In the characteristic of Fig. 8.2-6, the quantization noise is seen to be ± 0.5 LSB

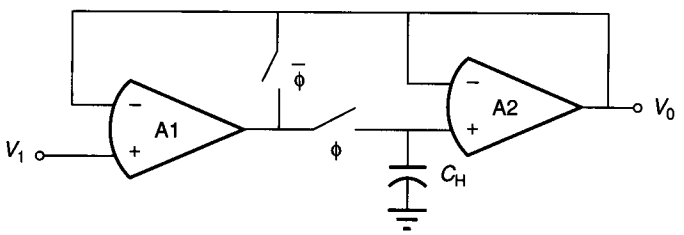

FIGURE 8.2-4
An improved sample-and-hold circuit.

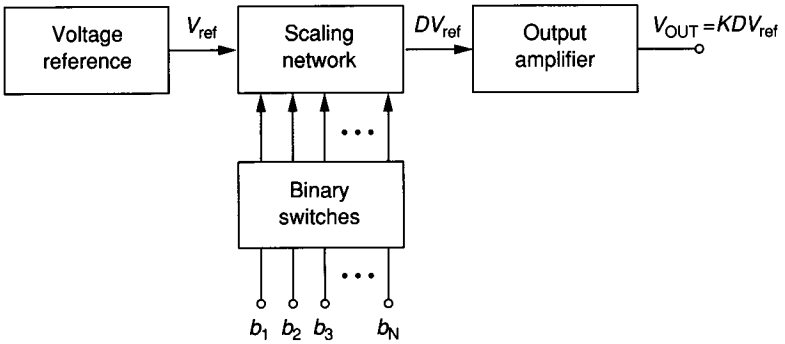

FIGURE 8.2-5
Block diagram of a D/A converter.

or $\pm FS/2^{N+1}$ about each of the multiples of FS/8. The straight line in Fig. 8.2-6 through the midpoint of each analog step change represents the ideal performance of the D/A converter as N approaches infinity.

The *full scale range* (FSR) is the difference between the maximum and minimum analog values and is equal to FS in Fig. 8.2-6 as N approaches infinity. The *dynamic range* (DR) of a noiseless converter is the ratio of the FSR to the smallest difference it can resolve. Thus, the DR can be given as

$$DR = 2^N \tag{8.2-5}$$

or in terms of decibels as

$$DR(dB) = 20\log_{10}(2^N) = 6.02N \tag{8.2-6}$$

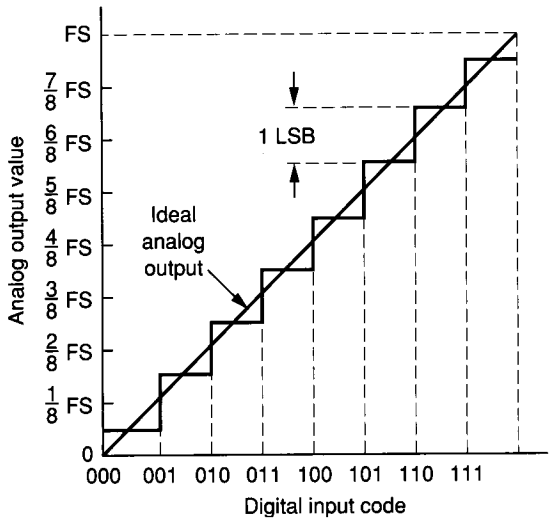

FIGURE 8.2-6
Ideal input-output characteristics for a 3-bit D/A converter.

The *signal-to-noise ratio* (S/N) is also useful in characterizing the capability of a converter. Assume that an analog ramp input is applied to an ideal A/D converter cascaded with an ideal D/A converter. If the analog output of the D/A converter is subtracted from the original analog ramp input, a sawtooth waveform of $\pm FS/2^{N+1}$ results. This sawtooth waveform represents the ideal quantization noise and has an rms value of $(FS/2^N)/\sqrt{12}$. The S/N expressed as a power ratio in dB can be found from the ratio of the peak-to-peak signal, FS, to the noise as

$$S/N(dB) = 10\log_{10}\left[\frac{FS}{FS/[2^N(12)^{1/2}]}\right]^2$$

$$= 20\log_{10}(2^N) + 20\log_{10}(12)^{1/2} = 6.02N + 10.8 \quad (8.2\text{-}7)$$

It can be seen that the S/N ratio increases by a factor of approximately 6 dB for each additional bit of resolution.

The remaining static characteristics include *offset error*, *gain error*, *nonlinearity*, and *nonmonotonicity*. Figure 8.2-7 illustrates the first three of these characteristics for a 3-bit D/A converter. In each case the ideal characteristic of Fig. 8.2-6 is shown by dashed lines for comparison. An illustration of offset error is shown in Fig. 8.2-7*a*. An offset error is seen to be a vertical shift in the D/A transfer characteristic of the ideal D/A transfer characteristic. The offset error is defined as the analog output value by which the transfer characteristic fails to pass through zero. It may be expressed in millivolts or percent of FS.

Figure 8.2-7*b* illustrates the gain or scale factor error of a 3-bit D/A converter. The gain or scale factor error is defined as the difference in the full scale values between the ideal and actual transfer characteristics when the offset error is zero and may be expressed in percent of full scale.

Figure 8.2-7*c* is an illustration of nonlinearity error in a 3-bit D/A converter. Nonlinearity is further divided into integral nonlinearity and differential nonlinearity. Integral linearity is a global measure of nonlinearity of the converter and is defined as the maximum deviation of the actual transfer characteristic from a straight line drawn between zero and the FS of the ideal converter. Integral nonlinearity is expressed in terms of percent of FS or in terms of LSBs. In the characteristics of Fig. 8.2-7*c*, the maximum deviation, which occurs at 111, is -1.5 LSB or -18.75% of FS.

Differential nonlinearity is defined as the maximum deviation of any of the analog output changes caused by an LSB change from its ideal size of $FS/2^N$ or 1 LSB. It is typically expressed in terms of $\pm$LSBs. In the characteristic of Fig. 8.2-7*c*, the maximum deviation also occurs at 111 and is a differential nonlinearity of ± 1 LSB. The characteristic of Fig. 8.2-8 shows how differential nonlinearity differs from integral nonlinearity. Figure 8.2-8*a* is for a 4-bit D/A converter having ± 2 LSB integral nonlinearity and ± 0.5 LSB differential nonlinearity. Figure 8.2-8*b* illustrates a 4-bit D/A converter having $\pm$ 0.5 LSB integral nonlinearity and $\pm$ 1 LSB differential nonlinearity.

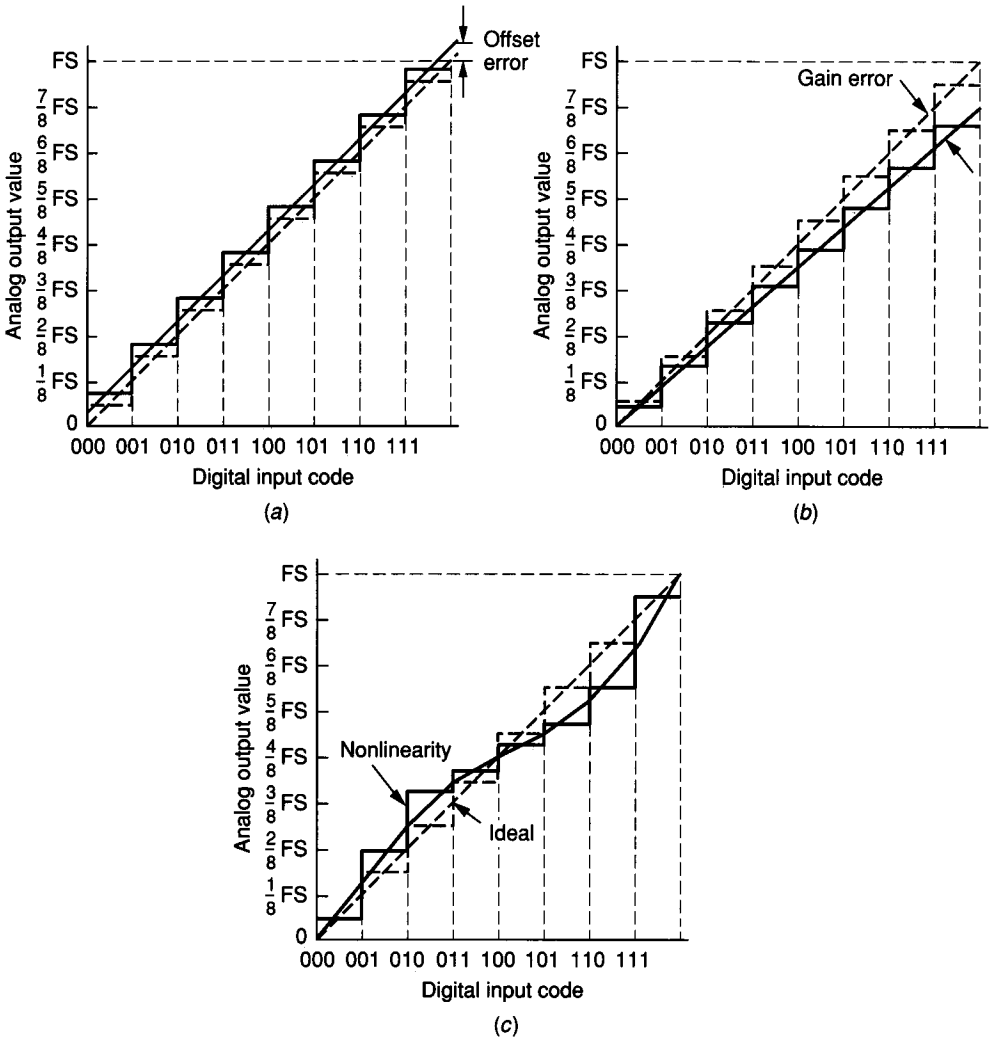

FIGURE 8.2-7
Examples of various types of static characteristics for a 3-bit D/A converter: (*a*) Offset error, (*b*) Gain error, (*c*) Nonlinearity.

Figure 8.2-9 illustrates a 3-bit D/A converter that is not monotonic. A monotonic D/A converter is one in which an increasing digital input code produces a continuously increasing analog output value. A nonmonotonic D/A converter can result if the differential nonlinearity error exceeds ± 1 LSB. In Fig. 8.2-9, a differential nonlinearity of ± 1.5 LSB occurs at a digital input code of 001. Note that there are two occurrences of nonmonotonicity in Fig. 8.2-9.

The dynamic characteristics of the D/A converter are associated with changes in the input digital word. The time required for the output of the converter to

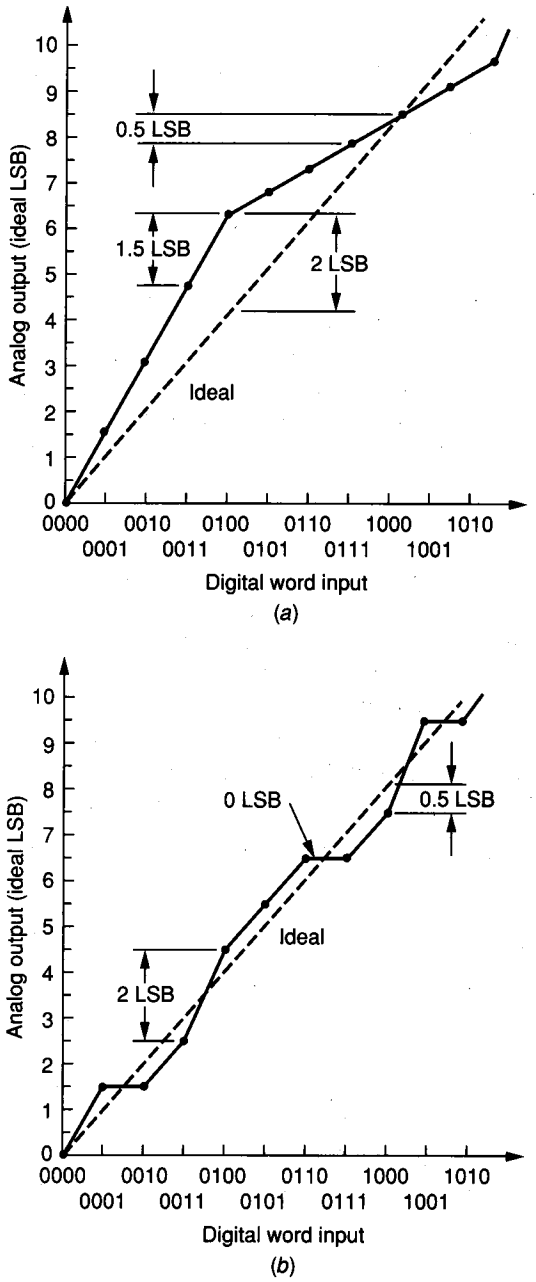

FIGURE 8.2-8
Distinction between integral and differential nonlinearity for a D/A converter: (*a* D/A converter with ±2 LSB integral nonlinearity and ±0.5 LSB differential nonlinearity, (*b*) D/A converter with ±0.5 LSB integral nonlinearity and ±1 LSB differential nonlinearity.

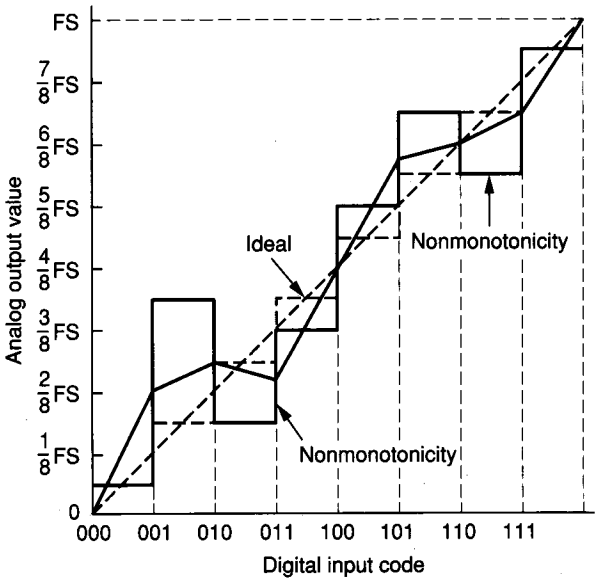

FIGURE 8.2-9
Example of a 3-bit D/A converter that is not monotonic.

respond to a bit change is called the *settling time* and is defined similarly to the settling time for op amps in Fig. 6.5-21. Settling time for D/A converters depends on the type of converter and can range from as much as 100 μs to less than 100 ns.

Many techniques have been used to implement D/A converters. Three approaches that are compatible with integrated circuit technology will be examined. These methods are current-scaling or division, voltage-scaling or division, and charge-scaling or division. Current-scaling is widely used with BJT technology, whereas voltage- and charge-scaling are popular for MOS technology.

8.2.1 Current-Scaling D/A Converters

The general principle of current-scaling or division D/A converters is shown in Fig. 8.2-10*a*. The reference voltage is converted to binary-weighted currents, $I_1, I_2, I_3, \ldots, I_N$. An implementation of this technique using resistors is shown in Fig. 8.2-10*b*. Each of the switches, S_i, is connected to V_{ref} if the ith bit, b_i, is 1 and to ground if b_i is 0. It is seen that the output voltage of the op amp can be expressed as

$$V_{\text{out}} = \frac{-R}{2} I_{\text{O}} = \frac{-R}{2}\left(\frac{b_1}{R} + \frac{b_2}{2R} + \frac{b_3}{4R} + \cdots + \frac{b_{\text{N}}}{2^{N-1}R}\right) V_{\text{ref}}$$

$$= -V_{\text{ref}}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N}) \quad (8.2\text{-}8)$$

The feedback resistor, R_F, can be used to achieve the scaling factor K of Eq. 8.2-1. The switches can be moved from the V_{ref} side of the resistors to the

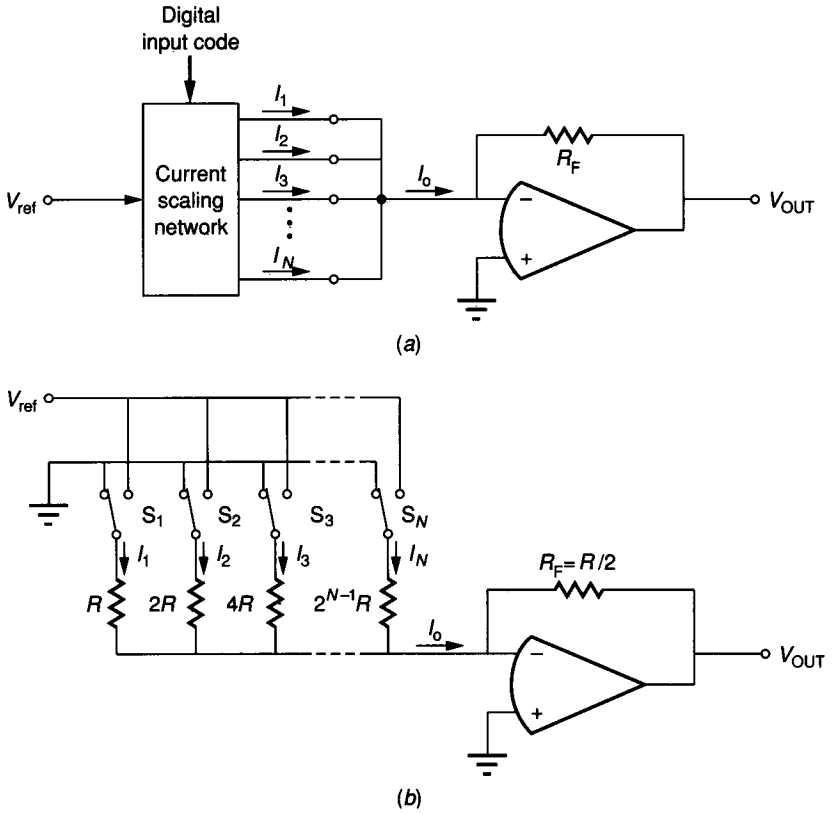

FIGURE 8.2-10
(*a*) Conceptual illustration of a current-scaling D/A converter, (*b*) Implementation of (*a*).

side connected to the inverting input of the op amp. The advantage of the latter configuration is that the voltages at the switch terminals are always ground. As a consequence, the switch parasitic capacitances are not charged or discharged.

The binary-weighted resistor ladder configuration of Fig. 8.2-10*b* has the disadvantage of a large ratio of component values. For example, the ratio of the resistor for the MSB, R_{MSB}, to the resistor for the LSB, R_{LSB}, is

$$\frac{R_{MSB}}{R_{LSB}} = \frac{1}{2^{N-1}} \tag{8.2-9}$$

For an 8-bit D/A converter, this gives a ratio of 1/128. The difficulty with this approach is that the accuracy of R_{MSB} must be much better than that of the value of R_{LSB} for the converter to work properly. For example, R_{MSB} of an 8-bit D/A converter must have a relative accuracy with respect to R_{LSB} to within $\pm 0.78\%$, and preferably better. Such accuracy is difficult to achieve without trimming the resistors, which is done for high-resolution D/A converters using binary-weighted components.

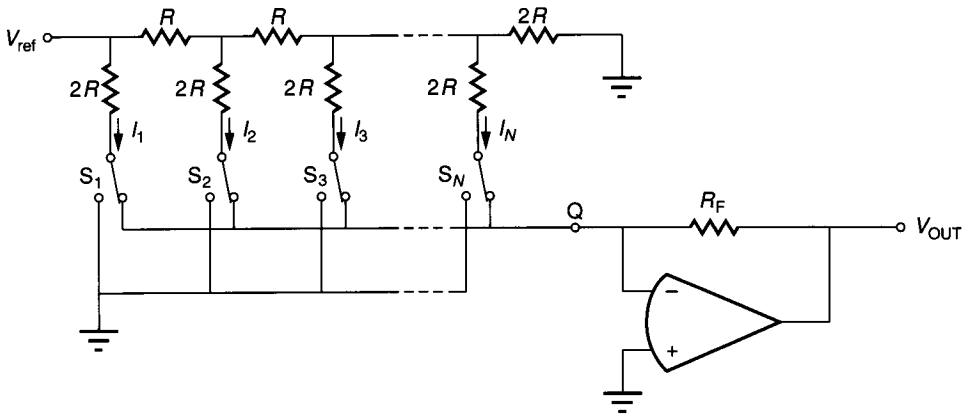

FIGURE 8.2-11
A current-scaling D/A converter using an *R*-2*R* ladder.

An alternative to the binary-weighted approach is the use of an *R*-2*R* ladder, shown in Fig. 8.2-11. Each of the switches, S_i, is connected to Q if the *i*th bit is 1 and to ground if the *i*th bit is 0. Q is the inverting input of the op amp. Obviously, the current I_1 is equal to $V_{ref}/2R$. Using the fact that the resistance to the right of any of the vertical $2R$ resistors is $2R$, we see that the currents I_1, I_2, I_3, . . . , I_N are binary-weighted and given as

$$I_1 = 2I_2 = 4I_3 = \ldots = 2^{N-1}I_N \tag{8.2-10}$$

Thus, the output voltage of the *R*-2*R* D/A converter of Fig. 8.2-11 is given by Eq. 8.2-8. Figure 8.2-11 is an example of using the switches connected either to ground or the inverting terminal of the op amp. V_{ref} and the inverting input of the op amp (point Q) can be interchanged if desired. While the *R*-2*R* D/A converter has twice as many resistors as the binary-weighted resistor D/A converter, it requires resistors with only the ratio of 2:1, which is more practical to accomplish. One disadvantage of the *R*-2*R* configuration is that there are up to 2^{N-1} floating nodes, which are sensitive to parasitic capacitances. Floating nodes are nodes with relatively large resistance to ground. The charging and discharging of these capacitances will require time and delay the response of the converter. Possible architectures for bipolar D/A converters using the *R*-2*R* ladder approach are shown in Fig. 8.2-12. Note that the emitter areas of the BJT devices must be proportional to the emitter current in Fig. 8.2-12*a*.

Two approaches for using binary-weighted D/A converters while keeping the MSB and LSB resistor ratios small deserve mention. The first is called *cascading* and is illustrated in Fig. 8.2-13*a*. The use of a current divider allows two 4-bit, binary-weighted current sources to be cascaded to achieve an 8-bit D/A converter. The accuracy of the 1:16 attenuating resistors must be within the magnitude of the LSB of the entire ladder. A second approach is shown in Fig. 8.2-13*b* and is called the *master-slave ladder*. In this approach, a master ladder consists of the

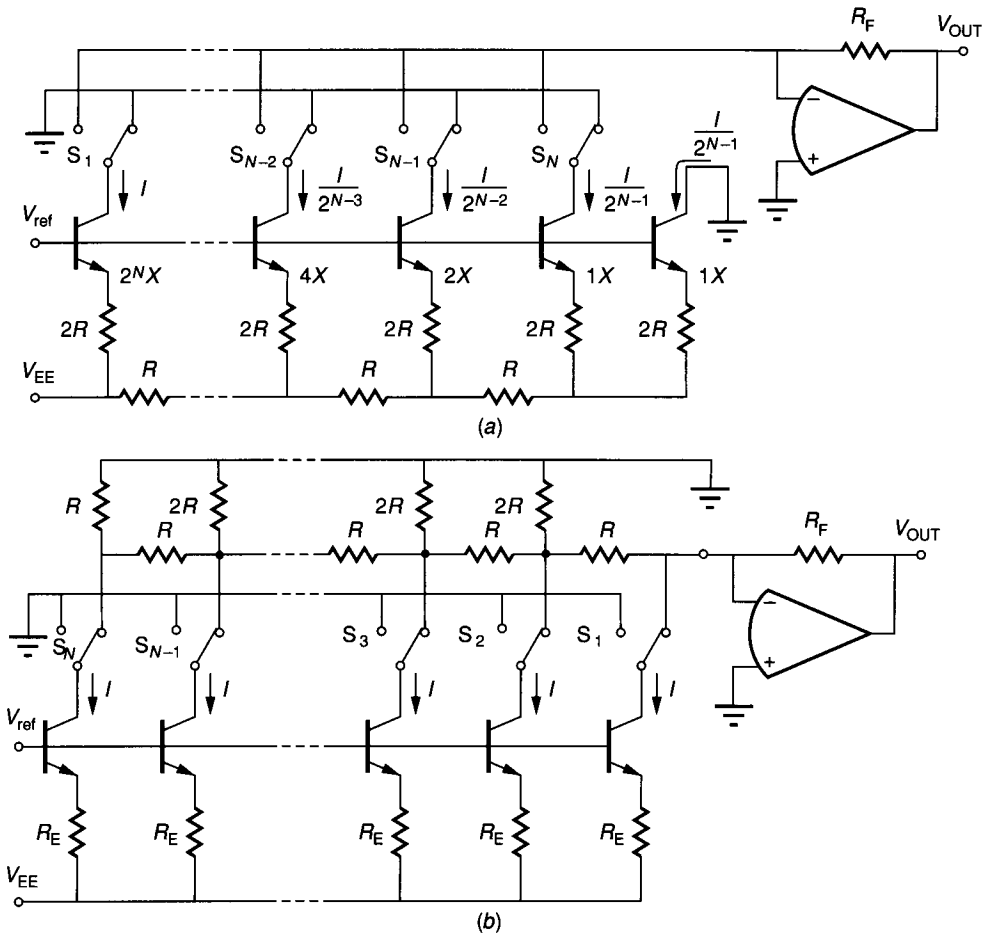

FIGURE 8.2-12
Two implementations of D/A converters using R-$2R$ ladders and BJT current sinks. (a) Binary-weighted emitter areas, and (b) Equal emitter areas. Both converters are described by $V_{OUT} = -R_F I\,[b_1 + 2^{-1}b_2 + \ldots + 2^{N-1}b_N]$.

half of the bits that are most significant, and the slave ladder consists of the half of the bits that are least significant. The crucial point in this approach is the accuracy of the $I/16$ current source for the slave ladder. It must have accuracy better than ± 0.5 LSB.

8.2.2 Voltage-Scaling D/A Converters

Voltage-scaling uses series resistors connected between V_{ref} and ground to selectively obtain voltages between these limits. For an N-bit converter, the resistor string would have at least 2^N segments. These segments can all be equal or

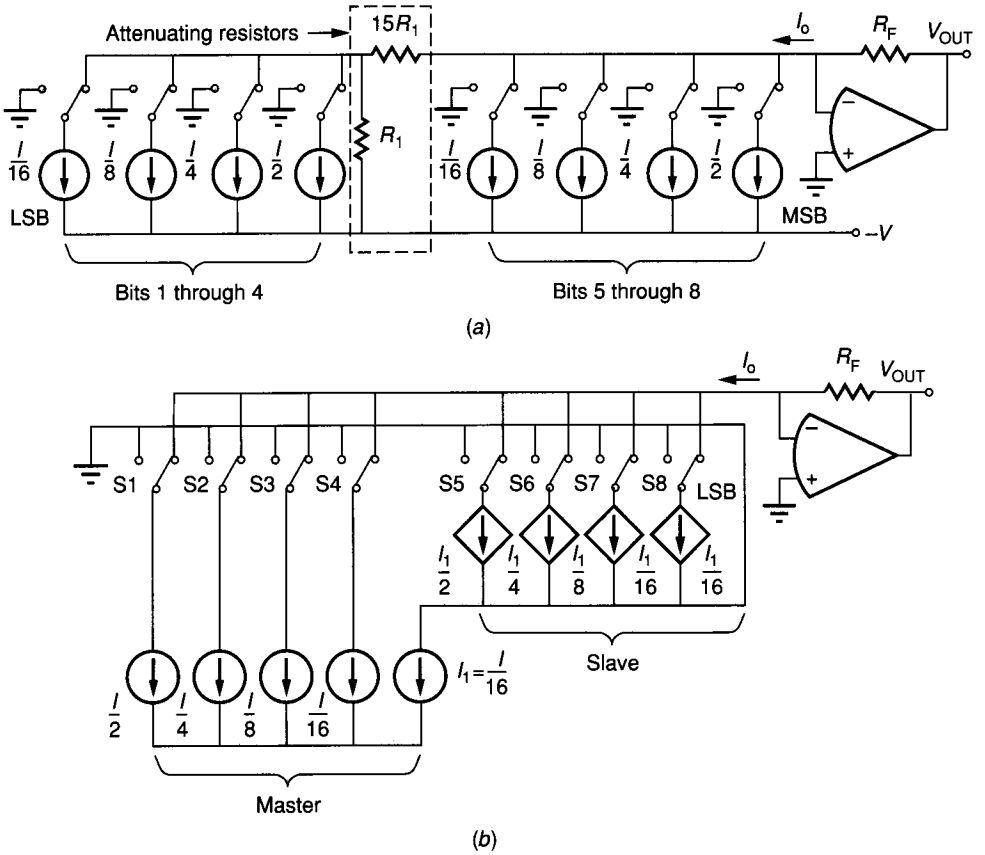

FIGURE 8.2-13
(*a*) Use of current division to cascade two 4-bit, binary-weighted current sinks to get an 8-bit D/A converter, (*b*) Master-slave technique to combine two 4-bit binary weighted current sources to obtain an 8-bit D/A converter. Note that $I_1 = I/16$.

the end segments may be partial values, depending on the requirements. Figure 8.2-14*a* shows a 3-bit voltage scaling D/A converter. Note that the op amp is used simply to buffer the resistor string. Each tap is connected to a switching tree whose switches are controlled by the bits of the digital word. If the ith bit is 1, then the switches controlled by b_i are closed. If the ith bit is 0, then the switches controlled by $\overline{b_i}$ are closed.

The voltage-scaling D/A converter of Fig. 8.2-14*a* works as follows. Suppose that the digital word to be converted is $b_1 = 1, b_2 = 0$, and $b_3 = 1$. Following the sequence of switches, we see that V_{OUT} is equal to 11/16 of V_{ref}. In general, the voltage at any tap i of Fig. 8.2-14*a* can be expressed as

$$V_i = \frac{V_{ref}}{8}(i - 0.5) \tag{8.2-11}$$

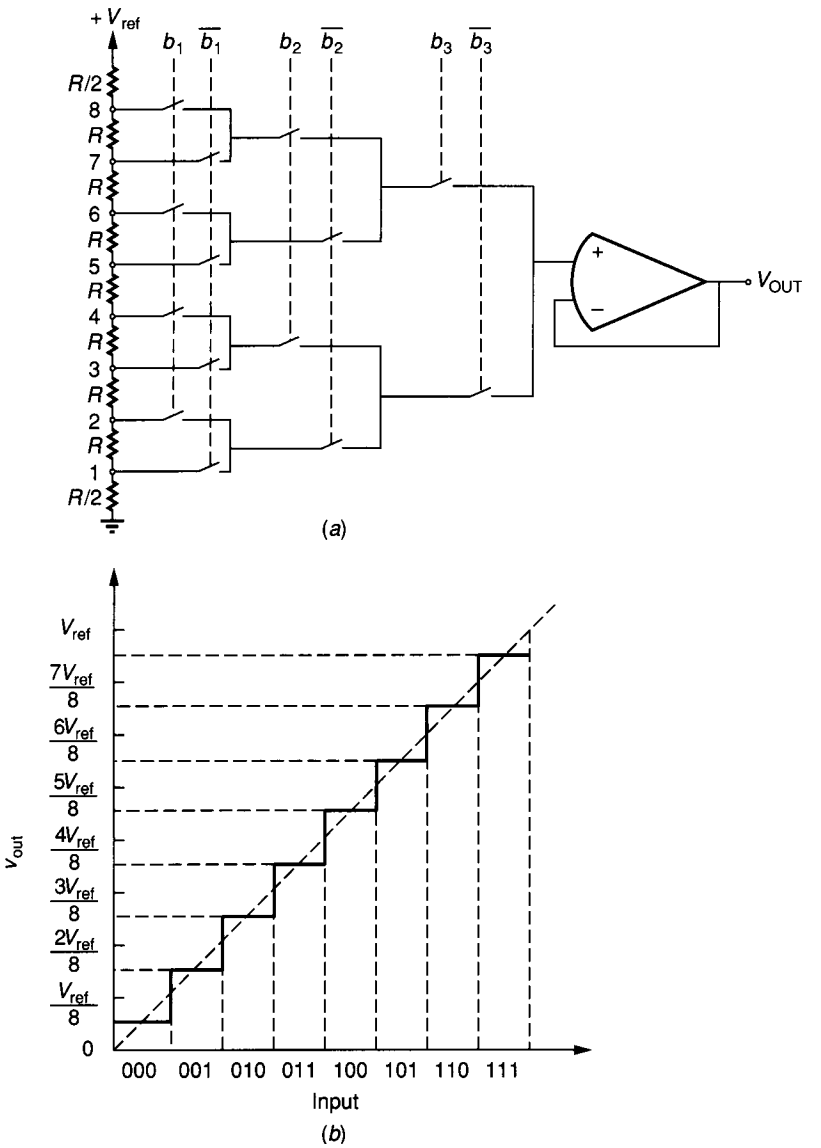

FIGURE 8.2-14
(*a*) Illustration of a 3-bit voltage-scaling D/A converter, (*b*) Input-output characteristics of *a*.

Figure 8.2-14*b* shows the input-output characteristics of the D/A converter of Fig. 8.2-14*a*. It may be desirable to connect the bottom tap to ground, so that a well-defined output (ground) is available when the digital word is all 0s.

Example 8.2-1. Find the accuracy requirement for a resistor string consisting of N equal segments as a function of the number of bits N. If the relative resistor accuracy is 2%, what is the largest number of bits than can be resolved to within $\pm$ 0.5 LSB?

Solution. The ideal voltage to ground across k resistors can be expressed as

$$V_k = \frac{kR}{2^N R} V_{\text{REF}}$$

The worst case variation in this voltage can be found by assuming that all resistors above this point in the string are maximum and below this point are minimum. Therefore, the worst case lowest voltage to ground across k resistors is

$$V'_k = \frac{kR_{\min} V_{\text{REF}}}{(2^N - k)R_{\max} + kR_{\min}}$$

The difference between the ideal and worst case voltages can be expressed as

$$\frac{V_k}{V_{REF}} - \frac{V'_k}{V_{REF}} = \frac{kR}{2^N R} - \frac{kR_{\min}}{(2^N - K)R_{\max} + kR_{\min}}$$

Since this difference must be less that 0.5 LSB, then the desired relationship can be obtained as

$$\frac{k}{2^N} - \frac{kR_{\min}}{(2^N - k)R_{\max} + kR_{\min}} < \frac{0.5}{2^N}$$

The relative accuracy of the resistor R can be expressed as $\Delta R/R$, which gives $R_{\max} = R + 0.5\Delta R$ and $R_{\min} = R - 0.5\Delta R$. Normally, the worst case occurs when k is midway in the resistor string or $k = 0.5(2^N)$. Assuming a relative accuracy of 2% and substituting the above values gives

$$|0.01| < 2^{-N}$$

Solving this equation for N gives $N = 6$ as the largest integer.

It is seen that the voltage-scaling D/A structure is very regular and thus well suited for MOS technology. An advantage of this architecture is that it guarantees monotonicity, since the voltage at each tap cannot be greater than the tap below it. The area required for the voltage-scaling D/A converter is large if the number of bits is 8 or more. The converter will be sensitive to parasitic capacitances at each of the floating nodes resulting in signal delays.

8.2.3 Charge-Scaling D/A Converters

Charge-scaling D/A converters operate by dividing the total charge applied to a capacitor array. Typically, all capacitors are discharged first. Figure 8.2-15*a* shows an illustration of a charge-scaling D/A converter. A nonoverlapping, two-phase clock is used. ϕ_1 indicates that a switch is closed during phase 1, and similarly for ϕ_2. During ϕ_1, all capacitors in the array are discharged. Next, during ϕ_2, the capacitors associated with bits that are 1 are connected to V_{ref} and those with bits that are 0 are connected to ground. The resulting situation can be described by equating the charge on the capacitors connected to V_{ref} (C_{eq}) to the charge in the total capacitors (C_{tot}). This is expressed as

$$V_{\text{ref}} C_{\text{eq}} = V_{\text{ref}} \left(b_1 C + \frac{b_2 C}{2} + \frac{b_3 C}{2^2} + \cdots + \frac{b_N C}{2^{N-1}} \right) = C_{\text{tot}} V_{\text{OUT}} = 2CV_{\text{OUT}} \tag{8.2-12}$$

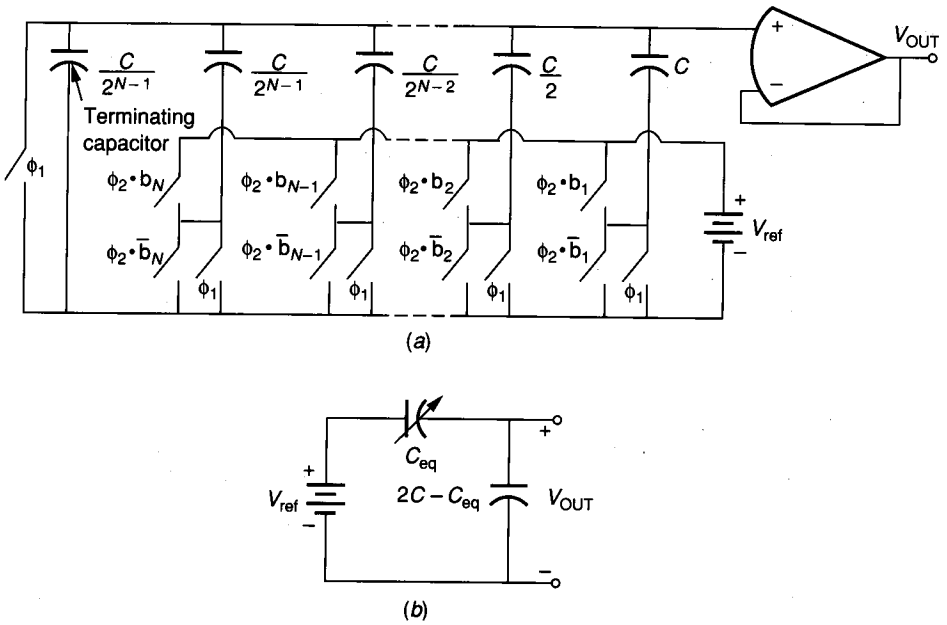

FIGURE 8.2-15
(*a*) Charge-scaling D/A converter, switches designated as $\phi_2 \cdot b_i (\phi_2 \cdot \bar{b}_i)$ close if both ϕ_2 and $b_i (\bar{b}_i)$ are true during ϕ_2, (*b*) Equivalent circuit of *a*.

From Eq. 8.2-12 we may solve for V_{OUT} as

$$V_{OUT} = (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N}) V_{ref} \qquad (8.2\text{-}13)$$

Another approach to understanding the circuit of Fig. 8.2-15*a* is to consider the capacitor array as a capacitive attenuator, illustrated in Fig. 8.2-15*b*. As before, C_{eq} consists of the sum of all capacitances connected to V_{ref}, and C_{tot} is the sum of all the capacitors in the array.

The D/A of Fig. 8.2-15*a* can be extended to have both + and − analog outputs if the bottom plates of all capacitors are connected to V_{ref} during the ϕ_1 phase period. During the ϕ_2 phase period, the capcitance associated with b_i, C_i is connected to ground if b_i is 1 or to V_{ref} if b_i is 0. The resulting output voltage is

$$V_{OUT} = -(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_N 2^{-N}) V_{ref} \qquad (8.2\text{-}14)$$

The decision to select the + or − output will require an additional sign bit. If V_{ref} is also bipolar, then a four-quadrant D/A converter results.

The accuracy of the capacitors and the area required are both factors that limit the number of bits used. The accuracy of the D/A converter is seen to depend totally on the capacitor ratios and any parasitics. The accuracy of the equal-valued capacitor ratios for an MOS technology can be as low as 0.1% or better. If all of the capacitor ratios have this accuracy, then the D/A converter

of Fig. 8.2-15*a* should be capable of a 10-bit resolution. However, this implies that the ratio between the MSB and LSB capacitors will be 1024:1 which is undesirable from an area viewpoint. Also, the 0.1% capacitor ratio accuracy is applicable only for ratios in the neighborhood of unity.

Example 8.2-2. Assume that unit capacitors of 50 $\mu \times 50$ μ are used in the charge-scaling D/A converters of Fig. 8.2-15*a* and that the relative accuracy is 0.1%. Find the number of bits possible using a worst case approach assuming that the worst conditions occur at midscale (1 MSB). Next, assume that the relative accuracy of the unit capacitors deteriorates with N as given by

$$\frac{\Delta C}{C} \simeq 0.001 + 0.0001N$$

and find the number of bits possible using a worst case approach.

Solution. From Fig. 8.2-15*b* the ideal output voltage of the charge-scaling D/A converter can be expressed as

$$\frac{V_{\text{OUT}}}{V_{\text{REF}}} = \frac{C_{\text{eq}}}{2C}$$

Assume the worst-case output voltage is given as

$$\frac{V'_{\text{OUT}}}{V_{\text{REF}}} = \frac{C_{\text{eq}}(\text{min})}{[2C - C_{\text{eq}}](\text{max}) + C_{\text{eq}}(\text{min})}$$

The difference between the ideal and the worst case output can be written as

$$\frac{V_{\text{OUT}}}{V_{\text{REF}}} - \frac{V'_{\text{OUT}}}{V_{\text{REF}}} = \frac{C_{\text{eq}}}{2C} - \frac{C_{\text{eq}}(\text{min})}{[2C - C_{\text{eq}}](\text{max}) + C_{\text{eq}}(\text{min})}$$

If we assume that the worst-case condition occurs at midscale, then C_{eq} is equal to C. Therefore the difference between the ideal output and the worst-case output is

$$\frac{V_{\text{OUT}}}{V_{\text{REF}}} - \frac{V'_{\text{OUT}}}{V_{\text{REF}}} = \frac{1}{2} - \frac{C(\text{min})}{C(\text{max}) + C(\text{min})}$$

Replacing $C(\text{max})$ by $C + 0.5\Delta C$ and $C(\text{min})$ by $C - 0.5\Delta C$ and setting the difference between the ideal and worst-case output voltage equal to ± 0.5 LSB results in the following equation

$$\frac{\Delta C}{2C} = \frac{1}{2^N}$$

Using a value of 0.001 for $\Delta C/C$ gives approximately 11 bits. Using the approximation for $\Delta C/C$ of

$$\frac{\Delta C}{C} \simeq 0.001 + 0.0001N$$

shows that a 9-bit D/A converter should be realizable.

The cascade configuration of Fig. 8.2-13*a* can also be applied to the charge-scaling configuration. Figure 8.2-16*a* shows a 13-bit D/A converter with bipolar capability for V_{ref}. The 1.016 pF capacitor acts as a 64:1 divider,

which scales up the last 6 bits by a factor of 64. An equivalent circuit to the 13-bit D/A converter is shown in Fig. 8.2-16*b*. Two voltage sources are shown that depend on the state of each of the switches. The right-hand voltage source is given as

$$V_R = \sum_{i=1}^{7} \frac{\pm b_i C_i V_{ref}}{127} \tag{8.2-15}$$

where $C_i = C/2^{i-1}$ and the polarity of V_{ref} depends on the polarity of the digital word. The left-hand voltage source is given as

$$V_L = \sum_{k=8}^{13} \frac{\pm b_k C_k V_{ref}}{64} \tag{8.2-16}$$

where $C_k = C/(2^{k-7})$. The overall output of the D/A converter of Fig. 8.2-16*a* can be written as

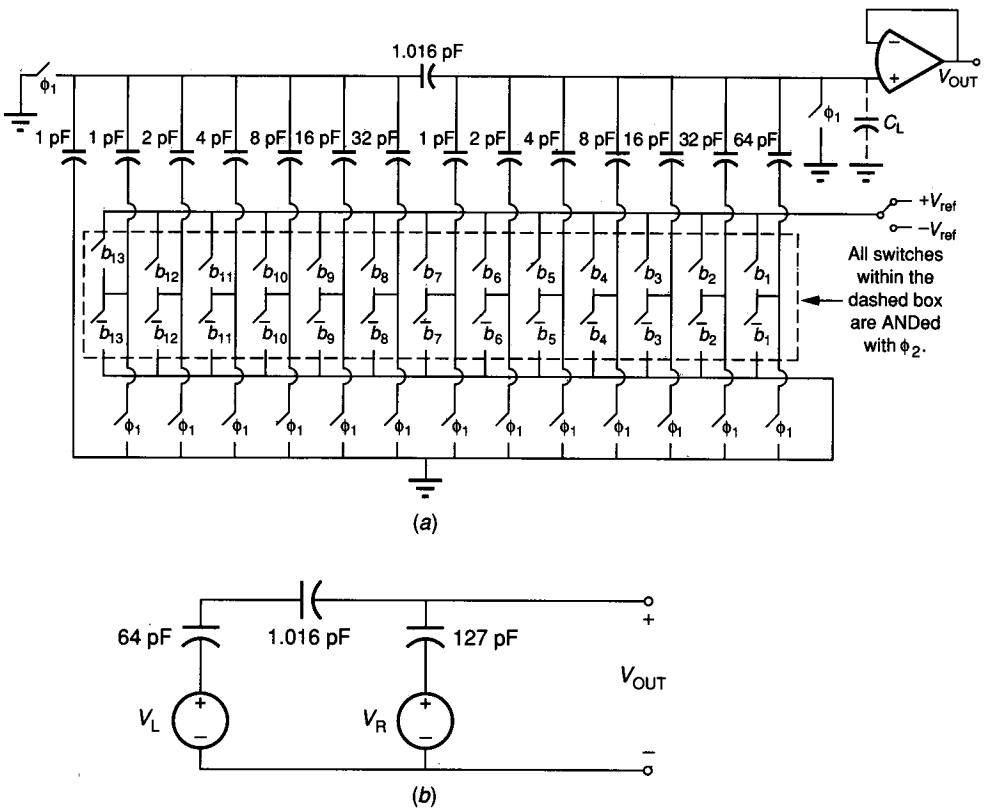

FIGURE 8.2-16
(*a*) A 13-bit, cascaded, charge-scaling D/A converter where C = 64 pF. Note that whether or not the switches in the dashed box close depends on the state of the binary variables, (*b*) An equivalent circuit of *a*.

$$V_{OUT} = \frac{\pm V_{ref}}{128}\left(\sum_{i=1}^{7} b_i C_i + \sum_{k=8}^{13} b_k \frac{C_k}{64}\right) \tag{8.2-17}$$

The charge-scaling D/A converters are sensitive to capacitive loading at the summing node. If this capacitance is designated as C_L, then Eq. 8.2-17 is modified as

$$V_{OUT} = \left(1 - \frac{C_L}{128}\right)\left(\frac{\pm V_{ref}}{128}\right)\left(\sum_{i=1}^{7} b_i C_i + \sum_{k=8}^{13} b_k \frac{C_k}{64}\right) \tag{8.2-18}$$

We see that C_L has caused an error of $\left[1 - (C_L/128)\right]$. If C_L is 1% of the total ladder capacitance, then a 1% error is introduced by the capacitance C_L.

The accuracy of the capacitor attenuator must also be good enough for the cascade approach to work. A deviation of the 1.016 pF divider capacitance from the desired ratio of 1.016:1 introduces both gain and linearity errors. Assuming a variation of $\pm\Delta C$ in the 1.016 pF capacitor modifies the output given in Eq. 8.2-17 to

$$V_{OUT} = \left(\frac{\pm V_{ref}}{128}\right)\left(1 - \frac{\Delta C}{128}\right)\left[\sum_{i=1}^{7} b_i C_i + (1 + \Delta C)\sum_{k=8}^{13} b_k \frac{C_k}{64}\right] \tag{8.2-19}$$

If we assume that $\Delta C/C = \pm 0.016$ (1.6% error), then the gain term has an error of

$$\text{Gain error term} = 1 - \left(\frac{\Delta C}{128}\right) = 1 - \left[\frac{1}{(64)(128)}\right] \tag{8.2-20}$$

which is negligible. The linearity error term is given by

$$\text{Linearity error term} = \Delta C \sum_{k=8}^{13} \frac{b_k C_k}{64} \tag{8.2-21}$$

The worst-case error occurs for all $b_i = 1$ and is essentially ΔC. It is also important to keep $+V_{ref}$ and $-V_{ref}$ stable and equal in amplitude. This influences the long-term stability and gain tracking of the D/A converter.

A different, charge redistribution, two-stage, 8-bit D/A converter is shown in Fig. 8.2-17. An op amp is connected in its inverting configuration with the $2C$ capacitor fed back from the output to the inverting input of the op amp. Because the input node is a virtual ground during operation, the capacitive parasitics associated with the input node to the op amp are eliminated. The converter of Fig. 8.2-17 should give better transient response and less error because of the removal of the influence of the capacitive parasitic at the op amp input.

8.2.4 D/A Converters Using Combinations of Scaling Approaches

The voltage-scaling and charge-scaling approaches to implementing D/A converters can be combined, resulting in converters having a resolution that exceeds the number of bits of the separate approaches. An M-bit resistor string and a K-bit binary-weighted capacitor array can be used to achieve an $N = (M + K)$-bit

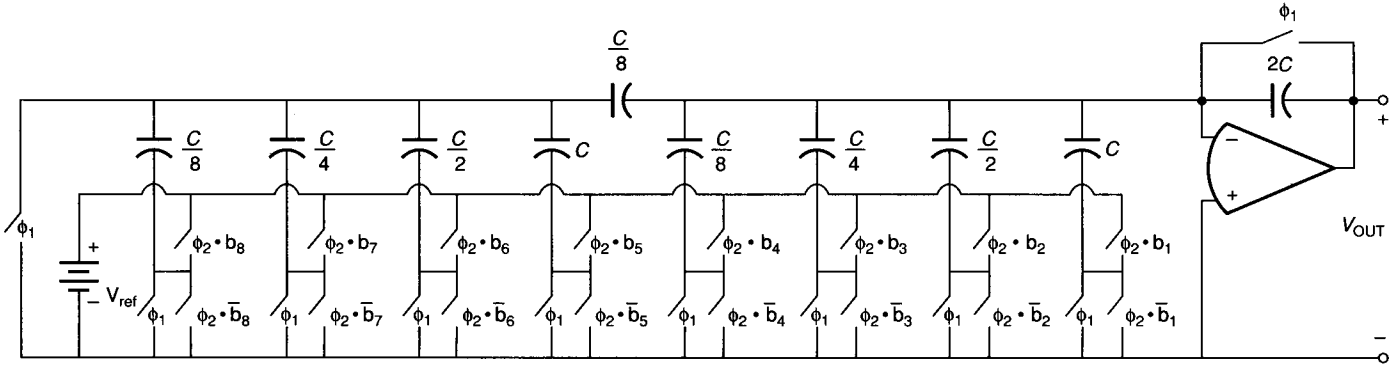

FIGURE 8.2-17
A cascade charge-scaling D/A converter that is insensitive to nodal capacitive parasitics for the MSB part.

conversion. Figure 8.2-18 gives an example of such a converter, where $M = 4$ and $K = 8$. The resistor string, R_1 through R_{2^M}, provides inherently monotonic V_{ref} for 2^M nominally identical voltage segments. The binary-weighted capacitor array, C_1 through C_K, is used to subdivide any one of these voltage segments into 2^K levels. This is accomplished by the following sequence of events. First, the switches S_F, S_B, and S_{M+1B} through $S_{K+M,B}$ are closed, connecting the top and bottom plates of the capacitors C_1 through C_K to ground. If the output of the D/A converter is applied to any circuit having an offset, switch S_B could be connected to this circuit rather than ground to cancel this offset. After opening switch S_F, the buses A and B are connected across one of the resistors of the resistor string as determined by the M MSBs. The upper and lower voltages across this resistor will be $V'_{\text{ref}} + 2^{-M} V_{\text{ref}}$ and V'_{ref}, respectively, where

$$V'_{\text{ref}} = V_{\text{ref}} (b_1 2^{-1} + b_2 2^{-2} + \cdots + b_{M-1} 2^{-(M-1)} + b_M 2^{-M}) \quad . \quad (8.2\text{-}22)$$

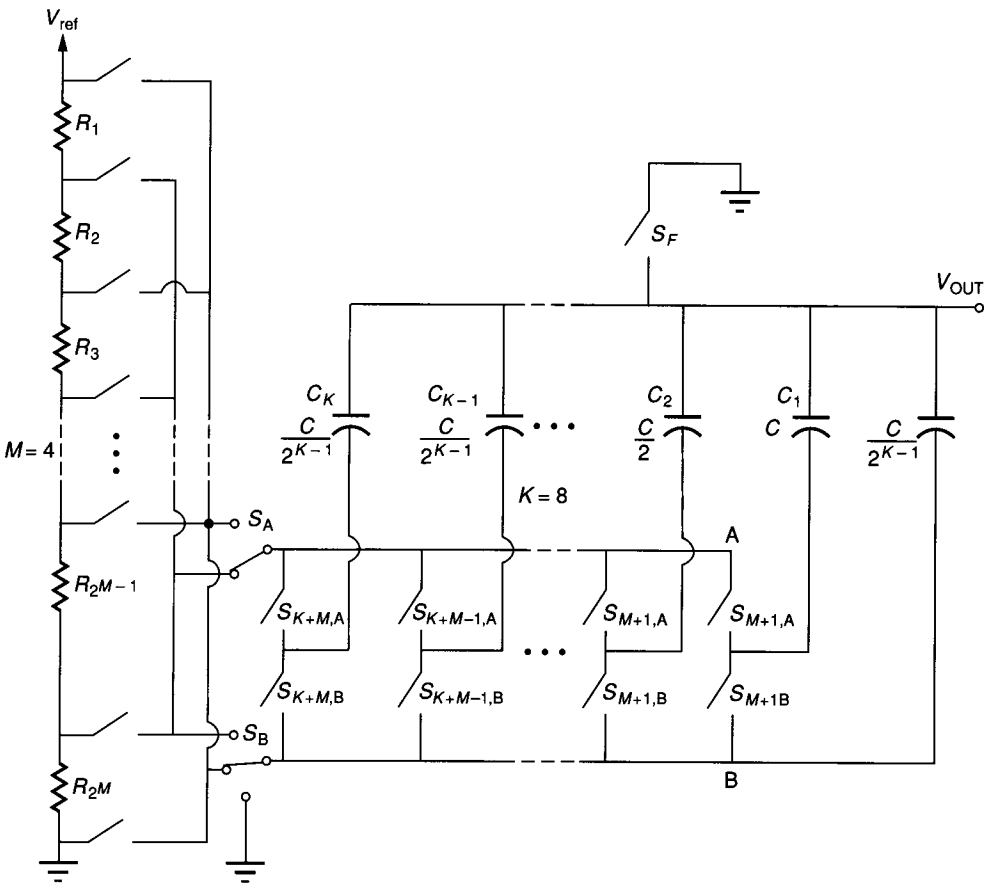

FIGURE 8.2-18
A D/A converter using a combination of voltage-scaling and charge-scaling techniques. The 4 MSBs are accomplished by voltage-scaling, and the 8 LSBs are accomplished by charge-scaling.

Although the resistor string could take the form of Fig. 8.2-14*a*, the configuration used in Fig. 8.2-18 switches both buses A and B. This causes any switch imperfections, such as clock feedthrough, to be canceled. The proper switch closures including S_A and S_B will require decoding of the M bits. After $2^{-M} V'_{ref}$ is applied between the buses A and B, we have the equivalent circuit of Fig. 8.2-19*a*. The final step is to decide whether or not to connect the bottom plates of the capacitors to bus A or bus B. This is determined by the bits of the digital word being converted. The equivalent circuit for the analog output voltage of the D/A converter of Fig. 8.2-18 is shown in Fig. 8.2-19*b*. The output of the D/A converter of fig. 8.2-18 is given as

$$V_{OUT} = V'_{ref} + V_{ref}\left[\frac{b_{M+1}}{2^{M+1}} + \frac{b_{M+2}}{s^{M+2}} + \cdots + \frac{b_{M+K+1}}{2^{M+K+1}} + \frac{b_{M+K}}{2^{M+K}}\right] \tag{8.2-23}$$

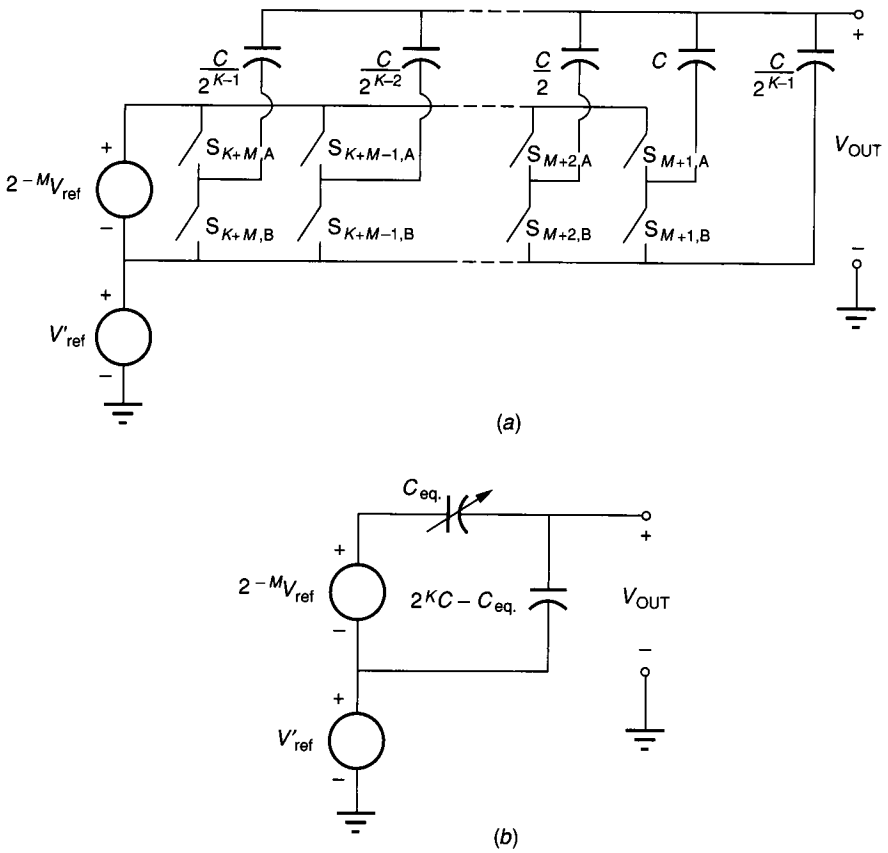

FIGURE 8.2-19
(*a*) Equivalent circuit of Fig. 8.2-18 for the voltage scaling part, (*b*) Equivalent circuit of the entire Fig. 8.2-18. C_{eq} is the sum of all the capacitors whose bit is 1.

The D/A converter of Fig. 8.2-18 has the advantage that, because the resistor string is inherently monotonic, the M MSB bits will be monotonic regardless of any resistor mismatch. This implies that the capacitor array has to be ratio-accurate to only K bits and still be able to provide $(M + K)$-bit monotonic conversion. The conversion speed for the resistors is faster than for the capacitors because no precharging is necessary. Therefore, some interesting tradeoffs can be made between area and speed of conversion. Techniques such as trimming the resistor string using polysilicon fuses can help to improve the integral linearity of this approach.

Other combinations of voltage scaling and charge scaling techniques are also possible. Instead of using resistive string techniques for the MSBs and binary-weighted capacitors for the LSBs, one can use binary-weighted capacitors for the MSBs and the resistor string for the LSBs. It is necessary to trim the resistors to maintain sufficient integral and differential nonlinearity for this case. Figure 8.2-20 illustrates how such a D/A converter could be implemented. The 3 to 4 MSBs will probably have to be trimmed, using a technique such as polysilicon fuses. The trimmed components are indicated by the dashed arrows through the appropriate capacitors in Fig. 8.2-20.

The combination of the voltage scaling and charge scaling allows for optimizing the performance. The choices are whether the MSBs will be resistors or capacitors and how the total number of bits will be divided into MSBs and LSBs.

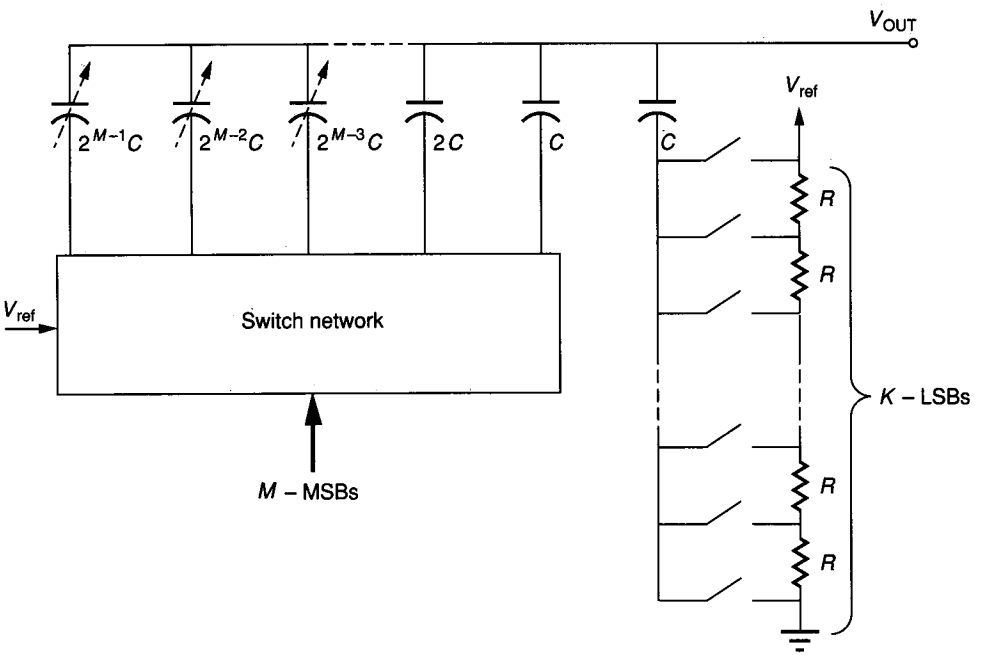

FIGURE 8.2-20
An illustration of a D/A converter using charge-scaling for MSBs and voltage-scaling for LSBs

For example, knowing the area of a unit resistor and a unit capacitor and their relative accuracies allows a tradeoff to be made in decreasing the area required and decreasing the nonlinearity of the D/A converter.

8.2.5 Serial D/A Converters

The last category of D/A converters to be considered in this section is the serial D/A converter. A serial D/A converter is one in which the conversion is done sequentially. In the best case, one clock cycle is required to convert one bit. Thus, N clock pulses would be required for the typical serial N-bit D/A converter. The two types of serial converters that will be examined here are the charge redistribution and the algorithmic D/A converters.

Figure 8.2-21 shows the simplified schematic of a serial charge redistribution D/A converter. We see that this converter consists of four switches, two equal-valued capacitors, and a reference voltage. The function of the switches is as follows. S1 is called the *redistribution switch* and places C_1 in parallel with C_2 causing their voltages to become identical through charge redistribution. Switch S2 is used to precharge C_1 to V_{ref}, if the ith bit, b_i, is a 1, and switch S3 is used to precharge C_1 to 0 V if the ith bit is 0. Switch S4 is used at the beginning of the conversion process to initially discharge C_2. An example is used to illustrate the operation of this D/A converter.

Example 8.2-3. Operation of the serial D/A converter. Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_1 = 1, b_2 = 1, b_3 = 0$, and $b_4 = 1$. Find the final voltage across C_1 and C_2 in terms of V_{ref}.

Solution. The conversion starts with the closing and opening of switch S4, so that $V_{C2} = 0$. Since $b_4 = 1$, then switch S2 is closed causing $V_{C1} = V_{ref}$. Next, switch S1 is closed, after switch S2 is opened, causing $V_{C1} = V_{C2} = 0.5V_{ref}$. This completes the conversion of the LSB. Figure 8.2-22 illustrates the waveforms across C_1 and C_2 in this example. Going to the next LSB, b_3, switch S3 is closed, discharging C_1 to ground. When switch S3 opens and switch S1 closes, the voltage across both C_1 and C_2 is $0.25V_{ref}$. Because the remaining bits are both 1, C_1 will be connected to V_{ref} and then connected to C_2 two times in succession. The final voltage across C_1 and C_2 will be $(13/16)V_{ref}$. This sequence of events will require nine sequential switch closures to complete the conversion.

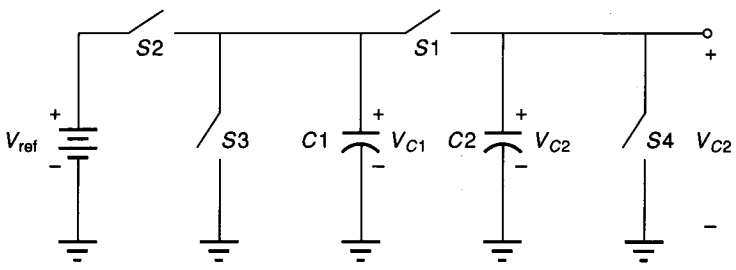

FIGURE 8.2-21
Simplified schematic of a serial charge redistribution D/A converter.

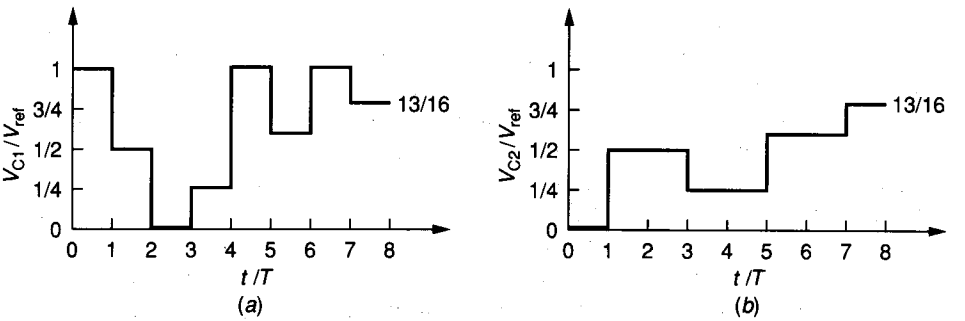

FIGURE 8.2-22
Waveforms of Fig. 8.2-21 for the conversion of 1101: (*a*) Voltage across C1, (*b*) Voltage across C2.

From this example, it can be seen that the serial D/A converter requires considerable supporting external circuitry to make the decision of which switch to close during the conversion process. Although the circuit for the conversion is extremely simple, several sources of error will limit the performance of this type of D/A converter. These sources of error include the capacitor parasitic capacitances, the switch parasitic capacitances, and the clock feedthrough errors. The capacitors C_1 and C_2 must be matched to within ± 0.5 LSB accuracy. This converter has the advantage of monotonicity and requires very little area for the portion shown in Fig. 8.2-21. An 8-bit converter using this technique has been fabricated and has demonstrated a conversion time of 13.5 μs.[4]

A second approach to serial D/A conversion is called *algorithmic*.[5] Figure 8.2-23 illustrates the pipeline approach to implementing an algorithmic D/A converter, consisting of unit delays and weighted summers. It can be shown that the output of this circuit is

$$V_{\text{out}}(z) = (d_1 z^{-1} + 2^{-1} d_2 z^{-2} + \cdots + 2^{-(N-1)} d_N z^{-N} + 2^{-N} d_{N+1} z^{-(N+1)}) V_{\text{ref}} \quad (8.2\text{-}24)$$

where d_i is a modified binary variable with a high state of $+1$ and a low state of -1 and z^{-1} is defined as the unit delay operator. Figure 8.2-23 shows that it takes n clock cycles for the digital word to be converted to an analog signal, even though a new digital word can be converted on every clock cycle. An advantage

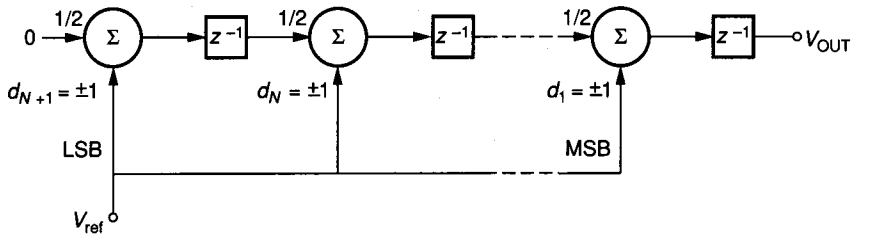

FIGURE 8.2-23
Pipeline approach to implementing an algorithmic D/A converter.

of the pipeline converter is that it can consist of similar stages. If a zero is input to the first amplifier, then the first stage is similar to the remaining stages.

The complexity of Fig. 8.2-23 can be reduced using the techniques of *replication* and *iteration*. Here we shall consider only the iteration approach. Equation 8.2-23 can be rewritten as

$$V_{\text{out}}(z) = \frac{d_i z^{-1} V_{\text{ref}}}{1 - 0.5z^{-1}} \tag{8.2-25}$$

where the d_i are either $+1$ or -1, determined as follows. Figure 8.2-24 shows a block diagram realization of Eq. 8.2-24. It consists of two switches, A and B. Switch A is closed when the ith bit is 1, and switch B is closed when the ith bit is 0. $d_i V_{\text{ref}}$ is summed with one-half of the previous output and applied to the sample-and-hold circuit, which outputs the results for the ith-bit conversion. The following example illustrates the conversion process.

Example 8.2-4. D/A conversion using the algorithmic method. Assume that the digital word to be converted is 11001 in the order of MSB to LSB and find the analog value of this digital word in terms of V_{ref}.

Solution. The conversion starts by zeroing the output (not shown in Fig. 8.2-24). Figure 8.2-25 is a plot of the output of this example. T is the period for the conversion of one bit. The process starts with the LSB, which in this case is 1. Switch A is closed and V_{ref} is summed with zero to give an output of $+V_{\text{ref}}$. On the second conversion, the bit is 0 so that switch B is closed. Thus, $-V_{\text{ref}}$ is summed with $(1/2)V_{\text{ref}}$ giving $-(1/2)V_{\text{ref}}$ as the output. On the third conversion, the bit is also 0, so that $-V_{\text{ref}}$ is summed with $-(1/4)V_{\text{ref}}$ to give an output of $-(5/4)V_{\text{ref}}$. On the fourth conversion, the bit is 1; thus, V_{ref} is summed with $-(5/8)V_{\text{ref}}$, giving $+(3/8)V_{\text{ref}}$ at the output. Finally, the MSB is unity, which causes V_{ref} to be summed with $(3/16)V_{\text{ref}}$, giving the final analog output of $+(19/16)V_{\text{ref}}$. Because the actual FSR of this example is $\pm V_{\text{ref}}$ or $2V_{\text{ref}}$, the analog value of the digital word 11001 is $(19/32) \times 2V_{\text{ref}}$, or $(19/16)V_{\text{ref}}$.

The algorithmic converter has the primary advantage of being independent of capacitor ratios; thus, it is often called the *ratio-independent* algorithmic D/A converter. However, the amplifier with a gain of 1/2 will still depend on capacitor

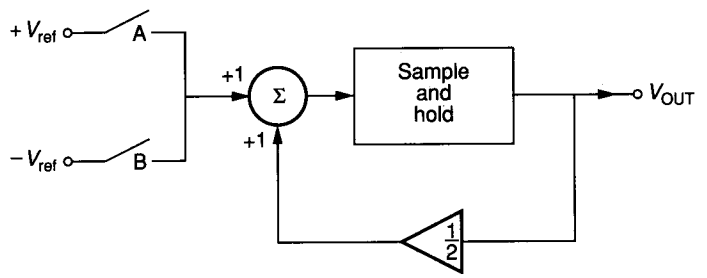

FIGURE 8.2-24
Equivalent realization of Fig. 8.2-23 using iterative techniques.

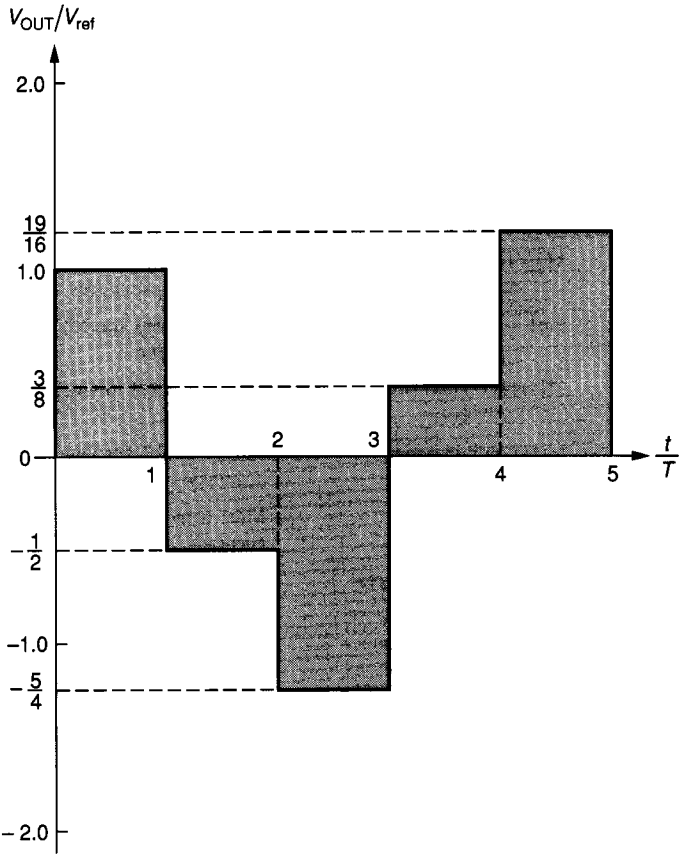

FIGURE 8.2-25
Output waveform for Fig. 8.2-24 for the conditions of Example 8.2-2.

ratios or other ratios and must have an accuracy better than ±0.5 LSB. The algorithmic converter will be presented again under the subject of serial A/D converters. The serial D/A converter is very simple but requires a longer time for conversion. In some applications, these characteristics are advantageous.

D/A converter techniques compatible with BJT and MOS technology have been presented in this section. Table 8.2-1 gives a summary of these D/A

TABLE 8.2-1
Comparison of the D/A conversion techniques compatible with BJT and MOS technology

D/A converters	Figure	Advantage	Disadvantage
Current-scaling, binary-weighted	8.2-10	Fast; insensitive to switch parasitics	Large element spread; nonmonotonic
Current-scaling, *R*-2*R* ladder	8.2-11	Fast; small element spread	Nonmonotonic; sensitive to switch parasitics

(continued)

TABLE 8.2-1
(Continued)

D/A converters	Figure	Advantage	Disadvantage
Current-scaling, cascade	8.2-13*a*	Minimum area; monotonic	R_1 must be accurate
Current-scaling, master-slave	8.2-13*b*	Minimum area; monotonic	I_1 must be accurate
Voltage-scaling	8.2-14*a*	Monotonic	Large area; sensitive to parasitic capacitances
Charge-scaling	8.2-15*a*	Fast	Large element spread; nonmonotonic
Charge-scaling, cascade	8.2-16*a*	Minimum area	Nonmonotonic; divider must be accurate
Voltage-scaling, charge-scaling	8.2-18	Monotonic in MSBs	Must trim for absolute accuracy
Charge scaling, voltage-scaling	8.2-20	Monotonic in LSBs	Must trim for absolute accuracy
Serial, charge redistribution	8.2-21	Simple; minimum area	Slow; requires complex external circuits
Serial, algorithmic	8.2-24	Simple; minimum area	Slow; requires complex external circuits

converters. In the following sections, we shall examine the complementary subject of A/D converters. Many of the A/D converters that will be discussed use the D/A converters developed and illustrated in this section.

8.3 ANALOG-TO-DIGITAL CONVERTERS

The principles and characteristics of analog-to-digital converters are examined in this section. The objective of an A/D converter is to determine the output digital word corresponding to an analog input signal. The A/D converter usually requires a sample-and-hold circuit at the input because it is not possible to convert a changing analog input signal. We shall see that A/D converters often make use of D/A converters, which is why this section follows the last. The types of A/D converters that will be considered include the serial, successive approximation, parallel (flash), and high performance A/D converters.

Figure 8.3-1 shows the block diagram of a basic parallel A/D converter. The input to the A/D is from a sample-and-hold circuit and is designated as V_{in}^*. The voltages V_0 through V_{N-1} represent reference voltages that are all proportional to a single reference voltage, V_{ref}. The input, along with a reference voltage, V_{ref}, is used to determine the digital word that best represents the sampled analog input signal. The comparator outputs, X_i, are then encoded into an output digital word. The means by which the conversion is accomplished may be different from that suggested in Fig. 8.3-1. Regardless of how the conversion is made, the A/D

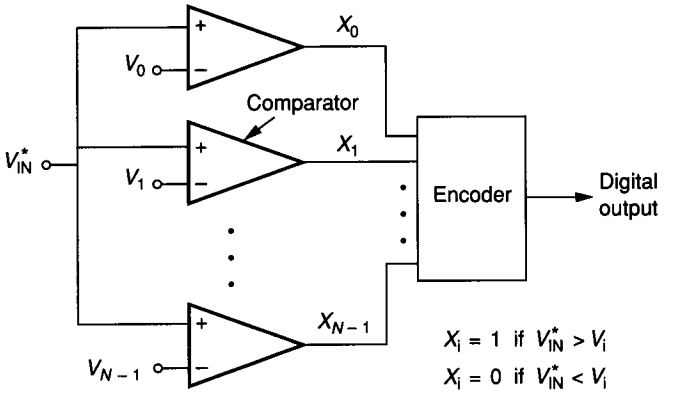

FIGURE 8.3-1
Block diagram of a general analog-to-digital converter.

converter is a device that converts a continuous range of input amplitude levels into a discrete, finite set of digital words.

The characterization of the A/D converter is almost identical to that of the D/A converter in the last section if the input and output definitions are interchanged. The static A/D converter properties will be considered first. Figure 8.3-2 shows the transfer characteristic of an ideal 3-bit A/D converter. This characteristic is analogous to Fig. 8.2-6 for the D/A converter. The analog input

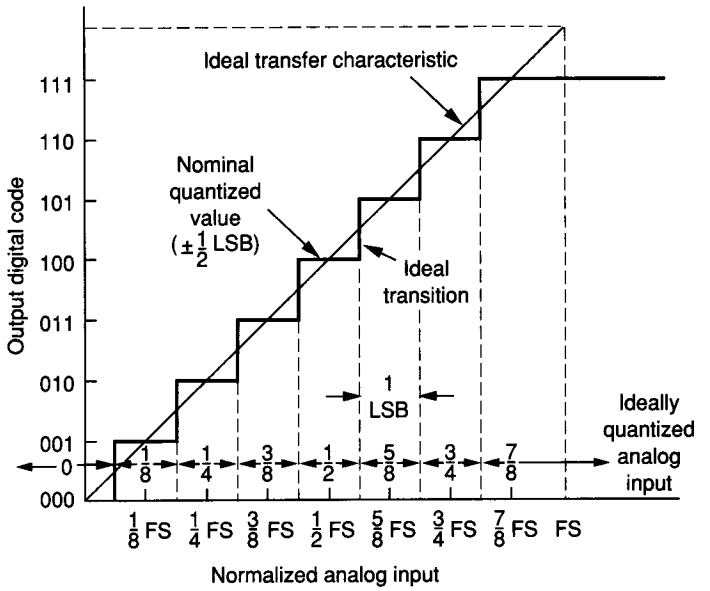

FIGURE 8.3-2
Ideal input-output characteristics for a 3-bit A/D converter.

voltage normalized to full scale (FS) is shown on the horizontal axis. The digital output code is given on the vertical axis.

The A/D converter has been designed so that the output digital word changes when the analog input is at odd multiples of FS/16. The LSB of the digital output code changes each time the analog input changes by $FS/2^n$ where n is equal to the number of digital bits. A change of $FS/2^n$ in the analog input is called an LSB in the same manner as defined for the D/A converter. In Fig. 8.3-2, an LSB is the length of the horizontal part of the stairstep, or FS/8. The ideally quantized ranges of the analog input are shown just above the horizontal axis on Fig. 8.3-2. These ranges are centered about even multiples of FS/16 except for the rightmost and leftmost, which have no right or left limits, respectively.

The definitions of resolution and quantization noise were given in Sec. 8.2 for both the A/D and D/A converter. The straight line on Fig. 8.3-2 through the midpoint of each step represents the ideal transfer characteristic of the A/D converter as the resolution approaches infinity. The full scale range, dynamic range, and the signal-to-noise ratio defined in Sec. 8.2 in terms of the analog axis of the characteristic also apply to the A/D converter.

The remaining static characteristics include offset error, gain error, nonlinearity, and monotonicity. Figure 8.3-3 illustrates each one of these characteristics for a 3-bit A/D converter. In each case, the ideal characteristic is shown by dashed lines for comparison. Because these characteristics are usually referred to the analog signal, the definitions given in Sec. 8.2 are also applicable for the A/D converter. Figure 8.3-3*a* illustrates the offset error in a 3-bit A/D converter. Figure 8.3-3*b* shows the gain error for the A/D converter and is similar to that of Fig. 8.2-7*b*. Figure 8.3-3*c* shows the nonlinearity characteristics of a 3-bit A/D converter. Integral and differential nonlinearity have the same definition as for the D/A converter. The maximum deviation from ideal occurs at the transition from 110 to 111 and is 1.5 LSB or 18.75% of FS. Figure 8.3-3*d* illustrates excessive differential nonlinearity, which causes nonmonotonic behavior in D/A converters. However, in A/D converters, nonmonotonicity typically manifests itself as missed codes. In Fig. 8.3-3*d* the digital codes 010, 011, and 110 are skipped.

The dynamic characteristics of an A/D converter have to do primarily with the speed of operation. Because either the input or the output of a converter is a digital word, sampling or discrete time signals are inherent. Therefore, the rate at which the converter can operate is of interest. The *conversion time* is the time from the application of the signal to start conversion to the availability of the completed output signal (digital or analog). Typically, a D/A converter can provide an analog output signal very soon after the digital word is applied (except for the serial converters). On the other hand, A/D converters may require one or more clock cycles following the application of the analog input signal before the output digital word is available.

Because a sample-and-hold circuit is a key aspect of the A/D converter, it is worthwhile to examine it in more detail than that of Fig. 8.2-3. Figure 8.3-4 shows the waveforms of a practical sample-and-hold circuit. The *acquisition time*, indicated by t_a, is the time during which the sample-and-hold circuit must remain in the sample mode to ensure that the subsequent hold mode output will be within a specified error band of the input level that existed at the instant of

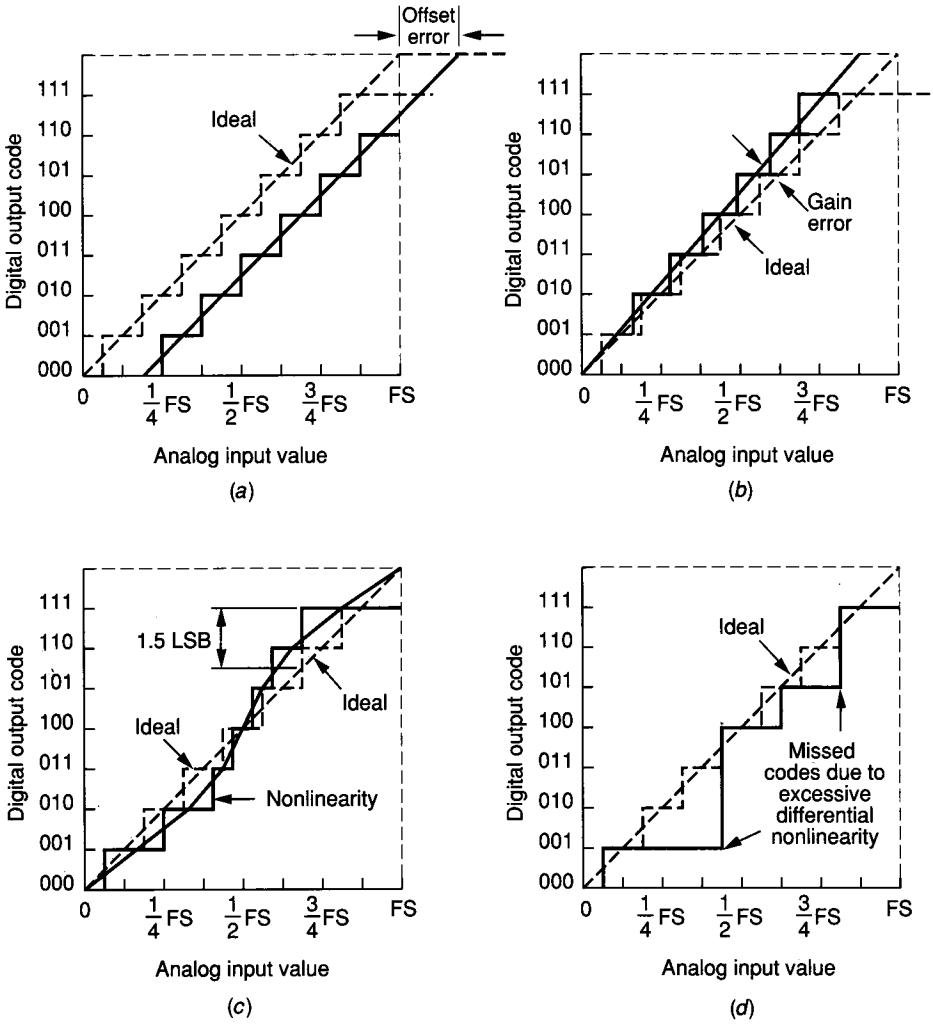

FIGURE 8.3-3
Characterization of a 3-bit A/D converter: (*a*) Offset error, (*b*) Scale factor (gain) error, (*c*) Integral linearity, (*d*) Differential linearity.

the sample-and-hold conversion. The acquisition time assumes that the gain and offset effects have been removed. The *settling time*, indicated by t_s, is the time interval between the sample-and-hold transition command and the time when the output transient and subsequent ringing have settled to within a specified error band. Thus, the minimum sample-and-hold time is equal to the sum of t_a and t_s. The minimum conversion time for an A/D converter is equal to T_{sample}, and the maximum sample rate is

$$f_{\text{sample}} = \frac{1}{T_{\text{sample}}} = \frac{1}{t_s + t_a} \tag{8.3-1}$$

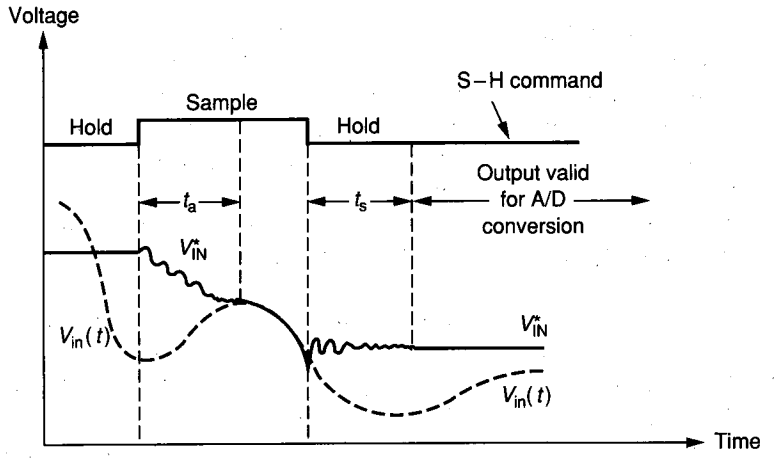

FIGURE 8.3-4
Waveforms for a sample-and-hold circuit.

The dynamic performance of the converter will depend largely on the dynamic characteristics of the op amps and comparators. Therefore, the slew rate, settling time, and overload recovery time of these circuits are of importance. It should be remembered that f_{sample} is the maximum sample rate and the effective bandwidth will be at least two times lower than f_{sample} to satisfy Nyquist criterion.

An important aspect of the conversion time is the aperture uncertainty. The *aperture uncertainty* is the time jitter in the sample point and is caused by short-term stability errors in the timebase generating the sample command to the A/D converter. The time jitter causes an amplitude uncertainty, which depends on the rate of rise of the signal at the sample point.

In addition to the dynamic characteristics of converters, there are characteristics having to do with stability of operation. These characteristics define the immunity of the converter to time, temperature, power supplies, and component aging. These characteristics are typically expressed in terms of the change of the converter performance parameter per unit change in the quantity affecting influence. Examples include the *temperature coefficient of linearity, temperature coefficient of gain,* and the *temperature coefficient of differential nonlinearity*. Also of importance to the stability of a converter is the voltage reference, which was presented in Chapter 5. The voltage reference can be supplied externally or internally to the integrated circuit converter. It is important that the reference provide the stability necessary for the proper operation of the converter.

It is of interest to consider how one can test converters. Testing is divided into static and dynamic tests for D/A and A/D converters. Most test configurations require the ability to resolve the analog signal to within ± 0.5 LSB, which can be very demanding if the number of bits is large. Techniques for testing both types of converters can be found in more detail in the literature.[6-8] Often, a computer