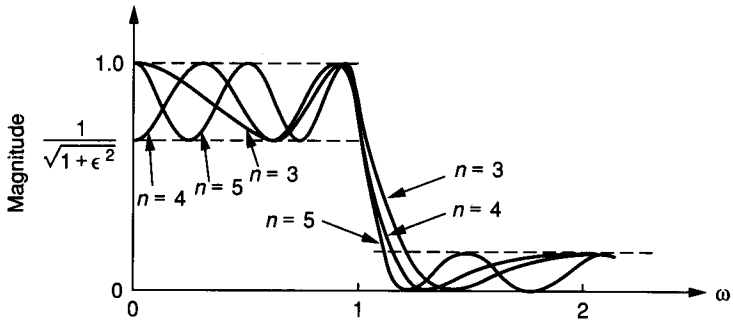

FIGURE 8.4-5
Magnitude characteristics of an elliptic approximation with arbitrary ϵ and for orders of n = 3, 4, and 5.

convert the vertical axis to a decibel range. Figure 8.4-6*a* shows the gain specifications, G, of a low-pass filter with the vertical axis specified in decibels and the frequency axis normalized to ω_{PB}. Ω is defined as ω_{SB}/ω_{PB} and G_Ω (dB) $= 20 \log_{10} G_{SB}$. Because the gains of most filters are less than unity, attenuation rather than gain is often used to describe their characteristics. Figure 8.4-6*b* shows the equivalent specification of Fig. 8.4-6*a* in terms of attenuation, $A = 1/G$, where $A_{PB} = 1/G_{PB}$ [A_{PB} (dB) $= -G_{PB}$ (dB)], and $A_\Omega = 1/G_\Omega$ [A_Ω (dB) $= -G_\Omega$ (dB)].

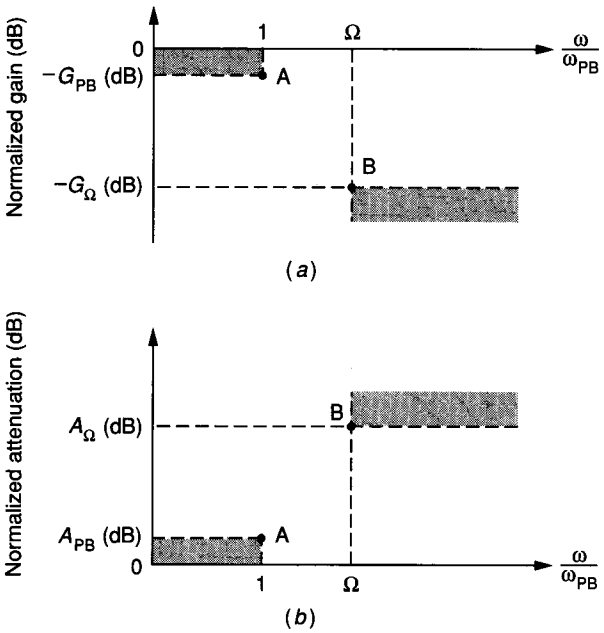

FIGURE 8.4-6
(*a*) Specifications for a low-pass filter in terms of gain, (*b*) Specifications for a low-pass filter in terms of attenuation.

From the parameters A_Ω, A_{PB}, and Ω, the order of the filter can be quickly determined using a set of nomographs.[35] Figure 8.4-7 is a nomograph for determining the order of the Butterworth filter approximation. The use of nomographs is illustrated in Fig. 8.4-8. A straight line is drawn through the specified values of A_{PB} and A_Ω, shown as points 1 and 2 in Fig. 8.4-8. The intersection with the

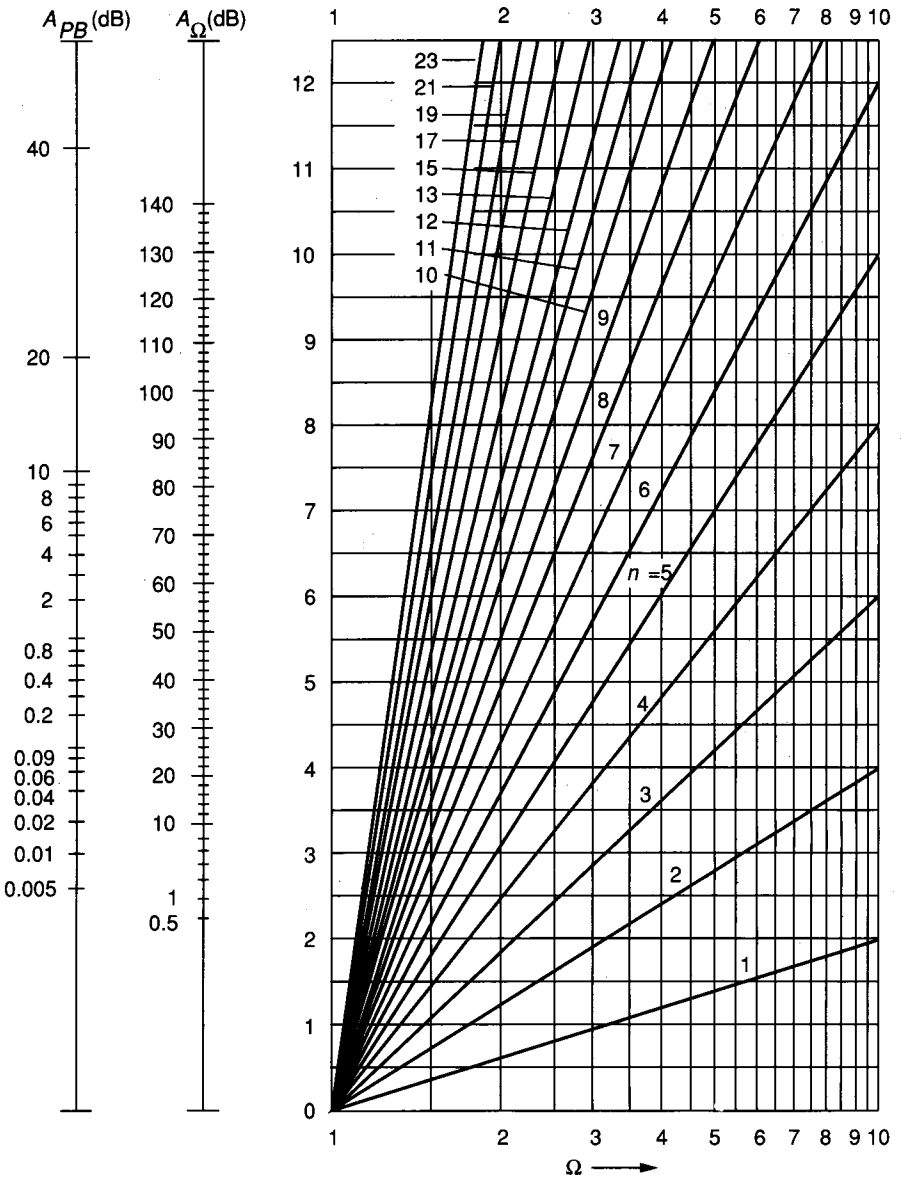

FIGURE 8.4-7
A nomograph for determining the order of a Butterworth magnitude function (Kawakami).

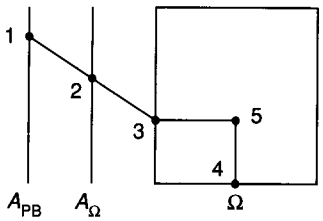

FIGURE 8.4-8
The method for using the nomograph of Fig. 8.4-7.

left side of the graph (point 3) is then extended horizontally until it meets a line drawn vertically from point 4, corresponding to the desired normalized stopband frequency, Ω. The resulting intersection at point 5 establishes the required order of the filter. If point 5 is between two of the *order loci*, the higher one must be used.

Example 8.4-1. Determination of the order of a low-pass Butterworth filter. Find the order of a Butterworth filter approximation to Fig. 8.4-6*b* where $A_{\Omega} = 40$ dB, $A_{PB} = 3$ dB, and $\Omega = 2$.

Solution. Using the nomograph of Fig. 8.4-7, we find that point 5 lies between $n = 6$ and $n = 7$. Therefore, the order of the filter approximation must be 7.

Figures 8.4-9 and 8.4-10 give the corresponding nomographs for determining the order or degree of Chebyshev and elliptic filter approximations, respectively. These nomographs are used in the same manner as the one in Fig. 8.4-7. An example will illustrate how the Chebyshev and elliptic filter approximations require lower order than the Butterworth filter approximation for the same design parameters.

Example 8.4-2. Determination of low-pass Chebyshev and elliptic filter approximations. Repeat the preceding example to find the order of the Chebyshev and elliptic filter approximations that will meet the same specifications.

Solution. From Fig. 8.4-9 we obtain $n = 4$ for the Chebyhev filter approximation, and from Fig. 8.4-10 we see that $n = 3$ is sufficient for the elliptic filter approximation to satisfy the specifications.

Once the order of the filter approximation is known, the designer must then decide how the filter is to be realized. Two approaches will be considered. The first approach starts with Eq. 8.4-6 in which the numerator and denominator polynomials are factored in the form of second-order products with real coefficients (a first-order product will be necessary if n is odd). This information can be found from the tabulations in the literature. For example, Table 8.4-1 shows the denominator coefficients of Eq. 8.4-6 with $b_0 = 1$ and gives the pole locations and quadratic functions of the denominator of Eq. 8.4-6 for the Butterworth filter approximations. The numerator polynomial of Eq. 8.4-6 for the Butterworth filter approximation is a constant. In this case the function $H(s)$ can be expressed as

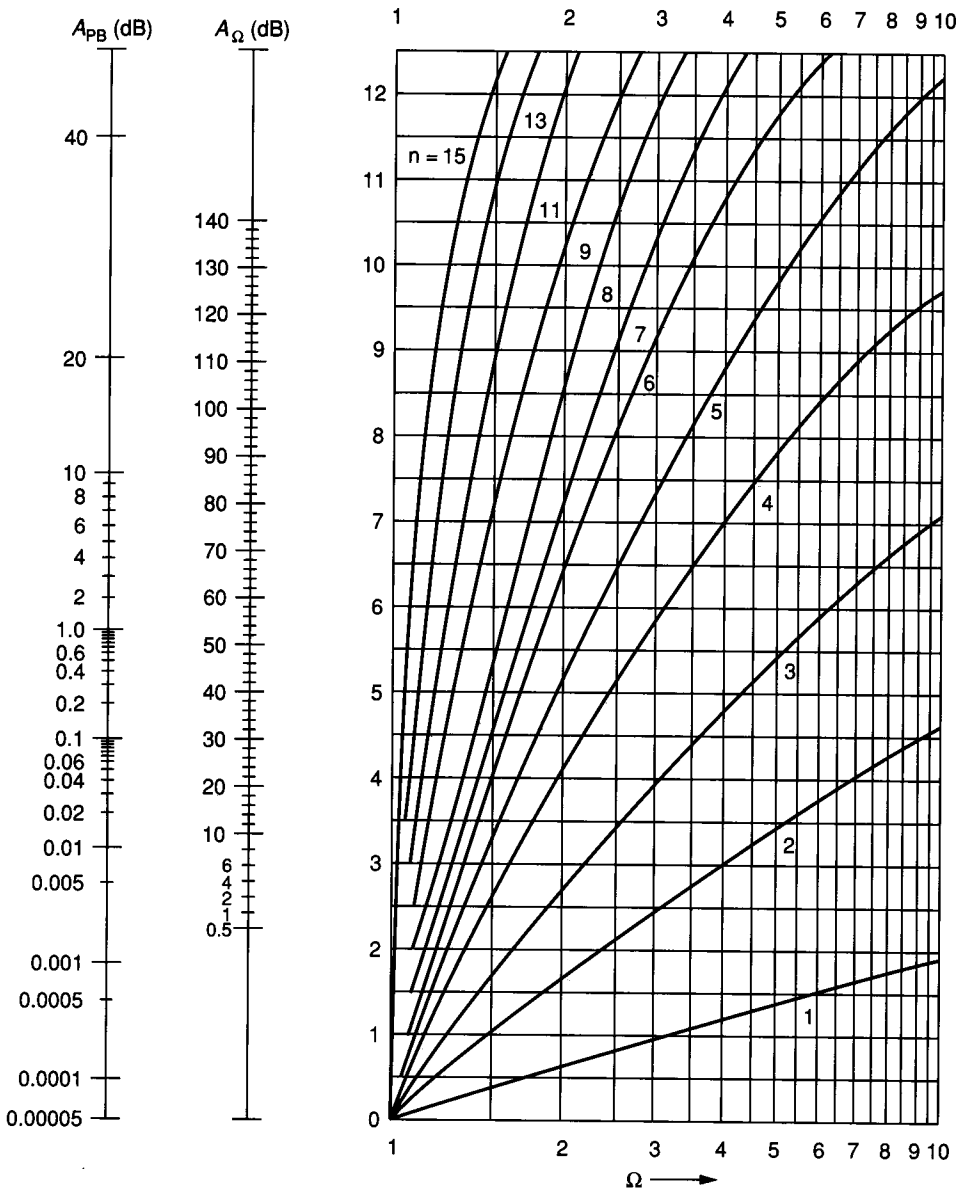

FIGURE 8.4-9
A nomograph for determining the order of a Chebyshev magnitude approximation (Kawakami).

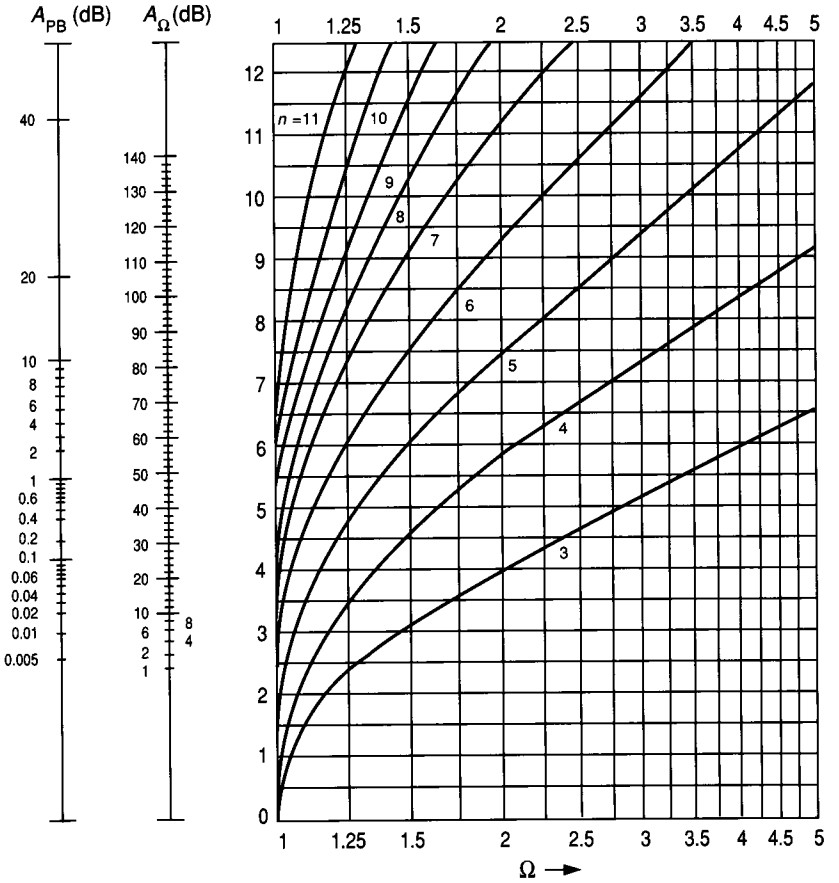

FIGURE 8.4-10
A nomograph for determining the order of an elliptic magnitude approximation (Kawakami).

TABLE 8.4-1*a*
Denominator coefficients of maximally flat magnitude (Butterworth) functions of the form: $s^n + b_{n-1}\,s^{n-1} + b_{n-2}\,s^{n-2} + \cdots b_2 s^2 + b_1 s + 1$ with passband 0 – 1 rad/s

n	b_1	b_2	b_3	b_4	b_5
2	1.414214				
3	2.000000				
4	2.613126	3.414214			
5	3.236068	5.236068			
6	3.863703	7.464102	9.141620		
7	4.493959	10.097835	14.591794		
8	5.125831	13.137071	21.846151	25.688356	
9	5.758770	16.581719	31.163437	41.986386	
10	6.392453	20.431729	42.802061	64.882396	74.233429

(By permission from L. P. Huelsman and P. E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill Book Co., New York, 1980.)

TABLE 8.4-1*b*
Pole locations and quadratic factors ($s^2 + b_1 s + 1$) of maximally flat magnitude (Butterworth) functions with passband 0 − 1 rad/s (*Note:* All odd-order functions also have a pole at $s = 1$)

n	Poles	b_1
2	$-0.70711 \pm j0.70711$	1.41421
3	$-0.50000 \pm j0.86603$	1.00000
4	$-0.38268 \pm j0.92388$	0.76536
	$-0.92388 \pm j0.38268$	1.84776
5	$-0.30902 \pm j0.95106$	0.61804
	$-0.80902 \pm j0.58779$	1.61804
6	$-0.25882 \pm j0.96593$	0.51764
	$-0.70711 \pm j0.70711$	1.41421
	$-0.96593 \pm j0.25882$	1.93186
7	$-0.22252 \pm j0.97493$	0.44504
	$-0.62349 \pm j0.78183$	1.24698
	$-0.90097 \pm j0.43388$	1.80194
8	$-0.19509 \pm j0.98079$	0.39018
	$-0.55557 \pm j0.83147$	1.11114
	$-0.83147 \pm j0.55557$	1.66294
	$-0.98079 \pm j0.19509$	1.96158
9	$-0.17365 \pm j0.98481$	0.34730
	$-0.50000 \pm j0.86603$	1.00000
	$-0.76604 \pm j0.64279$	1.53208
	$-0.93969 \pm j0.34202$	1.87938
10	$-0.15643 \pm j0.98769$	0.31286
	$-0.45399 \pm j0.89101$	0.90798
	$-0.70711 \pm j0.70711$	1.41421
	$-0.89101 \pm j0.45399$	1.78202
	$-0.98769 \pm j0.15643$	1.97538

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a product of biquadratic functions, $H_i(s)$, where the general form of the second-order (quadratic) function will be

$$H(s) = \frac{\pm H_{0i}\omega_{pi}^2}{s^2 + (\omega_{pi}/Q_i)s + \omega_{pi}^2} = \frac{\pm H_{0i}p_{1i}p_{2i}}{(s + p_{1i})(s + p_{2i})} \tag{8.4-7}$$

where H_{0i} is the gain at $\omega = 0$, ω_{pi} is the undamped natural frequency, and Q_i is the quality factor of the pole p_i and p_{2i} is the complex conjugate of p_{1i} if p_{1i} is not real.

Typically, the information tabulated on filter design is normalized so that ω_{PB} is unity. However, the actual filter specifications are usually in the neighborhood of thousands of cycles per second. To convert the *normalized frequency* values of the design tables to the actual filter frequency requires a *frequency denormalization*. This denormalization involves a change of the complex frequency variable. If we consider p as the normalized complex frequency variable and s as the denormalized (actual) one, then the frequency denormalization is defined as

$$s = \Omega_n p \tag{8.4-8}$$

where Ω_n is a dimensionless frequency denormalization constant. This denormalization is generally used at the synthesis stage of the design. Following this approach, a filter is initially synthesized to realize the normalized transfer function. The denormalization then entails a subsequent scaling of the component values in the filter. Table 8.4-2 shows how this denormalization acts on the normalized values of R, L, and C.

A second type of denormalization that is often used is called *impedance denormalization*. It permits an arbitrary scaling to be applied simultaneously to all the passive elements of a filter in order to get more practical component values. A normalized impedance $Z_n(s)$ can be denormalized to the impedance $Z(s)$ by the relation

$$Z(s) = z_n Z_n(s) \tag{8.4-9}$$

where z_n is a dimensionless impedance denormalization constant. Table 8.4-2 shows how this denormalization affects the passive elements. The combined effects of the denormalizations of Eqs. 8.4-8 and 8.4-9 are illustrated in this table. *This impedance denormalization does not affect the voltage or current gain of the filter.*

Figure 8.4-11 shows three possible active filter realizations of Eq. 8.4-7. Figure 8.4-11*a* uses a finite-gain amplifier and an RC feedback network. This circuit was originally proposed by Sallen and Key in 1955[36] and was one of the first active RC filter structures. This circuit does not have flexibility in realizing Eq. 8.4-7 if H_{oi} is also specified because H_{oi} is fixed and equal to $3 - (1/Q_i)$.

TABLE 8.4-2
Effect of frequency and impedance denormalization on network elements

Denormalized	R	C	L
$s = \Omega_n p$	R	$\frac{C}{\Omega_n}$	$\frac{L}{\Omega_n}$
$Z = z_n Z_n$	$z_n R$	$\frac{C}{z_n}$	$z_n L$
$Z(s) = z_n Z_n(p)$	$z_n R$	$\frac{C}{\Omega_n z_n}$	$\frac{z_n}{\Omega_n} L$

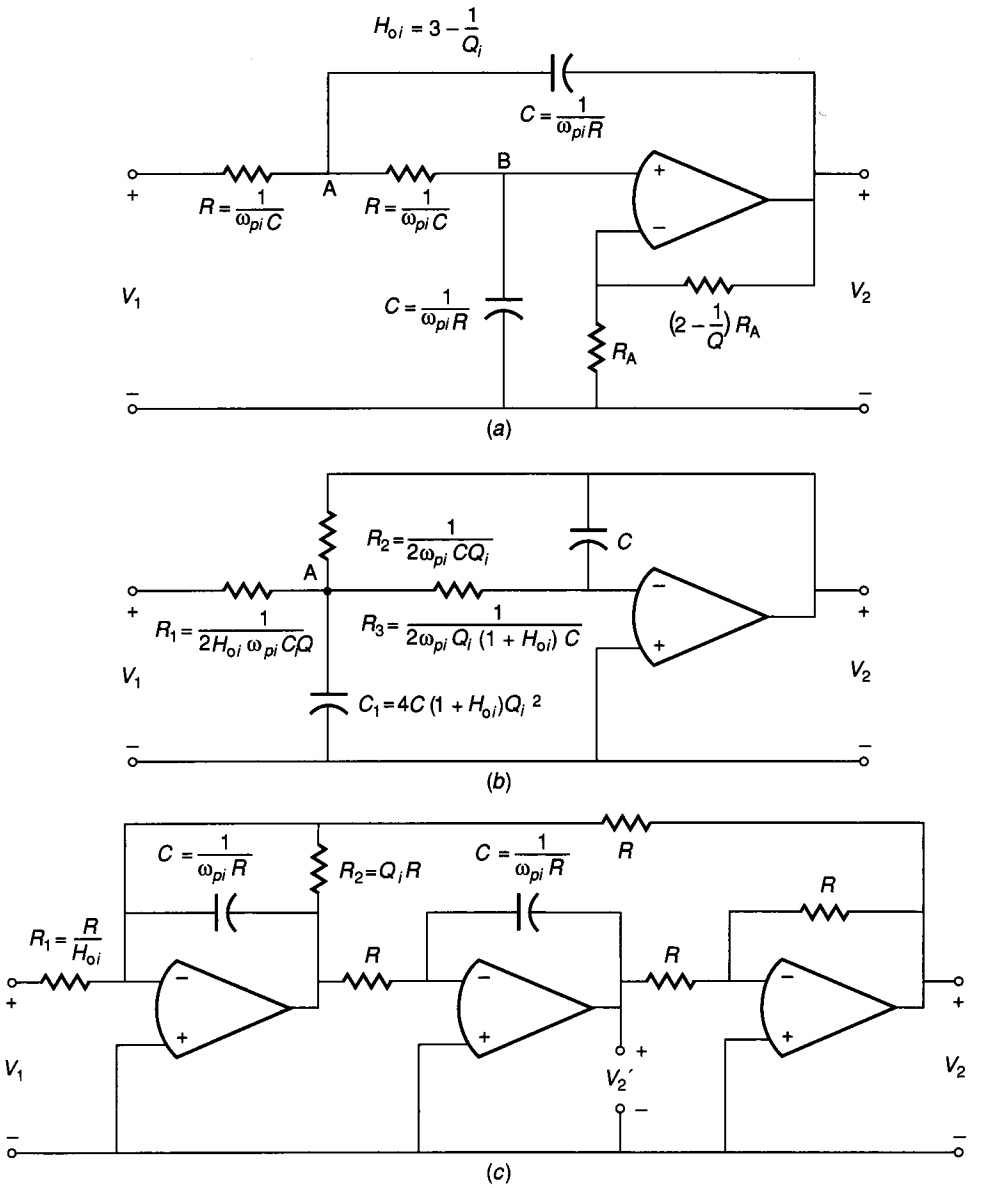

FIGURE 8.4-11
Three possible realizations of Eq. 8.4-7 (second-order, low-pass): (*a*) Sallen and Key (finite-gain) structure, (*b*) Infinite-gain structure, (*c*) Tow-Thomas (resonator) structure.

This is not considered a major limitation because the overall gain can be realized by adding a cascaded gain stage. In Fig. 8.4-11*a*, one may choose a suitable value for R; ω_{pi} and Q_i define the rest of the elements. Alternatively, one may choose a suitable value for the capacitors; then the resistors are defined as $(\omega_{pi}C)^{-1}$. The circuit of Figure 8.4-11*a* realizes Eq. 8.4-7 with a positive sign.

The circuit of Figure 8.4-11*b* is called an *infinite-gain realization*. It has the ability to realize simultaneously H_{oi}, ω_{pi}, and Q_i and realizes Eq. 8.4-7 with a negative sign. The circuit of Figure 8.4-11*c* is called the Tow-Thomas circuit[37,38] and consists of the cascade of a damped inverting integrator, an inverting integrator, and an inverter. This circuit has a great deal of flexibility and is very easy to tune. If the output is taken at V_2, then it realizes Eq. 8.4-7 with a negative sign. If the output is taken at V_2', then the circuit of Fig. 8.4-11*c* realizes Eq. 8.4-7 with a positive sign. In these circuits, a suitable value for either R or C is chosen and the remaining component values are calculated from the equations given in the figure. Many other realizations of Eq. 8.4-7 exist; however, the circuits of Fig. 8.4-11 are representative.

Example 8.4-3. Design of a low-pass Butterworth filter. A low-pass Butterworth filter is to be designed for the specifications of $A_\Omega = 30$ dB, $\omega_{PB} = 2000\pi$, and $\omega_{SB} = 4000\pi$.

Solution. If we normalize ω_{PB} to unity, we get $\Omega = 2$. From Fig. 8.4-7 we see that $n = 5$ will satisfy the filter specification. From Table 8.4-1, we conclude that this function can be realized with two second-order stages cascaded with one first-order stage. The realization is shown in Fig. 8.4-12*a*. The stage order is arbitrary, although one typically chooses the high-Q stages as the last stages. The normalized transfer function for each of the stages is shown, as well as Q_i and ω_{pi}. Note that stage 1 is a simple, first-order circuit so that Q is not defined. Stage 1 may be realized by a simple damped integrator, whereas one of the circuits in Fig. 8.4-11 can be used for stages 2 and 3. Selecting the circuit of Fig. 8.4-11*b* results in the realization of Fig. 8.4-12*b*, where the formulas of Fig. 8.4-12*a* have been used with $\omega_{pi} = 1$ for $i = 1, 2$ and 3, $Q_2 = 0.61804$, and $Q_3 = 1.61804$. The last step is to frequency-denormalize the realization using Eq. 8.4-8. To denormalize from a frequency of 1 rad/s to 2000π rad/s requires $\Omega_n = 2000\pi$. To avoid 1 Ω resistors, an impedance normalization of $z_n = 10^4$ will also be used. The resulting realization is shown in Fig. 8.4-12*c*. If a Butterworth filter approximation had been used for any value of A_{PB} other than -3 dB, then the normalized passband would not be unity. This must be taken into account when finding the proper Ω_n.

Note that the same circuit structure used in Fig. 8.4-12 could also be used to realize the Chebyshev function. In this case the quadratic functions would be obtained from tabulated data in the literature. Only the component values in Fig. 8.4-12*b* and *c* would vary in changing this realization from a Butterworth to a Chebyshev filter.

8.4.2 High-Pass Filters

Filters other than the low-pass type can be designed through the use of frequency transformations. These allow one to take the tabulated low-pass filter information

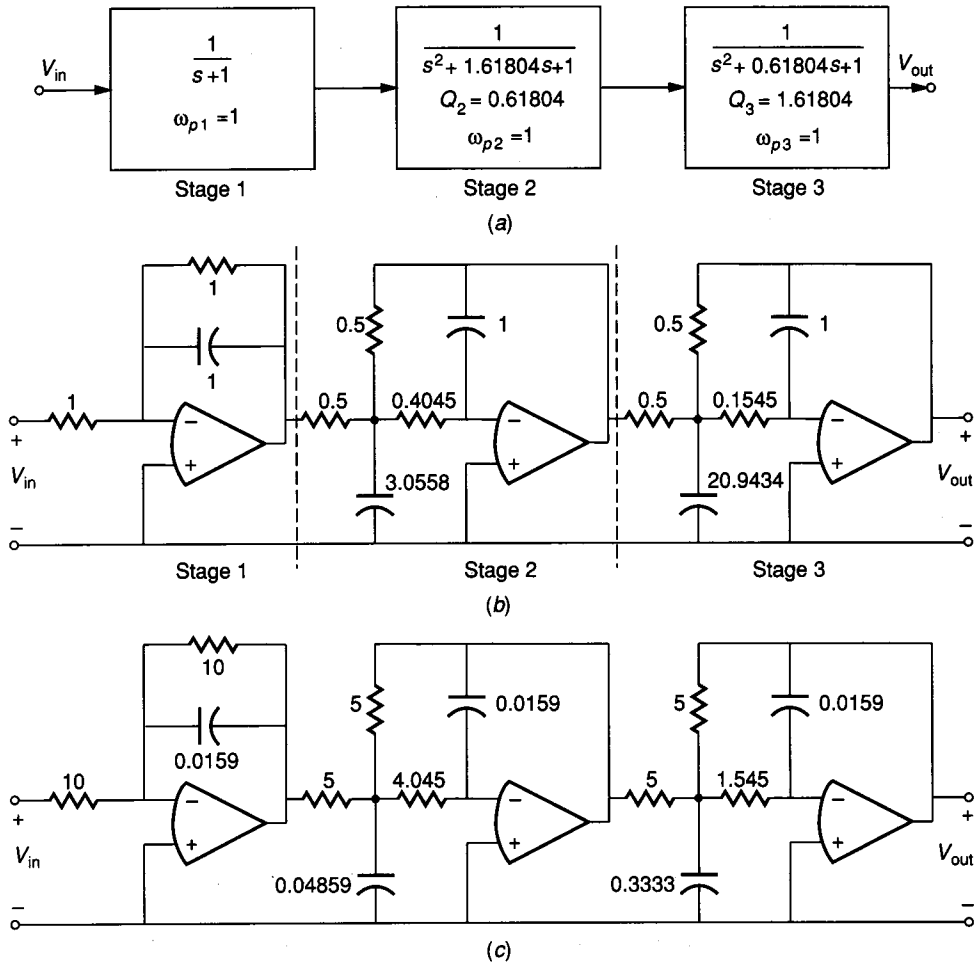

FIGURE 8.4-12
Realization for Example 8.4-3: (*a*) Stage ordering, (*b*) Normalized realization (all values in ohms or farads), (*c*) Frequency and impedance denormalized realization (all values in kilohms and microfarads).

and transform it to apply to high-pass, bandpass, or band-elimination filters. The transformed filter information can then be realized in a cascaded manner using the appropriate RC active stages. A low-pass to high-pass transformation can be defined as

$$s = \frac{1}{p} \tag{8.4-10}$$

where s is the low-pass complex frequency variable. Figure 8.4-13 illustrates how Eq. 8.4-10 transforms an ideal low-pass filter to an ideal high-pass filter. The poles of a high-pass filter can be found by substituting the low-pass poles for s in Eq. 8.4-10. One must also remember that a high-pass realization of order n

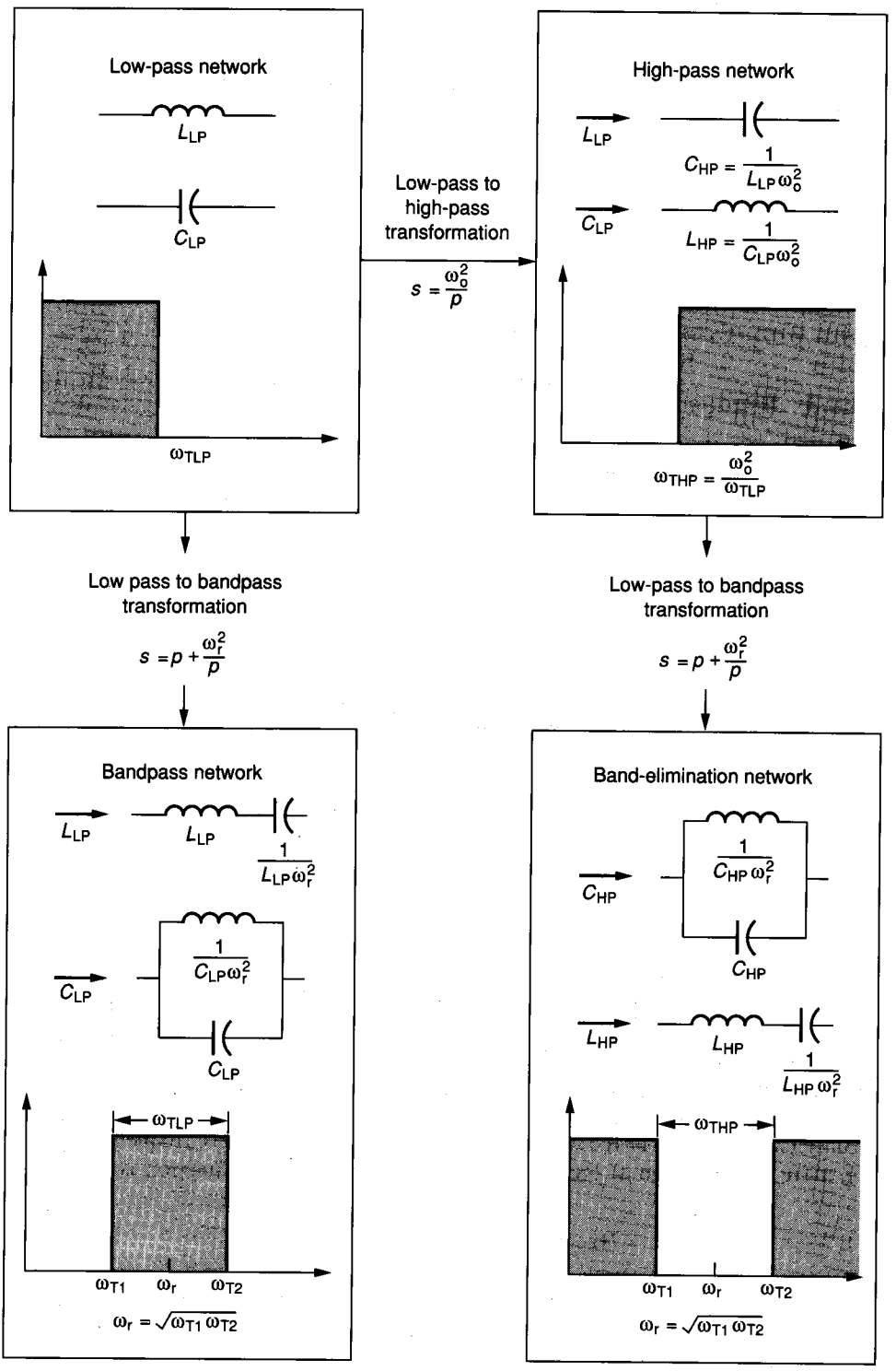

FIGURE 8.4-13
Changes of network elements under frequency transformations. (By permission of L. P. Huelsman and P. E. Allen, *Introduction to the Theory and Design of Active Filters,* McGraw-Hill Book Co., New York, 1980.)

has n zeros at the origin. Alternatively, one can use Eq. 8.4-10 to replace s in expressions such as Eq. 8.4-7 to get

$$H_{HPi}(p) = \frac{\pm H_{oi}p^2}{p^2 + (\omega_{pi}/Q_i)p + \omega_{pi}^2} \tag{8.4-11}$$

which is a high-pass quadratic form of Eq. 8.4-7. Second-order RC active realizations of Eq. 8.4-11 similar to those shown in Fig. 8.4-11 can be found in the literature on RC active filters. Figure 8.4-14 gives three realizations using the same types of structures as were used in Fig. 8.4-11.

8.4.3 Bandpass Filters

A low-pass to bandpass transformation can be defined as

$$s = p + \frac{\omega_r^2}{p} \tag{8.4-12}$$

where s is the low-frequency complex variable, p is the bandpass complex variable, and ω_r is defined in Fig. 8.4-13 as the geometric center frequency of the bandpass filter, given as

$$\omega_r = \sqrt{\omega_{T1}\omega_{T2}} \tag{8.4-13}$$

where ω_{T1} and ω_{T2} are defined in Fig. 8.4-13. The bandwidth is defined as $\omega_{T2} - \omega_{T1}$ and is equal to the original passband of the low-pass filter, ω_{TIP} (or ω_{PB}). The transformation of Eq. 8.4-12 is used in the same manner as the transformation of Eq. 8.4-10 to get either the new bandpass roots or the bandpass transfer function. The transformation of Eq. 8.4-12 doubles the order of the low-pass filter. For example, if a low-pass filter is given as

$$H_{LPi}(s) = \frac{H_{oi}(\omega_1/Q)}{s + (\omega_1/Q)} \tag{8.4-14}$$

then application of the low-pass to bandpass transformation of Eq. 8.4-12 gives

$$H_{BPi}(p) = \frac{\pm H_{oi}(\omega_1/Q)p}{p^2 + (\omega_1/Q)p + \omega_r^2} \tag{8.4-15}$$

It is seen that the second-order bandpass structure has two poles which are often complex and a zero at the origin and at infinity in the complex frequency plane. A more general form of the second-order bandpass transfer function is

$$H_{BPi}(s) = \frac{\pm H_{oi}(\omega_{pi}/Q_i)s}{s^2 + (\omega_{pi}/Q_i)s + \omega_{pi}^2} \tag{8.4-16}$$

where we have reverted to the notation of s for the complex frequency variable. Figure 8.4-15 shows three realizations of Eq. 8.4-16 using the same basic structures illustrated in Figs. 8.4-11 and 8.4-14.

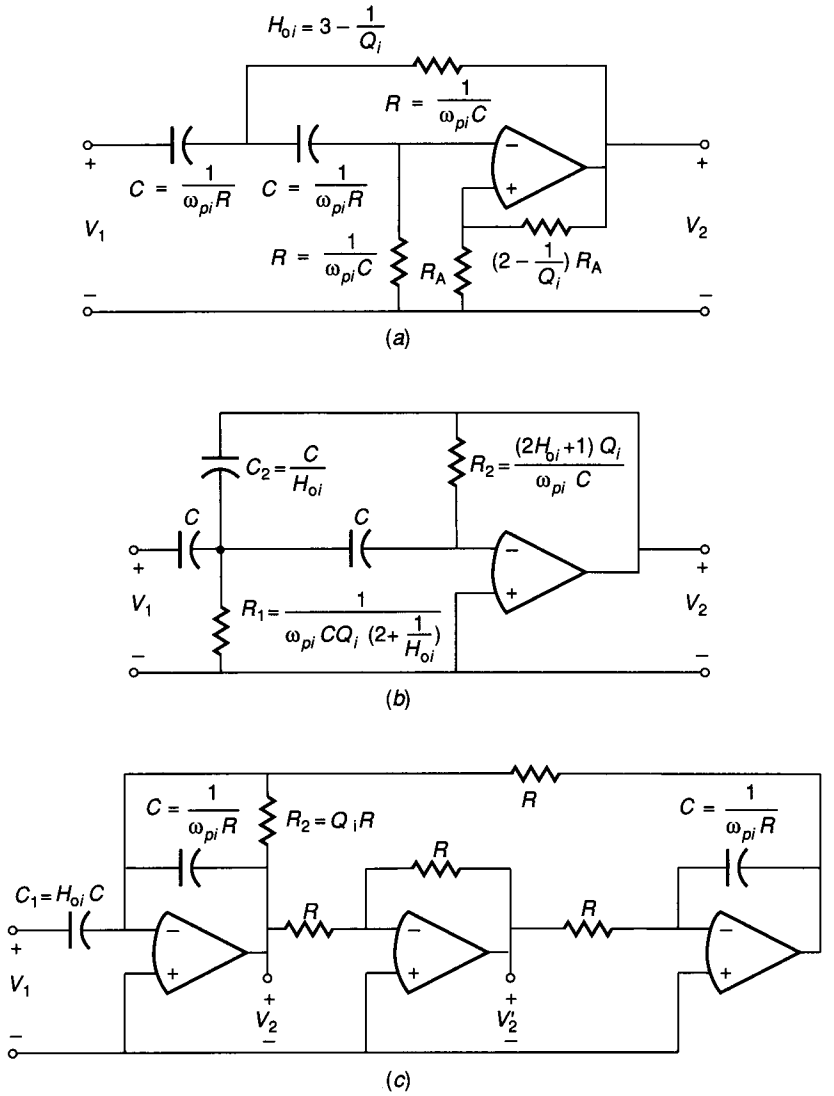

FIGURE 8.4-14
Three realizations of Eq. 8.4-11 (second-order, high-pass): (*a*) Finite-gain or Sallen and Key structure, (*b*) Infinite-gain structure, (*c*) Tow-Thomas or resonator structure.

A second major approach to active filter design, once the order of the filter is known, is to go directly to a passive realization. Passive RLC realizations for normalized low-pass filter approximations have also been tabulated and can be found in the literature.[26,27,28,34,39] To illustrate this approach, we repeat Example 8.4-3.

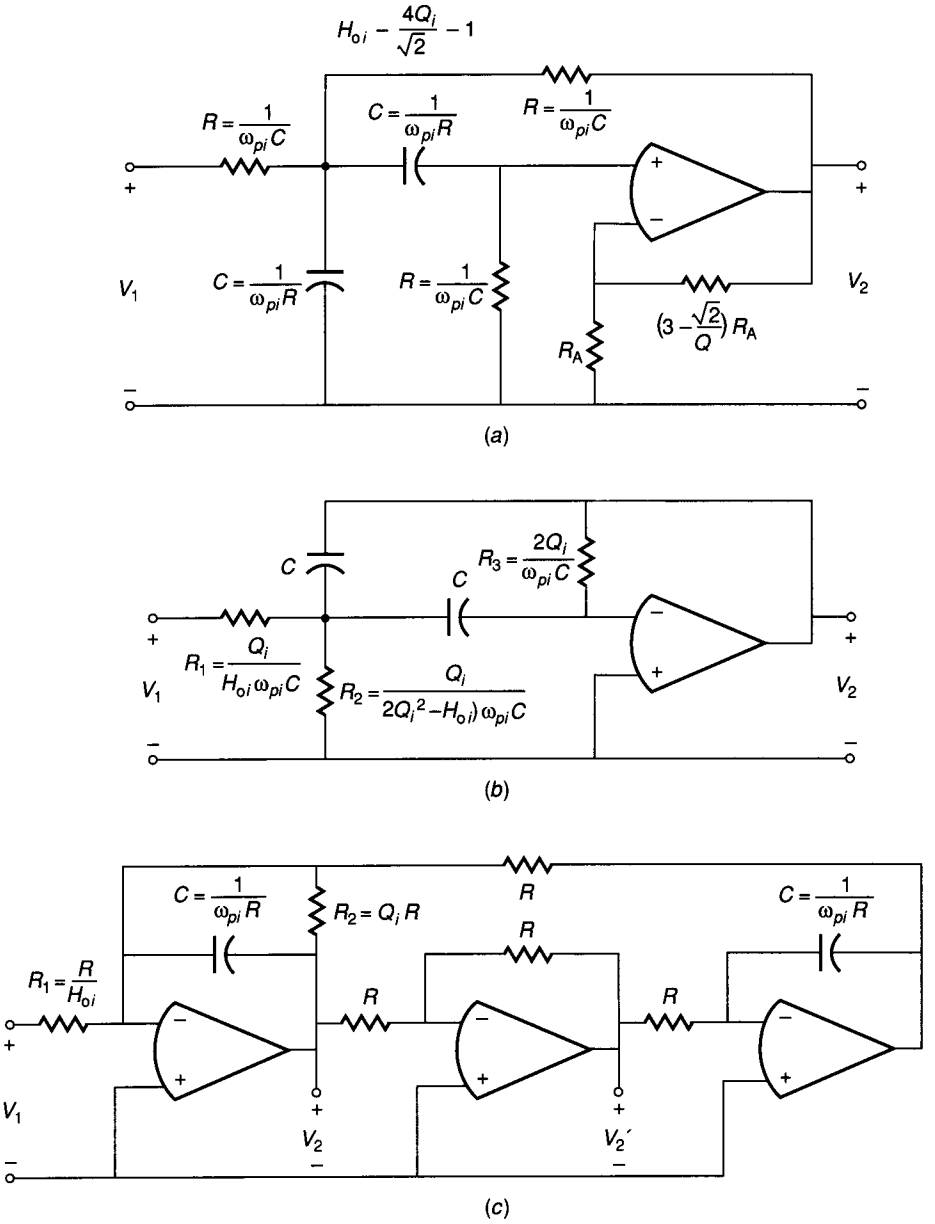

FIGURE 8.4-15
Three realizations of Eq. 8.4-16 (second-order, bandpass structure): (*a*) Finite-gain or Sallen and Key structure, (*b*) Infinite-gain, (*c*) Tow-Thomas or resonator structure.

Example 8.4-4. Realization of a passive RLC filter. Design a passive RLC filter that will satisfy the specifications of Example 8.4-3. This filter is to be driven from a voltage source having zero resistance and will be terminated in a 1000 Ω load.

Solution. From Example 8.4-3, we know that $n = 5$. From the tabulation found in the literature, we obtain the realization shown in Fig. 8.4-16. This realization has been normalized so that $\omega_{PB} = 1$ rps and $R_L = 1\ \Omega$. It is now necessary to denormalize using Eqs. 8.4-8 and 8.4-9. Because ω_{PB} of Fig. 8.4-16*a* is unity and we desire ω_{PB} of 2000π, then $\Omega_n = 2000\pi$. Because R_L of Fig. 8.4-16*a* is 1 Ω and we want $R_L = 1000\ \Omega$, then $z_n = 1000$. Applying the equations of Table 8.4-2 to the components of Fig. 8.4-16*a* results in the final realization shown in Fig. 8.4-16*b*, which has a transfer function equivalent to that of Fig. 8.4-12*c*.

The passive RLC low-pass realizations may be easily converted to high-pass, bandpass, or band-elimination using the transformations of Fig. 8.4-13. The passive RLC realizations are also used as the starting point in certain types of active filter design.

Figure 8.4-17 summarizes this section. The design of active RC filters starts with the filter specification, which is converted into a filter approximation. Sometimes, the classical approximations presented here are not adequate, and computer-generated approximations are used instead. The filter approximation will take the form of a rational polynomial transfer function. If the roots of the rational polynomial are factored into first- and second-order products, then the cascade realization approach illustrated here can be used. Methods also exist

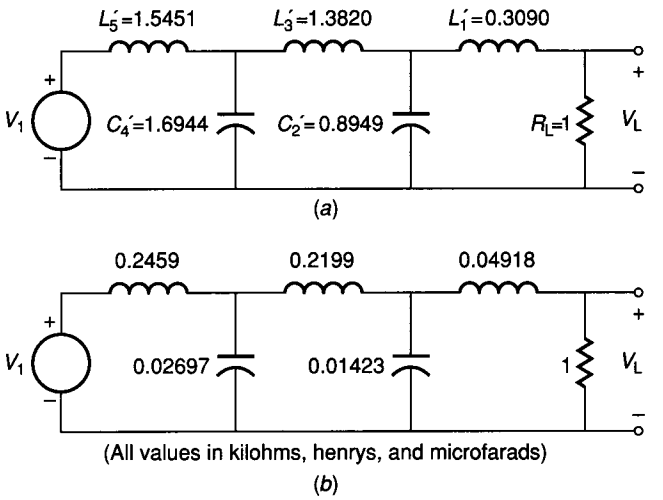

FIGURE 8.4-16
(*a*) Passive RLC normalized prototype for Example 8.4-4, (*b*) Denormalized realization of *a*.

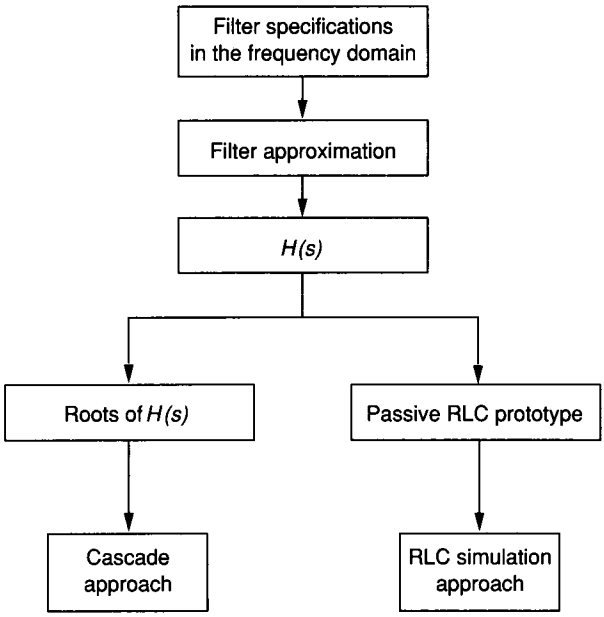

FIGURE 8.4-17
Summary of continuous-time filter design approaches.

for synthesizing a circuit directly from the rational polynomial without obtaining the roots, but they have not been discussed here. Tabulations of a passive RLC prototype circuit that implement the standard approximating functions are also widely available in the literature. The switched capacitor filters, which will be presented in the next section, start from the roots of the rational function, the rational function, or the passive RLC prototype.

8.5 SWITCHED CAPACITOR FILTERS

The use of switched capacitor methodology to design and implement analog filters using integrated circuit technology is illustrated in this section. It is necessary that the technology be capable of providing a good switch, a well-defined capacitor, and an op amp. Because all of these aspects are found in MOS technology, it has become the predominant technology for switched capacitor filters. Switched capacitor methods are not new and, in fact, were employed by James Clerk Maxwell in his discussion on the equivalent resistance of a periodically switched capacitor.[40] The key development that led to the rapid evolution of practical switched capacitor methods was the realization that switched capacitor concepts could be implemented in MOS technology.[41] This realization was followed by a rapid development and implementation of analog signal processing techniques in MOS technology. Today, many switched capacitor circuits, including filters, are found in various products, including telecommunications products.[42]

The material presented in this section is a brief description of how to design switched capacitor filters. Three basic methods will be described. The first is resistor substitution and replaces the resistors in an RC active circuit with a switched capacitor realization. The second uses switched capacitor integrators to simulate the passive RLC prototype circuit for a desired filter realization. The last uses a direct building block approach in the z-domain. The filter requirements are transformed from the continuous-time frequency domain to the discrete-time frequency domain (z-domain). These approaches are representative of the methods used in switched capacitor filter design. More information can be found in the references.

8.5.1 Resistor Realization

One of the simplest approaches in switched capacitor design is to replace the resistors of a continuous-time, active RC filter realization with a switched capacitor realization of each resistor. Resistor realizations contain capacitors and switches and simulate the continuous-time resistor very well as long as the rate at which the switches are opened and closed is much higher than the frequencies of interest in the analog signal. Figure 8.5-1*a* shows the configuration of a *parallel* switched capacitor realization of a resistor, R, connected between two voltage sources, V_1 and V_2, illustrated in Fig. 8.5-1*b*. The switches, ϕ_1 and ϕ_2, are controlled by the nonoverlapping clocks of period T_c, as shown in Fig. 8.5-1*c*.

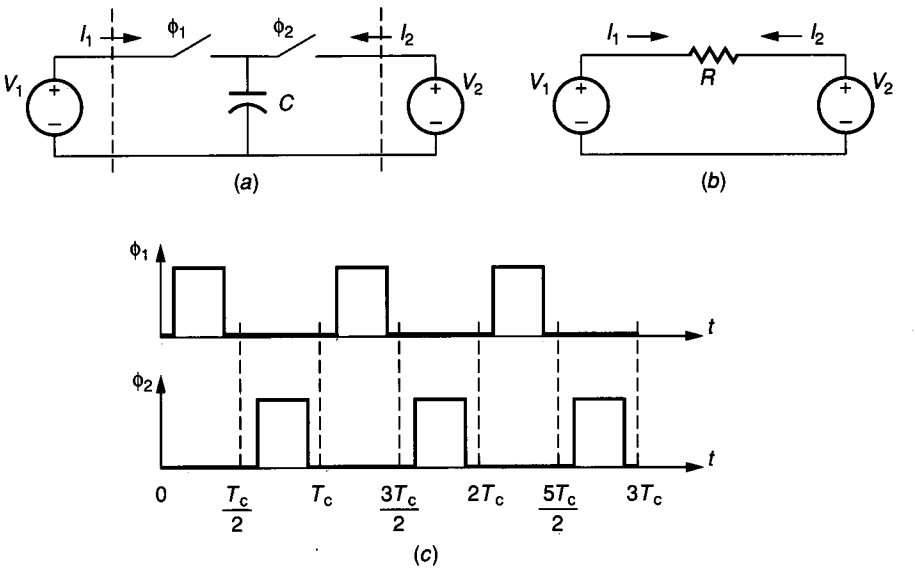

FIGURE 8.5-1
(*a*) Parallel switched capacitor realization of a resistor, (*b*) A continuous resistor, (*c*) Clock waveforms for the switched capacitor realization.

When the clock waveform in Fig. 8.5-1*c* is high, the switch designated by that waveform is closed.

To demonstrate the equivalence between the switched capacitor circuit in Fig. 8.5-1*a* and the resistor in Fig. 8.5-1*b*, assume that $V_1(t)$ and $V_2(t)$ are unchanged for several clock cycles. We shall designate these constant voltages as V_1 and V_2, respectively. During the time between 0 and $T_c/2$, switch ϕ_1 closes. If the switch resistance is small or the clock period large enough, the capacitor C will be charged to V_1. At $t = T_c/2$, we can define the total charge flow between 0 and $T_c/2$ past the left-hand vertical dashed line as $Q_1(T_c/2)$, which is given as

$$Q_1(T_c/2) = CV_1 \tag{8.5-1}$$

where C is initially uncharged. Next, consider the time interval between $T_c/2$ and T_c. Switch ϕ_2 closes and connects the charged capacitor to V_2. At time T_c, we can define the charge flow past the right-hand vertical dashed line as $Q_2(T_c)$ for $0 < t < T_c$, which is given as

$$Q_2(T_c) = C(V_2 - V_1) \tag{8.5-2}$$

Note that the flow of charge past the left-hand vertical dashed line during this period is

$$Q_1(T_c) = 0 \tag{8.5-3}$$

During the interval from T_c to $3T_c/2$, switch ϕ_1 closes again, resulting in the following charge flow during this interval.

$$Q_1\left(\frac{3T_c}{2}\right) = C(V_1 - V_2) \tag{8.5-4}$$

and

$$Q_2\left(\frac{3T_c}{2}\right) = 0 \tag{8.5-5}$$

As long as $V_1(t)$ and $V_2(t)$ remain constant, these equations hold for the charge flow into the capacitor C during the various switch closures.

The charge flows, Q_1 and Q_2, can be expressed in terms of the current that flows during the switch closure. This expression for Q_1 during the period from $T_c/2$ to $3T_c/2$ can be written as

$$Q_1 = Q_1(T_c) + Q_1\left(\frac{3T_c}{2}\right) = 0 + C(V_1 - V_2) = \int_{T_c/2}^{3T_c/2} I_1(t)\,dt \tag{8.5-6}$$

If we divide Eq. 8.5-6 by T_c, then the integral over the period T_c (in this case, from $T_c/2$ to $3T_c/2$) is equal to the average value of $I_1(t)$, designated as $I_1(\text{aver})$. Thus, from Eq. 8.5-6 we may write the following expression.

$$I_1(\text{aver}) = \frac{C}{T_c}(V_1 - V_2) \tag{8.5-7}$$

The average current flowing through the resistor R in the same time interval of length T_c is proportional to $V_1 - V_2$ and is expressed as

$$I_{1R}(\text{aver}) = \frac{V_1 - V_2}{R} \tag{8.5-8}$$

If V_1 and V_2 remain constant, then we can equate $I_1(\text{aver})$ and $I_{1R}(\text{aver})$ to obtain the equivalent resistance of the switched capacitor circuit. From Eq. 8.5-7 and Eq. 8.5-8 this is

$$R \cong \frac{T_c}{C} = \frac{1}{f_c C} \tag{8.5-9}$$

Equation 8.5-9 is a key result! It states that as long as V_1 and V_2 are approximately constant, the switched capacitor circuit of Fig. 8.5-1*a* realizes the resistor of Fig. 8.5-1*b*.

In reality, $V_1(t)$ and $V_2(t)$ are not constants but time-varying voltages. However, if the clock period is small enough, the values of $V_1(t + T_c)$ and $V_2(t + T_c)$ are not much different from $V_1(t)$ and $V_2(t)$. This can be stated in a different manner, assuming that the $V_1(t)$ and $V_2(t)$ waveforms are sinusoidal with a frequency of f_s. If f_s is much less than f_c, then T_s is much greater than T_c and Eq. 8.5-9 is valid. This condition is called the *high sampling approximation.*

Three other configurations of switched capacitor realizations of resistance along with the parallel switched capacitor configuration are shown in Fig. 8.5-2. The parallel switched capacitor resistance realization we have just discussed is shown in the first row. A second configuration, called the *series* switched capacitor realization, consists of two switches and one capacitor. If one repeats the preceding charge flow analysis, it can be shown that the equivalent resistance of the series switched capacitor realization is also given by Eq. 8.5-9. A third configuration, called the *series-parallel* switched capacitor realization, is shown in the third row of Fig. 8.5-2. The value of the resistor realization is shown in the last column and can be found in exactly the same manner as was done for the previous two configurations. Finally, the *bilinear* switched capacitor realization is shown. It uses four switches and one capacitor. If the high sampling frequency approximation is valid, all resistors of continuous-time RC active networks can be replaced on a one-for-one basis to obtain a switched capacitor realization.

The advantage of the switched capacitor methodology can be illustrated by comparing the RC product of a resistance designated as R_1 and a capacitance designated as C_2. Let us assume that the product of R_1 and C_2 forms the time constant τ, given as

$$\tau = R_1 C_2 \tag{8.5-10}$$

The dependence of the accuracy of τ on R_1 and C_2 can be written as

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \tag{8.5-11}$$

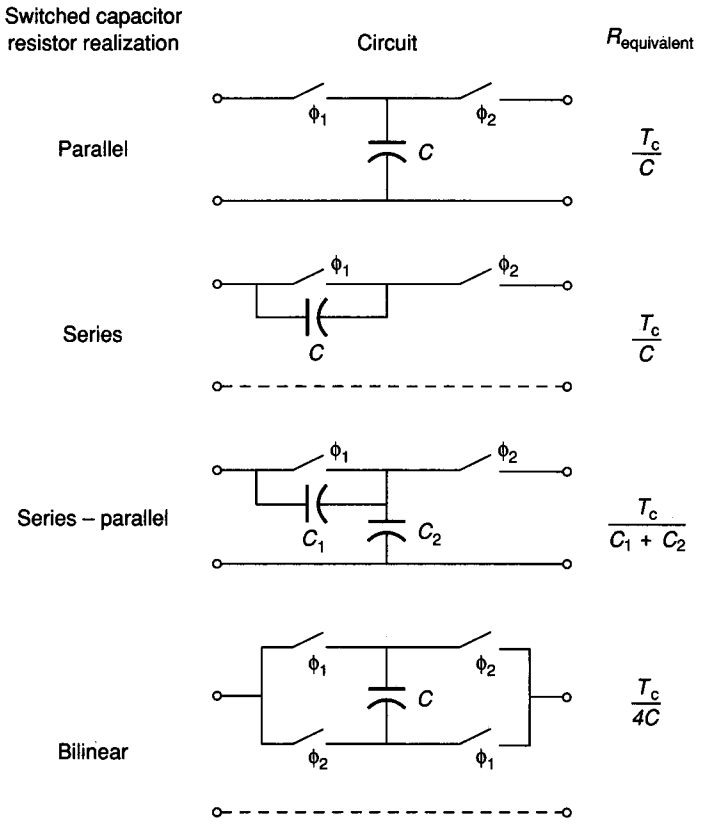

FIGURE 8.5-2
Summary of switched capacitor resistor simulations where $f << f_e$.

where dx/x is interpreted as the accuracy of x. The worst-case accuracy of τ will be the sum of the absolute accuracies of R_1 and C_2, which will be very poor if R_1 and C_2 are directly implemented by integrated circuit technology.

If R_1 is replaced by a switched capacitor resistance realization with a capacitor of value C_1 having an equivalent resistance given by Eq. 8.5-9, the time constant τ now becomes

$$\tau = \frac{1}{f_c}\frac{C_2}{C_1} = T_c\frac{C_2}{C_1} \tag{8.5-12}$$

The accuracy of the time constant, τ, in Eq. 8.5-12 can be expressed as

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \tag{8.5-13}$$

If the clock frequency is assumed to be constant, then Eq. 8.5-13 reduces to

$$\frac{d\tau}{\tau} \cong \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \tag{8.5-14}$$

We know from our previous studies that the relative accuracy of two capacitors fabricated on the same integrated circuit can be quite good. As a result, the value of Eq. 8.5-14 can be as low as 0.1%, which represents a tremendous improvement over Eq. 8.5-11 and is one of the key factors contributing to the success of integrated switch capacitor filters.

Unfortunately, the concept of a one-for-one replacement of resistors by switched capacitor resistor realizations breaks down if the high sampling frequency assumption is not valid. Although this does impact how switched capacitor circuits must be designed, it does not affect the accuracy or the small area achievable with switched capacitor circuits. The degree to which f_c must be larger than f_s for Eq. 8.5-9 to be valid depends on both the realization chosen and the circuit in which it is used. For a demonstration of some of these ideas, consider the first-order continuous-time RC circuit of Fig. 8.5-3. The continuous-time frequency-domain voltage transfer function can be written as

$$H(s) = \frac{1}{s\tau_1 + 1} = \frac{1}{s/\omega_1 + 1} \tag{8.5-15}$$

where $\tau_1 = 1/\omega_1 = R_1C_2$. The frequency response can be found by replacing s by $j\omega$ to get

$$H(j\omega) = \frac{1}{j(\omega/\omega_1) + 1} \tag{8.5-16}$$

The magnitude of Eq. 8.5-16 is

$$|H(j\omega)| = \frac{1}{[1 + (\omega R_1C_2)^2]^{1/2}} \tag{8.5-17}$$

and the argument, or phase shift, is

$$\text{Arg } H(j\omega) = -\tan^{-1}(\omega R_1C_2) \tag{8.5-18}$$

The frequency response of the circuit of Fig. 8.5-3 is shown in Fig. 8.5-4*a* and *b*. It is seen that this circuit is a first-order low-pass filter. The root of this filter is given in Fig. 8.5-4*c*.

A realization of the filter of Fig. 8.5-3 can be obtained by replacing the resistor, R_1, with any of the switched capacitor resistor realizations of Fig. 8.5-2. Figure 8.5-5*a* shows a switched capacitor realization using the parallel switched capacitor resistor realization. To analyze this circuit, the clock sequence must be specified. Figure 8.5-5*b* shows a shorthand method of illustrating the clock sequence for this circuit. ϕ_1 and ϕ_2 specify the phase periods during which the switches ϕ_1 and ϕ_2 close and will be denoted as the *odd* and *even* phase clocks, respectively. The odd phase periods (ϕ_1) will be designated by a superscript o, and the even phase periods (ϕ_2) will be designated by a superscript e.

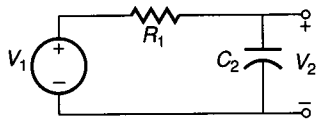

FIGURE 8.5-3
Continuous-time RC network.

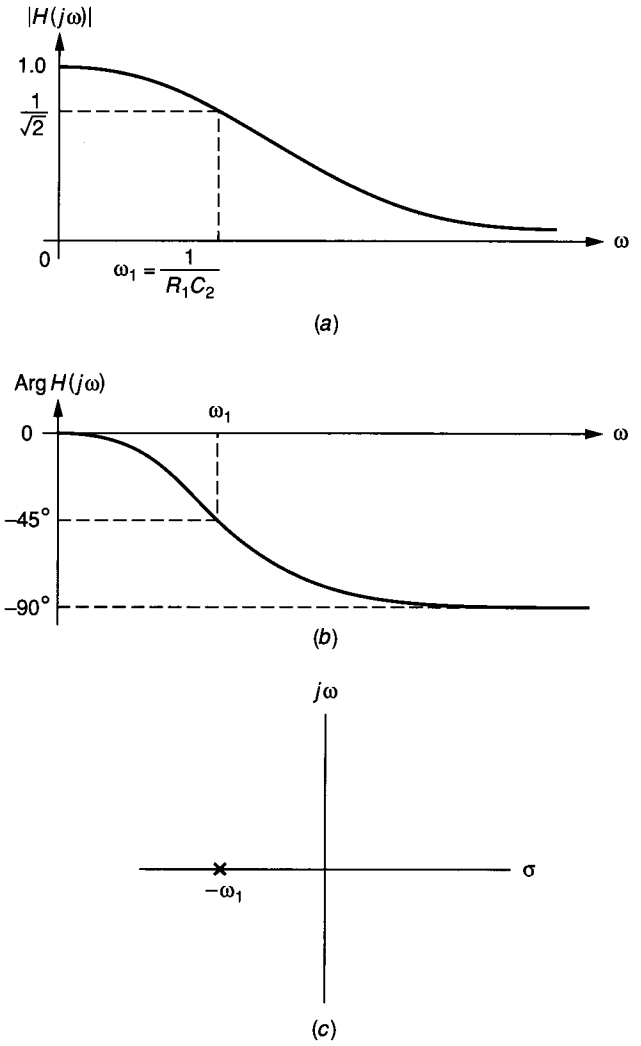

FIGURE 8.5-4
Frequency response of Fig. 8.5-3: (*a*) Magnitude, (*b*) Phase response, (*c*) Root locations of Fig. 8.5-3.

In the analysis of the circuit of Fig. 8.5-5*a* we assume that $V_1(t)$ is constant during the phase periods (which can be achieved by a sample-and-hold circuit). T will be used to denote T_c when there is no possible confusion. Consider the first odd phase period, where $(n-1) \leq (t/T) < (n-\frac{1}{2})$, when switch ϕ_1 is closed. In this analysis, we assume that switch ϕ_1 closes immediately after $t = (n-1)T$ and that C_1 is charged instantaneously to $V_1^{\circ}[(n-1)T]$. In practice, the time required for V_1 to charge C_1 to this value should be small compared with

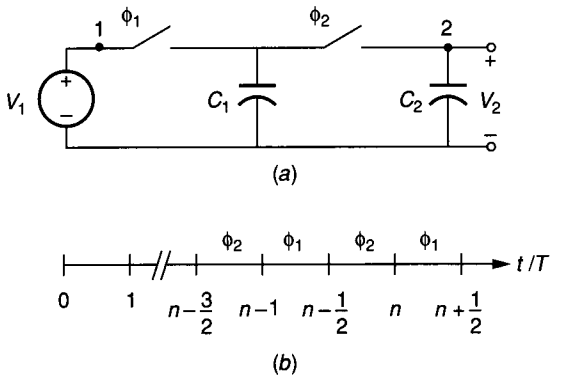

FIGURE 8.5-5
(*a*) Switched capacitor realization of Fig. 8.5-3, (*b*) Clock phasing.

$T/2$. During the odd phase period, we may redraw the circuit of Fig. 8.5-5*a* as shown in Fig. 8.5-6*a*. From this figure, we see that

$$V_{C1}(t) = V_1^o[(n-1)T] = V_1^o(n-1) \tag{8.5-19}$$

and

$$V_{C2}(t) = V_2^o[(n-1)T] = V_2^o(n-1) \tag{8.5-20}$$

The clock period T in Eqs. 8.5-19 and 8.5-20 has been dropped because it adds no useful information, thus simplifying the notation. This convention will be followed where no misinterpretation is likely.

In the next even phase period, $(n-\frac{1}{2}) \leq (t/T) < n$, switch ϕ_1 is open and switch ϕ_2 closes. Figure 8.5-6*b* represents Fig. 8.5-5*a* during this phase period. During this time, C_1 and C_2 are paralleled, resulting in a new value of V_2. The circuit of Fig. 8.5-6*b* may be converted to the equivalent circuit of Fig. 8.5-6*c* with uncharged capacitors. The voltage sources representing the initial voltages on the capacitors are assumed to be multiplied by a unit step function that starts at $t = (n-\frac{1}{2})T$ but whose value was established at $t = (n-1)T$. After closing switch ϕ_2, the charges on C_1 and C_2 must be redistributed to reestablish equilibrium. Using superposition techniques, V_2 can be expressed as

$$V_2(t) = \frac{C_1}{C_1+C_2}V_1^o(n-1) + \frac{C_2}{C_1+C_2}V_2^o(n-1) \tag{8.5-21}$$

Evaluating $V_2(t)$ at $t = (n-\frac{1}{2})T$, we obtain

$$V_2^e(n-\frac{1}{2}) = \frac{C_1}{C_1+C_2}V_1^o(n-1) + \frac{C_2}{C_1+C_2}V_2^o(n-1) \tag{8.5-22}$$

At the beginning of the next phase period $n \leq t/T < (n+\frac{1}{2})$, the voltage at V_2 can be written as

$$V_2^o(n) = V_2^e(n-\frac{1}{2}) \tag{8.5-23}$$

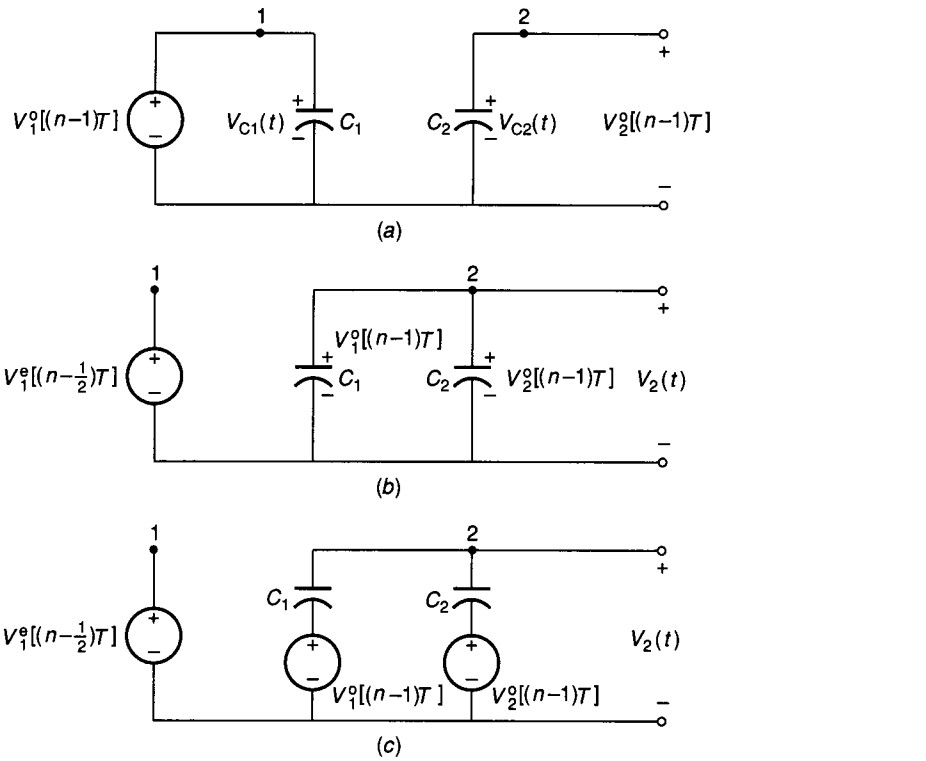

FIGURE 8.5-6
(*a*) Equivalent circuit of Fig. 8.5-5*a* when switch ϕ_1 is closed, (*b*) Equivalent circuit of Fig. 8.5-5*a* when switch ϕ_2 is closed, (*c*) Alternate form of *b*.

because the voltage V_2 has not changed from its value at $t = (n - \frac{1}{2})T$. Using Eq. 8.5-23 allows us to write

$$V_2^o(n) = \frac{C_1}{C_1 + C_2} V_1^o(n-1) + \frac{C_2}{C_1 + C_2} V_2^o(n-1) \tag{8.5-24}$$

Equation 8.5-24 recursively defines a sequence that can be transformed from the discrete-time domain to the z-domain by taking the z-transform characterized by

$$V(n) \rightarrow z^{-n} V(z) \tag{8.5-25}$$

Using this transformation on Eq. 8.5-24 results in

$$V_2^o(z) = \frac{C_1 z^{-1}}{C_1 + C_2} V_1^o(z) + \frac{C_2 z^{-1}}{C_1 + C_2} V_2^o(z) \tag{8.5-26}$$

Solving for $V_2^o(z)/V_1^o(z)$ results in the z-domain transfer function of the circuit of Fig. 8.5-5*a* sampled at the odd output phase.

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = \left(\frac{1}{1 + \alpha}\right) \frac{z^{-1}}{1 - [\alpha/(1 + \alpha)]z^{-1}} \tag{8.5-27}$$

where $\alpha = C_2/C_1$. Applying Eq. 8.5-25 to Eq. 8.5-23 results in $V_2^o(z) = z^{-1/2}V_2^e(z)$. Thus, Eq. 8.5-27 can be written as

$$H^{oe}(z) = \frac{V_2^e(z)}{V_1^o(z)} = \left(\frac{1}{1+\alpha}\right)\frac{z^{-1/2}}{1-[\alpha/(1+\alpha)]z^{-1}} \tag{8.5-28}$$

Thus,

$$H^{oo}(z) = z^{-1/2}H^{oe}(z) \tag{8.5-29}$$

The basic concepts of the z-transform have been used in an algorithmic manner in order to keep the presentation simple. The z-transform is rigorously developed elsewhere.[43]

The discrete-time frequency response can be found by replacing z by $e^{j\omega T}$, which is analogous to replacing s by $j\omega$ in the continuous-time frequency domain. Making this replacement in Eq. 8.5-27 gives the following expression, which is equivalent to the discrete-time frequency response of the circuit of Fig. 8.5-5*a*.

$$H^{oo}(e^{j\omega T}) = \frac{V_2^o(e^{j\omega T})}{V_1^o(e^{j\omega T})} = \frac{1}{(1+\alpha)\cos\omega T - \alpha + j(1+\alpha)\sin\omega T} \tag{8.5-30}$$

where Euler's formula ($e^{j\omega T} = \cos\omega T + j\sin\omega T$) has been used to remove $e^{j\omega T}$. The magnitude of Eq. 8.5-30 is

$$|H^{oo}(e^{j\omega T})| = \frac{1}{[1+2\alpha(1+\alpha)(1-\cos\omega T)]^{1/2}} \tag{8.5-31}$$

and the phase shift is

$$\text{Arg}\,[H^{oo}(e^{j\omega T})] = -\tan^{-1}\left[\frac{\sin\omega T}{\cos\omega T - \alpha/(1+\alpha)}\right] \tag{8.5-32}$$

In order to compare the performance of the circuit of Fig. 8.5-5 with the circuit of Fig. 8.5-3, we must appropriately choose the values of α and T_c. One of several methods used for making this comparison is to assume that ω_1 of Eq. 8.5-15 is much less than $\omega_c = 1/(2\pi T_c)$. In this case, z of Eq. 8.5-27 can be replaced by

$$z = e^{j\omega T} \simeq 1 + j\omega T \tag{8.5-33}$$

to get

$$H^{oo}(e^{j\omega T}) \simeq \frac{1}{j\omega(1+\alpha)T + 1} \tag{8.5-34}$$

Comparing Eq. 8.5-16 with Eq. 8.5-34 gives

$$\frac{1}{\omega_1} = T(1+\alpha) \tag{8.5-35}$$

The frequency response of Eq. 8.5-30 is plotted in Fig. 8.5-7 for the value of $\omega_c/\omega_1 = 10$, which from Eq. 8.5-35 corresponds to $\alpha = 0.5915$. Also plotted is the frequency response of Eq. 8.5-16 from the circuit of Fig. 8.5-3. For frequencies of ω less than $0.02\omega_c$, the switched capacitor circuit of Fig. 8.5-5*a* is a good approximation of the frequency response of the circuit of Fig. 8.5-3. However, as the frequency increases, the switched capacitor circuit is a very poor approximation. At $\omega/\omega_c = 0.5$, the greatest attenuation of the switched capacitor circuit occurs; and at $\omega = \omega_c$, the magnitude is at the starting value, with a phase shift of $-360°$. The roots of the circuit of as determined from Eq. 8.5-27 are shown in Fig. 8.5-8 and consist of a pole located at $\alpha/(1 + \alpha)$ on the positive real axis. To improve the switched capacitor realization of the circuit of Fig. 8.5-3, it is necessary to increase ω_c or, alternatively, reduce ω_1.

At this point, one can begin to use the resistor realization method to replace the resistances of an RC active network. This method has been applied to the filters of Figs. 8.4-11, 8.4-14, and 8.4-15. The disadvantages of this method are that the circuits are very difficult to analyze and they contain floating nodes. *Floating*

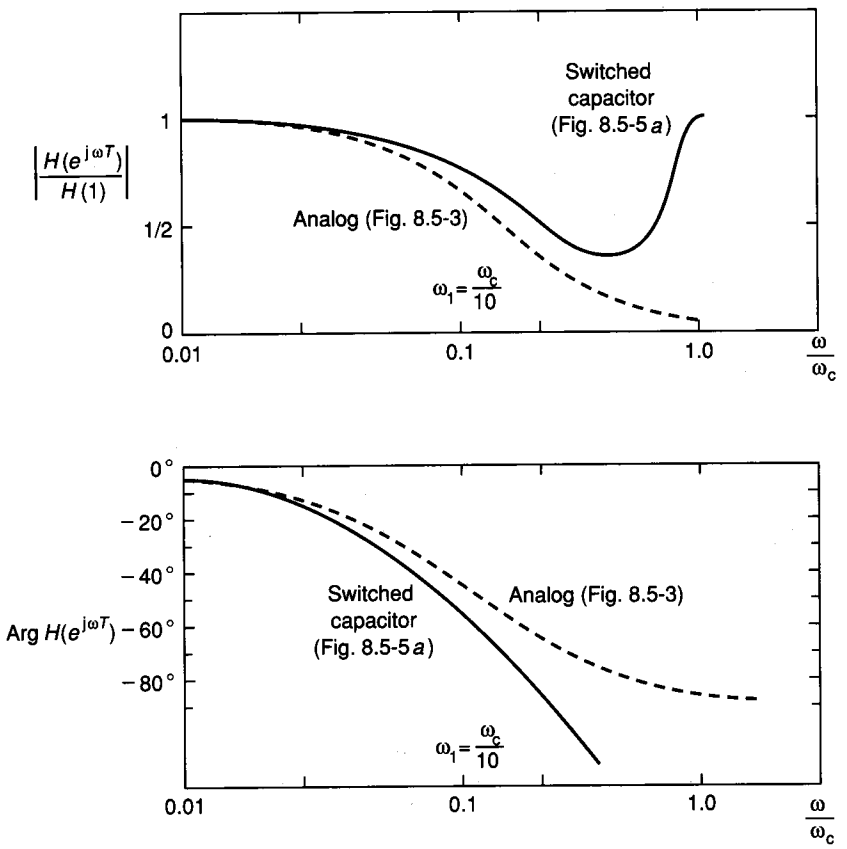

FIGURE 8.5-7
Frequency response of Fig. 8.5-5*a* compared with the frequency response of Fig. 8.5-3.

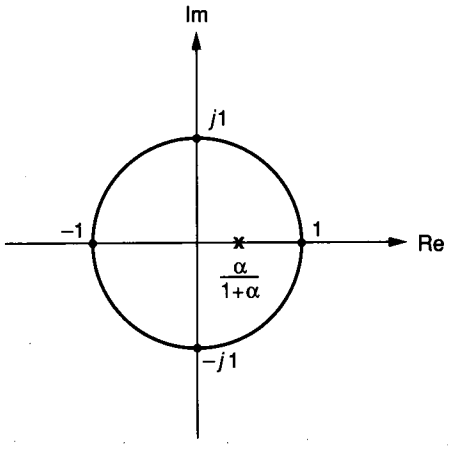

FIGURE 8.5-8
Roots of Fig. 8.5-5*a*.

nodes are nodes that are not connected to a voltage source or a virtual ground. Floating nodes cause a susceptibility to parasitic capacitance as well as complicate the analysis. Examples of floating nodes are nodes A and B in Fig. 8.4-11*a* and node A in Fig. 8.4-11*b*. Figure 8.4-11*c* has no floating nodes and thus is suitable for the resistor simulation approach. Because of these reasons, the resistor simulation method is restricted to simple configurations. The following two methods provide better and easier methods of realizing switched capacitor filters.

8.5.2 Passive RLC Prototype Switched Capacitor Filters

One of the more useful methods of synthesizing filters using switched capacitor networks is based on the realization of RLC ladder networks. Since the integrator is an important part of this method, we shall consider the implementation of switched capacitor integrators first. An inverting analog integrator is shown in Fig. 8.5-9. The transfer function can be found as

$$H(s) = \frac{V_2(s)}{V_1(s)} = \frac{-1}{sR_1C_2} = \frac{-1}{s\tau_0} = \frac{-\omega_0}{s} \tag{8.5-36}$$

where τ_0 is the time constant of the integrator. The transfer function magnitude of the inverting integrator is given as

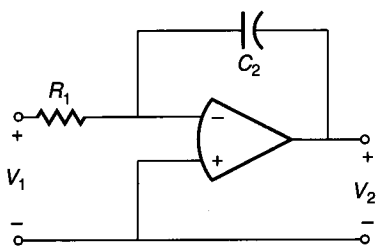

FIGURE 8.5-9
An inverting continuous-time integrator.

$$|H(j\omega)| = \frac{\omega_0}{\omega} \tag{8.5-37}$$

and the phase shift is

$$\text{Arg } H(j\omega) = \frac{\pi}{2} \tag{8.5-38}$$

A noninverting integrator has the same magnitude as the inverting integrator. The phase shift of the noninverting integrator is equal to $-\pi/2$.

A logical approach to a switched capacitor integrator realization is to replace the resistor R_1 of Fig. 8.5-9 by the parallel switched capacitor realization of Fig. 8.5-1*a*. The result is shown in Fig. 8.5-10*a* and is called the parallel switched capacitor integrator. Figure 8.5-10*b* shows the clock sequence for the switched capacitor integrator. During the odd phase periods, the charge on C_2 is constant. An equivalent circuit to Fig. 8.5-10*a* is shown in Fig. 8.5-10*c* for the even phase period. The charge left on C_2 at $t = (n - \frac{1}{2})T$, Q_L, is

$$Q_L^e(n - \frac{1}{2}) = C_2 V_2^e(n - \frac{1}{2}) \tag{8.5-39}$$

The charge on C_2 during the odd period, Q_M, is

$$Q_M^o(n - 1) = C_2 V_2^o(n - 1) \tag{8.5-40}$$

The charge that will be contributed to C_2 from C_1 during the even phase period, Q_C, is

$$Q_C^o(n - 1) = -C_1 V_1^o(n - 1) \tag{8.5-41}$$

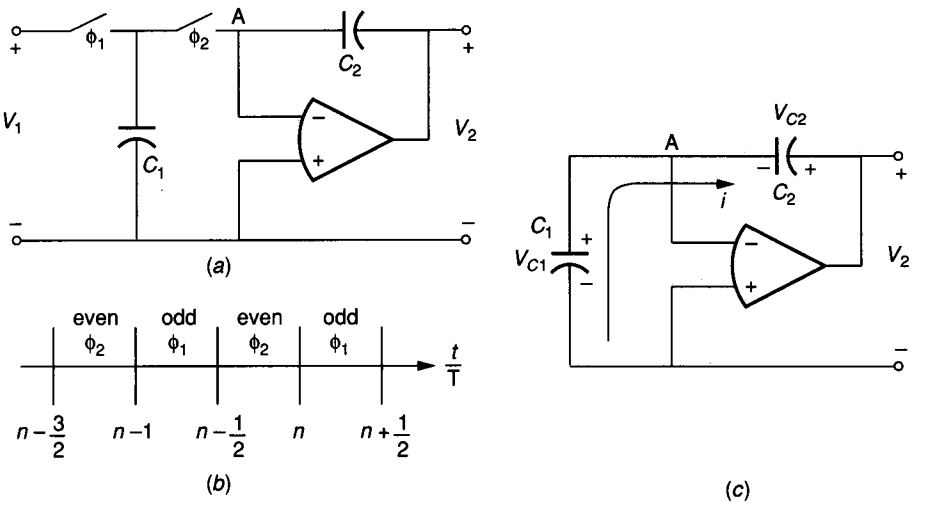

FIGURE 8.5-10
(*a*) Parallel switched capacitor inverting integrator, (*b*) Clock sequence, (*c*) Equivalent circuit during the ϕ_2 phase period.

Charge conservation techniques applied to node A of Fig. 8.5-10*c* result in

$$Q_L^e(n - \frac{1}{2}) = Q_M^o(n - 1) + Q_C^o(n - 1) \tag{8.5-42}$$

Making the substitutions of Eqs. 8.5-39 through 8.5-41 into Eq. 8.5-42 results in

$$C_2 V_2^e(n - \frac{1}{2}) = C_2 V_2^o(n - 1) - C_1 V_1^o(n - 1) \tag{8.5-43}$$

During the odd phase, the charge on C_2 does not change, so that

$$V_2^o(n) = V_2^e(n - \frac{1}{2}) \tag{8.5-44}$$

Combining Eqs. 8.5-43 and 8.5-44 results in

$$C_2 V_2^o(n) = C_2 V_2^o(n - 1) - C_1 V_1^o(n - 1) \tag{8.5-45}$$

Applying the transformation of Eq. 8.5-25 to Eq. 8.5-45 results in the desired z-domain transfer function

$$C_2 V_2(z) = C_2 z^{-1} V_2^o(z) - C_1 z^{-1} V_1^o(z) \tag{8.5-46}$$

This can be expressed as

$$H^{oo}(z) = \frac{V_2^0(z)}{V_1^0(z)} = -\frac{C_1}{C_2}\left(\frac{z^{-1}}{1 - z^{-1}}\right) \tag{8.5-47}$$

$H^{oe}(z)$ can be found by multiplying Eq. 8.5-47 by $z^{-1/2}$. $H^{oo}(z)$ of Eq. 8.5-47 and the corresponding $H^{oe}(z)$ are sometimes called the type *I* direct-transform discrete integrator and the type *I* lossless integrator, respectively.[43–45]

The frequency response of the circuit of Fig. 8.5-10*a* can be found by replacing z by $e^{j\omega T}$ in Eq. 8.5-47 to get

$$H^{oo}(e^{j\omega T}) = -\frac{C_1}{C_2}\left(\frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\right) \tag{8.5-48}$$

If we define $\omega_o = C_1/(TC_2)$, then Eq. 8.5-48 can be expressed as

$$H^{oo}(e^{j\omega T}) = -\frac{\omega_o}{j\omega}\left[\frac{\omega T/2}{\sin(\omega T/2)}\right]\exp(-j\omega T/2) \tag{8.5-49}$$

Thus, the magnitude and phase response of Eq. 8.5-49 can be expressed as

$$|H^{oo}(e^{j\omega T})| = \frac{\omega_o}{\omega}\left[\frac{\omega T/2}{\sin(\omega T/2)}\right] \tag{8.5-50}$$

and

$$\text{Arg } H^{oo}(e^{j\omega T}) = \frac{\pi}{2} - \left[\frac{\omega T}{2}\right] \tag{8.5-51}$$

We observe from Eqs. 8.5-50 and 8.5-51 that as ωT approaches zero, these equations approach Eqs. 8.5-37 and 8.5-38, respectively. Consequently, the terms

TABLE 8.5-1
Magnitude and phase (delay) errors in switched capacitor integrators versus normalized frequency

Normalized frequency f/f_c	Error in gain constant magnitude	Error in phase from ideal 90°
0.00	0.00%	0°
0.05	0.41%	9°
0.10	1.66%	18°
0.15	3.80%	27°
0.20	6.90%	36°
0.25	11.07%	45°
0.30	16.50%	54°
0.35	23.41%	63°
0.40	32.13%	72°
0.45	43.13%	81°
0.50	57.08%	90°

in the bracketed portions of Eqs. 8.5-50 and 8.5-51 can be considered magnitude and phase error terms. The effects of these error terms are shown in Table 8.5-1.

A noninverting switched capacitor integrator is shown in Fig. 8.5-11. It can be observed that C_1 is charged by V_1 in one direction and then reversed before it is discharged into C_2. The result is exactly the same transfer function as Eq. 8.5-47 except there is no minus sign. The phase shift is given as

$$\text{Arg } H^{oo}(e^{j\omega T}) = -\frac{\pi}{2} - \left[\frac{\omega T}{2}\right] \tag{8.5-52}$$

Consequently, the magnitude and phase errors given in Table 8.5-1 are also appropriate for the noninverting switched capacitor integrator.

Figure 8.5-11 has a very important property not found in any of the switched capacitor circuits previously considered in this section. This property is called *stray insensitivity*. In reality, every node in a circuit has some stray capacitance to ground. These capacitances are represented by C_A and C_B in Fig. 8.5-11. During the ϕ_1 phase, C_B is discharged and C_A is charged by the voltage source, V_1.

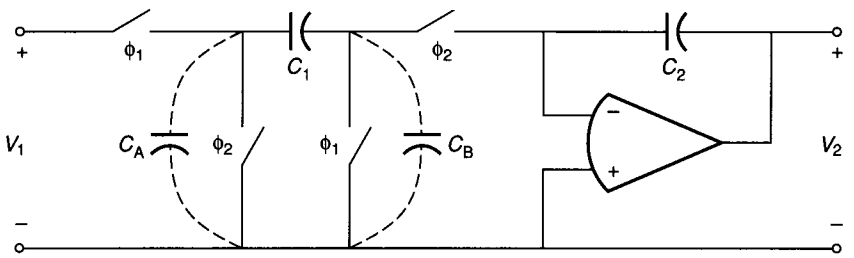

FIGURE 8.5-11
A stray-insensitive, noninverting switched capacitor integrator.

During the ϕ_2 phase, an uncharged C_B is paralleled with a virtual ground, and C_A is discharged to ground. Neither C_A nor C_B has any direct influence on the charge on C_1, which is transferred to C_2 during the ϕ_2 phase period. Consequently, Fig. 8.5-11 is insensitive to stray capacitances. Repeating this procedure with a stray capacitance in Fig. 8.5-10*a* will show that the charge transferred from C_1 to C_2 during the ϕ_2 phase period will be influenced by stray capacitances. Most commercial switched capacitor circuits use building blocks that are stray insensitive.

The stray-insensitive, inverting switched capacitor integrator of Fig. 8.5-12 will complete our repertoire of switched capacitor integrators. Although there are many other possible integrators, these will be sufficient for our purposes in this section. The transfer function of this integrator can be found by writing the expressions for the various charges that are being transferred. The clock phasing of Fig. 8.5-10*b* will be used for Fig. 8.5-12. The charge left on C_2 at the end of the even phase period is

$$Q_L^e\left(n - \frac{1}{2}\right) = C_2 V_2^e\left(n - \frac{1}{2}\right) \tag{8.5-53}$$

The charge on C_2 during the previous odd phase is

$$Q_M^o(n - 1) = C_2 V_2^o(n - 1) \tag{8.5-54}$$

The charge transferred to C_2 by the charging of C_1 to $V_1(n - \frac{1}{2})$ during the even phase is

$$Q_C^e\left(n - \frac{1}{2}\right) = -C_1 V_1^e\left(n - \frac{1}{2}\right) \tag{8.5-55}$$

Using charge conservation techniques gives

$$Q_L^e\left(n - \frac{1}{2}\right) = Q_M^o(n - 1) + Q_C^e\left(n - \frac{1}{2}\right) \tag{8.5-56}$$

Substituting Eqs. 8.5-53 through 8.5-55 into Eq. 8.5-56 results in

$$C_2 V_2^e\left(n - \frac{1}{2}\right) = C_2 V_2^o(n - 1) - C_1 V_1^e\left(n - \frac{1}{2}\right) \tag{8.5-57}$$

If we assume the input is from a sample-and-hold circuit, then $V_1^e(n - \frac{1}{2}) = V_1^o(n)$.

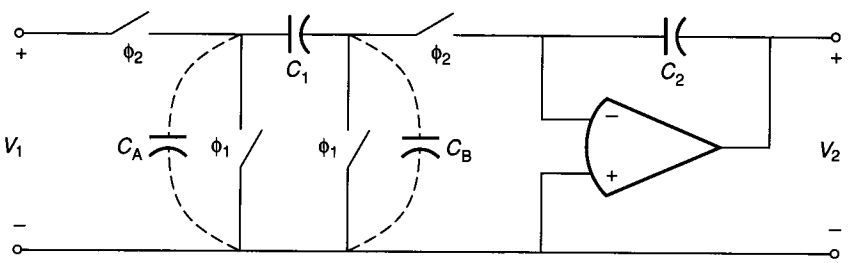

FIGURE 8.5-12
A stray-insensitive, inverting switched capacitor integrator.

During ϕ_1, $V_2^e(n-\frac{1}{2}) = V_2^o(n)$. Substituting these relations into Eq. 8.5-57 gives

$$C_2V_2^o(n) = C_2V_2^o(n-1) - C_1V_1^o(n) \tag{8.5-58}$$

Using Eq. 8.5-25 we obtain the desired transfer function for the circuit of Fig. 8.5-12 as

$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = -\frac{C_1}{C_2}\left(\frac{1}{1-z^{-1}}\right) \tag{8.5-59}$$

We see that for the inverting, stray-insensitive switched capacitor integrator, there is no delay in the forward path from the input to the output.

The frequency response of the circuit of Fig. 8.5-12 can be found by replacing z by $e^{j\omega T}$. Making this replacement and multiplying through the numerator and denominator by $e^{j\omega T}$ gives

$$H^{oo}(e^{j\omega T}) = -\frac{C_1}{C_2}\left(\frac{e^{j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\right) \tag{8.5-60}$$

We note that Eq. 8.5-60 is identical to Eq. 8.5-48 except for the minus sign in the numerator exponential. This means that the magnitude response of the circuit of Fig. 8.5-12 is given by Eq. 8.5-50 and the phase shift by Eq. 8.5-51, except that the phase error term is positive. The integrator error terms given in Table 8.5-1 are also applicable to the integrator of Fig. 8.5-12. The frequency response of various types of integrators is illustrated in Fig. 8.5-13 for a ratio of ω_o to ω_c of 0.1. The integrators we have just discussed are sufficient to implement practical switched capacitor filters. A more complete presentation, concerning other realizations and details, can be found in the literature.

Next we shall use the switched capacitor integrator to realize the passive RLC prototype ladder filter. Consider the fifth-order low-pass filter shown in Fig. 8.5-14. This filter is similar to the type that was considered in Sec. 8.4. The subscript n on the components indicates prototype or normalized values. The first step is to select the electrical variables that will be used to describe the circuit. Each component is characterized by a current, I_i, and a voltage, V_i, one of which can be expressed as the integration of the other variable. The integrand variable is current for an inductor and voltage for a capacitor. The integrand variables I_1, V_2, I_3, V_4, and I_5 are shown in Fig. 8.5-14.

The next step is to use these integrand variables to write a set of s-domain equations that describe the circuit. The selection of the integrand variables allows the realization using integrators. For the variable I_1, we may write the loop equation:

$$V_{in} - I_1(R_{0n} + sL_{1n}) - V_2 = 0 \tag{8.5-61}$$

Using the concept of a "voltage analog" of current, we express Eq. 8.5-61 as

$$V_{in} - \frac{V_1'}{R}(R_{0n} + sL_{1n}) - V_2 = 0 \tag{8.5-62}$$

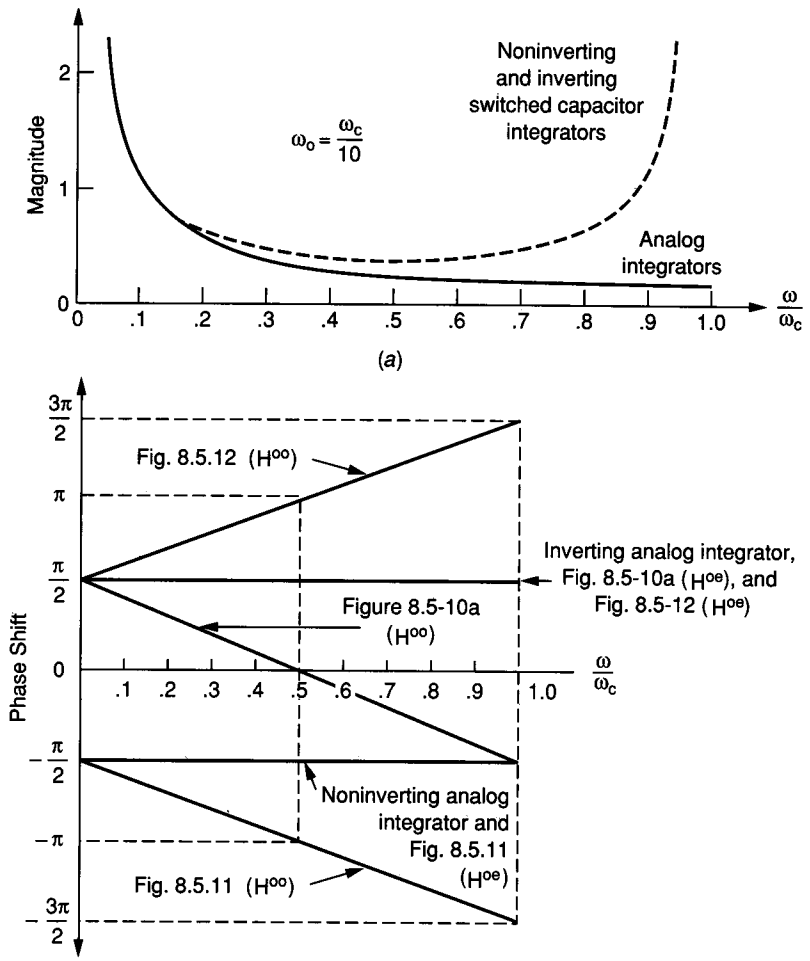

FIGURE 8.5-13
(*a*) Magnitude response of various switched capacitor integrators compared with a continuous-time integrator when $\omega_0/\omega_c = 1/10$, (*b*) Phase response of various switched capacitor and continuous-time integrators.

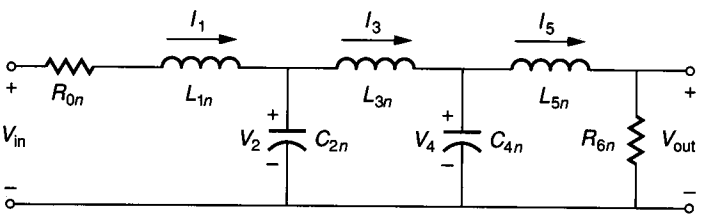

FIGURE 8.5-14
A fifth-order, low-pass, passive prototype filter.

where the voltage analog of I_1 is designated as V_1' and is defined as

$$V_1' = RI_1 \tag{8.5-63}$$

where R is an arbitrary scaling resistance (normally unity). Solving for V_1' of Eq. 8.5-62 results in

$$V_1' = \frac{R}{sL_{1n}}\left[V_{in} - V_2 - \left(\frac{R_{0n}}{R}\right)V_1'\right] \tag{8.5-64}$$

This expression can be implemented by an integrator that sums V_{in}, $-V_2$, and $-(R_{0n}/R)V_1'$. The fact that the output is in part equal to the integral of itself indicates nothing more than a damped integrator. Moving on to the next variable, V_2, we sum currents to get

$$I_1 - I_3 - sC_{2n}V_2 = 0 \tag{8.5-65}$$

Solving for the variable V_2 using voltage analogs of I_1 and I_2, we get

$$V_2 = \frac{1}{sRC_{2n}}[V_1' - V_3'] \tag{8.5-66}$$

The equation describing the variable I_3 can be written from the loop consisting of C_{2n}, L_{3n}, and C_{4n} as

$$V_2 - sL_{3n}I_3 - V_4 = 0 \tag{8.5-67}$$

Solving for the voltage analog of I_3 gives

$$V_3' = \frac{R}{sL_{3n}}(V_2 - V_4) \tag{8.5-68}$$

Next, the equation involving V_4 can be found by a nodal equation written as

$$I_3 - sC_{4n}V_4 - I_5 = 0 \tag{8.5-69}$$

Again using voltage analogs for I_3 and I_5 gives,

$$V_4 = \frac{1}{sRC_{4n}}(V_3' - V_5') \tag{8.5-70}$$

Finally, a loop equation involving C_{4n}, L_{5n}, and R_{6n} will be used to describe the variable I_5:

$$V_4 - sL_{5n}I_5 - I_5R_{6n} = 0 \tag{8.5-71}$$

which can be expressed in terms of voltage analogs as

$$V_5' = \frac{R}{sL_{5n}}\left(V_4 - \frac{R_{6n}}{R}V_5'\right) \tag{8.5-72}$$

However, we would prefer to have the variable V_{out} rather than V_5'. Because $V_{out} = (R_{6n}/R)V_5'$, we express Eq. 8.5-72 as

$$V_{out} = \frac{R_{6n}}{sL_{5n}}(V_4 - V_{out}) \tag{8.5-73}$$

The method of generating these equations should be obvious. Starting with Eq. 8.5-61, the equations are a succession of loop equations followed by a node equation. The substitution of V_{out} for V_5' was simply by application of Ohm's law. This method can be used for practically all low-pass ladder RLC filters.

The next step is the realization of Eqs. 8.5-64, 8.5-66, 8.5-68, 8.5-70, and 8.5-73. Equation 8.5-64 represents a summing integrator with inputs of V_{in}, V_2, and V_1' and output V_1'. It can be realized by switched capacitor circuits by combining the ideas of Figs. 8.5-11 and 8.5-12. The circuit of Fig. 8.5-15*a* results as a proposed realization of Eq. 8.5-64. Note that the right-hand switches have been combined to reduce the number of switches. Using the results of Eqs. 8.5-47 and 8.5-59, we write

$$V_1'(z) = \left(\frac{1}{1 - z^{-1}}\right)[\alpha_{11}z^{-1}V_{in}(z) - \alpha_{21}V_2(z) - \alpha_{31}V_1'(z)] \quad (8.5\text{-}74)$$

Next the high sampling approximation is made so that $1 - z^{-1}$ is approximately sT and z^{-1} is approximately $1 - sT \simeq 1$. Thus, Eq. 8.5-74 becomes

$$V_1'(s) \simeq \frac{1}{sT}[\alpha_{11}V_{in}(s) - \alpha_{21}V_2(s) - \alpha_{31}V_1'(s)] \quad (8.5\text{-}75)$$

Before Eq. 8.5-75 can be equated with Eq. 8.5-64, it must be frequency-denormalized. This is because Eq. 8.5-64 is based on a low-pass normalized prototype, having a cutoff frequency of 1 rps. This denormalization is accomplished by replacing the clock period, T, in Eq. 8.5-75 by

$$T = \frac{T_n}{\Omega_n} \quad (8.5\text{-}76)$$

where T_n is the normalized clock period and Ω_n is defined as

$$\Omega_n = \frac{\text{Actual cutoff frequency in rps}}{\text{Normalized cutoff frequency rps}} \quad (8.5\text{-}77)$$

Therefore, Eq. 8.5-75 can be written as

$$V_1'(s) \simeq \frac{1}{sT_n}[\alpha_{11}V_{in}(s) - \alpha_{21}V_2(s) - \alpha_{31}V_1'(s)] \quad (8.5\text{-}78)$$

Equating Eq. 8.5-78 and Eq. 8.5-64 results in the design of the first integrator of Fig. 8.5-15. These results are

$$\alpha_{11} = \alpha_{21} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n T}{L_{1n}} = \frac{R\Omega_n}{L_{1n}f_c} \quad (8.5\text{-}79)$$

and

$$\alpha_{31} = \frac{R_{0n}T_n}{L_{1n}} = \frac{R_{0n}\Omega_n T}{L_{1n}} = \frac{R_{0n}\Omega_n}{L_{1n}f_c} \quad (8.5\text{-}80)$$