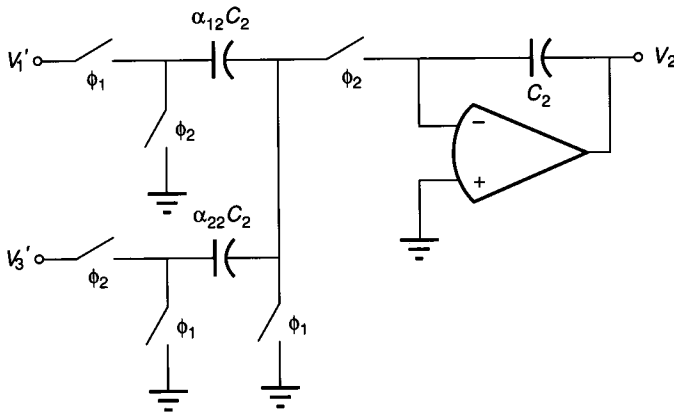
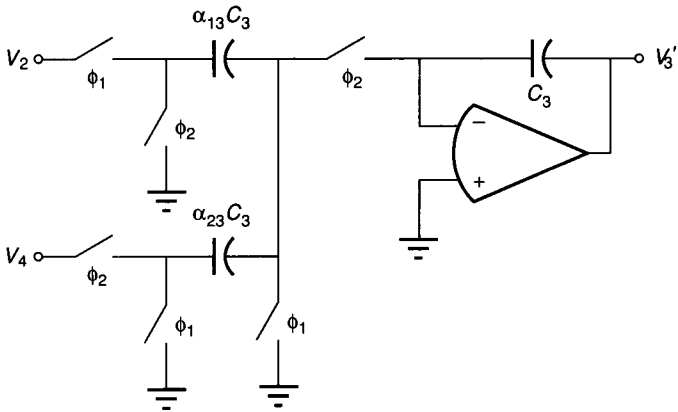


(a)

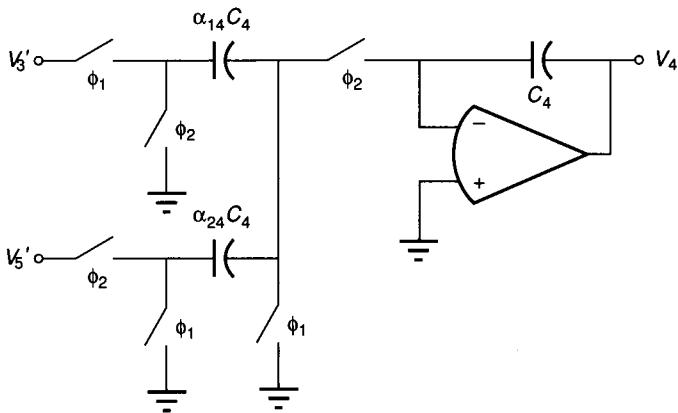


(b)

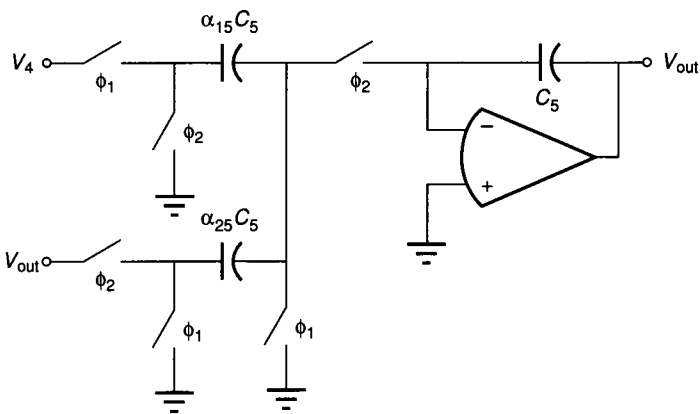
FIGURE 8.5-15
 Stage-by-stage realization of Fig. 8.5-14: (a) Input stage, (b) Second stage, (c) Third stage, (d) Fourth stage, (e) Output stage.



(c)



(d)



(e)

FIGURE 8.5-15
(Continued)

Next we repeat this process for the variable V_2 of Eq. 8.5-66. Figure 8.5-15*b* is a realization of Eq. 8.5-66. Using the high sampling approximation allows us to write the output of this circuit as

$$V_2(s) \approx \frac{1}{sT_n} [\alpha_{12}V'_1(s) - \alpha_{22}V'_3(s)] \quad (8.5-81)$$

employing the same approach that was used to get Eq. 8.5-78. Equating Eq. 8.5-66 with Eq. 8.5-81 results in

$$\alpha_{12} = \alpha_{22} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n T}{RC_{2n}} = \frac{\Omega_n}{RC_{2n}f_c} \quad (8.5-82)$$

The realizations for Eqs. 8.5-68, 8.5-70, and 8.5-73 are identical in concept to that of Eq. 8.5-66. Figure 8.5-15 shows the switched capacitor realizations of these equations. Using the same approach as before, we may express the design equations of Fig. 8.5-15*c* as

$$\alpha_{13} = \alpha_{23} = \frac{RT_n}{L_{3n}} = \frac{R\Omega_n T}{L_{3n}} = \frac{R\Omega_n}{f_c L_{3n}} \quad (8.5-83)$$

and Fig. 8.5-15*d* as

$$\alpha_{14} = \alpha_{24} = \frac{T_n}{RC_{4n}} = \frac{\Omega_n T}{RC_{4n}} = \frac{\Omega_n}{RC_{4n}f_c} \quad (8.5-84)$$

and Fig. 8.5-15*e* as

$$\alpha_{15} = \alpha_{25} = \frac{R_{6n}T_n}{L_{5n}} = \frac{R_{6n}\Omega_n}{L_{5n}f_c} \quad (8.5-85)$$

Equations 8.5-79, 8.5-80, and 8.5-82 through 8.5-85 permit the design of the filter in Fig. 8.5-14 according to a given set of specifications. When the various integrators of Fig. 8.5-15 are combined, the filter realization is that shown in Fig. 8.5-16. The filter structure consists of coupled internal feedback loops containing two integrators each. In order to achieve minimum delay around each loop, it is necessary that each integrator be sampled by the next integrator as soon as the new sample is available. Therefore, in one clock period, the signal circulates around the internal feedback loop. The clock scheme indicated will avoid a $T/2$ delay, which would create a difference between the actual realization and that desired. The following example illustrates the application of the preceding approach to the switched capacitor realization of a low-pass filter.

Example 8.5-1. A switched capacitor realization of a fifth-order low-pass Chebyshev filter. A fifth-order low-pass Chebyshev filter with a 1 dB ripple in the passband is to be designed for a cutoff frequency of 1000 Hz. The structure of Fig. 8.5-16 based upon the passive prototype of Fig. 8.5-14 is to be used. Find the switched capacitor realization for this filter if the clock frequency is 100 kHz.

Solution. The normalized values of the RLC passive prototype that satisfies the specifications are $R_{0n} = 1 \Omega$, $L_{1n} = 2.1349 \text{ H}$, $C_{2n} = 1.0911 \text{ F}$, $L_{3n} = 3.009 \text{ H}$,

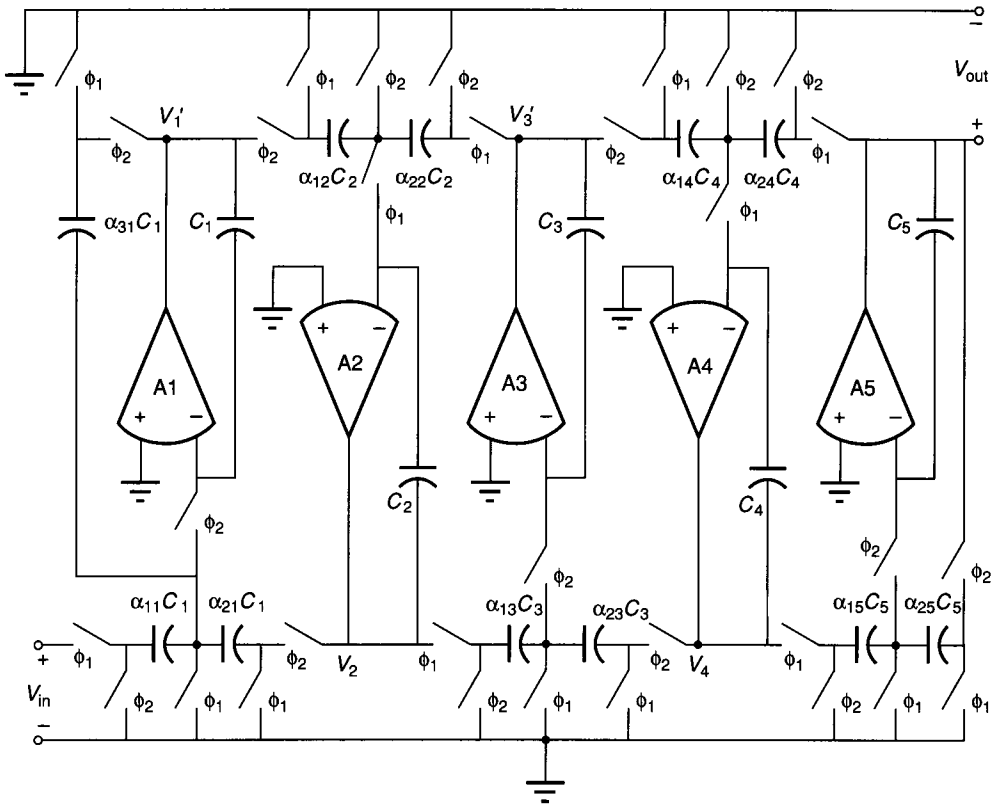


FIGURE 8.5-16
Switched capacitor realization of Fig. 8.5-14.

$C_{4n} = 1.0911$ F, $L_{5n} = 2.1349$ H, and $R_{6n} = 1 \Omega$. These values are found from tabulations in the literature.^{26,31} Using the preceding equations with $\Omega_n = 2000\pi$, we get

$$\alpha_{11} = \alpha_{21} = \alpha_{31} = 0.02943$$

$$\alpha_{12} = \alpha_{22} = 0.05759$$

$$\alpha_{13} = \alpha_{23} = 0.02094$$

$$\alpha_{14} = \alpha_{24} = 0.05759$$

$$\alpha_{15} = \alpha_{25} = 0.2943$$

One item of concern in switched capacitor filters is the total capacitance required in the realization. Large capacitor ratios are undesirable because of the loss of relative accuracy and increased area. If α_{ij} of the j th stage is less than unity, then $\alpha_{ij} C_j$ will be less than C_j . If we equate the smallest capacitor, $\alpha_{ij} C_j$, to a unity capacitance C_{uj} , then we may find the total relative capacitance of a stage by summing C_{uj} with all other capacitors being divided by α_{ij} . In the

preceding example if we let $C_{u1} = C_{u2} = C_{u3} = C_{u4} = C_{u5} = C_u$, then the total capacitance is $155.596C_u$. If C_u is selected as 1 pF, then 155.596 pF of capacitance is required for the filter. It is important to keep this number as small as possible if the filter is to be integrated. Reduction of the clock frequency will always reduce this number, but at the expense of not satisfying the high sampling approximation at the higher signal frequencies.

This design method starting from the low-pass, passive RLC prototype is general and can be applied to all types of symmetrical filters. Elliptic filters can also be synthesized by replacing the L cutsets or C loops with controlled sources.²⁶ The result requires a nonintegrated input to the integrator, which can be accomplished by an unswitched capacitor. Bandpass, high-pass, and band-elimination filters can be synthesized using the transformations of Fig. 8.4-13 applied to the low-pass, passive RLC prototype. The bandpass is realized by a second-order bandpass structure with the ability to sum multiple inputs. Such a structure could be derived from the circuit of Fig. 8.4-15c if the integrators are replaced by the appropriate combinations of the integrators of Fig. 8.5-11 and Fig. 8.5-12 with summing inputs.

The high-pass switched capacitor filter realizations present more of a challenge, although they use the same approach as that used for low-pass switched capacitor filters. The reason for the additional complexity is that the low-pass to high-pass transformation applied to the low-pass, passive RLC prototype will result in differentiators if the same integrand variables used for low-pass filters are selected. It is necessary to reselect the variables so that the equations can be realized with integrators.

Band-elimination filters are also possible using this approach. One first transforms the low-pass, passive RLC prototype to a band-elimination form. The switched capacitor realization will require a second-order structure with the ability to sum both integrated and nonintegrated inputs. For more information on the design of switched capacitor circuits from general symmetrical filters, the reader should consult Chapter 4 of the text *Switched Capacitor Circuits*.²⁶

8.5.3 Z-Domain Synthesis Techniques

In many cases, the designer is given the filter approximation in the z -domain rather than the s -domain. In this case, the realization of the filter takes place directly in the z -domain. Various methods of arriving at $H(z)$ given $H(s)$ are well developed and can be found elsewhere. Irrespective of how the transformation is made, the starting point of z -domain synthesis techniques is

$$H(z) = \frac{a_0 + a_1z + a_2z^2 + \dots + a_{m-1}z^{m-1} + a_mz^m}{b_0 + b_1z + b_2z^2 + \dots + b_{n-1}z^{n-1} + b_nz^n} \quad (8.5-86)$$

One approach is to convert Eq. 8.5-86 into a signal flow diagram consisting of amplifiers, delays, and summers.⁴³ Another approach is to break Eq. 8.5-86 into products of first- and second-order terms. An example of how the first approach works is illustrated by Fig. 8.5-17a. This is a general building block that consists of a combination of a stray-insensitive noninverting and inverting

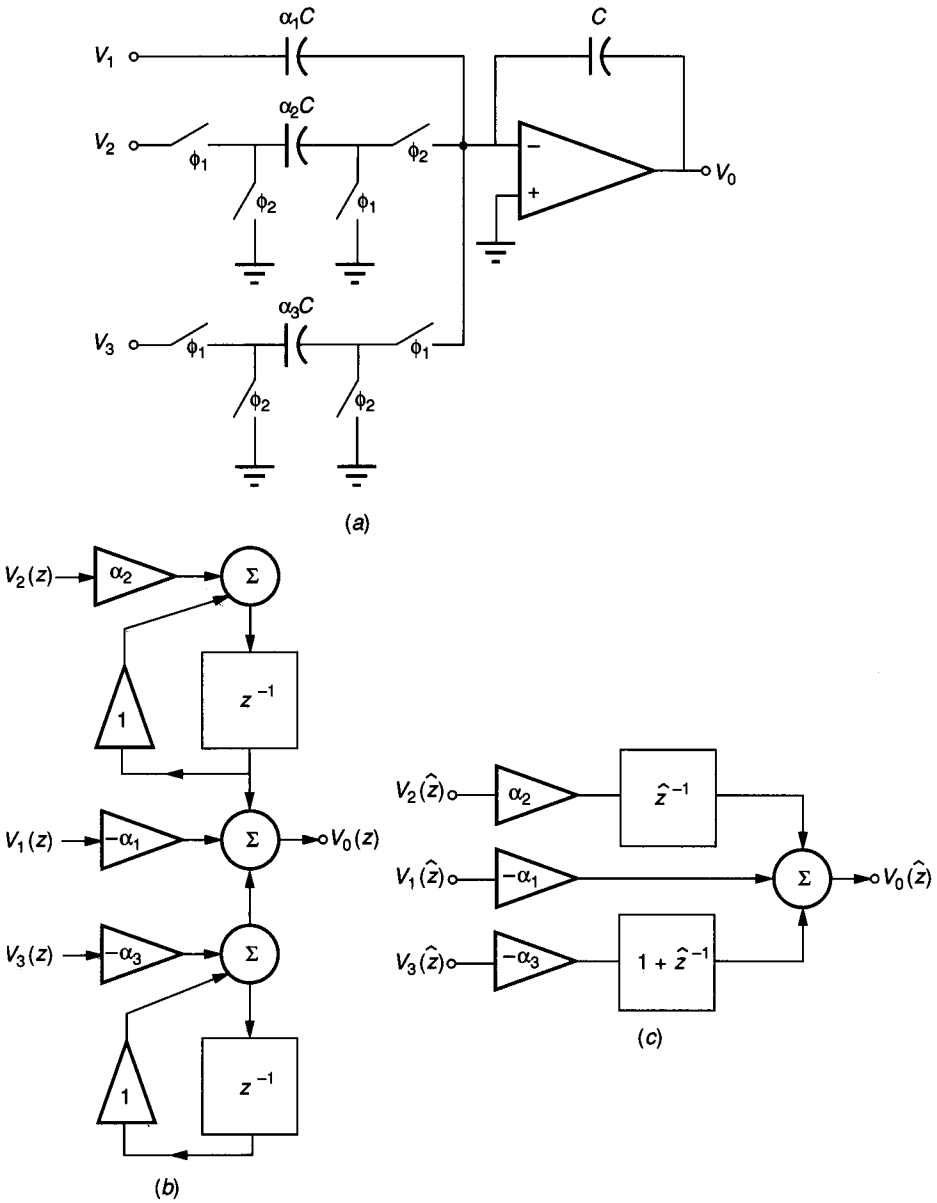


FIGURE 8.5-17
 General building block: (a) SC circuit, (b) z -domain block diagram, (c) \hat{z} -domain block diagram.

integrators and an inverting amplifier. Note that V_1 , V_2 , and V_3 can be connected at arbitrarily different points or to the same node to provide more flexibility for different structures. This general building block can provide different paths, including local feedback, overall feedback, and feedforward. Figure 8.5-17b shows the flow diagram of Fig. 8.5-17a in terms of z^{-1} delay elements. A change of the z -domain variable is introduced, which simplifies the flow diagram and improves the sensitivity performance of the various realizations.⁴⁶ This transformation is

$$\hat{z} = z - 1 \quad (8.5-87)$$

Figure 8.5-17c gives the \hat{z} flow diagram of the circuit of Fig. 8.5-17a. The output of the circuit of Fig. 8.5-17c, $V_o(\hat{z})$, is given by

$$V_o(\hat{z}) = \alpha_2 \hat{z}^{-1} V_2(\hat{z}) - \alpha_1 V_1(\hat{z}) - \alpha_3 (1 + \hat{z}^{-1}) V_3(\hat{z}) \quad (8.5-88)$$

The transformation used in Eq. 8.5-87 is arbitrary. The design procedure outlined in the following could equally well be applied to $H(z)$. Note that Eq. 8.5-88 may be simplified if $V_2(\hat{z}) = V_3(\hat{z})$. Combinations of this general building block can be used to realize various z -domain transfer functions when the transformation of Eq. 8.5-87 is made to Eq. 8.5-86 to get $H(\hat{z})$. When $H(\hat{z})$ is converted to a signal flow diagram, then the synthesis becomes a straightforward procedure. These ideas will be demonstrated for second- and third-order structures, which can be cascaded to obtain a filter of any order in the z -domain.

One popular method of designing higher-order filters is the cascade of first-, second-, and third-order sections.^{47,48} Because Fig. 8.5-17a represents a first-order filter, we will consider only the second-order (biquad) and third-order (triquad) realizations. The biquad is a fundamental building block for higher-order switched capacitor filters. The biquad flow diagram shown in Fig. 8.5-18 is a versatile structure and is one of many that could be considered. The properties of this structure are (1) the capability of realizing all stable z -domain biquadratic transfer functions, (2) sufficient flexibility to permit small total capacitance with low sensitivity, and (3) freedom from parasitic capacitances.

The general biquad structure is formed by the interconnection of the general building block of Fig. 8.5-17a. The biquadratic transfer function of the circuit of Fig. 8.5-18 is given as

$$H(\hat{z}) = \frac{V_o(\hat{z})}{V_i(\hat{z})} = \frac{A_0 + A_1 \hat{z}^{-1} + A_2 \hat{z}^{-2}}{1 + C_1 \hat{z}^{-1} + C_2 \hat{z}^{-2}} \quad (8.5-89)$$

where

$$\begin{aligned} A_0 &= D_0 B_3 - D_3 \\ A_1 &= D_1 - D_3 + D_3 B_0 - D_0 B_1 - D_2 B_3 + D_0 B_3 \\ A_2 &= D_3 B_0 + D_2 B_1 - D_2 B_3 - D_1 B_0 \\ C_1 &= B_2 B_3 - B_0 \\ C_2 &= B_2 B_3 - B_1 B_2 \end{aligned} \quad (8.5-90)$$

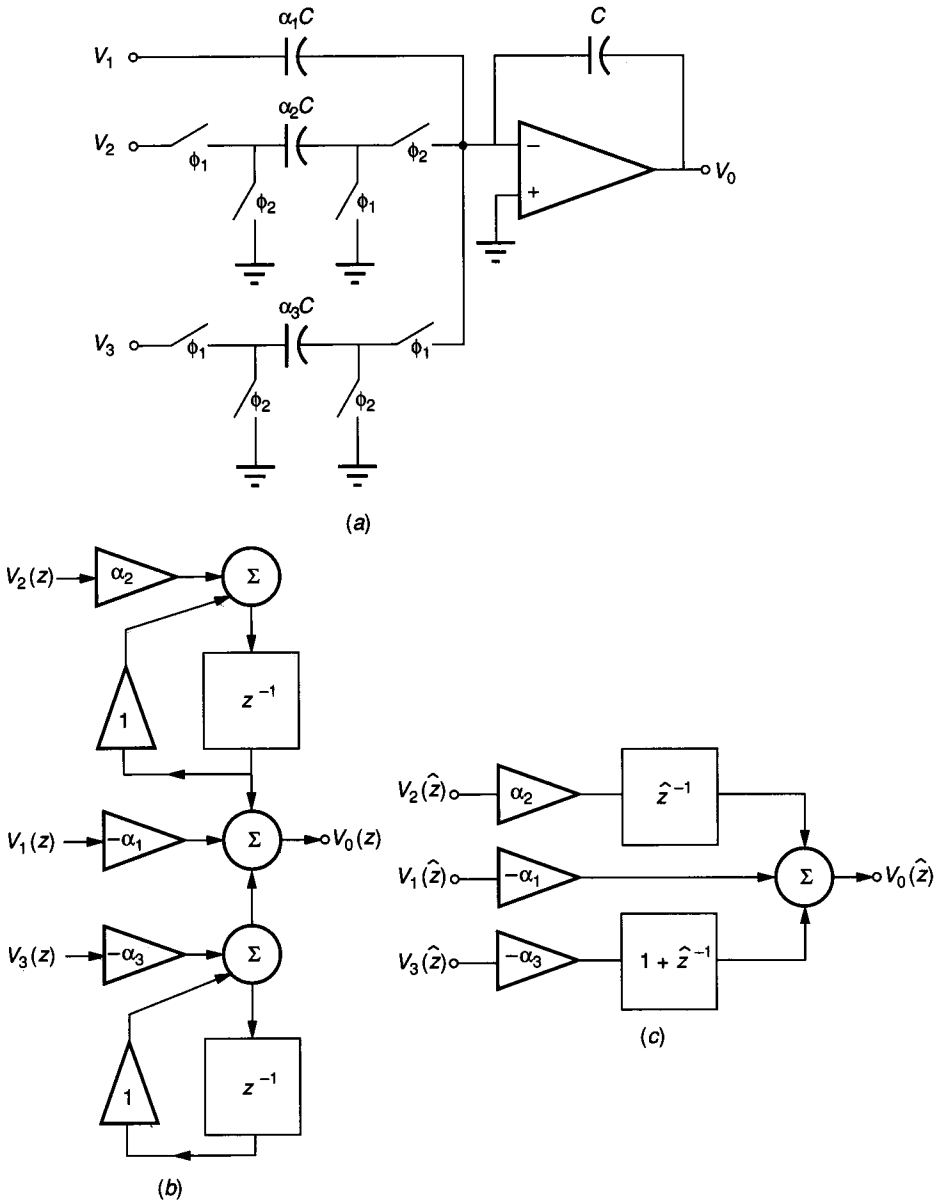


FIGURE 8.5-17
 General building block: (a) SC circuit, (b) z -domain block diagram, (c) \hat{z} -domain block diagram.

integrators and an inverting amplifier. Note that V_1 , V_2 , and V_3 can be connected at arbitrarily different points or to the same node to provide more flexibility for different structures. This general building block can provide different paths, including local feedback, overall feedback, and feedforward. Figure 8.5-17b shows the flow diagram of Fig. 8.5-17a in terms of z^{-1} delay elements. A change of the z -domain variable is introduced, which simplifies the flow diagram and improves the sensitivity performance of the various realizations.⁴⁶ This transformation is

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$$V_o(\hat{z}) = \alpha_2 \hat{z}^{-1} V_2(\hat{z}) - \alpha_1 V_1(\hat{z}) - \alpha_3 (1 + \hat{z}^{-1}) V_3(\hat{z}) \quad (8.5-88)$$

The transformation used in Eq. 8.5-87 is arbitrary. The design procedure outlined in the following could equally well be applied to $H(z)$. Note that Eq. 8.5-88 may be simplified if $V_2(\hat{z}) = V_3(\hat{z})$. Combinations of this general building block can be used to realize various z -domain transfer functions when the transformation of Eq. 8.5-87 is made to Eq. 8.5-86 to get $H(\hat{z})$. When $H(\hat{z})$ is converted to a signal flow diagram, then the synthesis becomes a straightforward procedure. These ideas will be demonstrated for second- and third-order structures, which can be cascaded to obtain a filter of any order in the z -domain.

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The general biquad structure is formed by the interconnection of the general building block of Fig. 8.5-17a. The biquadratic transfer function of the circuit of Fig. 8.5-18 is given as

$$H(\hat{z}) = \frac{V_{o2}(\hat{z})}{V_i(\hat{z})} = \frac{A_0 + A_1 \hat{z}^{-1} + A_2 \hat{z}^{-2}}{1 + C_1 \hat{z}^{-1} + C_2 \hat{z}^{-2}} \quad (8.5-89)$$

where

$$\begin{aligned} A_0 &= D_0 B_3 - D_3 \\ A_1 &= D_1 - D_3 + D_3 B_0 - D_0 B_1 - D_2 B_3 + D_0 B_3 \\ A_2 &= D_3 B_0 + D_2 B_1 - D_2 B_3 - D_1 B_0 \\ C_1 &= B_2 B_3 - B_0 \\ C_2 &= B_2 B_3 - B_1 B_2 \end{aligned} \quad (8.5-90)$$

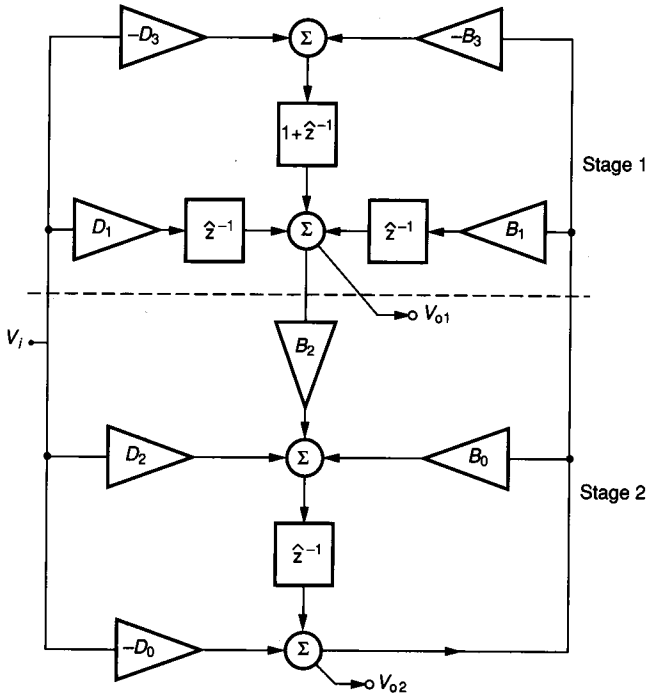


FIGURE 8.5-18
Signal flow diagram of a biquad.

It is observed in Fig. 8.5-18 that B_0 and B_1 are positive-feedback components. If B_0 and B_1 are zero, the filter will be stable from an ideal viewpoint. For nonzero values of B_0 and B_1 , the filter will remain stable if B_3 is greater than B_1 and B_0 is less than B_2B_3 .

Figure 8.5-19a shows a switched capacitor implementation of the flow diagram of Fig. 8.5-18. The two outputs are designated as V_{o1} and V_{o2} . The most general output of this realization is at V_{o2} because each coefficient can be realized independently of the other. The transfer function at V_{o2} is

$$H(\hat{z}) = \frac{V_{o2}(\hat{z})}{V_i(\hat{z})} = \frac{D_0 + (D_3B_2 - D_2)\hat{z}^{-1} + (D_3B_2 - D_1B_2)\hat{z}^{-2}}{1 + (B_2B_3 - B_0)\hat{z}^{-1} + (B_2B_3 - B_1B_2)\hat{z}^{-2}} \quad (8.5-91)$$

Note that the individual B s and D s represent a ratio of two capacitors. The circuit can be simplified in a number of ways depending on the actual transfer function required. For instance, if there is a zero at $\hat{z} = -2$ (i.e., $z = 1$), the “bilinearly” equivalent analog-domain zero frequency is at $s = \infty$; and if the zero is neglected, then D_0 becomes zero. The switched capacitor implementation of Fig. 8.5-19a with the minimum number of switches is shown in Fig. 8.5-19b.

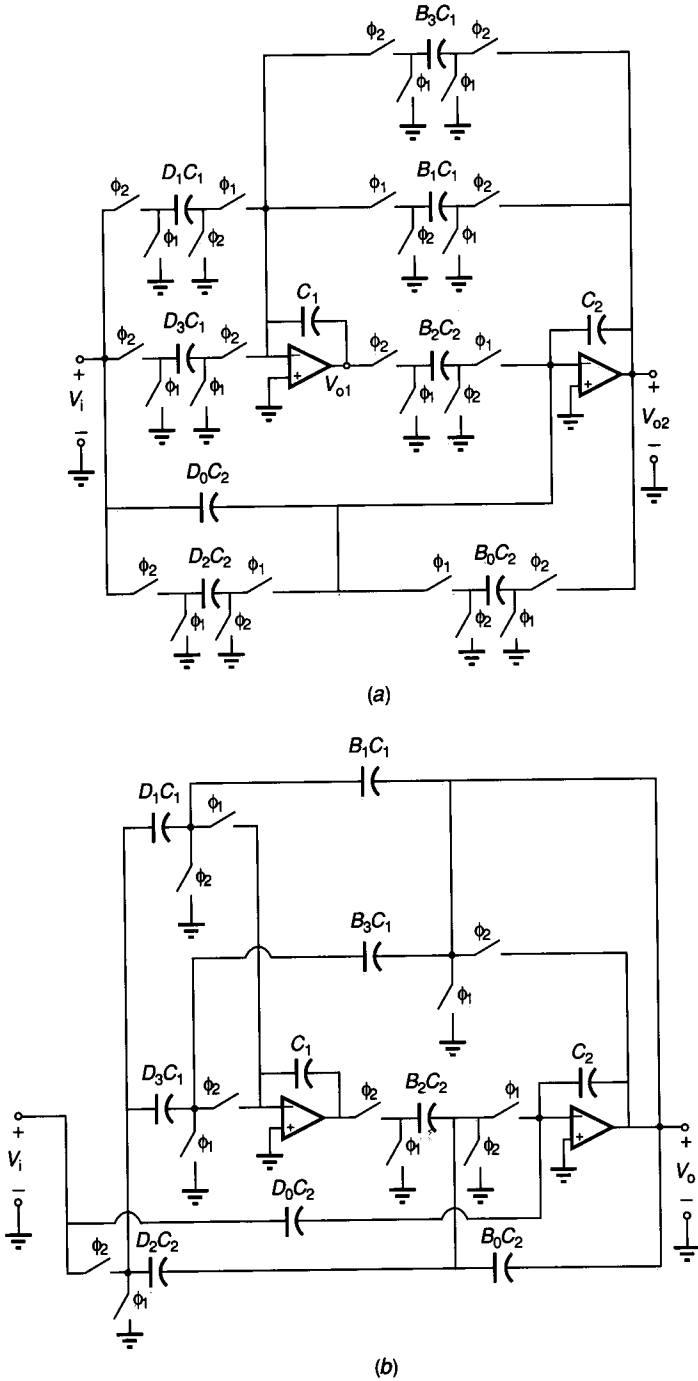


FIGURE 8.5-19
 (a) Switched capacitor implementation of Fig. 8.5-18, (b) Switched capacitor biquad with a minimum number of switches.

Generally, the second-order z -domain transfer function is given in terms of its z -domain roots. A general expression for Eq. 8.5-91 in terms of the roots is

$$H(\hat{z}) = \frac{1 + (2 - 2r_o \cos \theta_o)\hat{z}^{-1} + (1 + r_o^2 - 2r_o \cos \theta_o)\hat{z}^{-2}}{1 + (2 - 2r \cos \theta)\hat{z}^{-1} + (1 + r^2 - 2r \cos \theta)\hat{z}^{-2}} \quad (8.5-92)$$

where the locations of the poles and zeros in the z -plane are at $re^{\pm j\theta}$ and $r_o e^{\pm j\theta_o}$, respectively. Expressions for the root locations in terms of the coefficients are

$$r = [1 - B_1 B_2 + B_0]^{1/2} \quad (8.5-93)$$

$$\cos \theta = \frac{2 - B_2 B_3 + B_0}{2r} \quad (8.5-94)$$

$$r_o = [1 + (D_2 - D_1 B_2)/D_0]^{1/2} \quad (8.5-95)$$

and

$$\cos \theta_o = \frac{2 + (D_2 - D_3 B_2)/D_0}{2r_o} \quad (8.5-96)$$

A possible set of design equations is developed next. The root locations described by r , r_o , θ , and θ_o are assumed to be given. Because there are several extra degrees of freedom, we can arbitrarily choose B_2 , B_3 , D_2 , and D_3 . Therefore, the rest of the components can be calculated from

$$B_0 = 2r \cos \theta - 2 + B_2 B_3 \quad (8.5-97)$$

$$B_1 = 0.5[2 - B_2 B_3 + B_0] \quad (8.5-98)$$

$$D_0 = \frac{D_2 - D_3 B_2}{2(r_o \cos \theta_o - 1)} \quad (8.5-99)$$

and

$$D_1 = \frac{D_2 + (1 - r_o^2)D_0}{B_2} \quad (8.5-100)$$

It is observed that the general biquad can be simplified by choosing as many of the capacitor values as possible to be equal to zero. The coefficients of Eq. 8.5-91 are a result of the multiplication and subtraction of several individual capacitor ratios. Thus, the biquad is capable of realizing very small coefficients. However, we must keep in mind that the sensitivity might be inversely proportional to that small difference. Typically, a tradeoff between sensitivities and total capacitance is possible and will be illustrated shortly.

Next, a third-order realization is developed. This structure is useful when the filter has an odd order. Figure 8.5-20a shows a general third-order structure in its signal flow diagram form. The transfer function of this structure is

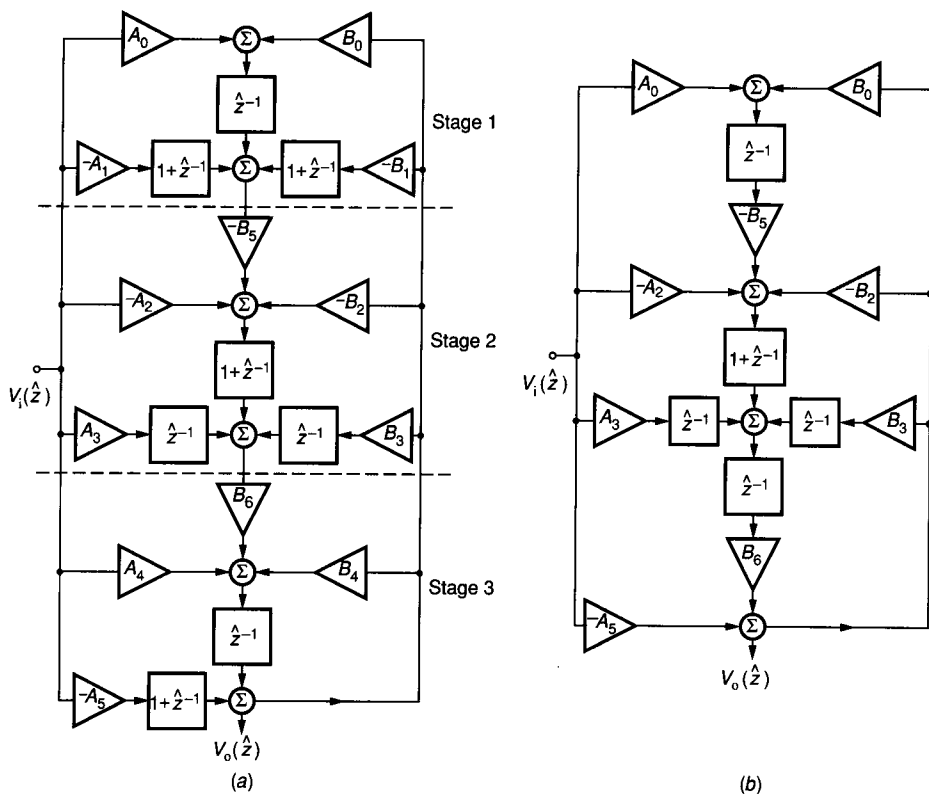


FIGURE 8.5-20
 (a) General third-order block diagram, (b) Simplified third-order block diagram (signal flow graph).

$$H(\hat{z}) = \frac{V_o(\hat{z})}{V_i(\hat{z})} = \frac{\alpha_0 + \alpha_1\hat{z}^{-1} + \alpha_2\hat{z}^{-2} + \alpha_3\hat{z}^{-3}}{1 + \beta_1\hat{z}^{-1} + \beta_2\hat{z}^{-2} + \beta_3\hat{z}^{-3}} \quad (8.5-101)$$

where

$$\alpha_0 = -A_5 \quad (8.5-102)$$

$$\alpha_1 = A_1B_5B_6 - A_2B_6 + A_4 - A_5 \quad (8.5-103)$$

$$\alpha_2 = 2A_1B_5B_6 - A_0B_5B_6 + A_3B_6 - A_2B_6 \quad (8.5-104)$$

$$\alpha_3 = B_5B_6(A_1 - A_0) \quad (8.5-105)$$

$$\beta_1 = B_2B_6 - B_1B_5B_6 - B_4 \quad (8.5-106)$$

$$\beta_2 = B_0B_5B_6 - 2B_1B_5B_6 - B_3B_6 + B_2B_6 \quad (8.5-107)$$

and

$$\beta_3 = B_5B_6(B_0 - B_1) \quad (8.5-108)$$

Besides the transfer function of Eq. 8.5-101, two other transfer functions for each op amp output can be obtained. Equation 8.5-101 is chosen for its flexibility. A simplified yet versatile structure is considered next.

If $B_1 = B_4 = A_1 = A_4 = 0$, and if we omit the $1 + \hat{z}^{-1}$ following A_5 , then the flow diagram Fig. 8.5-20*b* results. The coefficients of Eq. 8.5-101 become

$$-\alpha_0 = A_5 \quad (8.5-109)$$

$$-\alpha_1 = A_2 B_6 \quad (8.5-110)$$

$$-\alpha_2 = B_6(A_0 B_5 - A_3 + A_2) \quad (8.5-111)$$

$$-\alpha_3 = A_0 B_5 B_6 \quad (8.5-112)$$

$$\beta_1 = B_2 B_6 \quad (8.5-113)$$

$$\beta_2 = B_6(B_0 B_5 - B_3 + B_2) \quad (8.5-114)$$

and

$$\beta_3 = B_0 B_5 B_6 \quad (8.5-115)$$

A switched capacitor implementation of Fig. 8.5-20*b* is shown in Fig. 8.5-21. Table 8.5-2 shows the generality of the third-order building block in designing the transmission zeros. This table gives the values of the α coefficients and the capacitor ratios required for several conventional types of filters. In addition to the tradeoff between sensitivity and total capacitance mentioned before, we have added the constraint that the largest-to-smallest capacitor ratio be less than 10. More details regarding the tradeoff between sensitivity, output voltage swing, and total capacitance are given elsewhere.⁴⁹

If the third-order specifications are given in terms of root locations, then it is necessary to relate the coefficients to the root locations. The root locations include one real pole at r_1 , two complex poles at $r e^{\pm j\theta}$, and two complex zeros at $r_0 e^{\pm j\theta_0}$. These expressions are

$$\alpha_0 = 0 \quad (8.5-116)$$

$$\alpha_1 = 1 \quad (8.5-117)$$

$$\alpha_2 = 2 - 2r_0 \cos \theta_0 \quad (8.5-118)$$

$$\alpha_3 = 1 + r_0^2 - 2r_0 \cos \theta_0 \quad (8.5-119)$$

$$\beta_1 = 3 - r_1 - 2r \cos \theta \quad (8.5-120)$$

$$\beta_2 = 3 - 2r_1 + r^2 - 4r \cos \theta + 2rr_1 \cos \theta \quad (8.5-121)$$

and

$$\beta_3 = 1 - r_1 + r^2 - r_1 r^2 - 2r \cos \theta + 2rr_1 \cos \theta \quad (8.5-122)$$

To illustrate the synthesis procedure, the second-order and third-order blocks are used to design a fifth-order low-pass filter. The specifications of the filter are a 0.125 dB passband ripple, a cutoff frequency of 3.4 kHz, a stopband minimum attenuation of 32 dB above 4.6 kHz and a clock frequency of 128 kHz. The design begins with the roots of the s -domain rational polynomial approximation, $H(s)$. These roots are mapped to the z -domain through the bilinear transformation.²⁶

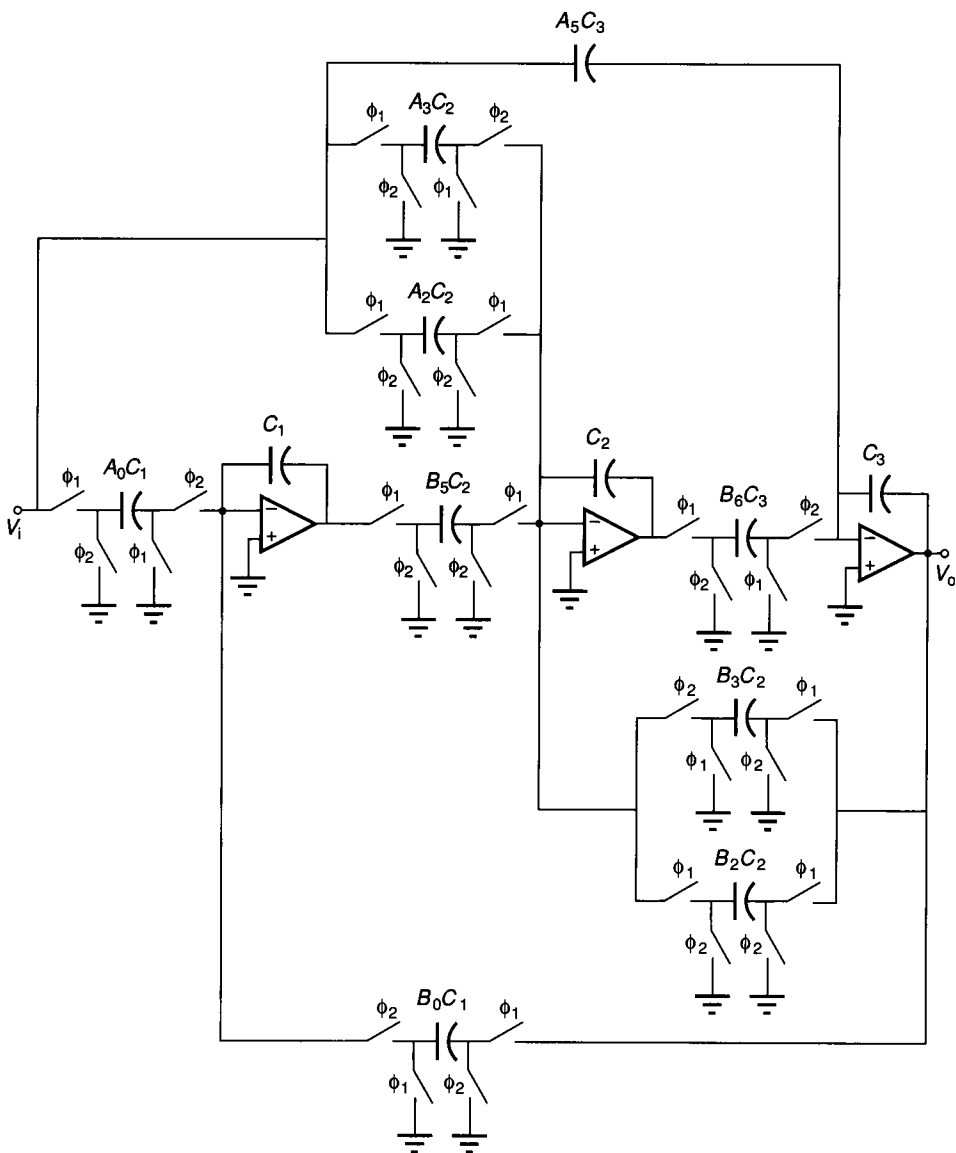


FIGURE 8.5-21
Switched capacitor implementation of Fig. 8.5-20b.

TABLE 8.5-2
Values of coefficients of zeros of the third-order filter

Filter type	Zeros in z-plane	Coefficient of $H(z)$					Corresponding capacitor ratios				
		α_0	α_1	α_2	α_3		A_0	A_2	A_3	A_5	
Low-pass	$z_1 = -1$	0	0	0	1		B_0^a	0	$A_0 B_5$	0	
Band-pass	$z_1 = -1$	0	0	1	0		0	0	A_3^b	0	
	$z_2 = 1$	1	0	0	0		0	0	0	A_5^b	
Notch	$z_1 = e^{j\theta_0}$	0	1	$2(1 - \cos \theta_0)$	$2(1 - \cos \theta_0)$		$\frac{\alpha_2}{B_5 B_6}$	$\frac{1}{B_6}$	$\frac{1}{B_6}$	0	
	$z_2 = e^{-j\theta_0}$	0	1	$2(1 - \cos \theta_0)$	$2(1 - \cos \theta_0)$						

^a $A_0 = B_0$ to obtain a 0 dB dc gain.

^b A_3 and A_5 to be chosen to give the required center (cutoff) frequency gain.

^c A_0 , A_2 , and A_3 can be scaled to obtain the desired dc gain.

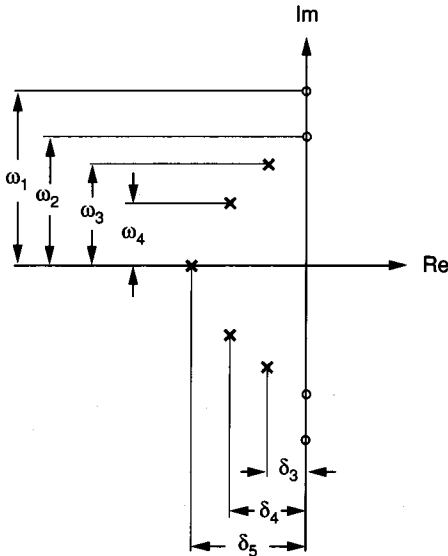


FIGURE 8.5-22
 Root locations in the s -plane of the fifth-order filter: \circ = zeros, \times = poles; $\omega_1 = 40.792 \times 10^3$, $\omega_2 = 28.367 \times 10^3$, $\omega_3 = 22.604 \times 10^3$, $\omega_4 = 17.83 \times 10^3$, $\delta_3 = 1.938 \times 10^3$, $\delta_4 = 8.514 \times 10^3$, $\delta_5 = 15.474 \times 10^3$.

The s -domain zero at infinity that maps to $\hat{z} = -2$ is ignored. The location of the roots in the s -domain are illustrated in Fig. 8.5-22. The second-order realization has two zeros and two poles, $\pm j\omega_2$ and $\delta_4 \pm j\omega_4$, respectively. The corresponding root locations in the \hat{z} -domain are $r = 0.92838$, $\theta = \pm 7.722^\circ$, and $r_o = 1.0$, $\theta_o = \pm 12.928^\circ$ for the poles and zeros, respectively. The third-order stage realizes two zeros and three poles: $\pm j\omega_1$, δ_5 , and $\delta_3 \pm j\omega_3$, respectively. The corresponding root locations in the z -domain are $r = 0.938$, $\theta = \pm 9.88^\circ$, $r_1 = 0.878$, $r_o = 1.0$, and $\theta_o = \pm 18.9^\circ$ for the poles and zeros, respectively.

It should be noted that in obtaining the coefficients in both filters, the dc gain of each stage was adjusted to be near unity. For the specified values of r and θ , the capacitor ratios of the biquad can be calculated by setting $B_2 = 0.1$, $B_3 = 1.6$, $D_2 = 0.0$, and $D_3 = 0.22$. The final results are summarized in Table 8.5-3. The total capacitance for the biquad is $28.172 C_u$. The capacitor ratios for the third-order building block are given in Table 8.5-4. The total capacitance for the third-order building block is $39.481 C_u$. After simplifications,⁴⁹ the total capacitance is $33.28 C_u$. The total filter capacitance is $C_T = 61.452 C_u$. It has been shown that there is a tradeoff between sensitivity, total capacitance, and dynamic range.²⁶ Figure 8.5-23 shows the resulting fifth-order low-pass filter realization.

TABLE 8.5-3
Capacitor values in units of C_μ for the biquad circuit

Capacitor	$B_2 C_2$ $B_3 C_1$	$B_1 C_1$	$B_0 C_2$ $D_2 C_2$	$D_3 C_1$	$D_0 C_2$	$D_1 C_1$	C_1	C_2
Value	1	6.2863	0	1	4.3336	0	4.5517	10

TABLE 8.5-4
Capacitor values in units of C_μ for the triquad circuit

Capacitor	A_0C_1 B_0C_1	C_1 C_3	B_6C_3 A_2C_2	A_3C_2	B_2C_2	B_3C_2	C_2	B_5C_2
Value	1	10	1	1	5.684	4.657	3.057	1.083

The performance of this filter is shown in Fig. 8.5-24. The simulated results and the experimental results agree quite closely.⁵⁰

A brief overview of the methods of designing switched capacitor filters has been shown. The three approaches selected were resistor replacement or simulation by switched capacitor equivalents, the use of integrators to realize passive RLC prototype ladder filters, and the direct synthesis of the z -domain transfer function. Many more approaches exist, and they should be considered if the above approaches do not provide the required performance.

Because of the lack of space, topics such as the prewarping of the s -domain specifications to account for the $(\sin x)/x$ effect of the sample-and-hold circuit on the filter performance have not been discussed. Also, the influence of the switches and the op amp performance (gain and bandwidth) have not been considered. Another problem the designer is faced with when designing switched capacitor circuits is a method of analysis. Because the switched capacitor circuit is an analog sampled-data system, aliasing can occur, and it is often necessary to use an antialiasing filter, which must be a continuous-time filter. Fortunately, the accuracy requirement of the continuous-time, antialiasing filter is not severe, and RC active filter techniques can be used.

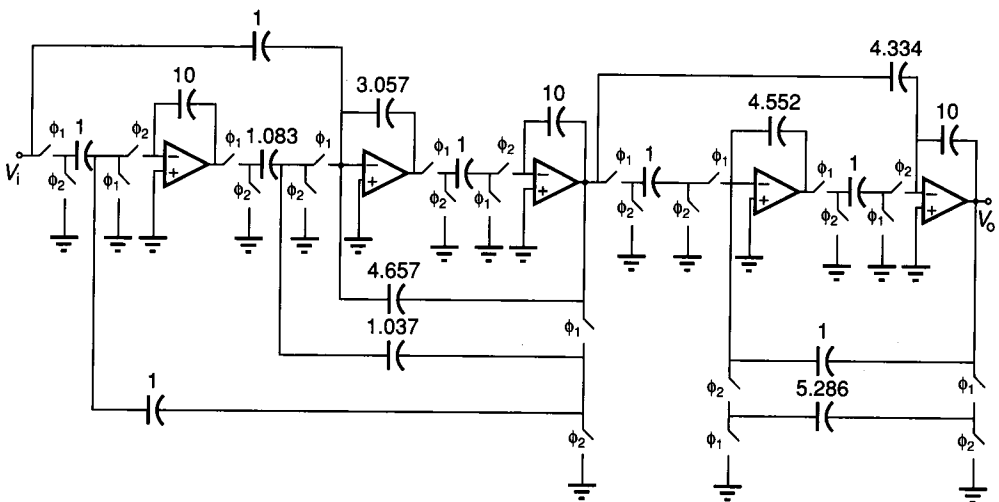


FIGURE 8.5-23

SC circuit diagram of the fifth-order filter, capacitor values in C_μ units.

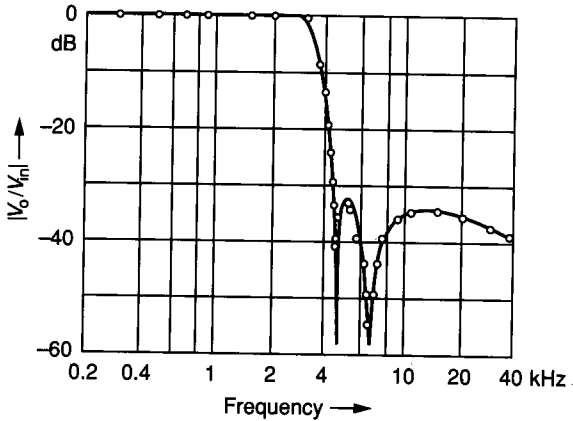


FIGURE 8.5-24

Experimental and theoretical frequency response of the filter of Fig. 8.5-23: \circ = experiment, — = theory.

The success of switched capacitor filters has created the demand for increased performance in the area of dynamic range and frequency. The influence of the feedthrough of the switches has been found to be a serious factor in limiting dynamic range. Besides using small switches and other methods previously discussed to reduce feedthrough, it is important to keep the summing nodes of switched capacitor circuits physically away from the clock lines. In fact, any analog input line should be isolated from lines that carry digital signals. Another factor limiting the dynamic range is noise. The noise can come from the op amp or from switched capacitors (kT/C noise). Of particular concern is the folding of high-frequency noise into the baseband of the switched capacitor circuit.

The frequency limits of switched capacitor circuits are primarily due to the op amp frequency limitations. Design methods exist that allow the signal bandwidth to approach half the sampling frequency. One of the benefits of these methods is that the capacitor ratios are reduced and the area required for capacitors is minimum. The finite gain bandwidth of the op amp will cause the actual switched capacitor filter performance to deviate from the desired performance.

Careful layout, the use of high-frequency op amps, and a fully differential signal path have resulted in switched capacitor filters with very good dynamic range and with high-frequency performance. Of the three approaches presented, the RLC ladder approach using fully differential integrators or the cascaded biquad are typically used. The designer generally tries to minimize the area and power dissipation in addition to achieving the filter performance requirements.

Switched capacitor techniques are also useful for nonfilter applications. Many of the circuits covered in the next section can be implemented using switched capacitor circuit methods. The full application of switched capacitor circuit techniques has yet to be investigated with respect to analog signal processing circuits.

8.6 ANALOG SIGNAL PROCESSING CIRCUITS

One of the largest areas of application of analog signal processing circuits is filtering. This has been the subject of the last two sections. In this section, we consider nonfilter applications of analog signal processing circuits. These applications include precision breakpoint circuits, multipliers and modulators, oscillators, and phase-locked loops. Many other circuits and systems could be included, but these are representative of the concepts and principles.

8.6.1 Precision Breakpoint Circuits

In many applications it is necessary to realize a voltage transfer characteristic similar to those given in Fig. 8.6-1. In these transfer characteristics, the breakpoint is the point where two straight-line segments join, which is at the origin for each

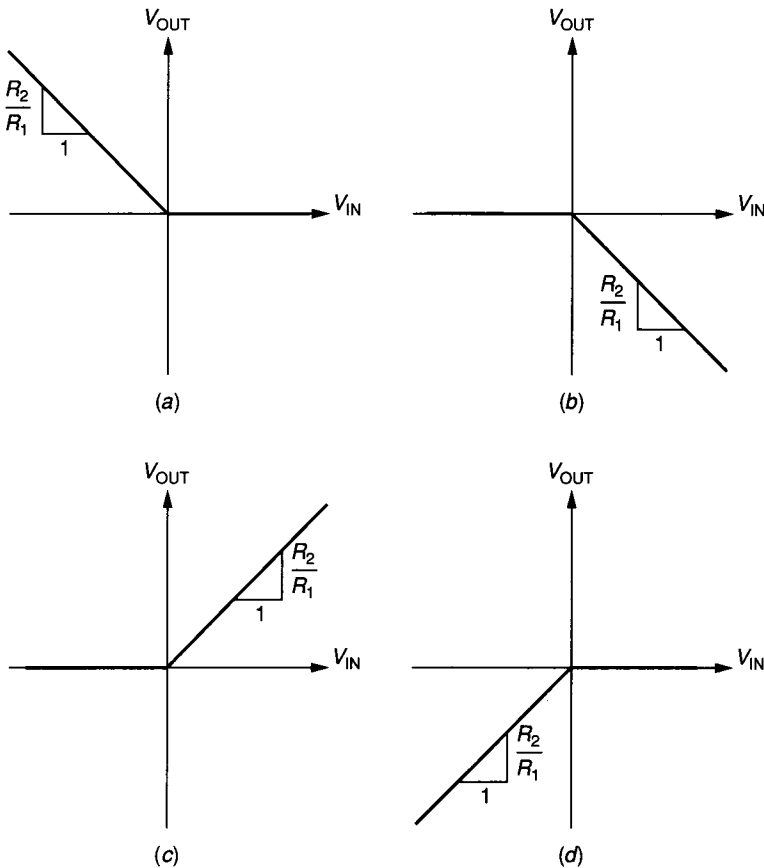


FIGURE 8.6-1

Four possible types of nonlinear voltage transfer characteristics having the breakpoint at $V_{IN} = 0$.

of these cases. If the technology used can implement a diode, a resistor, and an op amp, then Fig. 8.6-2 shows a realization of each of the respective voltage transfer characteristics of Fig. 8.6-1. The slopes of the realizations will be determined by the ratio of R_2 and R_1 . Because the diodes are in the feedback path, they behave as ideal diodes. This permits the drain-gate connected MOSFET to function in place of the diodes in Fig. 8.6-2.

In every diode circuit, it is necessary to first find the breakpoints of the circuits related to either the input or output variable. In Fig. 8.6-2, the current

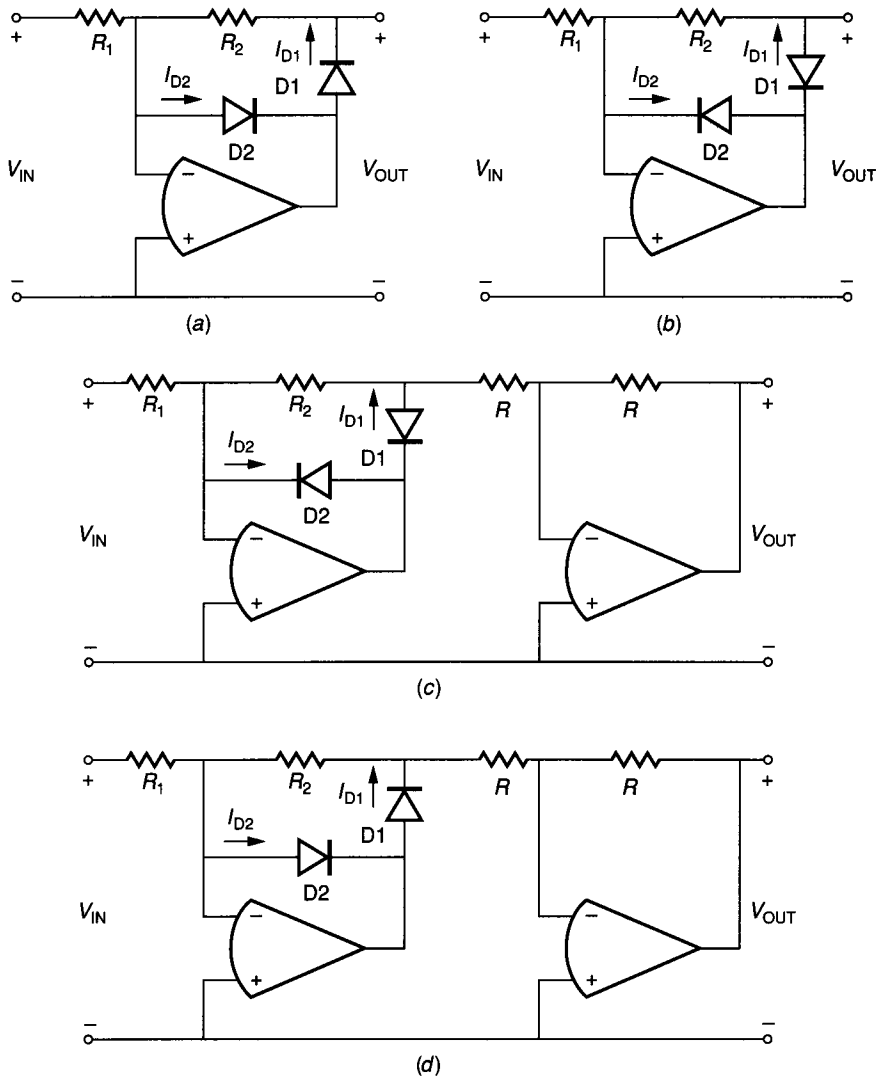


FIGURE 8.6-2 Realizations of the characteristics of Fig. 8.6-1: (a) Fig. 8.6-1a with slope $-R_2/R_1$, (b) Fig. 8.6-1b with slope $-R_2/R_1$, (c) Fig. 8.6-1c with slope R_2/R_1 , (d) Fig. 8.6-1d with slope R_2/R_1 .

flow in or out of the op amp can flow only through D1 or D2 but not both at the same time. Therefore, the only possible states of D1 and D2 are D1 on–D2 off or D1 off–D2 on. The breakpoint in the circuits of Fig. 8.6-2 will occur when both diode currents are zero. The direction of I_{D1} and I_{D2} is not important because they will be equated to zero to find the breakpoint. For example, consider Fig. 8.6-2a. The currents I_{D1} and I_{D2} can be expressed as

$$I_{D1} = \frac{V_{IN}}{R_1} + \frac{V_{OUT}}{R_2} \quad I_{D2} = \frac{V_{OUT}}{R_2} \quad (8.6-1)$$

Setting I_{D1} and I_{D2} to zero gives the breakpoints as $V_{OUT(BP)} = 0$ and $V_{IN(BP)} = 0$.

In many cases, the breakpoint is to be shifted away from zero. This can be accomplished for the circuit of Fig. 8.6-2b as illustrated in Fig. 8.6-3a. A dc voltage, E_r , has been connected to the inverting input through a resistor, R_3 . Using the principles just explained, we solve for I_{D1} and I_{D2} as

$$I_{D1} = \frac{V_{IN}}{R_1} + \frac{E_r}{R_3} + \frac{V_{OUT}}{R_2} \quad I_{D2} = \frac{V_{OUT}}{R_2} \quad (8.6-2)$$

Setting I_{D1} and I_{D2} to zero in Eq. 8.6-2 gives the breakpoint as

$$V_{IN(BP)} = -\frac{E_r R_1}{R_3} \quad V_{OUT(BP)} = 0 \quad (8.6-3)$$

Figure 8.6-3b shows the voltage transfer characteristics of the circuit of Fig. 8.6-3a.

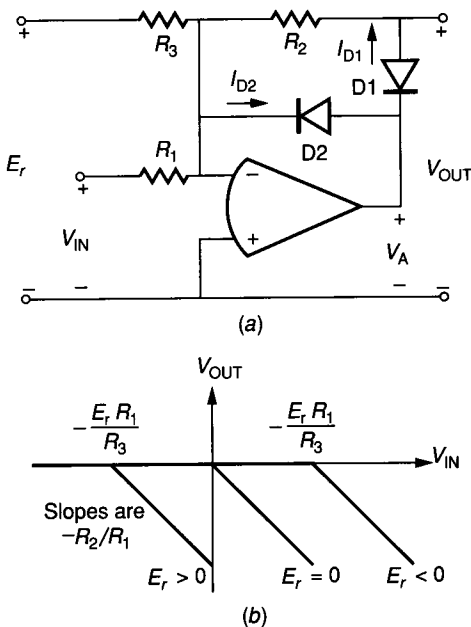


FIGURE 8.6-3
 (a) Method of shifting the breakpoint of Fig. 8.6-1b, (b) Transfer characteristics of (a).

Mathematically, we may express the output voltage of Fig. 8.6-3a as

$$V_{OUT} = \begin{cases} -R_2 v_{IN}/R_1 + R_2 E_r/R_1 & V_{IN} \geq -R_1 E_r/R_3 \\ 0 & V_{IN} < -R_1 E_r/R_3 \end{cases} \quad (8.6-4)$$

We note that E_R can be positive or negative, which will shift the breakpoint to the left or right, respectively. The same principle can be applied to the other circuits of Fig. 8.6-2 to develop a general capability of establishing a breakpoint at any value of V_{IN} .

These concepts can be extended to synthesize a voltage transfer function by using piecewise linear segments. Figure 8.6-4a shows a number of circuits similar to the circuit of Fig. 8.6-3a summed into a summing amplifier. The resulting

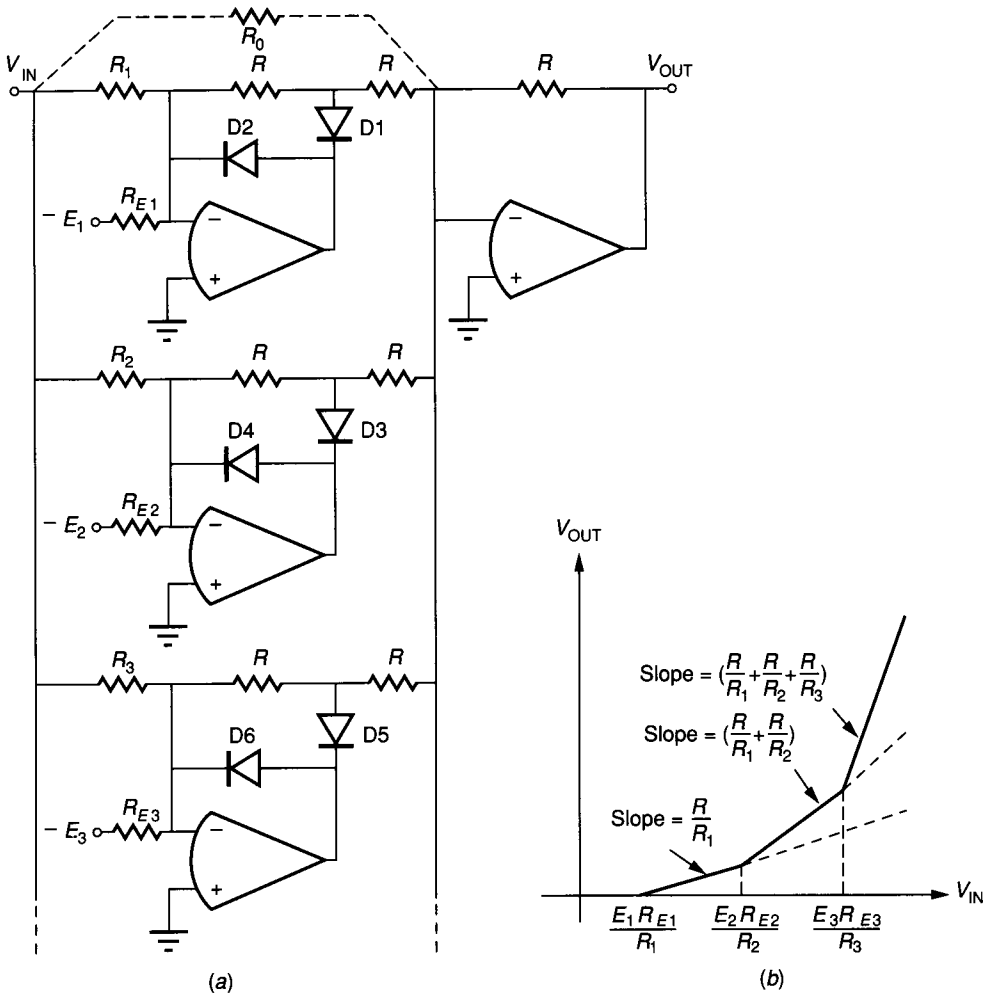


FIGURE 8.6-4 (a) Summation of individual segments to form a piecewise linear approximation, (b) Voltage transfer characteristics of (a).

transfer characteristic is shown in Fig. 8.6-4b. Each of the individual outputs implements one line segment. We note that all E_i s can be identical, and the R_{E_i} resistors can be used to design the breakpoints. On the other hand, all R_{E_i} s can be identical and the E_i voltage sources used to design the breakpoints. The slopes of the line segments become increasingly larger and are indicated on the curve. If the diodes are all reversed and the polarities of E_i changed, the piecewise linear curve moves to the third quadrant. R_0 shown in Fig. 8.6-4a can be added to allow a line segment with a nonzero slope to go through the origin of Fig. 8.6-4b.

The curve of Fig. 8.6-4b is monotonically increasing in slope. If the slope is to decrease, then one could place an inverter in with each breakpoint circuit of Fig. 8.6-4a before summing its output. All possible monotonically increasing and decreasing slopes are realizable in any of the four quadrants using these ideas.

Although the diodes and op amps of the above circuits can easily be implemented in BJT or MOS technology, the resistors are not practical. Resistors are not sufficiently accurate for most applications and require too much area. A method of eliminating the resistors in MOS technology using switched capacitor methods will be presented next.

Consider the switched capacitor implementation of a noninverting amplifier shown in Fig. 8.6-5. This circuit is similar to the noninverting stray-insensitive integrator of Fig. 8.5-11 except for the switch added to discharge C_2 during the ϕ_1 phase. This switch essentially removes the memory of the integrator, resulting in an amplifier. It can be shown that the z -domain transfer function of the circuit of Fig. 8.6-5 is

$$H^{oe}(z) = \frac{V_{OUT}(z)}{V_{IN}(z)} = \frac{C_1}{C_2} z^{-1/2} \quad (8.6-5)$$

Equation 8.6-5 represents a noninverting gain function that is valid during the ϕ_2 phase and is delayed by a half clock period from the input. A sample and hold circuit can be added to hold the output for the entire clock period. If the output is sampled and held, then Eq. 8.6-5 is multiplied by $z^{-1/2}$ to get a full delay of $H^{oo}(z)$. One of the disadvantages of the circuit of Fig. 8.6-5 is that the op amp output is slewed to zero during each ϕ_1 phase and back to the desired output during each ϕ_2 phase. This is unnecessary and can be prevented by the introduction of more capacitors and switches as will be shown later.

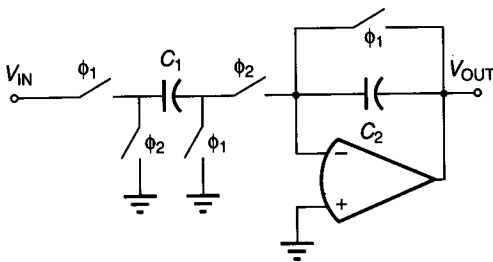


FIGURE 8.6-5
Noninverting switched capacitor amplifier realization.

If the leftmost pair of switches has the phasing reversed, then the amplifier is inverting, and the transfer function is given as

$$H(z) = \frac{V_{OUT}(z)}{V_{IN}(z)} = -\frac{C_1}{C_2} \tag{8.6-6}$$

where the output is valid only at the ϕ_2 phase. If we assume that the high sampling approximation is valid, then Fig. 8.6-5 can be considered as a simple noninverting or inverting amplifier depending upon the phasing of the leftmost switch pair.

The voltage transfer characteristics of Fig. 8.6-1 can be realized using MOS technology if we combine a comparator with the amplifier of Fig. 8.6-5, as shown in Fig. 8.6-6a. Note that the comparator output controls the switch that couples C_1 into the inverting input of the op amp (called the transfer switch). If this switch is open during the ϕ_2 phase period, the output of the op amp will be zero. If the transfer switch is closed during the ϕ_2 phase period, the output will be given by Eq. 8.6-5 or 8.6-6, depending on the phasing of the leftmost switch pair. To see how the circuit works, consider the circuit of Fig. 8.6-6a with a positive value of V_{IN} . The comparator output will be high, causing the transfer switch to be closed. Thus, the output is given by Eq. 8.6-5. If V_{IN} is less than zero, the comparator output is low, causing the transfer switch to be open. Therefore, the circuit of Fig. 8.6-6a realizes the voltage transfer curve of Fig. 8.6-1c with outputs valid during the ϕ_2 clock phase. If the comparator inputs are reversed, Fig. 8.6-6a realizes the voltage transfer curve of Fig. 8.6-1d. If the phases of the leftmost switches (input switches) are reversed, the circuit of Fig. 8.6-6b results. With the inputs to the comparator as shown, this circuit realizes the voltage transfer curve of Fig. 8.6-1b. If the comparator inputs are reversed, the voltage transfer curve of Fig. 8.6-1a is realized.

The switched capacitor breakpoint realizations can be implemented by alternate configurations, but all will utilize a comparator controlling one or more switches. It is easy to shift the breakpoint of the realization by connecting the

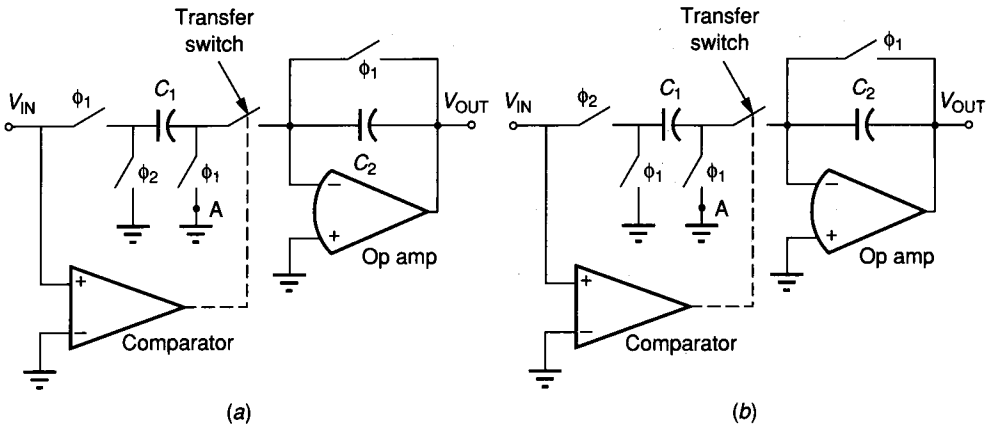


FIGURE 8.6-6
 (a) Switched capacitor realization of Fig. 8.6-1c, (b) Switched capacitor realization of Fig. 8.6-1b.

grounded input terminal of the comparators of Fig. 8.6-6a and b to the voltage E_r . It is also necessary to remove point A from ground and connect it to the voltage E_r . A positive value of E_r applied to the inverting input of the comparator of Fig. 8.6-6a will cause the breakpoint to occur at $V_{IN} = E_r$. The outputs of several shifted breakpoint realizations can be summed in a manner similar to Fig. 8.6-4 to obtain a piecewise linear approximation of a voltage transfer function.⁵¹ The switched capacitor realizations of the precision breakpoint circuits are compatible with MOS technology and have been employed in many commercial applications.

8.6.2 Modulators and Multipliers

Modulators include a class of circuits with multiple inputs where one input can modify or control the signal flow from the other input to the output. Figure 8.6-7 illustrates the modulator on a block diagram basis. $V_1(t)$ and $V_2(t)$ are input signals. The modulator output signal can be expressed in general as

$$V_{OUT}(t) = f_A[V_1(t)]f_B[V_2(t)] \quad (8.6-7)$$

where f_A and f_B are two arbitrary functions of the respective inputs. If $f_A[V_1(t)]$ and $f_B[V_2(t)]$ are linearly dependent upon $V_1(t)$ and $V_2(t)$, respectively, the modulator is called a *multiplier*. Thus, Eq. 8.6-7 becomes

$$V_{OUT}(t) = K_1 V_1(t) V_2(t) \quad (8.6-8)$$

where K_1 is the combination of the individual constants for $V_1(t)$ and $V_2(t)$.

Figure 8.6-8 shows a BJT modulator using the differential amplifier configuration of Fig. 6.4-7 with resistor loads and a current sink implemented by a current mirror. The output voltage can be expressed as

$$V_{OUT} = R_c(I_{C1} - I_{C2}) = \alpha_F I_{EE} R_c \left[\frac{1}{1 + e^{-V_1/V_t}} - \frac{1}{1 + e^{V_1/V_t}} \right] \quad (8.6-9)$$

using Eqs. 6.3-52 and 6.3-53. Equation 8.6-9 can be rewritten as

$$V_{OUT} = \alpha_F I_{EE} R_c \tanh \left(\frac{V_1}{2V_t} \right) \approx I_{EE} R_c \left(\frac{V_1}{2V_t} \right) \quad (8.6-10)$$

if V_1 is much less than 50 mV. Because I_{EE} is equal to $[V_2 - V_{BE(on)}]/R$, we may express Eq. 8.6-10 as

$$V_{OUT} = \frac{R_c}{2V_t R} V_1 \cdot [V_2 - V_{BE(on)}] = K_1 V_1 [V_2 - V_{BE(on)}] \quad (8.6-11)$$

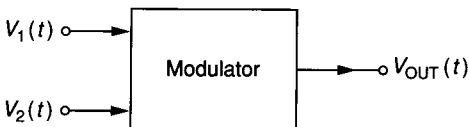


FIGURE 8.6-7
Block diagram for a modulator.

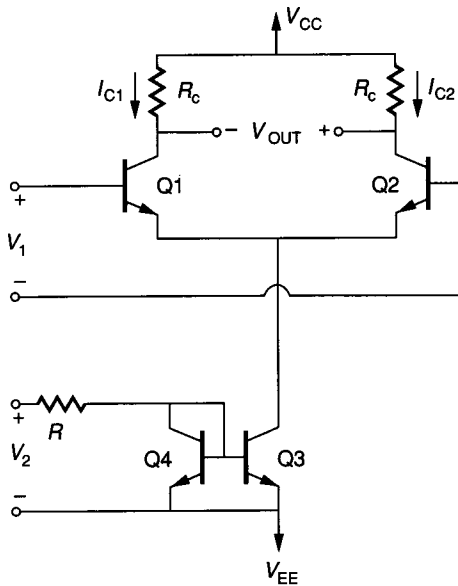


FIGURE 8.6-8
A simple BJT modulator using a differential amplifier.

The multiplier of Fig. 8.6-8 has several problems. The first is that V_2 is offset by $V_{BE(on)}$. The second is that V_2 must always be positive, resulting in a two-quadrant multiplier. A third problem is that the dynamic range is limited because of the approximation necessary to replace $\tanh x$ by x where $x = V_1/2V_t$ in Eq. 8.6-10.

The first two problems can be solved by the Gilbert cell⁵² shown in Fig. 8.6-9. The Gilbert cell allows four-quadrant operation and is the basis for most integrated circuit balanced multipliers. The operation of this key cell is as follows. The collector currents of Q3 and Q4 are

$$I_{C3} = \frac{I_{C1}}{1 + \exp(-V_1/V_t)} \tag{8.6-12}$$

and

$$I_{C4} = \frac{I_{C1}}{1 + \exp(V_1/V_t)} \tag{8.6-13}$$

Similarly the collector currents for Q5 and Q6 are

$$I_{C5} = \frac{I_{C2}}{1 + \exp(V_1/V_t)} \tag{8.6-14}$$

and

$$I_{C6} = \frac{I_{C2}}{1 + \exp(-V_1/V_t)} \tag{8.6-15}$$

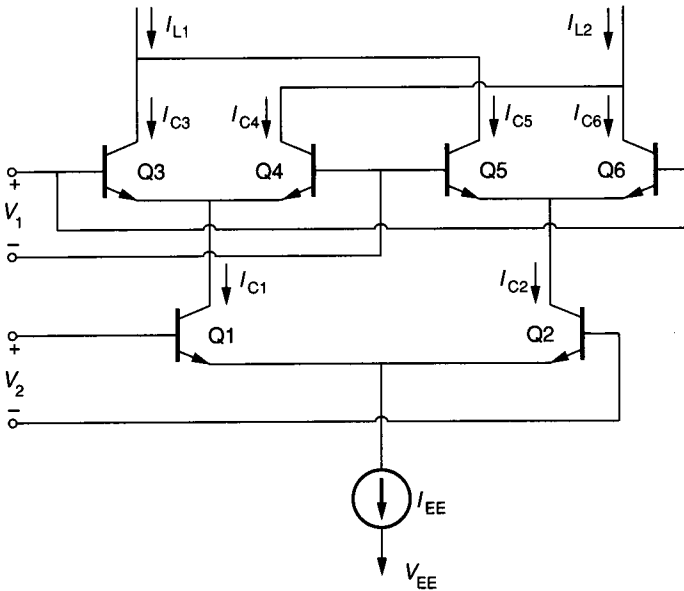


FIGURE 8.6-9
The Gilbert multiplier cell.

The two collector currents I_{C1} and I_{C2} can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + \exp(-V_2/V_t)} \quad (8.6-16)$$

and

$$I_{C2} = \frac{I_{EE}}{1 + \exp(V_2/V_t)} \quad (8.6-17)$$

Substituting Eqs. 8.6-16 and 8.6-17 into Eqs. 8.6-12 through 8.6-15 results in

$$I_{C3} = \frac{I_{EE}}{[1 + \exp(-V_1/V_t)][1 + \exp(-V_2/V_t)]} \quad (8.6-18)$$

$$I_{C4} = \frac{I_{EE}}{[1 + \exp(V_1/V_t)][1 + \exp(-V_2/V_t)]} \quad (8.6-19)$$

$$I_{C5} = \frac{I_{EE}}{[1 + \exp(V_1/V_t)][1 + \exp(V_2/V_t)]} \quad (8.6-20)$$

and

$$I_{C6} = \frac{I_{EE}}{[1 + \exp(-V_1/V_t)][1 + \exp(V_2/V_t)]} \quad (8.6-21)$$

Next we define the differential output current, ΔI , as

$$\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6}) = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5}) \quad (8.6-22)$$

Substituting Eqs. 8.6-18 through 8.6-21 into Eq. 8.6-22 and using the exponential formulae for hyperbolic functions results in the differential output current being expressed as

$$\Delta I = I_{EE} \left[\tanh \left(\frac{V_1}{2V_t} \right) \right] \left[\tanh \left(\frac{V_2}{2V_t} \right) \right] \quad (8.6-23)$$

If the input signals V_1 and V_2 are small enough, the Gilbert cell of Fig. 8.6-9 functions as a four-quadrant analog multiplier. The output voltage, V_{OUT} , can be generated from ΔI by using two equal-valued resistors connected to V_{CC} with current $I_{L1}(=I_{C3} + I_{C5})$ flowing through one and current $I_{L2}(=I_{C4} + I_{C6})$ flowing through the other.

The circuit of Fig. 8.6-9 can be used as a modulator when one of the inputs is very large and the other sufficiently small so that $\tanh x$ is approximately equal to x . The large input will cause the transistors to which it is applied to act like switches. This effectively multiplies the small signal by a square wave. Such modulators are called *synchronous modulators* and have many applications in signal processing, including demodulation and phase detection. The amplitude range of V_2 can be extended considerably by placing resistors between the emitters and the I_{EE} current source of the Gilbert cell.

The amplitude constraints on the inputs of the Gilbert cell can be removed using a predistortion technique that results in a linear relationship between V_1 and V_{OUT} and V_2 and V_{OUT} . Figure 8.6-10 illustrates the complete four-quadrant multiplier. The three boxes, which are voltage-to-current converters or current-to-voltage converters, will be considered shortly. The predistortion is implemented by the emitters of Q7 and Q8. The currents I_9 and I_{10} create a voltage between the emitters of Q7 and Q8 that is proportional to the inverse hyperbolic tangent of V_1 . This will remove the hyperbolic tangent expressions in Eq. 8.6-23.

The analysis of the circuit of Fig. 8.6-10 can be accomplished as follows. It can be shown that the currents through base-emitter junctions that are connected in series, such as Q7, Q3, Q4, and Q8, can be expressed as

$$I_9 I_3 = I_4 I_{10} \quad (8.6-24)$$

where $I_7 = I_9$ and $I_8 = I_{10}$. Similarly, for the series connection of Q7, Q6, Q5, and Q8, we have

$$I_9 I_6 = I_5 I_{10} \quad (8.6-25)$$

Next we note that

$$I_1 = I_3 + I_4 \quad (8.6-26)$$

$$I_2 = I_5 + I_6 \quad (8.6-27)$$

$$I_{L1} = I_3 + I_5 \quad (8.6-28)$$

$$I_{L2} = I_4 + I_6 \quad (8.6-29)$$

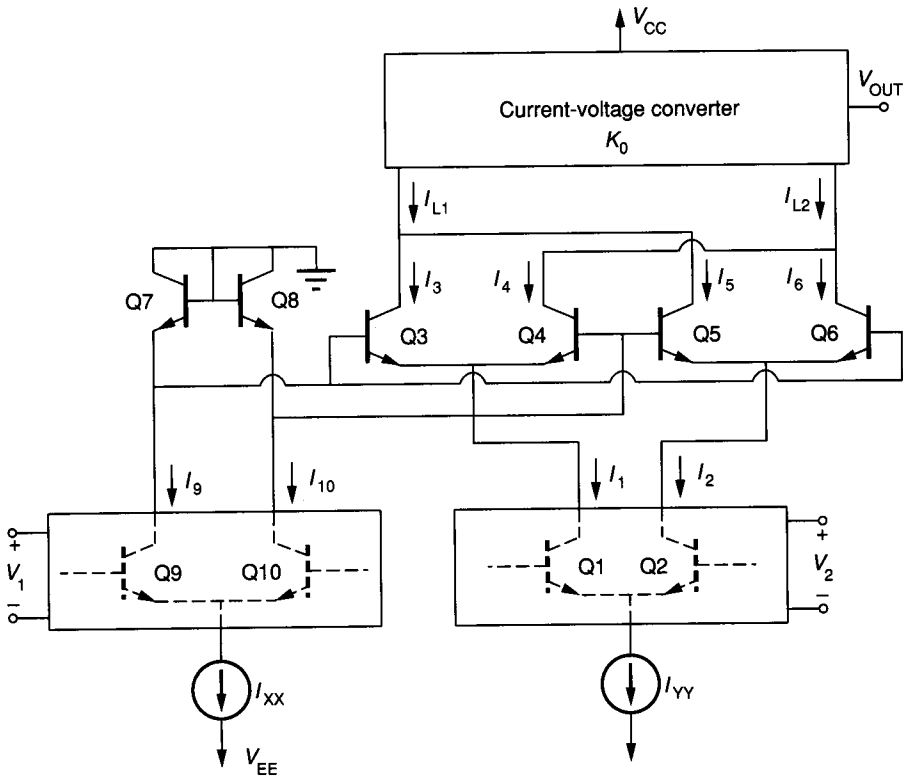


FIGURE 8.6-10
Complete four-quadrant analog multiplier.

and

$$I_{XX} = I_9 + I_{10} \quad (8.6-30)$$

Let us assume that the transfer characteristics of the rectangular blocks of Fig. 8.6-10 are given by

$$I_9 - I_{10} = V_1/K_1 \quad (8.6-31)$$

$$I_1 - I_2 = V_2/K_2 \quad (8.6-32)$$

and

$$V_{OUT} = K_0(I_{L2} - I_{L1}) \quad (8.6-33)$$

where K_0 , K_1 , and K_2 are constants depending on the implementation. Replacing I_{L2} and I_{L1} by Eqs. 8.6-28 and 8.6-29 results in

$$V_{OUT} = K_0[(I_4 + I_6) - (I_3 + I_5)] = K_0 \left[\left(I_4 + I_5 \frac{I_{10}}{I_9} \right) - \left(I_4 \frac{I_{10}}{I_9} + I_5 \right) \right] \quad (8.6-34)$$