Rearranging Eq. 8.6-34 results in

$$V_{OUT} = K_o\left(\frac{I_9 - I_{10}}{I_9}\right)(I_4 - I_5) \tag{8.6-35}$$

We desire to replace $(I_4 - I_5)$ by $(I_1 - I_2)$, which can be accomplished as follows.

$$I_1 - I_2 = (I_3 + I_4) - (I_5 + I_6) = \left(I_4\frac{I_{10}}{I_9} + I_4\right) - \left(I_5 + I_5\frac{I_{10}}{I_9}\right) \tag{8.6-36}$$

Combining terms and solving for $(I_4 - I_5)$ gives

$$(I_4 - I_5) = \left(\frac{I_9}{I_9 + I_{10}}\right)(I_1 - I_2) \tag{8.6-37}$$

Substituting Eq. 8.6-37 into Eq. 8.6-35 provides the desired result.

$$V_{OUT} = K_o\left(\frac{I_9 - I_{10}}{I_9 + I_{10}}\right)(I_1 - I_2) = \frac{K_o V_1 V_2}{I_{XX} K_1 K_2} = K_m V_1 V_2 \tag{8.6-38}$$

where the definitions of Eqs. 8.6-30 through 8.6-32 have been used to obtain Eq. 8.6-38. Because no approximations were used in the derivation of Eq. 8.6-38, the input signal amplitudes are not constrained.

Figure 8.6-11 shows a practical implementation of the four-quadrant analog multiplier of Fig. 8.6-10. It can be seen that

$$I_1 - I_2 = \frac{2V_2}{R_Y} \tag{8.6-39}$$

and

$$I_9 - I_{10} = \frac{2V_1}{R_X} \tag{8.6-40}$$

where it has been assumed that the part of V_1 and V_2 across the base-emitter of $Q9$, $Q10$, and $Q1$, $Q2$ are small compared to the drop across the resistors. Substituting Eqs. 8.6-39 and 8.6-40 into Eq. 8.6-38 results in

$$V_{OUT} = \frac{4K_o R_c V_1 V_2}{I_{XX} R_X R_Y} = K_m V_1 V_2 \tag{8.6-41}$$

where R is much greater than R_c. These concepts have been used to implement high-performance four-quadrant analog multipliers having good performance. One of the problems with the integrated circuit implementation is the need to be able to trim the various errors due to offsets and mismatches.

Four-quadrant multipliers have also been implemented in MOS technology.[53–56] Most of the realizations use a linearized Gilbert cell approach similar to the bipolar implementation above. A somewhat different approach is based on the cascade of two differential amplifier pairs has been found to give good results.[53] The principle of operation is illustrated in Fig. 8.6-12. If we assume

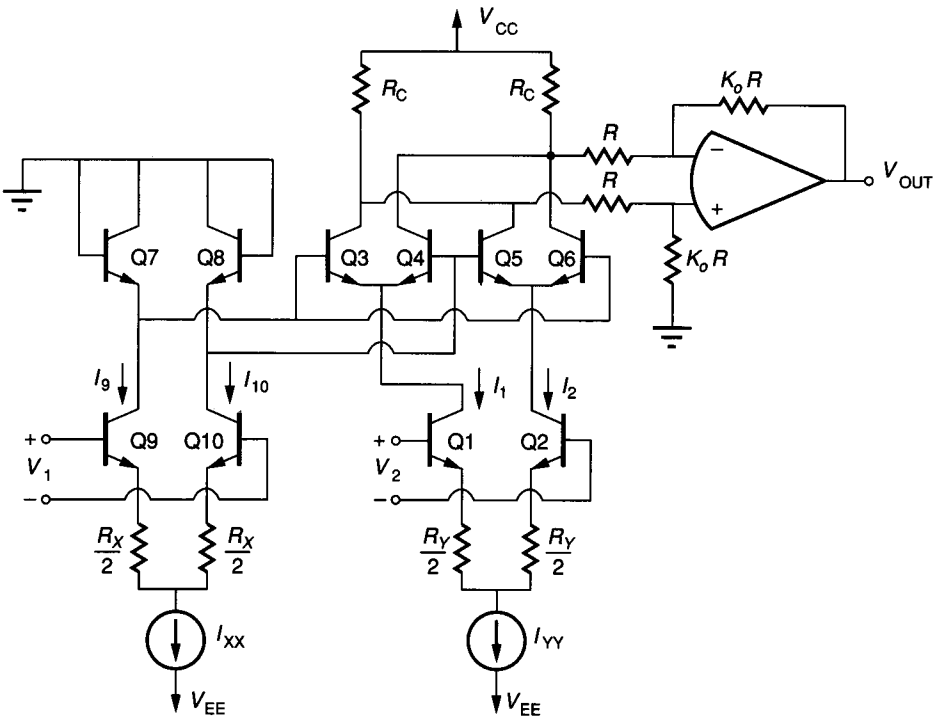


FIGURE 8.6-11
Practical implementation of Fig. 8.6-10.

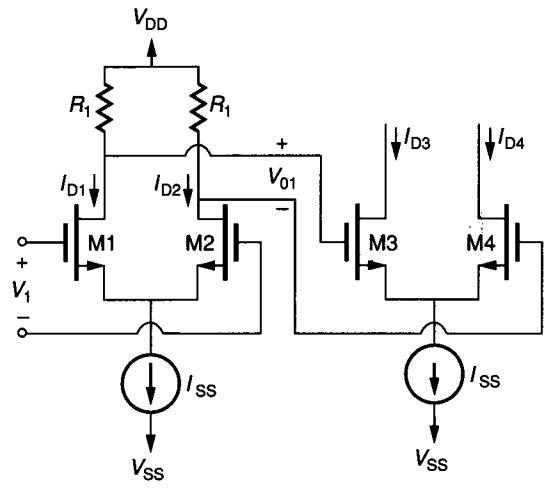


FIGURE 8.6-12
Cascaded MOS differential amplifiers.

that M1 and M2 are in the saturation region, then using Eqs. 6.3-7 and 6.3-8, we may write

$$I_{D1} - I_{D2} = I_{SS}\left[\frac{\beta_1 V_1^2}{I_{SS}} - \frac{\beta_1^2 V_1^4}{4I_{SS}^2}\right]^{1/2} = \beta_1 V_1\left[\frac{I_{SS}}{\beta_1} - \frac{V_1^2}{4}\right]^{1/2} \tag{8.6-42}$$

whre $\beta_1 = KW_1/L1$. It is seen that $I_{D1} - I_{D2}$ depends nonlinearly on V_1 and I_{SS}. Let us define V_{O1} as

$$V_{O1} = -R_1(I_{D1} - I_{D2}) \tag{8.6-43}$$

We can find a similar expression to Eq. 8.6-42 for $I_{D3} - I_{D4}$, which is

$$I_{D3} - I_{D4} = \beta_3 V_{O1}\left[\frac{I_{SS}}{\beta_3} - \frac{V_{O1}^2}{4}\right]^{1/2} \tag{8.6-44}$$

where $\beta_3 = kW_3/L3$. If we restrict V_1 to less than $0.3(I_{SS}/\beta_1)^{1/2}$, then we can approximate Eq. 8.6-42 as

$$I_{D1} - I_{D2} \simeq \beta_1 V_1[I_{SS}/\beta_1]^{1/2} \tag{8.6-45}$$

It has been shown that this assumption results in less than 0.2% total harmonic distortion in $I_{D1} - I_{D2}$. Substituting Eqs. 8.6-43 and 8.6-45 into Eq. 8.6-44 results in

$$I_{D3} - I_{D4} = V_1[-R_1 I_{SS}(\beta_1\beta_3)^{1/2}][1 - (\beta_1\beta_3 R_1^2 V_1^2/4)]^{1/2} \tag{8.6-46}$$

It is seen that $I_{D3} - I_{D4}$ depends linearly on I_{SS}. However, there is still a nonlinear dependence upon V_1. This dependence could be removed by restricting the amplitude of $I_{D3} - I_{D4}$. An alternative approach is to use the predistortion circuit of Fig. 8.6-13. In this circuit, V_1 is created by the difference in two currents, $I_{X1} - I_{X2}$. This difference, designated as I_X, can be expressed as

$$I_X = I_{X1} - I_{X2} = V_1(I_{DX}\beta_5)^{1/2}[1 - (\beta_5/4I_{DX})V_1^2]^{1/2} \tag{8.6-47}$$

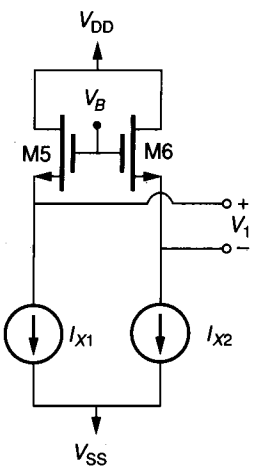


FIGURE 8.6-13
Predistortion circuit for the cascade MOS differential multiplier of Fig. 8.6-12.

where $I_{DX} = I_{X1} + I_{X2}$. Since the bracketed terms of Eqs. 8.6-46 and 8.6-47 have the same form, we can achieve predistortion by equating these two terms to get

$$\beta_5 = \beta_1\beta_3 R_1^2 I_{DX} \tag{8.6-48}$$

Therefore, Eq. 8.6-46 can be reduced to

$$I_O = I_{D3} - I_{D4} = -R_1\left[\frac{\beta_1\beta_3}{I_{DX}\beta_5}\right]^{1/2} I_{SS} I_X \tag{8.6-49}$$

Equation 8.6-49 is the form of an ideal current multiplier. I_{SS} and I_X will be generated by voltage-to-differential current amplifiers, and the output voltage will be derived from I_O.

In order to get four-quadrant operation, I_{SS} must be able to be negative. This can be accomplished by taking the difference of two of the preceding circuits. The resulting MOS realization using only n-channel transistors is shown in Fig. 8.6-14. Several practical modifications can be made to improve the performance of the multiplier with regard to temperature and linearity. This MOS four-quadrant analog multiplier is capable of linearity better than 0.3% at 75% of full scale. It has a bandwidth of dc to 1.5 MHz and an output noise 77 dB below full scale.

Other techniques exist that allow the implementation of multipliers compatible with CMOS technology. A straightforward approach using an A/D and a D/A converter is shown in Fig. 8.6-15. The input to the A/D converter is one of the multiplier inputs designated as V_1. The reference voltage for an n-bit, A/D converter is provided by another analog input, V_2, to the multiplier. The digital output word of the A/D converter is given as

$$D = \frac{V_1}{V_2} = b_1 2^{-1} + b_2 b^{-2} + \cdots + b_{n-1}2^{-n+1} + b_n 2^{-n} \tag{8.6-50}$$

where D is digital word for the value of V_1 scaled by V_2. This digital word is then applied to an n-bit, D/A converter that has an analog input, V_3, applied as its reference voltage. The analog output of the D/A converter is given as

$$V_O = DV_3 = b_1 2^{-2} + b_2 2^{-2} + \cdots + b_{n-1}2^{n-1} + b_n 2^{-n} \tag{8.6-51}$$

Substituting Eq. 8.6-50 into Eq. 8.6-51 results in the following multiplier/divider with n-bit resolution.

$$V_O = \frac{V_1 V_3}{V_2} \tag{8.6-52}$$

Any of the D/A and A/D converters of Sec. 8.2 and 8.3 can be used to implement a multiplier by this principle.

In the preceding results, we notice that the V_2 input of Fig. 8.6-15 is a dividing input. Obviously, V_2 cannot be zero. Another method of implementing a divider circuit is shown in Fig. 8.6-16. Figure 8.6-16*a* shows the block diagram

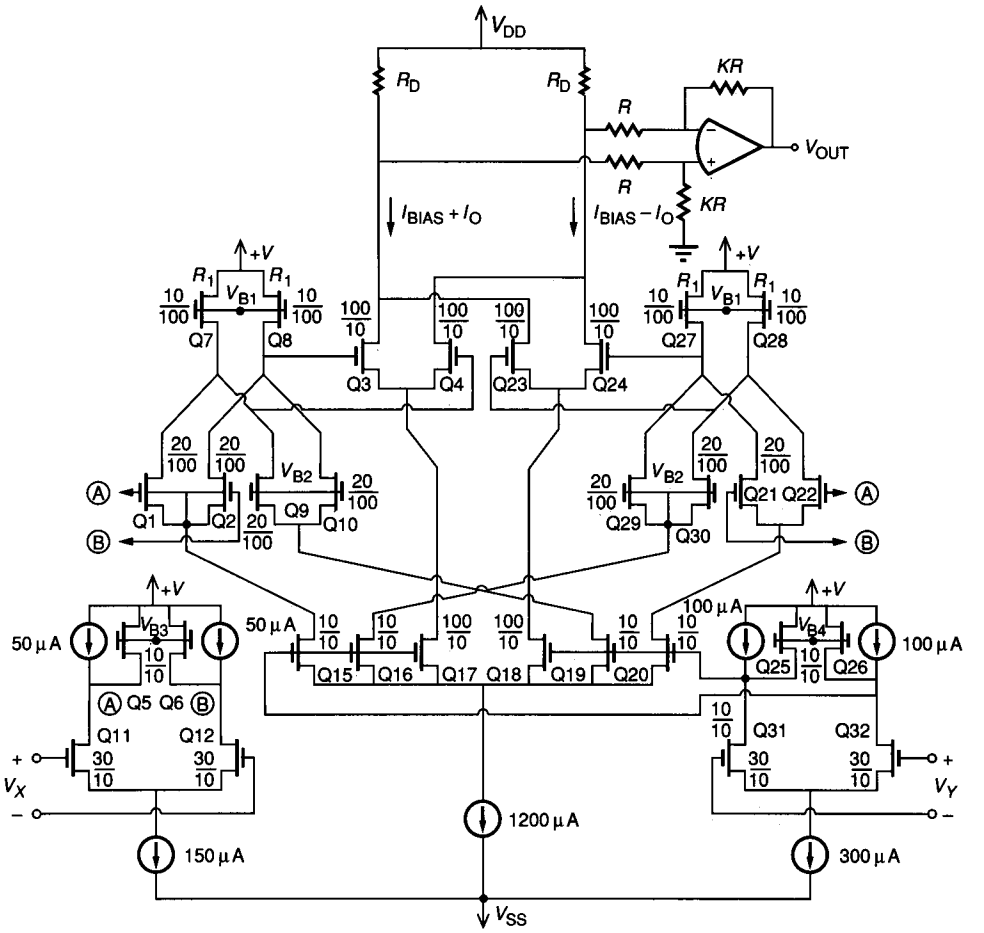


FIGURE 8.6-14
MOS four-quadrant analog current multiplier simplified schematic (values shown are W/L in microns/microns).

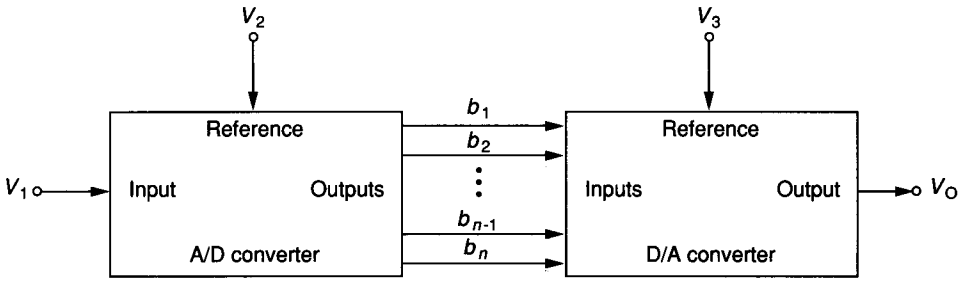


FIGURE 8.6-15
A/D–D/A converter analog multiplier.

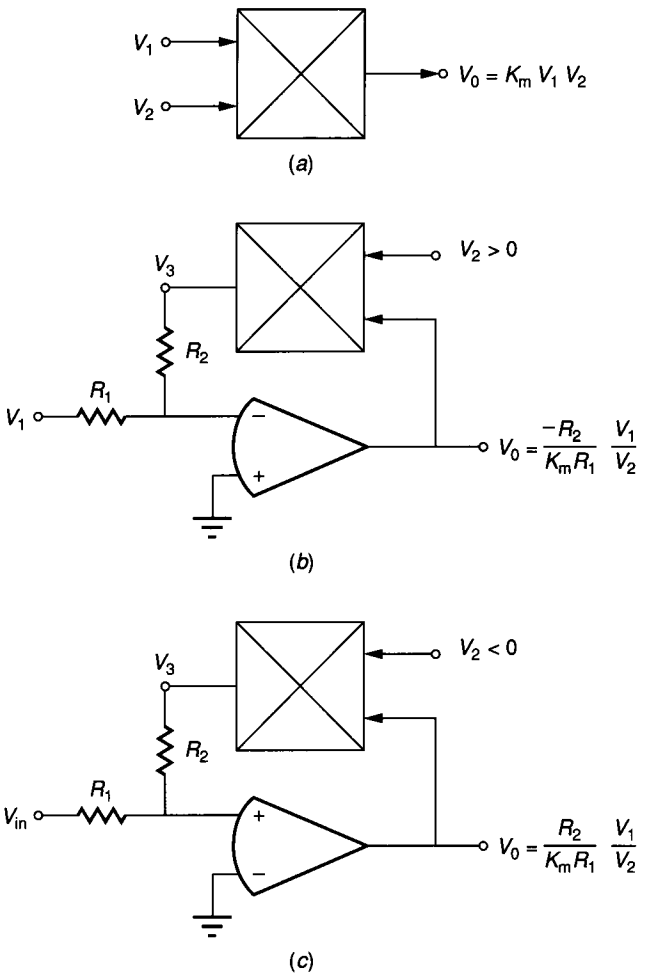


FIGURE 8.6-16
a) Block diagram symbol for a multiplier, (*b*) Negative divider, (*c*) Positive divider.

symbol for a multiplier. If the multiplier is placed in the feedback path of an inverting amplifier, as shown in Fig. 8.6-16*b*, then the output can be written as

$$V_O = \frac{-R_1}{K_m R_2}\left(\frac{V_1}{V_2}\right) \tag{8.6-53}$$

where $V_2 > 0$. If $V_2 < 0$ and the input terminals of the op amp are reversed, as indicated in Fig. 8.6-16*c*, a positive divider circuit is obtained. The phase margin of the op amp in Fig. 8.6-16 will be reduced because of the presence of the multiplier in the feedback path.

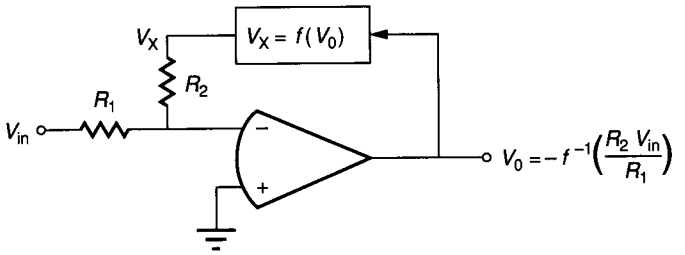


FIGURE 8.6-17
Illustration of the principle of creating the inverse function.

The principle used to develop the dividers of Fig. 8.6-16 can be generalized. This principle, illustrated in Fig. 8.6-17, is that if a functional block is placed in the feedback path of a circuit, the closed-loop response is the inverse of that function. In the previous case, division is the inverse of multiplication. If a circuit that generates the sine of an input is placed in the feedback path, the closed-loop transfer characteristic would be the inverse sine of the input.

A simple modulator compatible with MOS technology is shown in Fig. 8.6-18. If V_2 is greater than zero, then switches S2 and S3 are on and switches S1 and S4 are off. We see that the amplifier of Fig. 8.6-5 results, with the

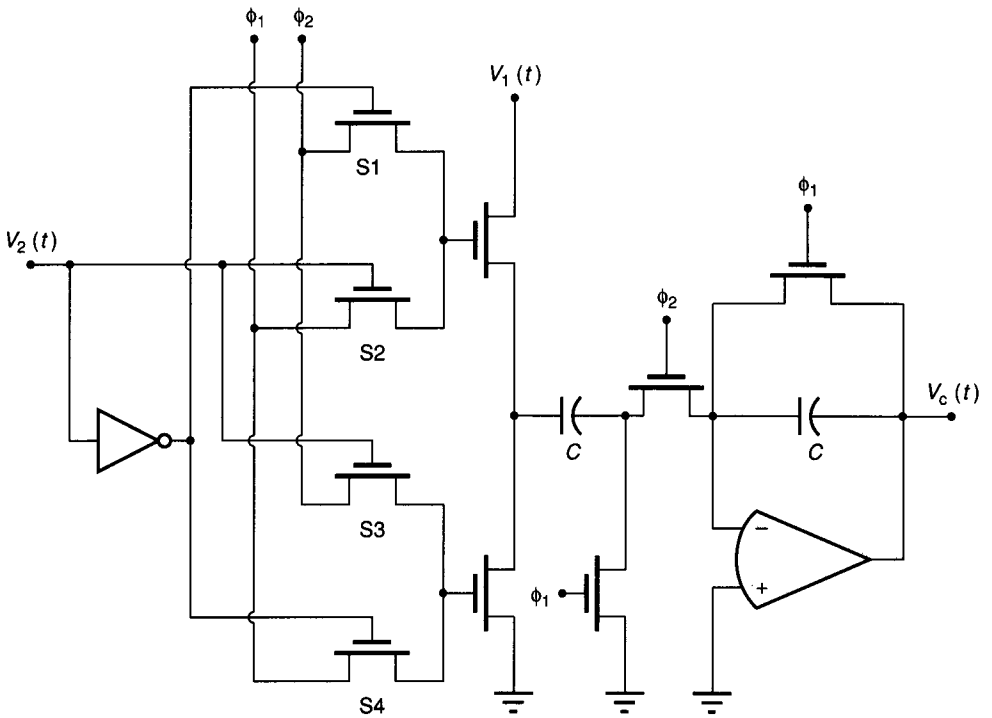


FIGURE 8.6-18
A modulator compatible with MOS technology.

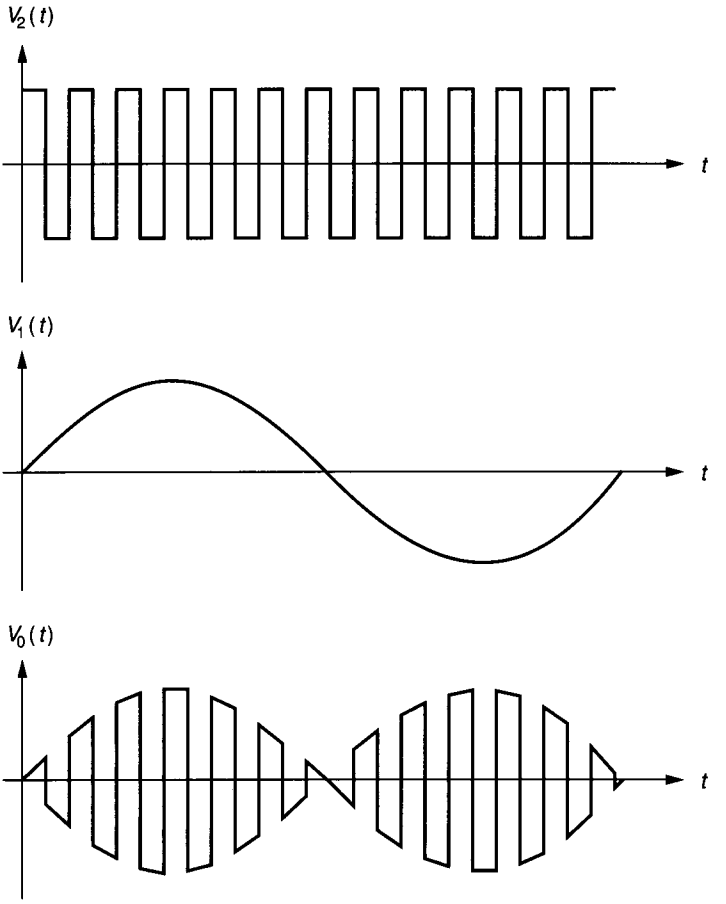


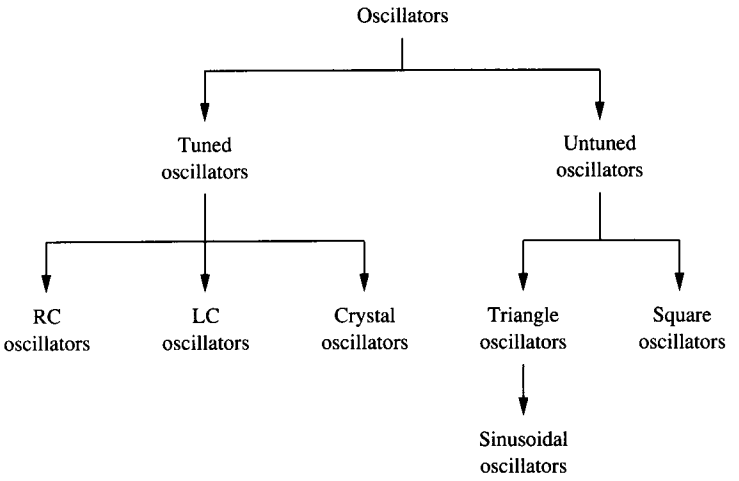
FIGURE 8.6-19
Illustration of the waveforms of Fig. 8.6-18 used as a modulator.

corresponding transfer function of Eq. 8.6-5. If V_2 is less than zero, then switches S1 and S4 are on and switches S2 and S3 are off. The phasing is reversed on the input switches, resulting in the inverting transfer function of Eq. 8.6-6. If the output is sampled and held, or if the high sampling approximation is valid, the effect of V_2 is to multiply V_1 by $+1$ when $V_2 > 0$ and by -1 when $V_2 < 0$. Figure 8.6-19 shows the waveforms of the modulator of Fig. 8.6-18 when V_1 is a sinusoid and V_2 is a square wave whose frequency is greater than that of the sinusoid but much less than the clock frequency of ϕ_1 and ϕ_2.

8.6.3 Oscillators

Oscillators are circuits that convert dc power into a periodic waveform or signal. Oscillators can be classified as shown in Table 8.6-1. The two general classes are tuned and untuned oscillators. Tuned oscillators produce nearly sinusoidal

TABLE 8.6-1
Classification of oscillators



outputs, whereas untuned oscillators produce square and/or triangle waveforms. Tuned oscillators can be further divided into RC, LC, and crystal oscillators. We shall only consider RC oscillators since these are most suitable for integrated circuit technology, although crystal oscillators are often employed with the crystal external to the integrated circuit. The outputs of the untuned oscillator are typically square waves and triangle waves. The untuned oscillator can create a sinusoid by applying the triangle wave to a sine-shaping circuit, such as the one considered in Prob. 8.40 or one made up from a sufficient number of piecewise linear line segments. The untuned oscillators are compatible with integrated circuit technology, which in part accounts for their widespread use. They are also capable of implementing a voltage-controlled oscillator (VCO), which has many uses in signal processing circuits. Due to lack of space, the considerations of oscillators will be limited. Much more information can be found in the references.[57–61]

The following discussion will consider both tuned and untuned oscillators. The principles of operation and an example will be given. Only oscillators that use op amps, capacitors, and resistors or resistor equivalents will be considered. Figure 8.6-20 shows a block diagram of a single-loop feedback system. This diagram consists of an amplifier (A), a feedback network (β), and a summing junction. The variables shown are V_S, V_F, V_I, and V_O which are the source, feedback, input, and output voltages, respectively. The + sign next to the feedback input to the summing junction indicates that the feedback is positive. If the circuit of Fig. 8.6-20 is assumed to be linear, the *loop gain*, G, is the voltage gain around the loop when $V_S = 0$ and is expressed as

$$G\big|_{V_S=0} = A\beta \tag{8.6-54}$$

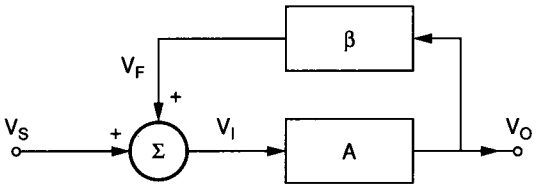


FIGURE 8.6-20
Block diagram of a single-loop feedback system.

The *closed-loop gain*, A_f, is equal to V_O/V_S and is given as

$$A_f = \frac{V_O}{V_S} = \frac{A}{1 - A\beta} = \frac{A}{1 - G} \tag{8.6-55}$$

The principle of a tuned oscillator can be seen from Eq. 8.6-55. If there is no input, $V_S = 0$, then for a finite output, V_O, Eq. 8.6-55 must be equal to infinity. This can only happen if $G = 1$. Thus, the criterion for oscillation in a tuned oscillator is

$$\text{Loop gain} = G(j\omega_0) = A(j\omega_0)\beta(j\omega_0) = 1 \tag{8.6-56}$$

where ω_0 is called the *radian frequency of oscillation*. An alternative form of Eq. 8.6-56 is

$$\text{Re}\,[G(j\omega_0)] + j\,\text{Im}\,[G(j\omega_0)] = 1 + j\,0 \tag{8.6-57}$$

or

$$|\,G(j\omega_0)\,|\,\angle\text{Arg}\,[G(j\omega_0)] = 1\angle 0° \tag{8.6-58}$$

In order to satisfy this criterion, the oscillator must be able to achieve a phase shift of 360° at some frequency, ω_0, where the loop gain is exactly unity. The analysis of oscillators is simple and consists of calculating the loop gain and using Eq. 8.6-56, 8.6-57, or 8.6-58 to find the frequency of oscillation, ω_0, and the magnitude of the amplifier gain, A, necessary for oscillation. Figure 8.6-21*a* shows an *RC* oscillator called the *Wien bridge oscillator*. This oscillator consists of an amplifier, whose gain is K, and a feedback network consisting of R_1, C_1, R_2, and C_2. Figure 8.6-21*b* shows how to open the feedback loop in order to calculate the loop gain, G. The key principle in opening the feedback loop is to do so at a point in the loop where the resistance looking forward in the loop is much greater than the resistance looking backward in the loop. In this case, the op amp in the noninverting configuration offers infinite resistance looking into the noninverting terminal. Note that the loop could also be broken at point A because resistance looking back into the op amp with negative feedback approaches zero. Assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the loop gain can be written as

$$G(s) = \frac{K(s/RC)}{s^2 + (3/RC)s + (1/RC)^2} \tag{8.6-59}$$

Substituting for s by $j\omega$ and equating to $1 + j\,0$ results in

$$G(j\omega_0) = \frac{jK\omega_0/RC}{[(1/RC)^2 - \omega_0^2] + j3\omega_0/RC} = 1 + j0 \tag{8.6-60}$$

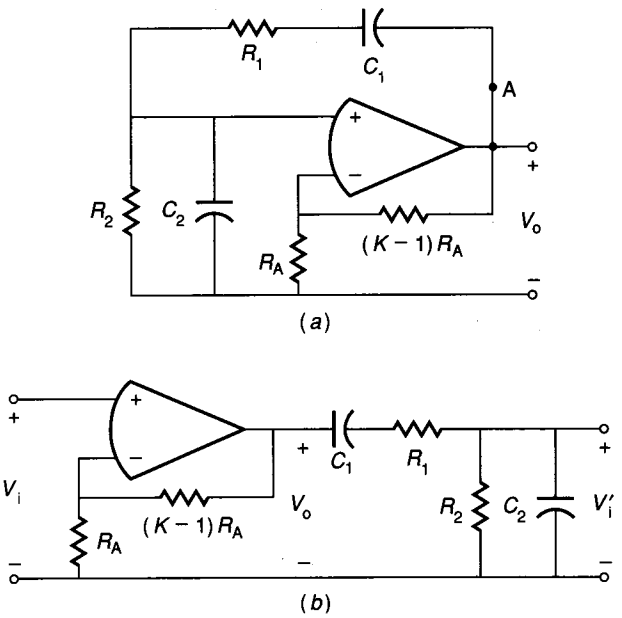


FIGURE 8.6-21
(*a*) Wien bridge *RC* oscillator, (*b*) Open-loop version of (*a*).

Equation 8.6-60 is satisfied if $K = 3$ at $\omega_0 = 1/RC$, which are precisely the conditions for oscillation of the oscillator of Fig. 8.6-21*a*. To obtain a 1 kHz oscillator, we could choose $C = 0.01$ μF, which gives $R = 15.9$ kΩ. Unfortunately, Fig. 8.6-21 is not practical for IC technologies unless the resistors were replaced with switched capacitors.

The amplitude of oscillation is indeterminate in the linear tuned oscillator. In practice, the amplitude of the oscillation is determined by a limiting nonlinearity. Figure 8.6-22 shows a possible nonlinear voltage transfer characteristic for the amplifier with gain K in Fig. 8.6-21*a*. For small values of V_O, the gain of the amplifier is designed to be greater than K (3 in the preceding example). When the gain is greater than 3, the amplitude of the sinusoidal oscillation grows. As the amplitude grows, the average gain over one cycle becomes smaller. The oscillator stabilizes at the amplitude where the time average gain is approximately equal to 3. If the amplitude should increase above this level for some reason, the oscillation will begin to decay because the effective gain is less than K. The amplitude stabilization is an important part of the oscillator. If the harmonic content of the sinusoid can be large, then the limiting effects of the power supplies can be used, although the waveform will no longer be sinusoidal. Many different schemes have been successfully used to achieve a stable oscillator amplitude. These include piecewise limiting circuits, thermistors, and the large signal transfer characteristics of differential amplifiers.

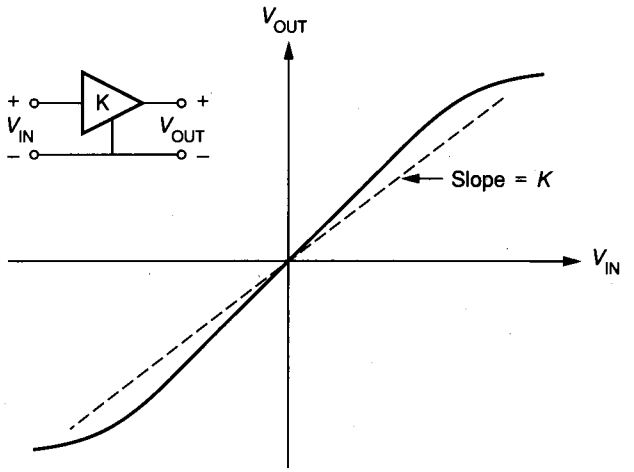


FIGURE 8.6-22
Nonlinear amplifier transfer function necessary for amplitude stabilization.

Because the RC products determine the oscillator frequency, the accuracy of an untrimmed integrated RC oscillator may not be sufficient. Switched capacitor techniques can be used to replace the resistors of the RC oscillators with resistor equivalents. Figure 8.6-23 shows a switched capacitor realization of the circuit of Fig. 8.6-21*a*. The resistor ratio, R_A/R_B, is assumed to be sufficiently accurate for this realization. If the high sampling assumption holds, then we may simply replace the resistor R with a switched capacitor equivalent resistance of T/C_R to get

$$\omega_0 \simeq \frac{C_R}{CT} = \frac{C_R}{C} f_c \tag{8.6-61}$$

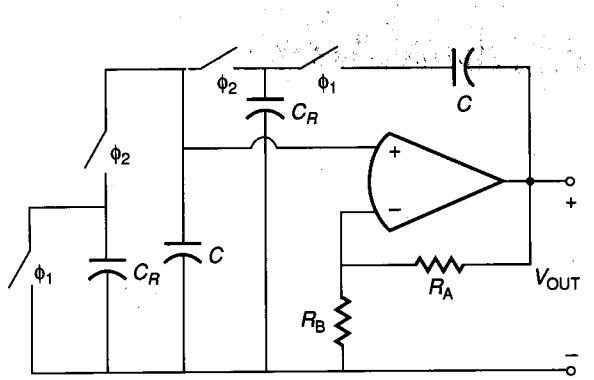


FIGURE 8.6-23
A switched capacitor realization of the Wien bridge RC oscillator of Fig. 8.6-21*a*.

We see that a switched capacitor implementation of an oscillator is really a circuit that scales the clock frequency to the oscillator frequency. The success of this implementation depends on the availability of a stable higher-frequency oscillator, f_c. The switched capacitor implementation also requires amplitude limiting.

The quadrature oscillator (see Prob. 8.42) is one in which switched capacitor techniques are suitable. The quadrature oscillator is essentially the Tow-Thomas realization of Fig. 8.4-11*c* with the $Q_i R$ resistor equal to infinity and the R/H_{oi} resistor removed. The result is a noninverting integrator and inverting integrator cascaded in a loop. The integrators of Sec. 8.5 could be used to achieve a switched capacitor implementation of the quadrature oscillator.

In general, the tuned oscillator is not widely used in integrated circuits for several reasons. The requirement for accurate RC products or an accurate clock is difficult to accomplish without using external components. The untuned oscillator or relaxation oscillator is more compatible with integrated circuit technology. The principle of operation can be seen from the block diagram of Fig. 8.6-24. This block diagram consists of an integrator cascaded with a bistable circuit. Although we have not yet discussed the realization of the bistable circuit, let us first consider the operation of Fig. 8.6-24. During the time interval from 0 to T_1, the integrator integrates the voltage L_+ provided by the bistable circuit. If K is the constant of integration, we find that the value of V_T at $t = T_1$ is given as

$$V_T(T_1) = S_- + K\int_0^{T_1} L_+ dt = S_- + KL_+T_1 = S_+ \qquad (8.6\text{-}62)$$

From Eq. 8.6-62, we may solve for the time, T_1, to get

$$T_1 = \frac{S_+ - S_-}{KL_+} \qquad (8.6\text{-}63)$$

We may solve for $V_T(T_2)$ using the same methods to get

$$V_T(T_2) = V_T(T_1) + K\int_{T_1}^{T_2} L_- dt = S_- + KT_2L_- = S_- \qquad (8.6\text{-}64)$$

Solving for T_2 gives

$$T_2 = \frac{S_- - S_+}{KL_-} \qquad (8.6\text{-}65)$$

The sum of T_1 and T_2 gives the period T and is written as

$$T = \frac{1}{f_o} = T_1 + T_2 = \left[\frac{S_+ - S_-}{K}\right]\left[\frac{1}{L_+} - \frac{1}{L_-}\right] = \frac{4S}{KL} \qquad (8.6\text{-}66)$$

if $L_+ = -L_- = L$ and $S_+ = -S_- = S$.

The above equations show that the bistable is a key element in the untuned oscillator. The bistable is a circuit that has two stable output states and exhibits

hysteresis when switching between the two states. Bistables may be clockwise or counterclockwise and can be shifted from the origin. Figure 8.6-25 shows the two possible generalized bistable characteristics. In this case, $L_+ = V_Y + V_L, L_- = V_Y - V_L, S_+ = V_X + V_H$, and $S_- = V_X - V_H$. Generally, $L_+ = L_-$ and $S_+ = S_-$. Figure 8.6-26*a* shows a realization of a clockwise (CW) bistable. If the output, V_S, is equal to V_{HH} (the positive power supply for the op amp), then the voltage at the noninverting input of the op amp is $V_{HH}R_3/(R_2 + R_3)$. If the input, V_T, is less than this value, then the output is in fact equal to V_{HH}. However, if V_T

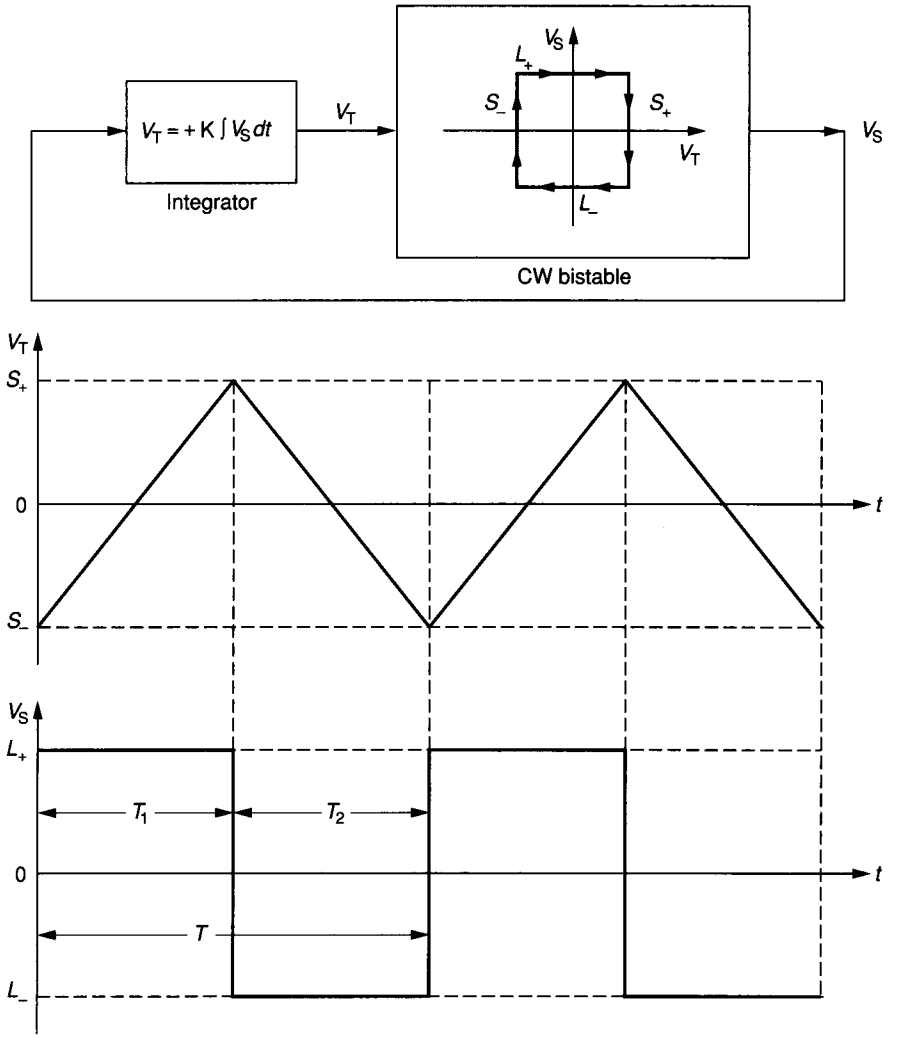


FIGURE 8.6-24
Block diagram of an untuned oscillator and the resulting waveforms.

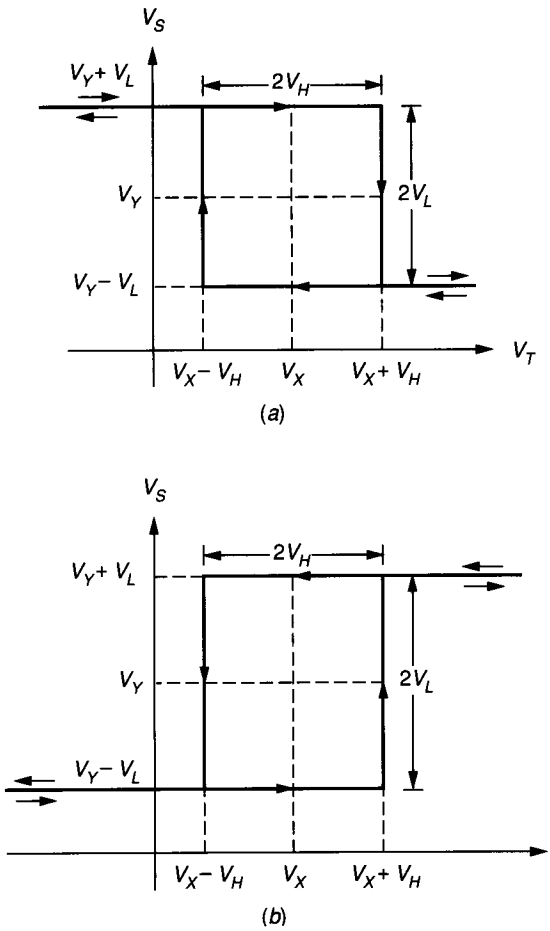


FIGURE 8.6-25
(*a*) CW bistable characteristic, (*b*) CCW bistable characteristic.

increases above this value from below, then the output voltage switches to V_{LL} (the negative power supply of the op amp) and voltage at the noninverting input changes to $V_{LL}R_3/(R_2 + R_3)$. From this discussion we see that $L_+ = V_{HH}, L_- = V_{LL}, S_+ = V_{HH}R_3/(R_2 + R_3)$, and $S_- = V_{LL}R_3/(R_2 + R_3)$. If possible, it is desirable to limit the output of the op amp to a voltage less than the power supplies.

The inverting input of the circuit of Fig. 8.6-26*a* could be grounded and the voltage V_T applied to the grounded end of R_3 to realize a counterclockwise (CCW) bistable. However, consider Fig. 8.6-26*b*, which shows a CCW bistable that limits the op amp swings to less than the power supplies. It can be shown that $L_+ = -R_6V_{LL}/R_7, L_- = -R_5V_{HH}/R_4, S_+ = -R_2(L_-)/R_3$, and $S_- = -R_2(L_+)/R_3$. Diodes D1 and D2 serve to keep the output of op amp A1 from swinging from V_{HH} to V_{LL}, thus permitting quick transition of states.

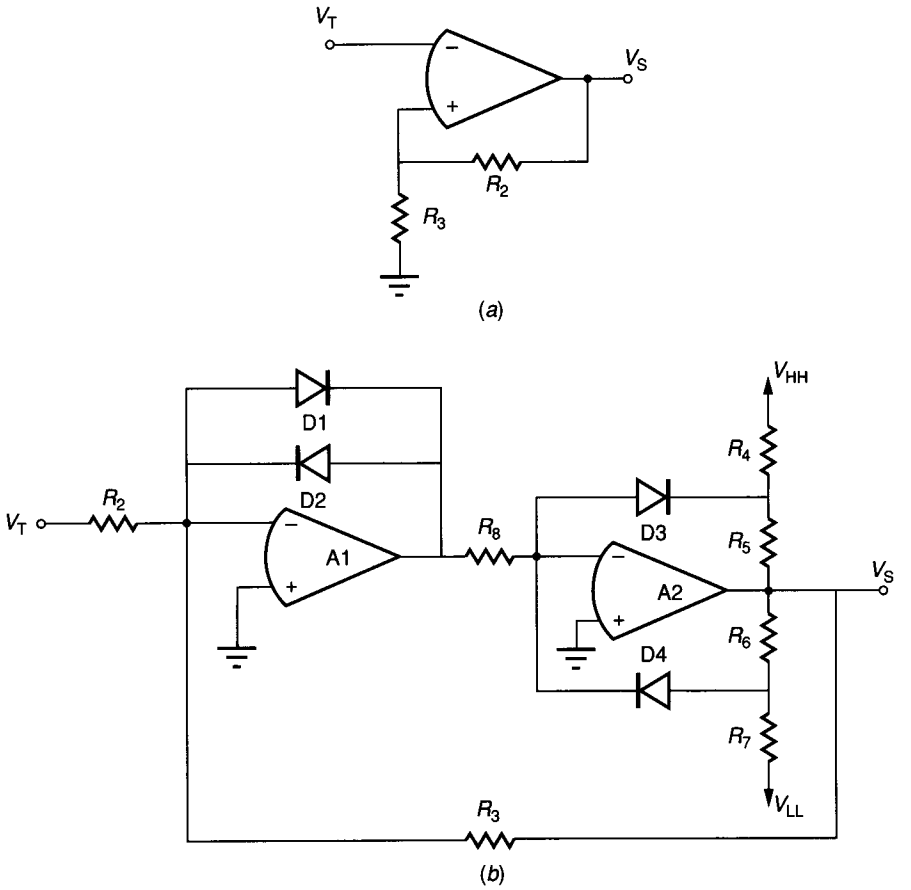


FIGURE 8.6-26
(*a*) Simple CW bistable, (*b*) CCW bistable with internal limiting.

A bistable circuit can also be implemented using switched capacitor techniques. Figure 8.6-27 shows a realization of the bistable characteristics of Fig. 8.6-25. The upper circuit, consisting of op amps 1 and 2, implements a switched capacitor amplifier with a sample-and-hold at the output and the ability to change the sign of the gain of the upper input, depending upon the output of comparator 3. The inputs to the comparator are the bistable input, V_T, and the output of the amplifier above, V_{TH}. The lower amplifier is similar to the upper amplifier. C_1 and C_2 are equivalent to the series switched capacitor simulations for a resistor. The discrete time voltages V_{TH}, V_C, and V_S are given as follows using the notation of Fig. 8.6-25.

$$V_{TH}(z) = \left\{ \frac{C_{12}}{C_1} V_{HH} + [\operatorname{sgn} V_C(z)] \left(\frac{C_{11}}{C_1} \right) V_{HH} \right\} z^{-1}$$

$$= \{ V_X + [\operatorname{sgn} V_C(z)] V_H \} z^{-1} \quad (8.6\text{-}67)$$

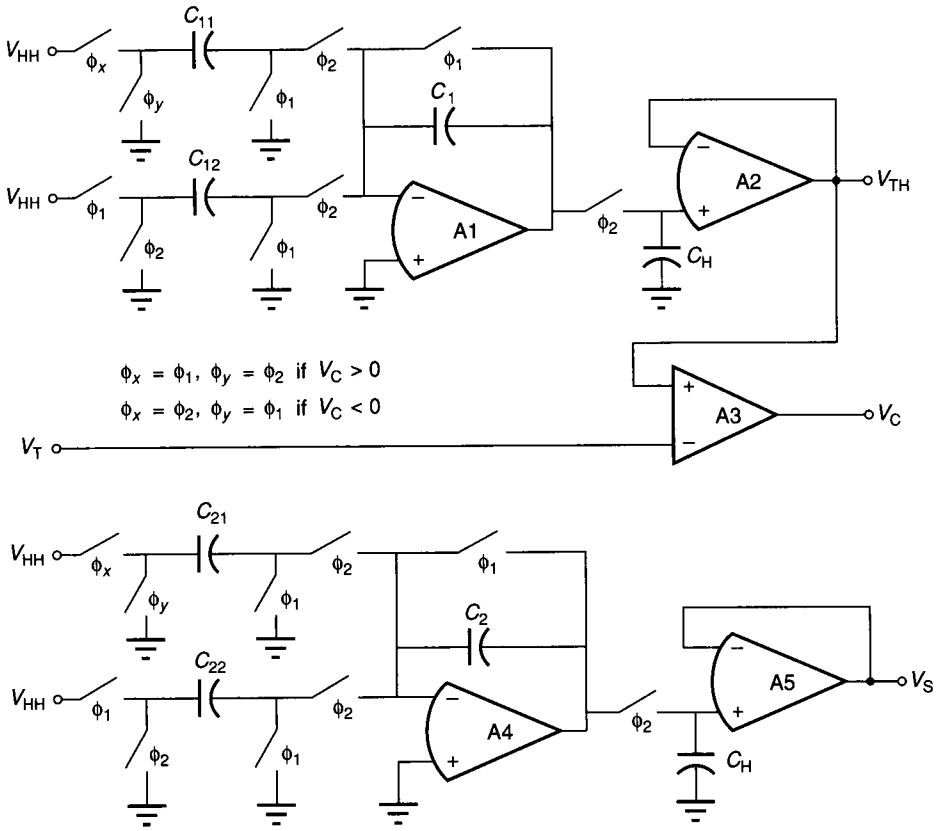


FIGURE 8.6-27
A switched capacitor implementation of the bistables of Fig. 8.6-25.

$$V_C(z) = \text{sgn}\{[V_{TH}(z) - V_T(z)]\} V_{HH} \tag{8.6-68}$$

and

$$V_S(z) = \left\{ \frac{C_{22}}{C_2} V_{HH} + [\text{sgn } V_C(z)] \left(\frac{C_{21}}{C_2} \right) V_{HH} \right\} z^{-1}$$

$$= \{ V_Y + [\text{sgn } V_C(z)] V_L \} z^{-1} \tag{8.6-69}$$

where sgn x is 1 if $x > 0$ and -1 if $x < 0$. A CW bistable characteristic is obtained when the ϕ_X and ϕ_Y of the C_{21} switched capacitor are as shown in Fig. 8.6-27 where V_T is the input and V_S is the output. If ϕ_X and ϕ_Y are reversed, then a CCW bistable is obtained. It is observed that the bistable characteristics are completely general and can be shifted as desired by varying the appropriate V_{HH}, by adjusting the capacitor ratios, and/or by changing ϕ_X and ϕ_Y of C_{21}.

The solid portion of Fig. 8.6-28 shows a simplified implementation of a CW bistable circuit based on the concepts of Fig. 8.6-27. It can be shown that the second amplifier is not needed for a CW bistable characteristic with V_X and

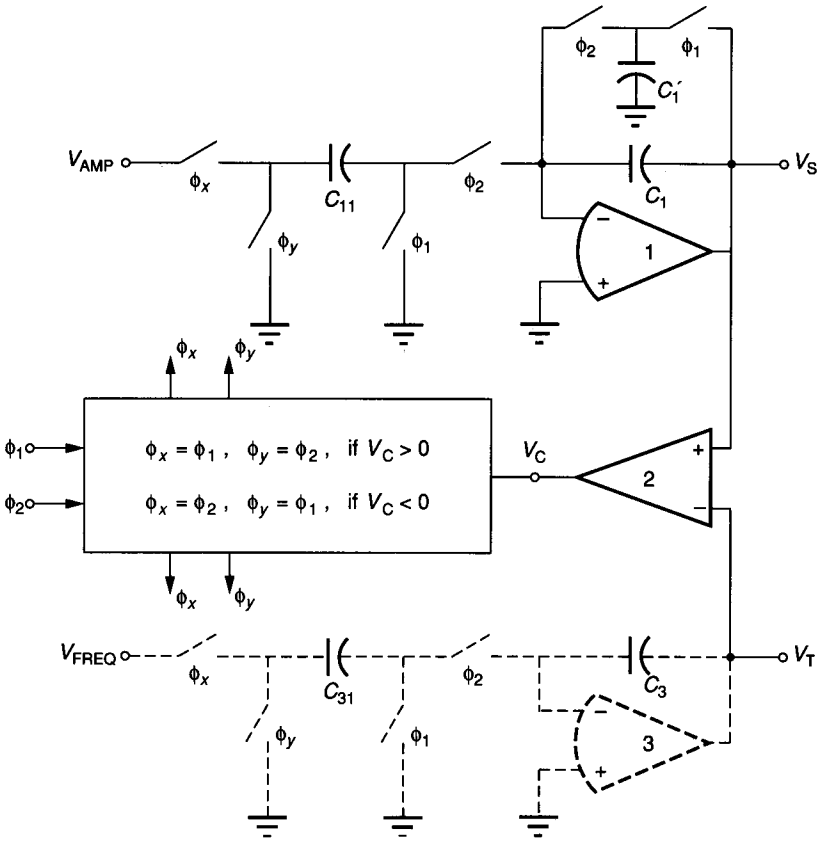


FIGURE 8.6-28
Simplified CW bistable circuit. The dotted portion is required for the waveform generator implementation.

V_Y of Fig. 8.6-25 equal to zero. The output is taken at V_S and the input is applied at V_T. The notation ϕ_X and ϕ_Y implies that these clocks are reversed depending upon the sign of V_C. For the case of Fig. 8.6-28, $\phi_X = \phi_1$ and $\phi_Y = \phi_2$ will give a noninverting gain. The phase reversal circuit can be implemented using the ideas represented in Fig. 8.6-18.

The bistable can now be combined with the proper type of integrator (noninverting or inverting) to achieve an implementation of the untuned oscillator block diagram of Fig. 8.6-24. An untuned oscillator using the CCW bistable of Fig. 8.6-26*b* and an inverting integrator is shown in Fig. 8.6-29. The integrating constant K is equal to $1/(R_1C_1)$, and the various limits of the bistable have already been shown to be $L_+ = -R_6V_{LL}/R_7, L_- = -R_5V_{HH}/R_4, S_+ = -R_2L/R_3$, and $S_- = -R_2L_+/R_3$. For example, if $V_{HH} = -V_{LL} = 15$ V, $R_1 = 100$ kΩ, $C_1 = 1$ nF, $R_2 = R_3 = 100$ kΩ, $R_4 = R_7 = 30$ kΩ, and $R_5 = R_6 = 20$ kΩ, then $L_+ = -L_- = S_+ = -S_- = 10$ V. From Eq. 8.6-66 we find that the frequency of

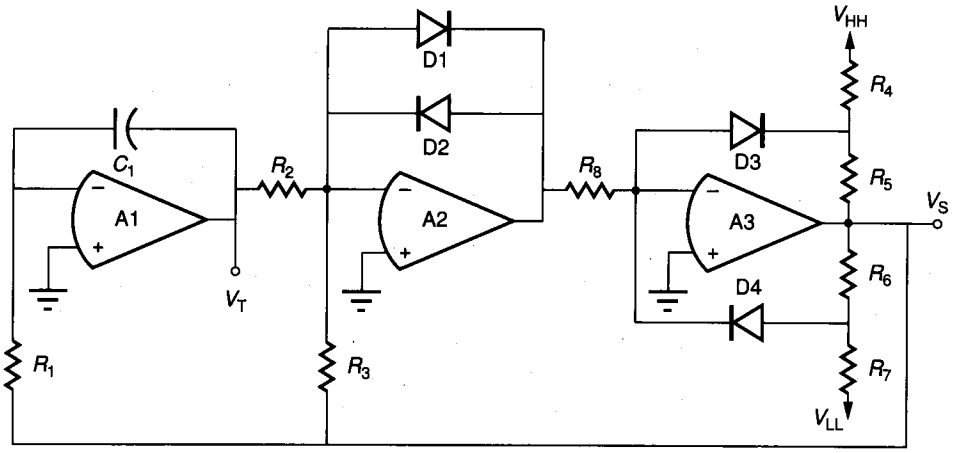


FIGURE 8.6-29
Untuned oscillator using the bistable of Fig. 8.6-26*b*.

oscillation, f_o, is 2500 Hz. Although the circuit of Fig. 8.6-29 is presented to illustrate concepts and is not practical for integration, the reader should be able to convert it to a form suitable for integration.

One of the advantages of an untuned oscillator is that the frequency can be easily controlled by a voltage. Figure 8.6-30 shows an example of how this might be accomplished. The output voltage, V_S, is used to connect the inverting integrator to a positive or negative value of a voltage called V_M. The limits of V_S effectively become $L_+ = -L_- = V_M$. Thus, the frequency of the untuned oscillator as developed in Eq. 8.6-66 becomes

$$f_o = \frac{V_M}{2R_1C_1(S_+ - S_-)} = \frac{V_M}{4R_1C_1S} \tag{8.6-70}$$

where $S = S_+ = -S_-$. The range of the control or modulating voltage, V_M, will be from the power supplies to the point at which op amp offsets become significant. Consequently, this voltage-controlled oscillator (VCO) should have two to three decades of frequency range. Other methods of controlling the oscillator frequency include a diode bridge[62] and current-controlled multivibrators.[63]

Many of the components of Fig. 8.6-29 can be removed, at the expense of some deterioration of the performance. Figure 8.6-31*a* shows an example of an untuned oscillator using only a single op amp. The analysis of this oscillator starts by assuming that the output is at L_+. Consequently, the voltage at the positive input terminal of the op amp is $R_3L_+/(R_2 + R_3) = \alpha L_+$. If V_1 is less than this voltage, then C_1 will begin to charge to L_+ through R_1. However, when V_1 is equal to αL_+, the output of the op amp switches to L_-. Now the voltage at the positive input terminal of the op amp is αL_-. Since this voltage is less than V_1, C_1 begins to discharge toward L_- through R_1. From

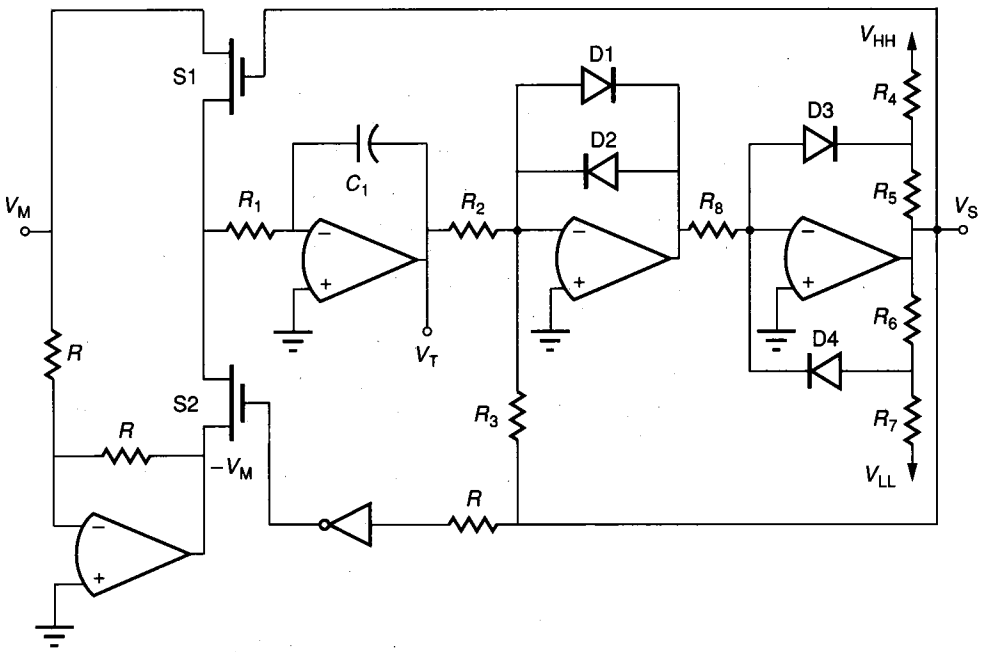


FIGURE 8.6-30
Voltage-controlled oscillator using the untuned oscillator of Fig. 8.6-29.

this analysis we see that $S_+ = \alpha L_+$ and $S_- = \alpha L_-$. The waveform at V_1 is no longer triangular but is exponential. It can be shown that the frequency of oscillation is

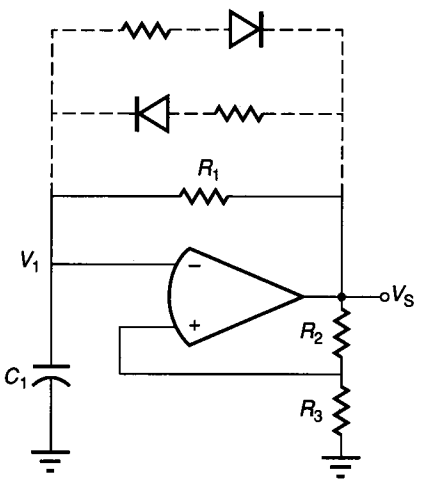
$$f_o = \frac{1}{2R_1C_1 \ln [(1 + \alpha)/(1 - \alpha)]} \tag{8.6-71}$$

where $\alpha = R_3/(R_2 + R_3)$. The square wave can be made asymmetrical through the use of diodes and resistors, as indicated in Fig. 8.6-31 in the dotted portion of the figure.

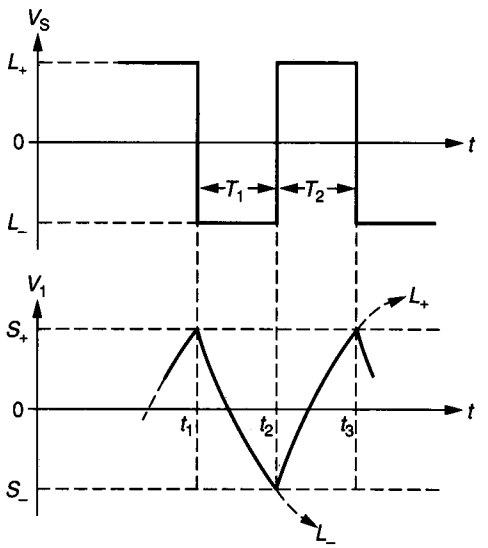
The switched capacitor bistable can also be used to implement an untuned oscillator that can be controlled by a voltage. This untuned oscillator is shown in Fig. 8.6-28 if the dotted portion is included. The amplifier of this realization uses a scheme to avoid requiring the op amp output to be zeroed during each clock cycle. The use of a parallel switched capacitor resistor realization in shunt with C_1 gives the following discrete time transfer function from V_{AMP} to V_S.

$$\frac{V_S(z)}{V_{AMP}(z)} = \frac{[\text{sgn } V_C(z)](C_{11}/C_1)z^{-1}}{1 - z^{-1}(1 - C'_1/C_1)} = [\text{sgn } V_C(z)]\left(\frac{C_{11}}{C_1}\right)z^{-1} \tag{8.6-72}$$

if $C_1 = C'_1$. C'_1 opposes the charge being transferred from C_{11} to C_1. Only the charge difference on C_{11} between consecutive samples is transferred. As a



(a)



(b)

FIGURE 8.6-31
(*a*) Simple untuned oscillator, (*b*) Waveforms of *a*.

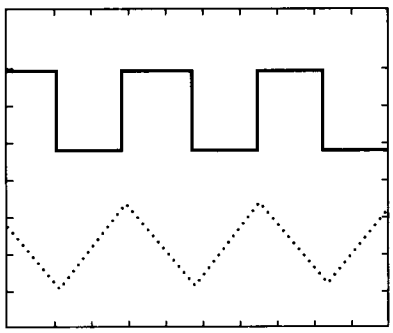
result, the op amp output voltage changes only by the difference in the input voltage multiplied by the gain factor of the amplifier. The circuit of Fig. 8.6-28 functions as a VCO where the amplitude and frequency of the square and triangle waveforms are given as

$$\text{Amplitude} = \left(\frac{C_{11}}{C_1}\right) V_{\text{AMP}}(t) \tag{8.6-73}$$

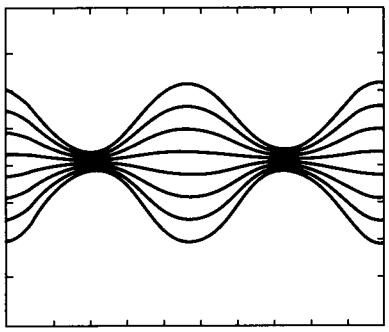
and

$$f_o = \left(\frac{C_1 C_{31} f_c}{4 C_3 C_{11}}\right) \frac{V_{\text{FREQ}}(t)}{V_{\text{AMP}}(t)} \tag{8.6-74}$$

It is seen that the switched capacitor VCO of Fig. 8.6-28 is capable of both amplitude and frequency modulation. Amplitude modulation is accomplished by connecting both $V_{FREQ}(t)$ and $V_{AMP}(t)$ to the source of modulation. Frequency modulation is accomplished by connecting only $V_{FREQ}(t)$ to the source of modulation and keeping $V_{AMP}(t)$ constant. Figure 8.6-32 shows the waveforms of the circuit of Fig. 8.6-28 used as an unmodulated, untuned oscillator, an amplitude-modulated oscillator, and a frequency-modulated oscillator (VCO).[64]



(*a*)



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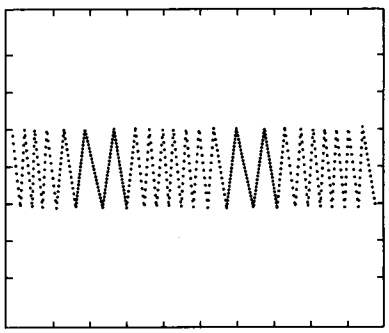


(*c*)

FIGURE 8.6-32
Drawings of actual oscilloscope waveforms. (*a*) Square and triangle waveforms, (*b*) Use of the circuit of Fig. 8.6-28 for amplitude modulation, (*c*) Use of the circuit of Fig. 8.6-28 for frequency modulation.

There are many other oscillators compatible with integrated circuit technology that have not been presented here. They include ring oscillators, constant-current oscillators, and multivibrators, including collector (drain) or emitter (source) coupled multivibrators. Other performance aspects of oscillators, including their temperature and power supply stability, has not been covered. These subjects are addressed in the technical literature.

8.6.4 Phased-Locked Loops

The last circuit we will consider in this section is the phase-locked loop (PLL). The phase-locked loop consists of a voltage controlled oscillator (VCO) whose frequency is equal to the frequency of the PLL input. The voltage controlling the VCO should vary monotonically with the frequency of the input to the PLL. A block diagram of a phase-locked loop is shown in Fig. 8.6-33. It is seen that a phase-locked loop consists of a negative feedback loop in which the output of a phase detector is applied to the control input of a VCO. The VCO applies a periodic waveform to the phase detector, the phase of which is compared with the phase of the input signal. The phase-locked loop has many applications, such as FM demodulation, frequency synchronization, signal conditioning, frequency multiplication and division, frequency translation, and AM detection.

A more detailed block diagram of the phase-locked loop is shown in Fig. 8.6-34. In the following analysis, the phase-locked loop is assumed to be locked. The input signal is assumed to be a sinusoid given as

$$V_{IN}(t) = V_p \sin(\omega t + \theta_i) \tag{8.6-75}$$

If the phase shift of the signal at the output of the VCO is θ_{osc}, then the average value of the output of the phase detector is

$$V_B = K_d(\theta_i - \theta_{osc}) \tag{8.6-76}$$

where θ_i and θ_{osc} are phase shifts with respect to an arbitrary reference. The phase of the signal at the output of the VCO as a function of time is equal to

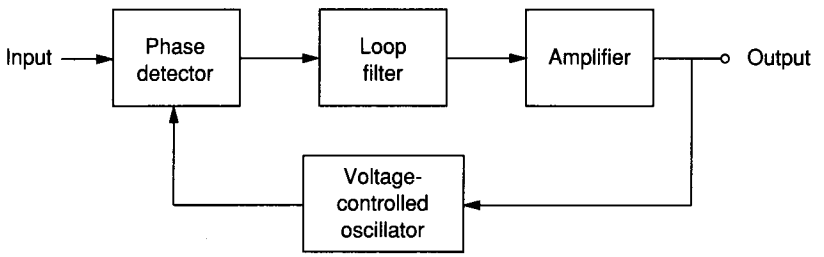


FIGURE 8.6-33
Block diagram of a phase-locked loop.

the integral of the frequency of the VCO, which can be expressed in differential form as

$$\omega_{osc}(t) = \frac{d\theta_{osc}(t)}{dt} \tag{8.6-77}$$

Thus, in the block diagram of Fig. 8.6-34, this integration is represented in the VCO block as $1/s$. If we assume that the oscillator frequency is given as

$$\omega_{osc} = \omega_o + K_o V_O \tag{8.6-78}$$

where ω_o is the free-running frequency of the oscillator when $V_O = 0$, then the transfer function of the phase-locked loop becomes

$$\frac{V_O(s)}{\theta_i(s)} = \frac{sK_dF(s)A}{s + K_dK_oAF(s)} \tag{8.6-79}$$

or

$$\frac{V_O(s)}{\omega_i(s)} = \frac{V_O(s)}{s\theta_i(s)} = \frac{K_dF(s)A}{s + K_dK_oAF(s)} \tag{8.6-80}$$

If $F(s) = 1$, then the loop inherently has a first-order, low-pass transfer response. The loop bandwidth is defined as $K_v = K_oK_dA$. Various types of filters have been used to achieve different dynamic performances for the phase-locked loop.[65]

The loop lock range is defined as the range of frequencies about ω_o for which the phase-locked loop maintains the relationship:

$$\omega_i = \omega_{osc} \tag{8.6-81}$$

If the phase detector can determine the phase difference between θ_i and θ_{osc} over a $\pm\pi/2$ range, then the loop lock range is expressed as

$$\omega_L = \pm\Delta\omega_{osc} = K_dAK_o(\pm\pi/2) = \pm K_v(\pi/2) \tag{8.6-82}$$

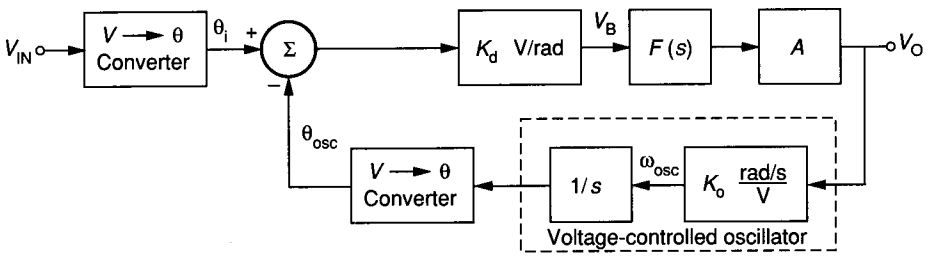


FIGURE 8.6-34
More detailed block diagram of a phased-locked loop.

The capture range is the range of input frequencies for which an initially unlocked loop will lock on an input signal. If $F(s) = 1$, then the capture range is equal to the lock range. If $F(s) = (1 + s/\omega_1)^{-1}$, then the capture range is less than the lock range. If the capture range is designated as $2\omega_C$, then Fig. 8.6-35 illustrates the relationships between the loop and capture ranges of a phase-locked loop with $F(s) = (1 + s/\omega_1)^{-1}$. The loop and capture ranges are very dependent on the loop bandwidth, K_v. If K_v decreases, the capture time increases, the capture range decreases, and the interference rejection properties of the phase-locked loop improve. The blocks shown in Fig. 8.6-34 can be implemented by circuits that we have examined previously in this chapter or in Chapter 6 for both MOS and BJT technologies.

Circuits that are representative of analog processing circuits have been introduced in this section. These circuits included the precision breakpoint circuit, multipliers and modulators, oscillators, and phase-locked loops. At this point the reader has a sufficient repertoire of circuits to undertake the design of systems using analog processing circuits or to undertake the design of a different type of analog signal processing circuit.

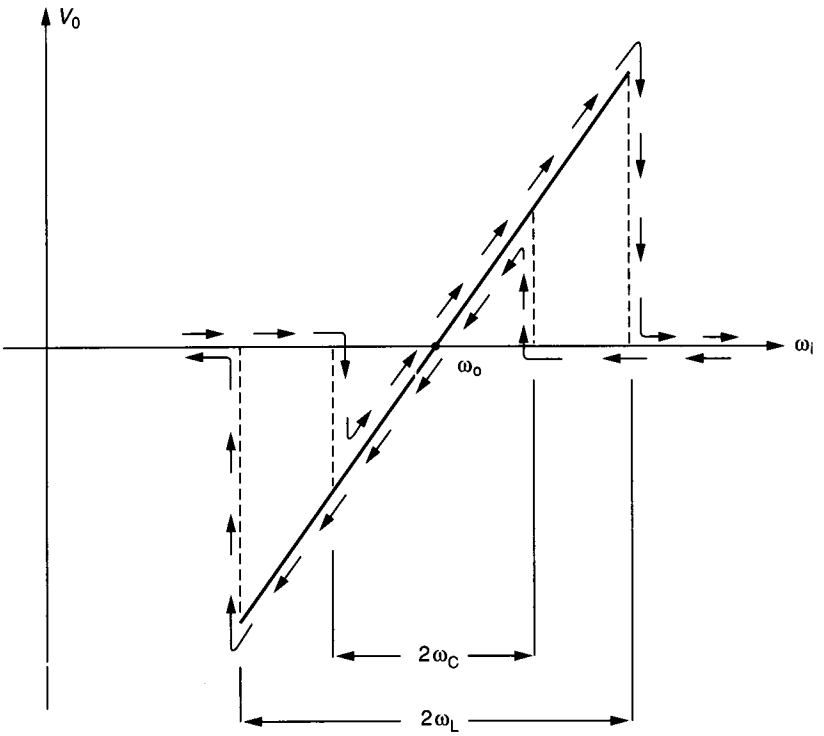


FIGURE 8.6-35
Illustration of the loop and capture ranges for a phase-locked loop.

8.7 SUMMARY

This chapter has introduced the elements of analog systems. An introduction to analog signal processing showed the important relationships between digital circuits, analog circuits, BJT technology, and MOS technology. It was seen that there is likely to be a mixture of digital and analog circuit techniques to implement signal processing systems. The selection of the appropriate technique is decided by many factors, including space, performance, and technology compatibility. The existence of technologies combining both BJT and MOS technologies offers some exciting advantages to the circuit and system designer.

Next, techniques of interfacing analog and digital circuits were presented. This subject was divided into digital-to-analog converters and analog-to-digital converters. The performance of the various types of converters was reviewed, followed by a consideration of current-scaling, voltage-scaling, charge-scaling, combination-scaling, and serial digital-to-analog converters. Analog-to-digital converters were presented, with the serial, successive approximation, parallel, and high performance analog-to-digital architectures considered.

One of the largest applications of analog circuits at the present is linear filtering. A review of continuous-time filters was presented, followed by a discussion of switched capacitor filters. The switched capacitor circuit technique is a practical adaptation of circuit design methods to match the technology, once again demonstrating the important influence of technology upon circuits and systems design. The key aspect of switched capacitor circuits is that equivalent RC products become equal to the product of capacitor ratios and an external clock frequency. This results in time constant accuracies as good as 0.1%. Three switched capacitor filter design approaches were presented; resistor replacement or substitution, passive RLC prototype based ladder synthesis, and direct realization of the filter in the z-domain.

The chapter concluded with a section on analog signal processing circuits. A number of nonfilter circuits were examined. These included waveshaping or precision breakpoint circuits; multipliers and modulators; oscillators, including tuned and untuned oscillators; and phase-locked loops. These are examples of circuits that might be used to implement a signal processing system. The boundary between a circuit and a system is very fuzzy. The topics presented in this chapter could be considered circuits from one viewpoint and systems from another. We have chosen to emphasize the circuit viewpoint over the application.

In closing, we will consider a signal processing system and examine how the design of such a system is hierarchically organized. Figure 8.7-1 shows a block diagram of an integrated circuit modem. A modem is a system that converts outgoing data in the form of a serial bit string to a form suitable for transmission over telephone lines and also converts the incoming data back to a serial bit string. This is a challenging problem because of the limited bandwidth of the telephone system and the desire to transmit data at as high a bit rate as possible. The particular modem considered is a 1200 bits/second, full-duplex, voice-band modem.[66] This system represents a reasonably complex design in terms of man-months of effort.

The details of the design of the modem will not be considered. Rather, the emphasis here will be on how the system is broken into smaller blocks that

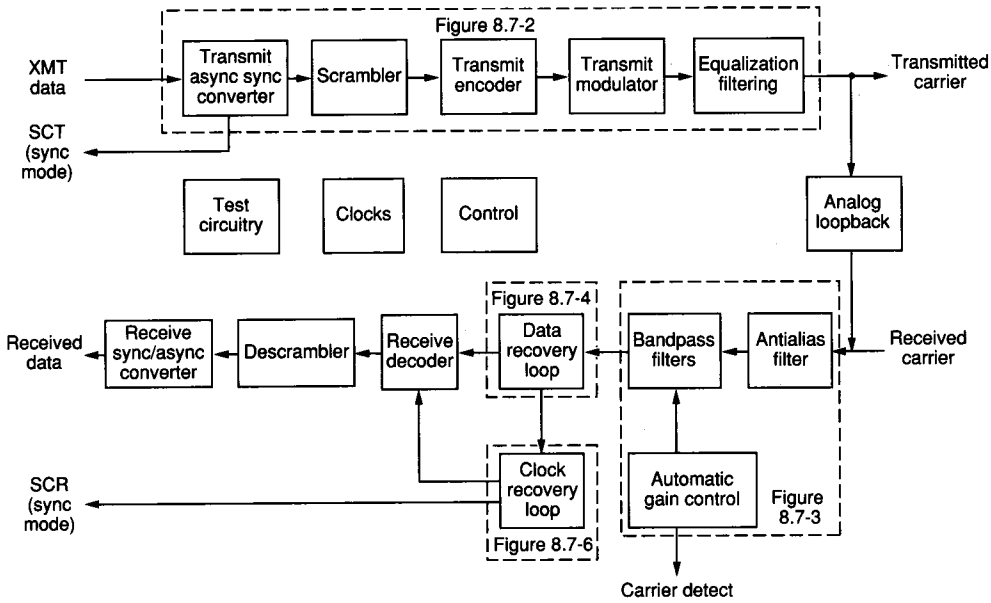


FIGURE 8.7-1
Integrated modem block diagram.

ultimately are recognizable as circuits we have considered in our study. For example, the transmitter is shown in more detail in Fig. 8.7-2. Here some of the blocks are recognizable, such as the filters, the mixers, and the summer. The asynchronous-to-synchronous converter, the scrambler, and the phase encoder are implemented by digital techniques such as those discussed in Chapters 7 and 9. The first part of the receiver channel is the automatic gain control circuit shown in Fig. 8.7-3. The analog blocks in this figure include filters, a full-wave rectifier (see Probs. 8.32 and 8.34), and a comparator.

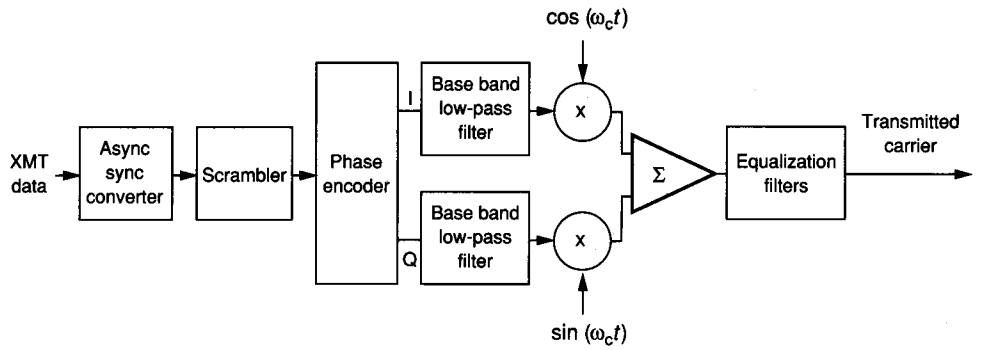


FIGURE 8.7-2
Differential QPSK transmitter.

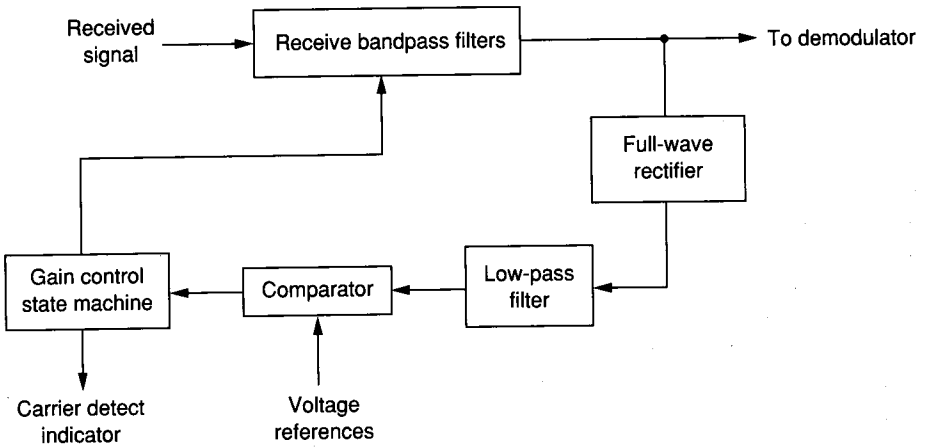


FIGURE 8.7-3
Automatic gain control circuit.

The next part of the receiver channel is called the data recovery loop and is implemented by a Costas phase-locked loop that preprocesses the received signals through Hilbert filters, as shown in Fig. 8.7-4. The Hilbert filters consist of two parallel filters, one shifted by 90° compared to the other. The data recovery loop consists of many analog circuits that have been previously considered, including

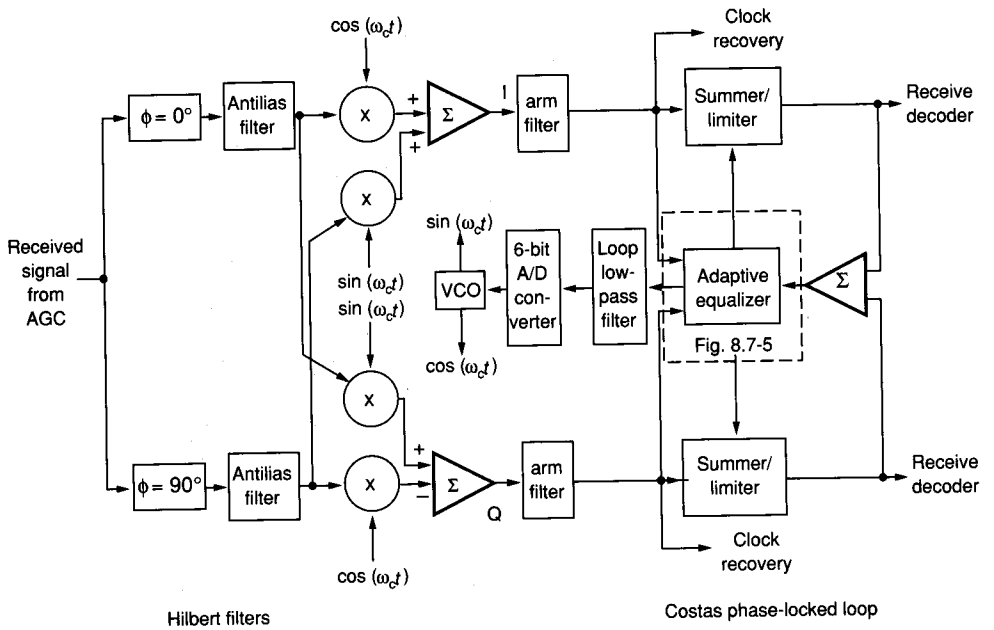
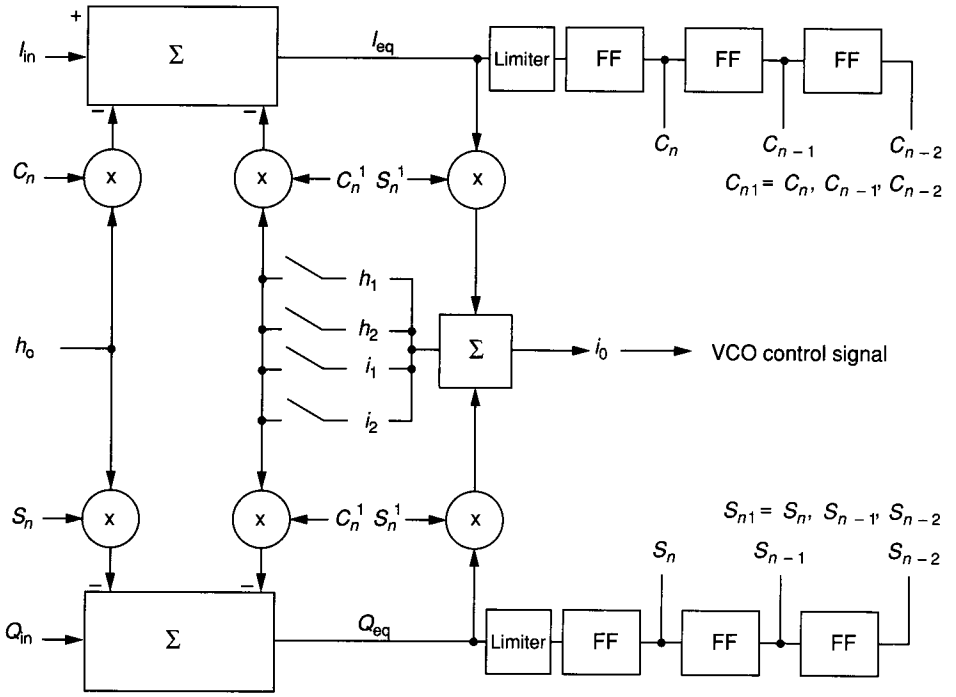


FIGURE 8.7-4
Coherent QPSK demodulation.

a 6-bit A/D converter. The adaptive equalizer of the data recovery loop is shown in more detail in Fig. 8.7-5, where we see a combination of analog and digital circuits. Another part of the receiver channel containing analog circuits is the clock recovery loop, shown in Fig. 8.7-6. The switched capacitor implementation of a part of this loop is illustrated in Fig. 8.7-7.

Figure 8.7-8 shows a photograph of the integrated circuit modem. This modem was implemented in an NMOS technology and used about 11,000 transistors. The modem used approximately 60 op amps and had a power dissipation of 750 mW. A CMOS version has reduced the power consumption significantly.

This example illustrates the hierarchy and decomposition of a system into circuits and similar components. Many other examples exist, such as speech processing circuits, other telecommunications circuits, and automotive control systems. One of the difficult problems facing the system designer is the simultaneous simulation of both the digital and analog parts of the system. In many cases, only partial simulation is possible.



$$I_{eq} = I_{in} - C_{n-2}h_2 - C_{n-1}h_1 - S_{n-2}i_2 - S_{n-1}i_1$$

$$Q_{eq} = Q_{in} - S_{n-2}h_2 - S_{n-1}h_1 + C_{n-2}i_2 - C_{n-1}i_1$$

$$\Delta i_o = K((I_{eq} - C_n h_o)S_n - (Q_{eq} - S_n h_o)C_n)$$

Where $h(t)$ = in phase impulse response

$i(t)$ = cross channel impulse response

FIGURE 8.7-5
Adaptive equalizer.

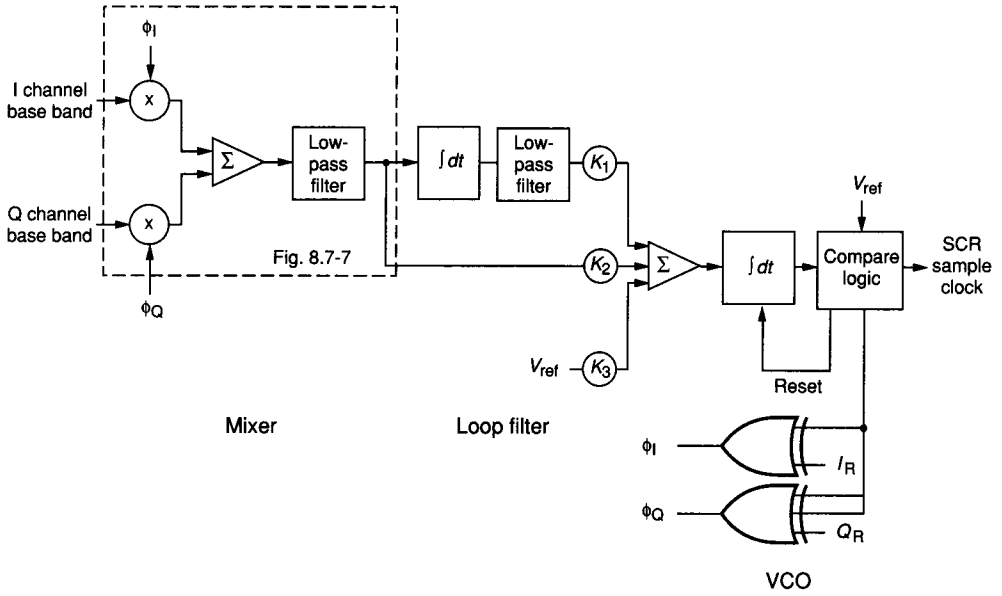


FIGURE 8.7-6
Clock recovery phase-locked loop.

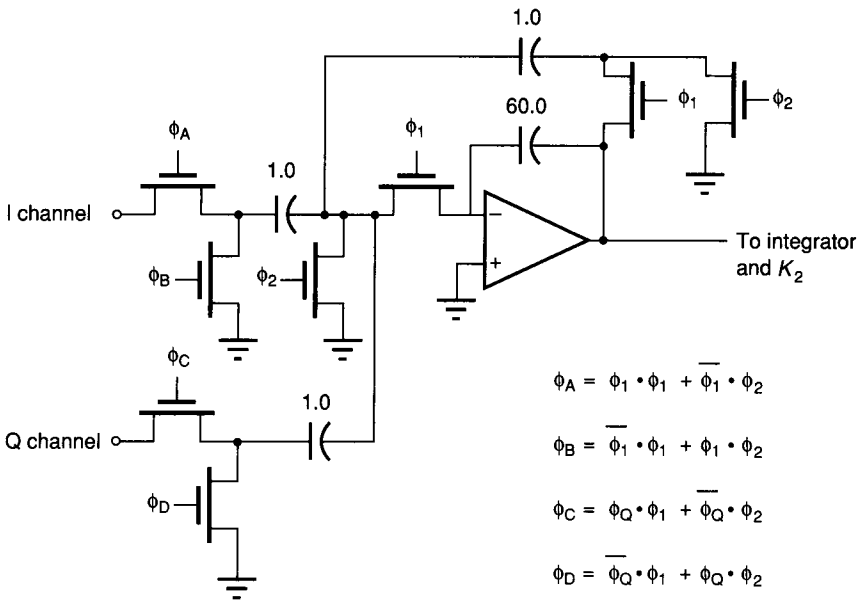


FIGURE 8.7-7
Clock PLL input.

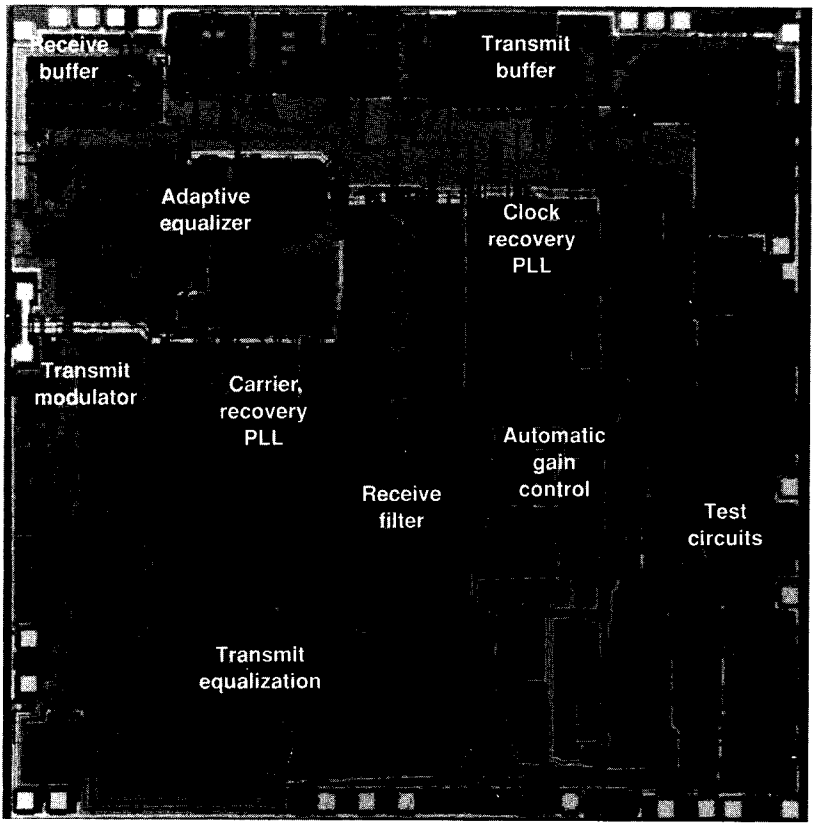


FIGURE 8.7-8
Integrated modem photograph (Courtesy of Texas Instruments).

The thrust of Chapters 5, 6, and 8 has been to present a hierarchically oriented introduction to the design of analog integrated circuits. Referring to Table 5.0-1, we have studied the design of analog circuits from the building block level in Chapter 5, through the basic circuit level in Chapter 6, up to the systems and complex circuit level of this chapter. The intent has been to give the reader an overview and the ability to know where and how to begin his or her design. The reader who faces the design of an analog circuit or system is encouraged to review the literature carefully in order to pick up some of the practical aspects and the circuit ideas and techniques that were not discussed here.

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PROBLEMS

Section 8.2

8.1. Compare the sample-and-hold circuit of Fig. 8.2-3*a* with that of Fig. 8.2-4 and discuss why the circuit of Fig. 8.2-4 can have faster sample times. Assume that ϕ and $\overline{\phi}$ are nonoverlapping clock signals.

8.2. Draw a transfer characteristic of a 3-bit D/A converter that has the largest possible integral nonlinearity when the differential nonlinearity is limited to ± 0.5 LSB. What is this maximum value of integral nonlinearity?

8.3. Express the output voltage of the binary-weighted resistor D/A converter shown in Fig. P8.3. Assume that the switches are connected to V_{ref} if the ith bit is 0, and to $-V_{\text{ref}}$ if the ith bit is 1.

8.4. Demonstrate that Fig. 8.2-12*b* will implement the function $V_{\text{OUT}} = -R_F I\,[b_1 + 2^{-1}b_2 + \cdots + 2^{-N+1}b_N]$ by considering a 4-bit example.

8.5. Find the accuracy required for R_{MSB} of a 12-bit D/A converter that uses the binary-weighted resistor approach in order to achieve monotonicity.

8.6. What is the maximum percentage tolerance of the current source (I_1) for the slave ladder of Fig. 8.2-13*b* if monotonicity is to be achieved for a 10-bit D/A converter?

8.7. Show how to modify the circuit of Fig. 8.2-15*a* to implement the bipolar operation of Eq. 8.2-13.

8.8. If an approximate formula for the ratio accuracy of capacitors is

$$\text{Ratio accuracy} \simeq 0.01 \times (\text{Capacitor ratio})^{0.25}$$

find the maximum number of bits that a charge-scaling D/A, such as in Fig. 8.2-15*a*, can have.

8.9. If A_R is the area of the resistors and A_C is the area of the capacitors of the D/A converter of Fig. 8.2-18, show that for minimum area

$$K - M = \frac{\ln\,(A_R/A_C)}{\ln 2}$$

where K is the number of bits that are charge-scaled and M is the number of bits that are voltage-scaled.

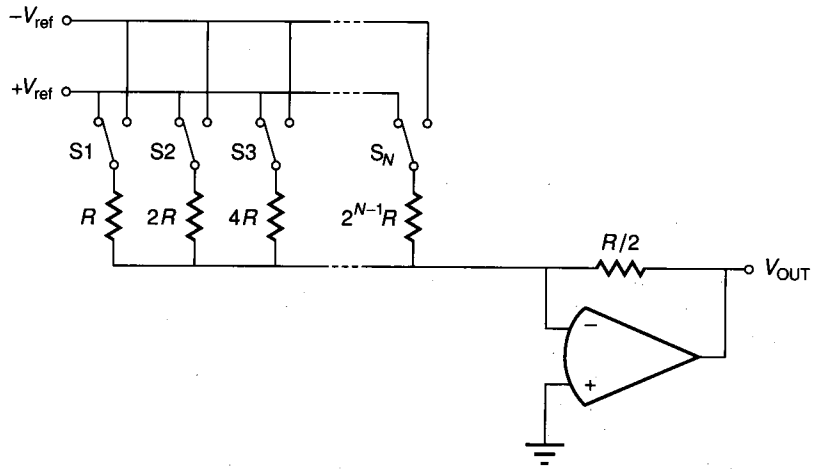

FIGURE P8.3

8.10. Determine the value of V_{C1} in Fig. 8.2-21 following the sequence of switch closing and openings: S4, S3, S1, S2, S1, S3, S1, S2, and S1. Assume that $C_1 = C_2$.

8.11. Repeat Prob. 8.10 if $C_1 = 1.05C_2$.

8.12. Show how Eq. 8.2-25 can be derived from Eq. 8.2-24. Give a realization of Fig. 8.2-24 using op amps, switches, and passive components.

8.13. Repeat Example 8.2-2 for the digital word 10101.

8.14. Assume that the amplifier with a gain of 0.5 in Fig. 8.2-24 has a gain error of ΔA. What is the maximum value ΔA can have in Example 8.2-2 without causing the conversion to be incorrect?

Section 8.3

8.15. Plot the transfer characteristic of a 3-bit A/D converter that has the largest possible differential nonlinearity when the integral nonlinearity is limited to ± 1 LSB. What is the maximum value of differential nonlinearity?

8.16. Find the 8-bit digital word if the input to Ex. 8.3-1 is 0.3215 V_{ref}.

8.17. Continue Example 8.3-2 out to the 10th bit and find the equivalent analog voltage.

8.18. Repeat Example 8.3-1 for the case where the gain-of-2 amplifiers actually have a gain of 2.1.

8.19. How many bits will an A/D converter with a sampling frequency of 10 MHz have in 1998? What technology will this converter use?

Section 8.4

8.20. Use the three circuits of Fig. 8.4-11 to obtain a realization of a second-order, low-pass Butterworth filter with a −3 dB frequency of 1000 Hz and a gain of 1 at dc. In Fig. 8.4-11*a*, additional stages may be necessary to achieve a gain of 1 at dc.

8.21. Repeat Example 8.4-3 using Fig. 8.4-11*c*, for stage 2 and stage 3.

8.22. Use the transformations of Fig. 8.4-13 to convert the result of Example 8.4-4 to a bandpass filter having a bandwidth of 500 Hz centered at 1000 Hz.

Section 8.5

8.23. Prove that the equivalent resistance given in Fig. 8.5-2 for the series switched capacitor resistance simulation is valid.

8.24. Repeat Prob. 8.23 for the series-parallel switched capacitor resistance simulation.

8.25. Repeat Prob. 8.23 for the bilinear switched capacitor resistance simulation.

8.26. Replot the frequency response of the circuit of Fig. 8.5-5*a* if $\omega_1 = 0.02\omega_c$. Compare with the frequency response (magnitude and phase) of Fig. 8.5-2.

8.27. Replace the parallel switched capacitor resistor simulation in Fig. 8.5-5*a* with the series switched capacitor resistor simulation of Fig. 8.5-2 and find the discrete-time frequency response similar to Eq. 8.5-27. Develop an expression for the magnitude and phase response and compare it with the results of Fig. 8.5-5*a*.

8.28. Obtain the exact frequency response at ϕ_1 of the switched capacitor circuit shown in Fig. P8.28. Define $\alpha = C_1/C_2$, and solve for the -3 dB frequency, in hertz, when $\alpha = 3$ and the clock frequency is (*a*) 64 kHz and (*b*) 128 kHz. The clock phases are nonoverlapping, and V_1 is from a sample-and-hold circuit.

8.29. Develop an expression for the discrete-time magnitude and phase response for H^{oe} of the noninverting switched capacitor integrator of Fig. 8.5-10*a*. Plot the magnitude and phase for frequencies from 0 to ω_c if $\omega_0/\omega_c = 0.1$.

8.30. Repeat Prob. 8.29 for the inverting switched capacitor integrator of Fig. 8.5-12.

8.31. Find the actual magnitude and phase of the noninverting switched capacitor integrator of Fig. 8.5-10*a* for H^{oo} if the frequency applied to the integrator is 10 kHz, the clock frequency is 100 kHz, and ω_0 is 20π krps.

Section 8.6

8.32. Develop a realization of $V_{OUT} = |V_{IN}|$ using resistors, diodes, and two op amps.

8.33. Develop a realization of $V_{OUT} = -|V_{IN} - 1|$ using resistors, diodes, and the minimum number of op amps.

8.34. Repeat Prob. 8.32 using capacitors, switches, one comparator, and the minimum number of op amps.

8.35. Repeat Prob. 8.33 using capacitors, switches, one comparator, and the minimum number of op amps.

8.36. (*a*) Design a circuit that realizes the transfer characteristic of Fig. P8.36 using resistors, diodes, and op amps.
(*b*) Repeat using capacitors, switches, comparators, and op amps.

8.37. (*a*) Design a circuit that realizes the transfer characteristic of Fig. P8.37 using resistors, diodes, and op amps.
(*b*) Repeat using capacitors, switches, comparators, and op amps.

8.38. Derive Eqs. 8.6-24 and 8.6-25 from Fig. 8.6-10.

8.39. Use a four-quadrant analog multiplier, op amps, and resistors to develop a circuit that produces an output voltage of $-K(V_1)^{1/2}$ when $V_1 > 0$.

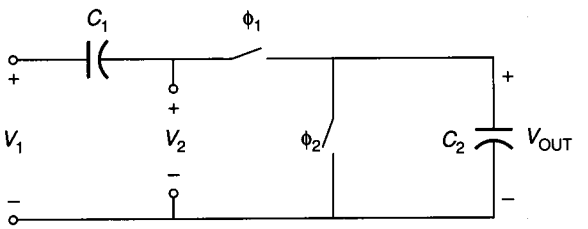

FIGURE P8.28

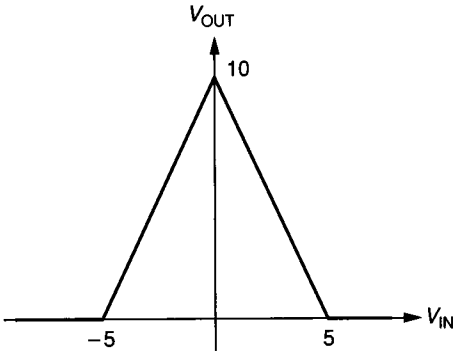

FIGURE P8.36

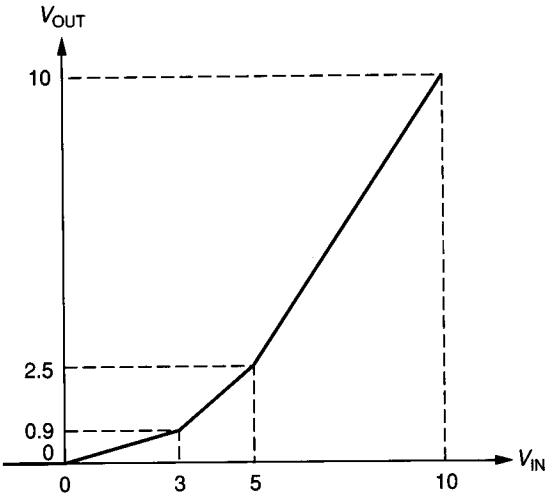

FIGURE P8.37

8.40. The sine of an input voltage V_1 can be approximated by the formula, $\sin V_1 \simeq 1.155V_1 - 0.33V_1^2$, to within $\pm 2\%$ over the range of $0 < V_1 < \pi/2$. Use multipliers and op amps to find a realization of $\sin V_1$ using this formula.

8.41. Find the frequency of oscillation, in hertz, and the value of R_f necessary for oscillation of the *RC* phase shift oscillator shown in Fig. P8.41.

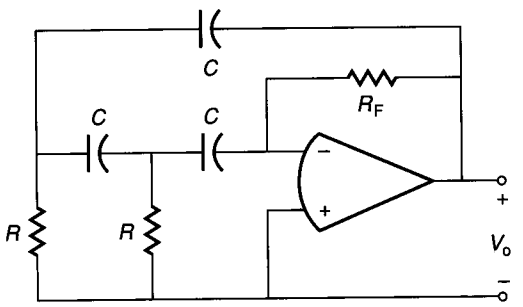

FIGURE P8.41

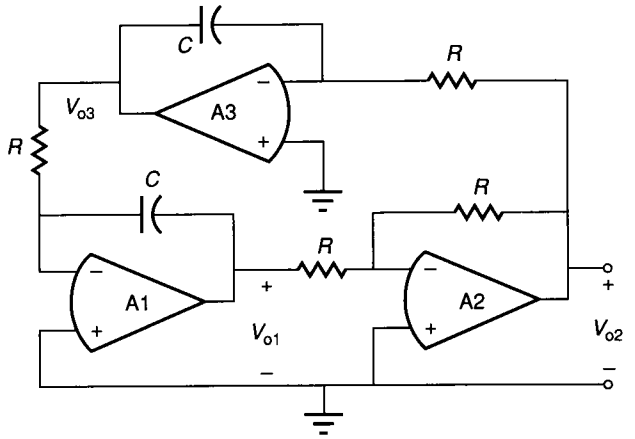

FIGURE P8.42

8.42. Find the frequency of oscillation, in hertz, of the quadrature oscillator of Fig. P8.42. Give expressions for the voltages V_{o1}, V_{o2}, and V_{o3} if the amplitude of the sinusoid at V_{o1} is 1 V peak.

8.43. Determine the values for the resistors not given in the bistable circuit of Fig. P8.43 and determine whether to connect R_q to $+15$ V or -15 V in order to realize the output-input transfer characteristic shown.

8.44. Show how to use a CW bistable to implement an untuned oscillator, and design the oscillator to produce a ± 10 V square wave at 3000 Hz.

8.45. Develop the expression for the frequency of oscillation of the circuit in Fig. 8.6-31 given in Eq. 8.6-71. What is the frequency of oscillation, in hertz, if $R_2 = R_3, R_1 = 100$ kΩ, and $C_1 = 1$ nF?

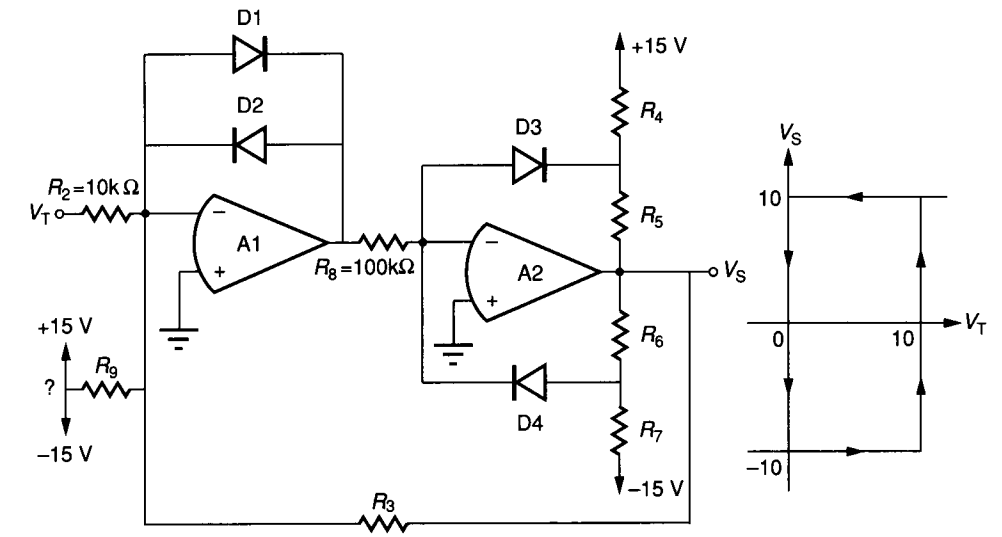

FIGURE P8.43