Problem 1  There are a small number of different ADC architectures that dominate the commercial parts that are available today. The dominant architectures are SAR, Pipelined, and Delta-Sigma. Speed and resolution are the driving factors that dictate which architecture is most suitable though the process node may affect the tradeoffs. The figure below (extracted from a TI presentation) shows the conventional wisdom of which structures are best associated with different applications. Though not explicitly shown in this figure, the power dissipation is a factor in determining the most suitable architecture. A listing of all of the ADCs available from Analog Devices are included in the linked spreadsheet. From this spreadsheet, create a method of graphically showing how the breakdown between these different architectures occurs. In this comparison the number of parts in each part of the resolution/conversion rate plane should be appropriately represented. (Note: I have used the Analog Devices parts because the relevant information is readily available in spreadsheet form. Texas Instruments and Maxim are major players in this market space and also have spreadsheets listing data converter specifications but TI does not include the sampling rate field and Maxim does not include the power dissipation field thereby making it difficult to sort on these fields without adding the appropriate information for each device in their catalogs which together total over 1400 parts).

Problem 2  Power is often of considerable concern when specifying an ADC. Increases in resolution and increases in conversion rate invariably require more power but this relationship is highly nonlinear. Based upon the spreadsheet from Analog Devices, develop a model that relates resolution, conversion rate, and power dissipation and make a comparison of how the Analog Devices parts fit in this model. (Note: you may need to change the units in the speed column before doing sorts to be sure all are consistent). Based upon your model, identify outliers that are most attractive and outliers that are least attractive. In the spreadsheet, some parts have several parallel channels. In those parts that have parallel channels, divide the total power by the number of channels to get the power for each converter.
This is not completely a fair comparison since some circuitry may be shared between converters but it should not cause major inconsistencies. (Actually electrical performance should be measured in terms of ENOB instead of resolution but this information is not readily available in the spreadsheet)

Problem 3 This is closely related to Problem 2. Many journal and conference papers use as a figure of merit $F = \frac{P}{f_s 2^{n_{\text{eff}}}}$ where $f_s$ is the sampling rate and $n_{\text{eff}}$ is the effective resolution (or ENOB). The goal with this figure of merit is to have a figure of merit that is unaffected by $P$, $f_s$, and $n_{\text{eff}}$. Following this thought process, a good design will have a low value for $F$ and presumably good parts throughout the $f_s$-resolution plane will all have the same value of $F$.

a) Assuming $n_{\text{eff}}$ is simply the resolution of commercial ADCs, compute $F$ for the Analog Devices parts (as before, convert the power column to power/channel to more fairly include multi-channel components).

b) Is this figure of merit independent of $f_s$ and $n$ for the Analog Devices parts?

c) Identify 5 ADCs that have appeared in either ISSCC or the IEEE Journal of Solid State Circuits in the past 12 months and compare $F$ for these circuits compared to what is actually commercially available from Analog Devices. Comment on your observations.