EE 505

CMOS and BiCMOS Data Conversion Circuits

Course Information:

Lecture Instructor:

Randy Geiger
351 Durham
Voice: 294-7745
e-mail: rlgeiger@iastate.edu
WEB: www.randygeiger.org

Laboratory Instructor:

Jake Sloat
Room 310 Durham
Voice: 294-8343
e-mail: jacob.sloat@gmail.com

Course Information:

Analog VLSI Circuit Design

Lecture: TR 11:00 Rm 1304 Howe

Labs: to be arranged

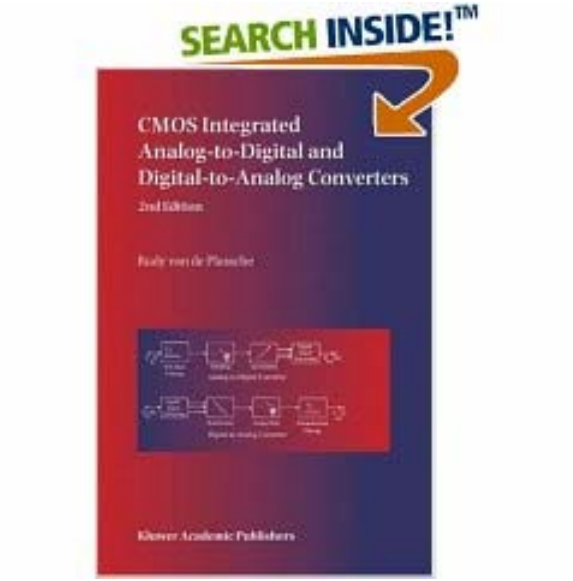
Course WEB Site: http://class.ee.iastate.edu/ee505/

Course Description:

Theory, design and applications of data conversion circuits (A/D and D/A converters) including: architectures, characterization, quantization effects, conversion algorithms, spectral performance, element matching, design for yield, and practical comparators, implementation issues.

Course Information:

Key Reference Text:

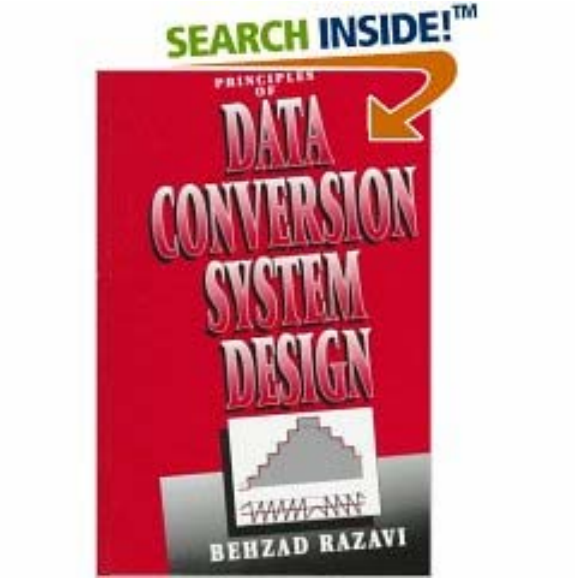


CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters – 2nd Edition
by Rudy van de Plassche, Kluwer, 2003

Course Information:

Other Reference Texts:

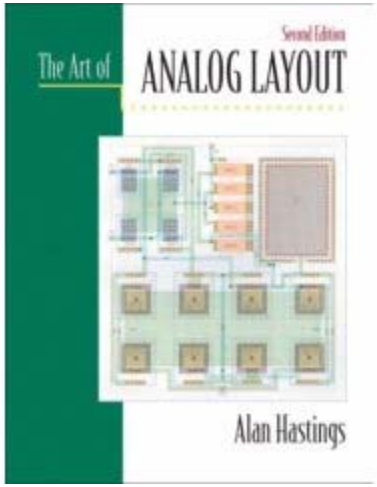
Data Converters
by F. Maloberti, Springer, 2007



Principles of Data Conversion System Design
by B. Razavi, IEEE Press, 1995

Course Information:

Other Reference Texts:

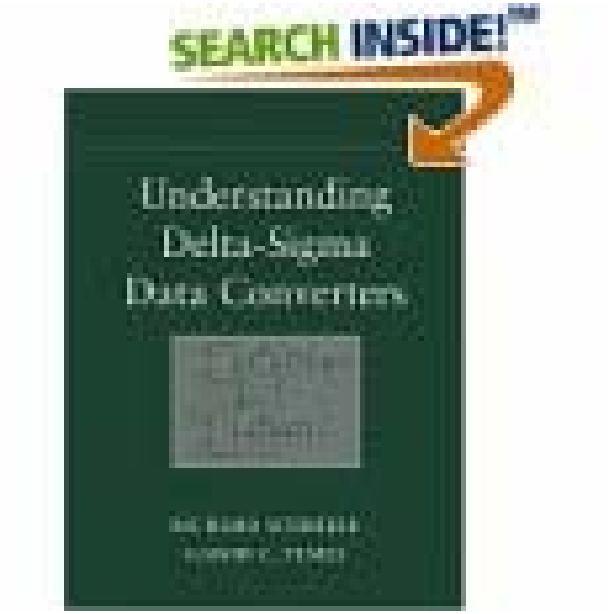


Data Conversion Handbook
by Analog Devices, 2005

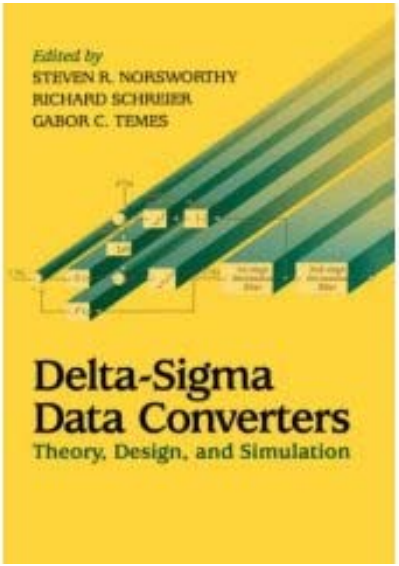
The Art of Analog Layout
by A. Hastings, Prentice Hall, 2001

Course Information:

Other Reference Texts:



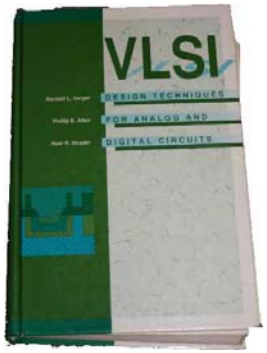
Understanding Delta-Sigma Data Converters
by R. Schreier and G. Temes, Wiley, 2005



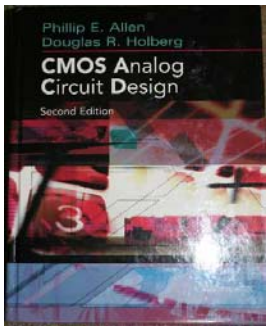
Delta-Sigma Data Converters – Theory, Design, and Simulation
edited by S. Norsworthy, R. Schreier and G. Temes, Wiley, 1997

Course Information:

Reference Texts:



VLSI Design Techniques for Analog and Digital Circuits
by Geiger, Allen and Strader, McGraw Hill, 1990



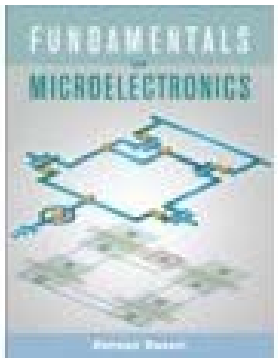
CMOS Analog Circuit Design
by Allen and Holberg, Oxford, 2002.

Course Information:

Reference Texts:

CMOS: Circuit Design, Layout, and Simulation – Second Edition by J. Baker, Wiley, 2007.

Fundamentals of Microelectronics
by B. Razavi, McGraw Hill, 2008



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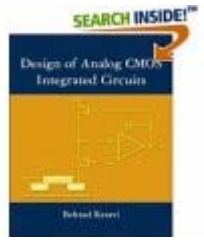
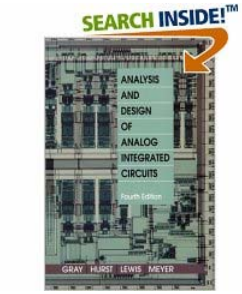
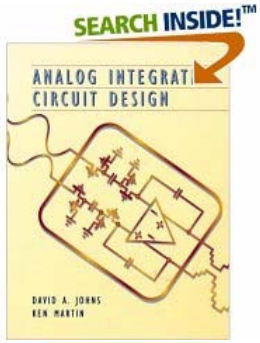
Reference Texts:



Design of Analog CMOS Integrated Circuits
by B. Razavi, McGraw Hill, 1999



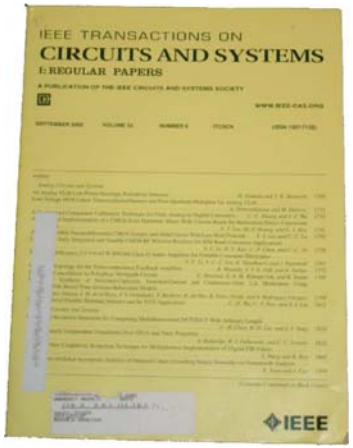
Analysis and Design of Analog Integrated Circuits-Fourth Edition
Gray,Hurst,Lewis and Meyer, Wiley, 2001

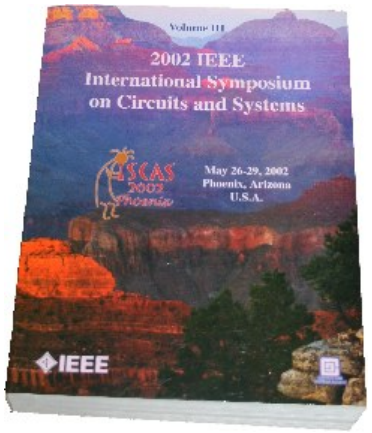


Analog Integrated Circuit Design
by D. Johns and K. Martin, Wiley, 1997

Course Information:

Reference Materials:





Course Information:

Grading: Points will be allocated for several different parts of the course. A letter grade will be assigned based upon the total points accumulated. The points allocated for different parts of the course are as listed below:

1 Exams	100 pts
1 Final	100 pts.
Homework	100 pts.total
Lab and Lab Reports	100 pts.total
Design Project	100 pts.

Note: In the event that one of the exams is not given, the weight of the remaining exam will be increased to somewhere between 100 pts and 200 pts.

Course Information:

Design Project:

The design project will be assigned by mid-term. Additional details about the design project will be given after relevant material is covered in class. The option will exist to have this project fabricated through the MOSIS program. The design should be ready for fabrication and post-layout simulations are to be included as a part of the project.

Course Information:

E-MAIL:

I encourage you to take advantage of the e-mail system on campus to communicate about any issues that arise in the course. I typically check my e-mail several times a day. Please try to include “EE 505" in the subject field of any e-mail message that you send so that they stand out from what is often large volumes of routine e-mail messages.

Topical Coverage

- Data Converter Operation, Characterization and Specifications
  - Transfer Characteristics
  - Noise
  - Spectral characterization
- Component Matching and Yield
- Nyquist-Rate Data Converter Design
  - DACs
    - Architectures
    - Building Blocks
    - Analysis, Simulation, and Yield
  - ADCs
    - Architectures
    - Building Blocks
    - Analysis, Simulation, and Yield
- Over-Sampled Data Converters
  - Operation
  - Architectures
  - Building Blocks

Data Converters

Types:

A/D (Analog to Digital)

Converts Analog Input to a Digital Output

D/A (Digital to Analog)

Converts a Digital Input to an Analog Output

A/D is the world's most widely used mixed-signal component

D/A is often included in a FB path of an A/D

A/D and D/A fields will remain hot indefinitely

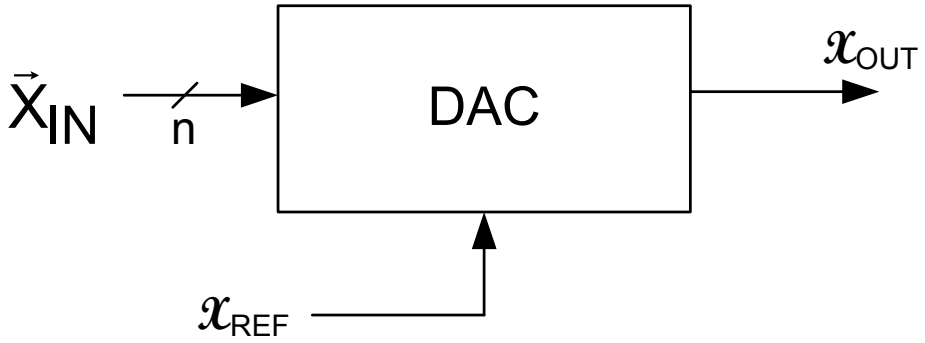
technology advances make data converter design more challenging

embedded applications

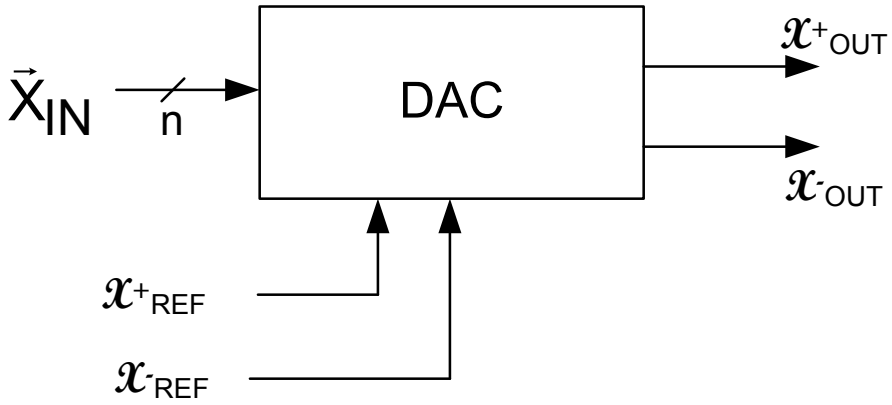
designs often very application dependent

D/A Converters

Basic structure:

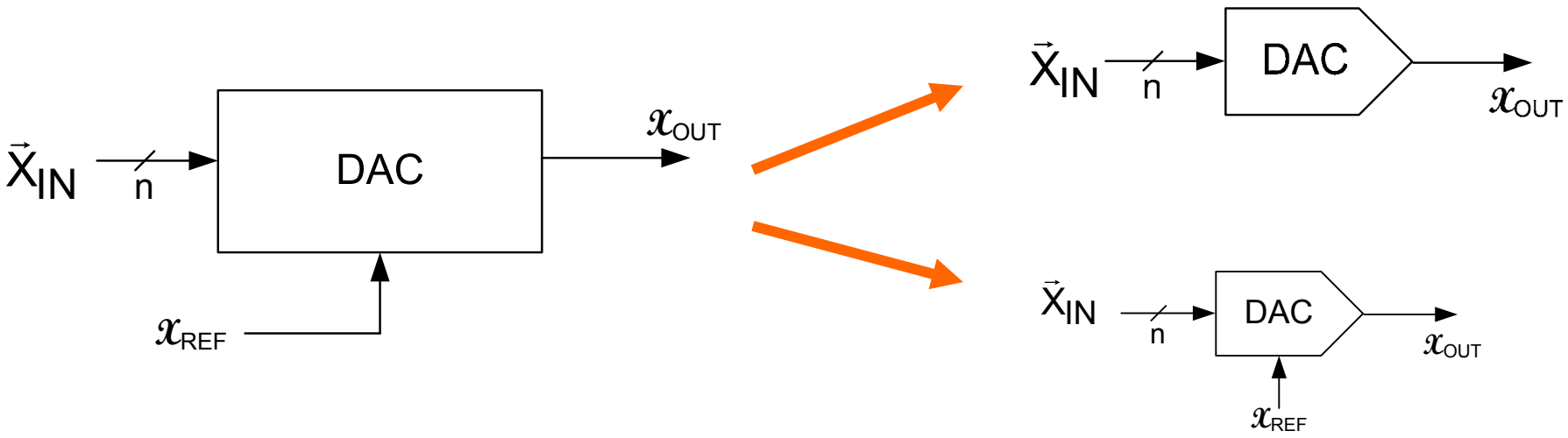


Basic structure with differential outputs::



D/A Converters

Notation:



D/A Converters

$$\vec{X}_{IN}=<b_{n-1},b_{n-1},\ldots b_1,b_0>$$

b_0 is the Least Significant Bit (LSB)

b_{n-1} is the Most Significant Bit (MSB)

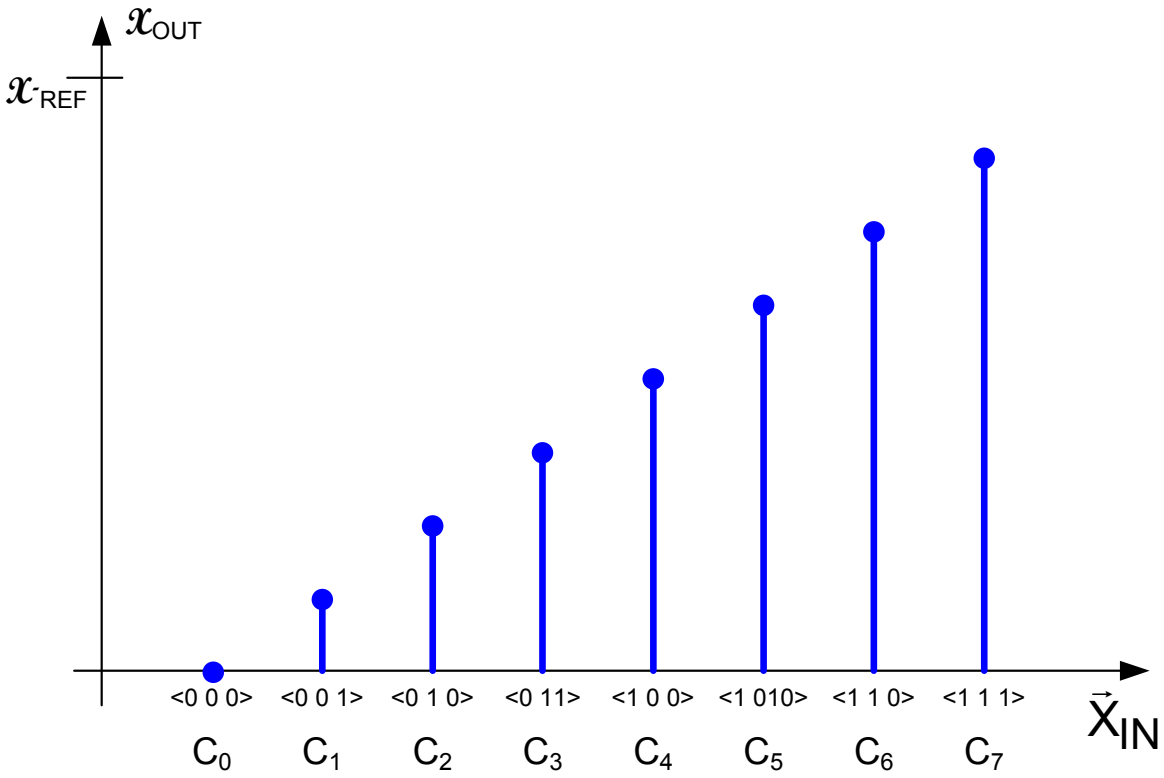
Note: some authors use different index notation

An Ideal DAC is characterized at low frequencies by its static performance

D/A Converters

$\vec{X}_{IN}=<b_{n-1},b_{n-1},...b_1,b_0>$

An Ideal DAC transfer characteristic (3-bits)

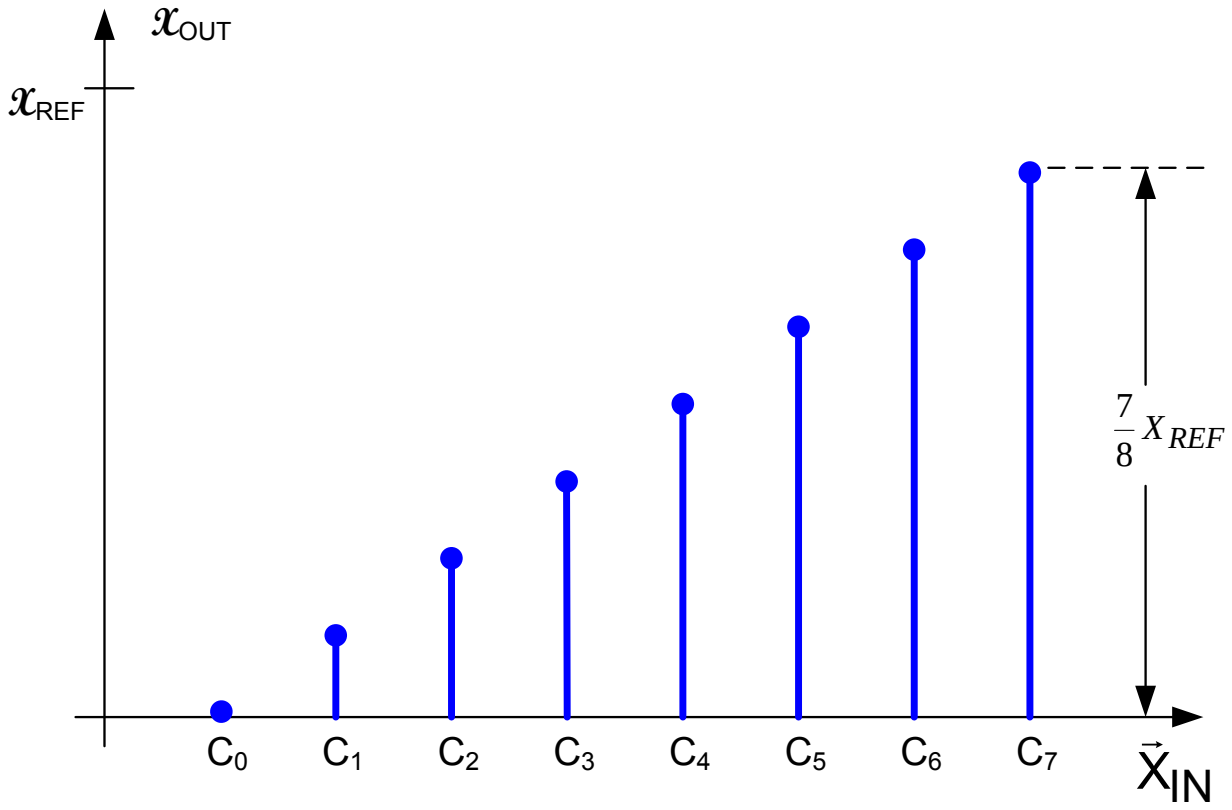


Code C_k is used to represent the decimal equivalent of the binary number $<b_{n-1} .. b_0)>$

D/A Converters

$\vec{X}_{IN}=<b_{n-1},b_{n-1},...b_1,b_0>$

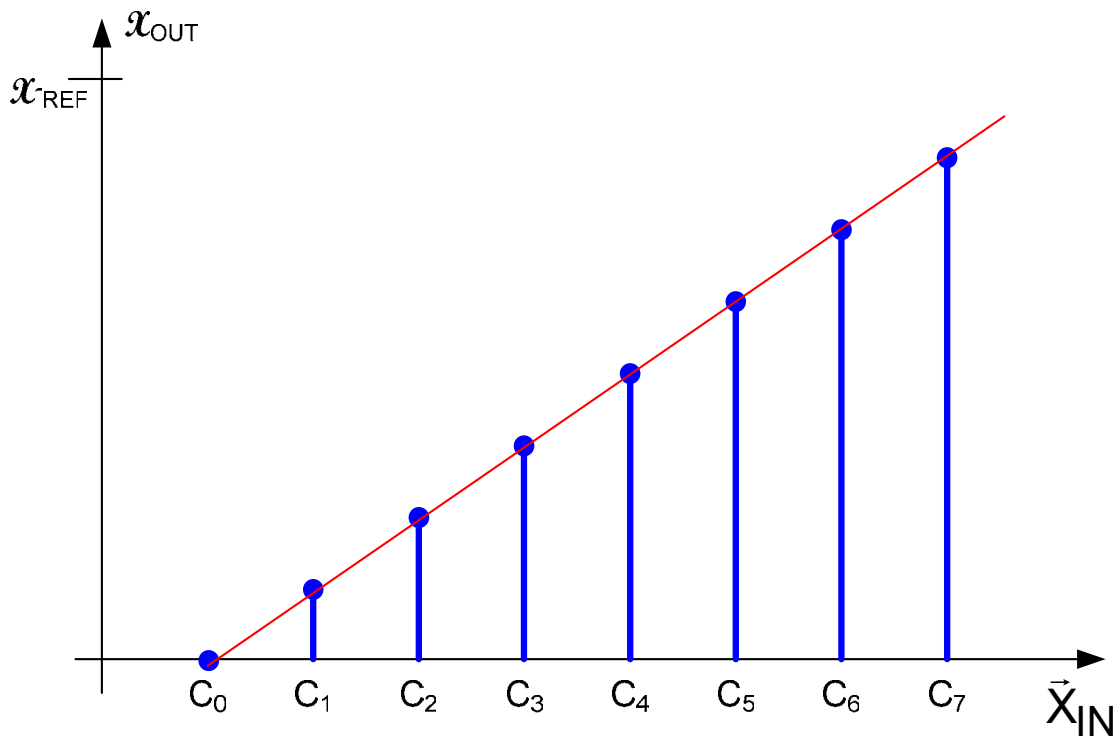
An Ideal DAC transfer characteristic (3-bits)



D/A Converters

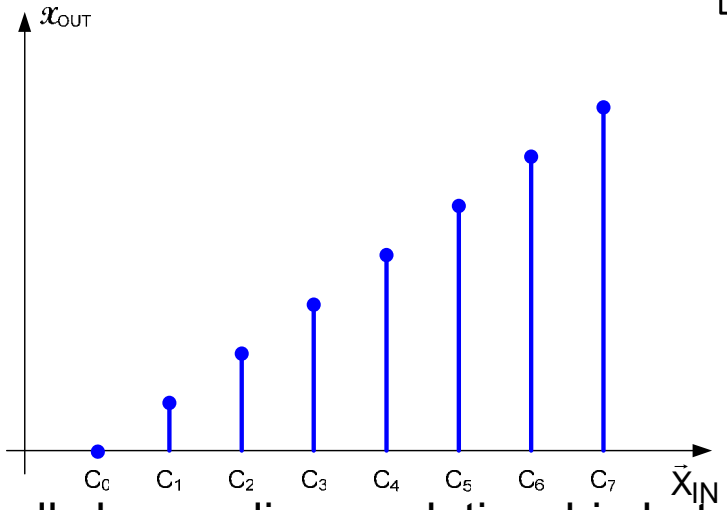
$\vec{X}_{IN}=<b_{n-1},b_{n-1},...b_1,b_0>$

An Ideal DAC transfer characteristic (3-bits)



All points of this ideal DAC lie on a straight line

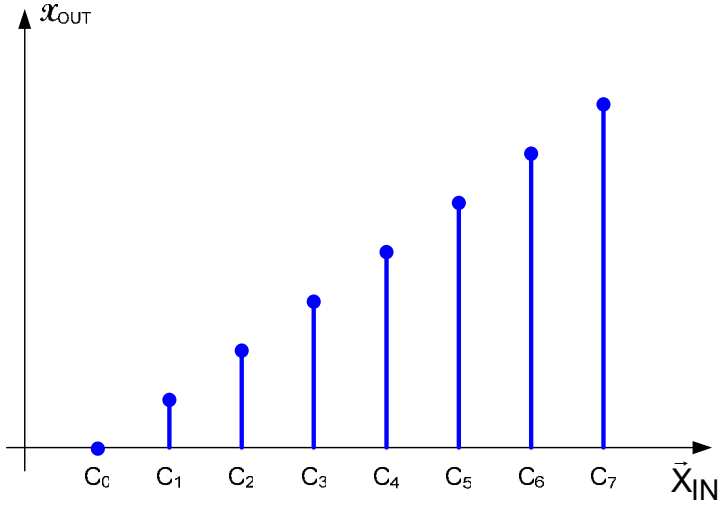
D/A Converters



- Most D/A ideally have a linear relationship between binary input and analog output
- Output represents a discrete set of continuous variables
- Typically this number is an integral power of 2, i.e. 2^n
- $\vec{X}_{IN}$ is always dimensionless

- x_{OUT} could have many different dimensions
- An ideal nonlinear characteristic is also possible (waveform generation and companding)
- Will assume a linear transfer characteristic is desired unless specifically stated to the contrary

D/A Converters



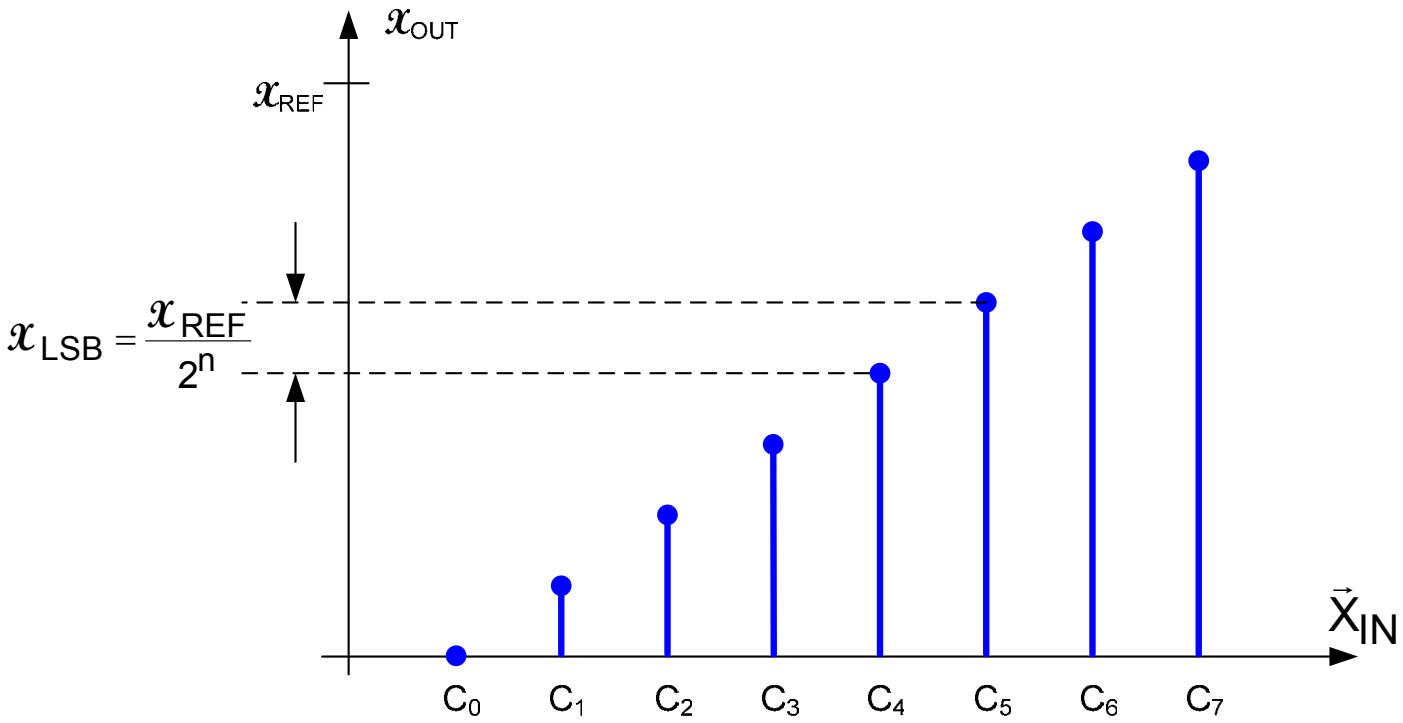
For this ideal DAC

$$X_{OUT} = X_{REF}\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \frac{b_{n-3}}{8} + \ldots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right)$$

$$X_{OUT} = X_{REF}\sum_{j=1}^{n}\frac{b_{n-j}}{2^j}$$

- Number of outputs gets very large for n large
- Spacing between outputs is $X_{REF}/2^n$ and gets very small for n large

D/A Converters

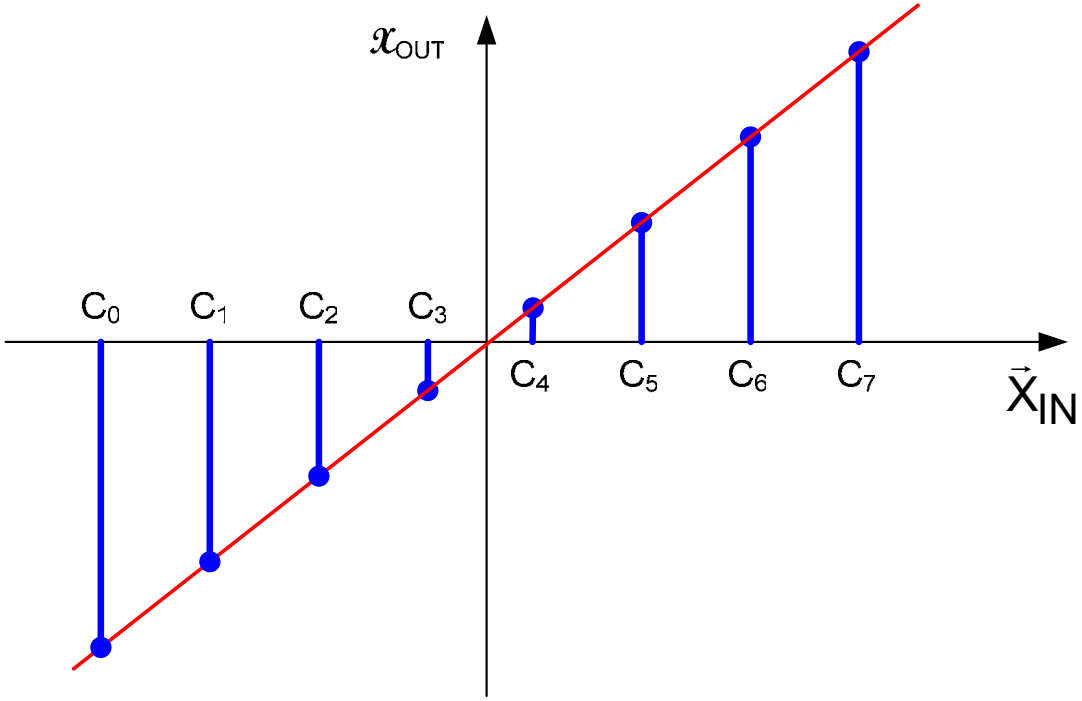


- Ideal steps all equal and termed the LSB
- x_{LSB} gets very small for small x_{REF} and large n

e.g. If x_{REF}=1V and n=16, then N=2^{16} =65,536, x_{LSB}=15.25μV

D/A Converters

An alternate ideal 3-bit DAC

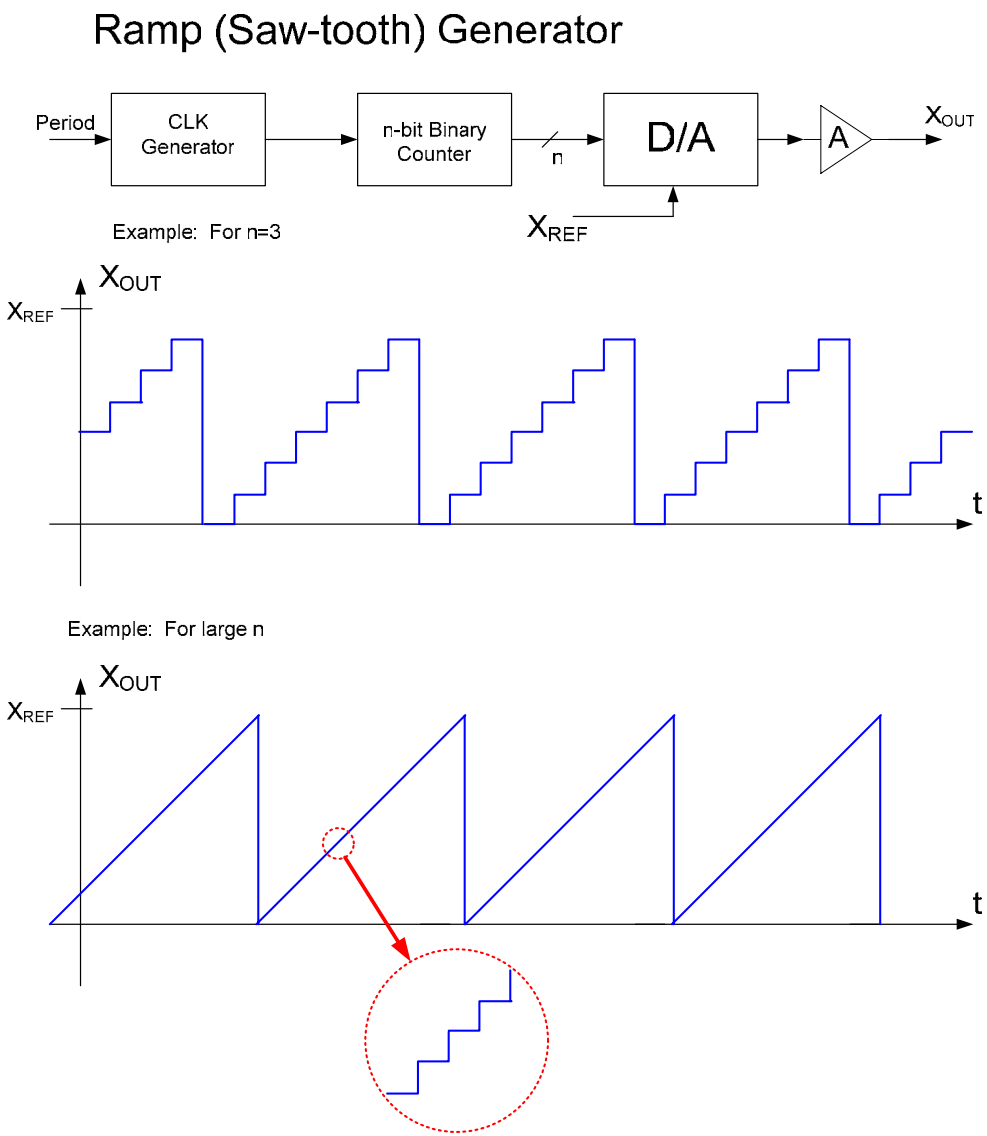


Irrespective of which form is considered, the increment in the output for one Boolean bit change in the input is x_{LSB} and the total range is 1LSB less than x_{REF}

Applications of DACs

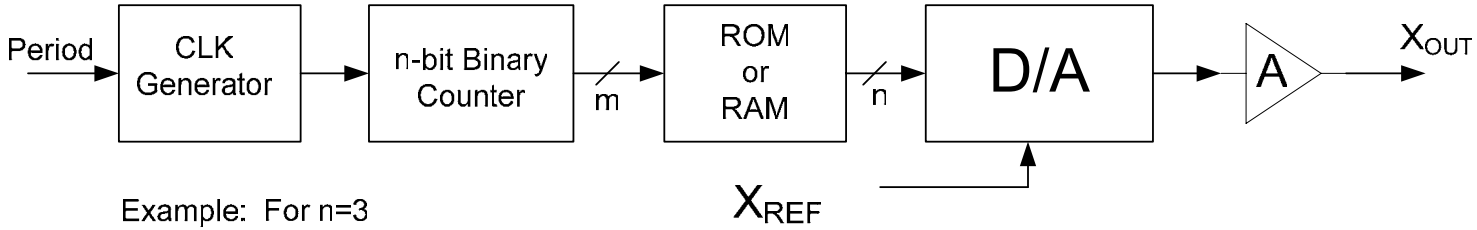
- Waveform Generation
- Voltage Generation
- Analog Trim or Calibration
- Industrial Control Systems
- Feedback Element in ADCs
- ….

Waveform Generation with DACs

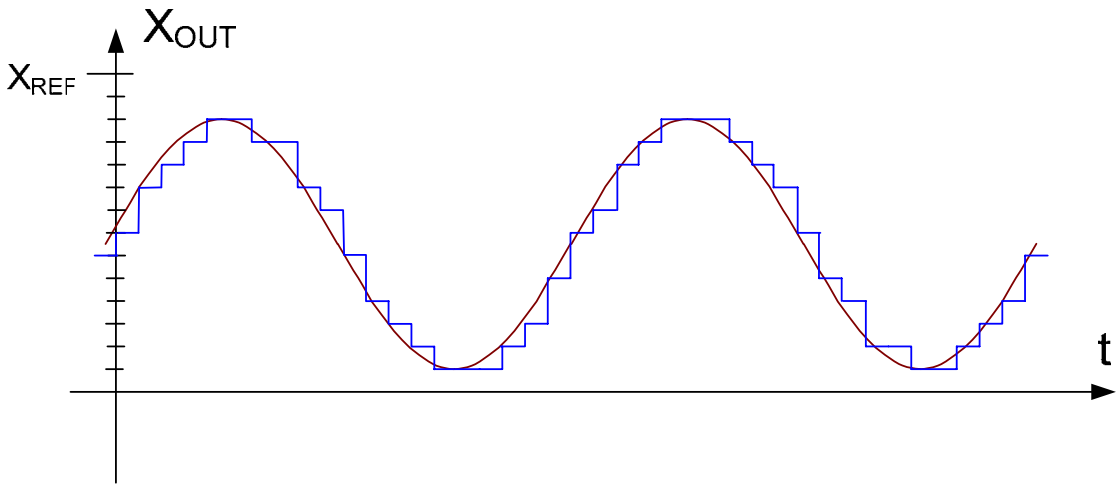


Waveform Generation with DACs

Sine Wave Generator



Example: For n=3

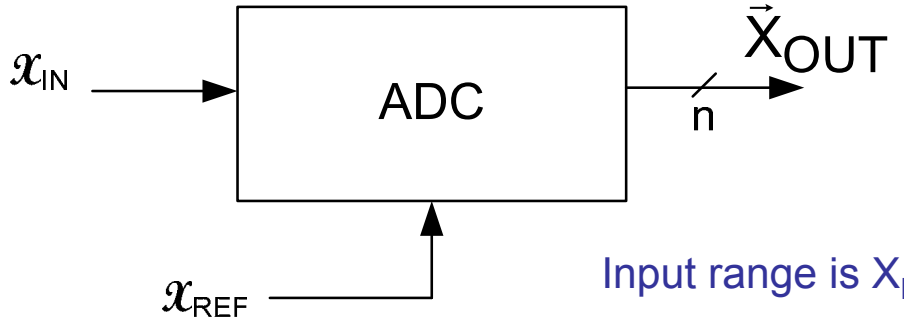


Distortion of the desired waveforms occurs due to both time and amplitude quantization

Often a filter precedes or follows the buffer amplifier to smooth the output waveform

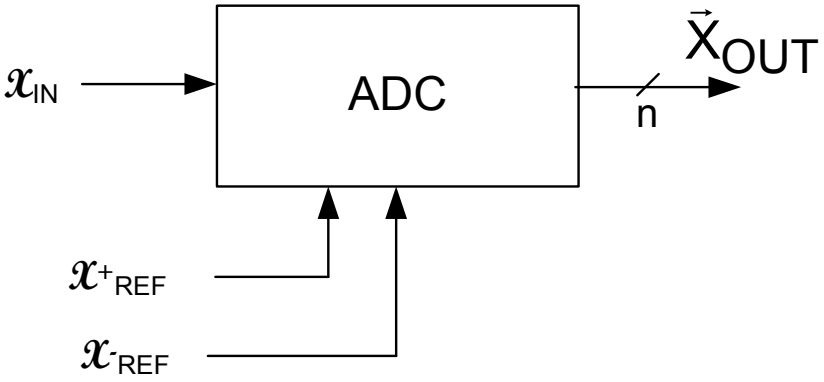
A/D Converters

Basic structure:

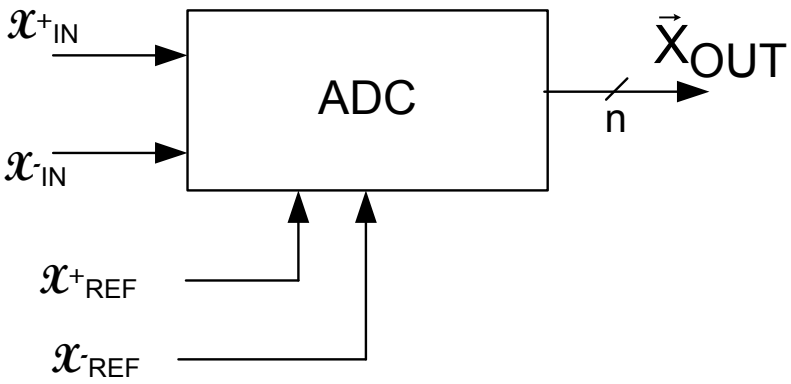


Input range is X_{REF}

Basic structure with differential inputs/references:



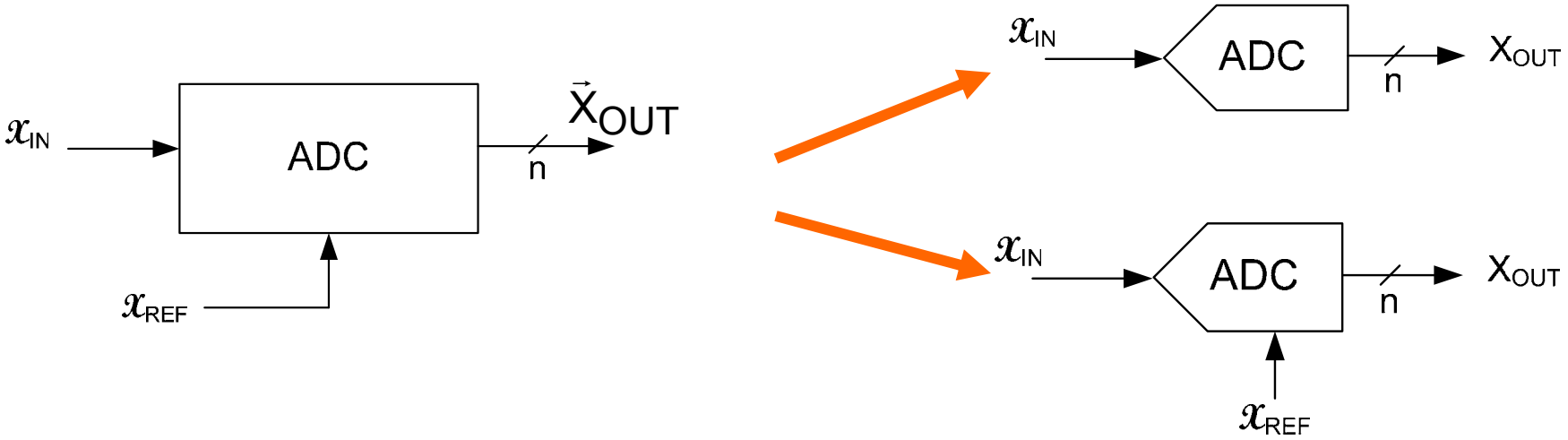
Input range is $X^+_{REF} - X^-_{REF}$



Input range is $2(X^+_{REF} - X^-_{REF})$

A/D Converters

Notation:



A/D Converters

$$\vec{X}_{OUT} = \langle d_{n-1}, d_{n-2}, \ldots d_0 \rangle$$

d_0 is the Least Significant Bit (LSB)

d_{n-1} is the Most Significant Bit (MSB)

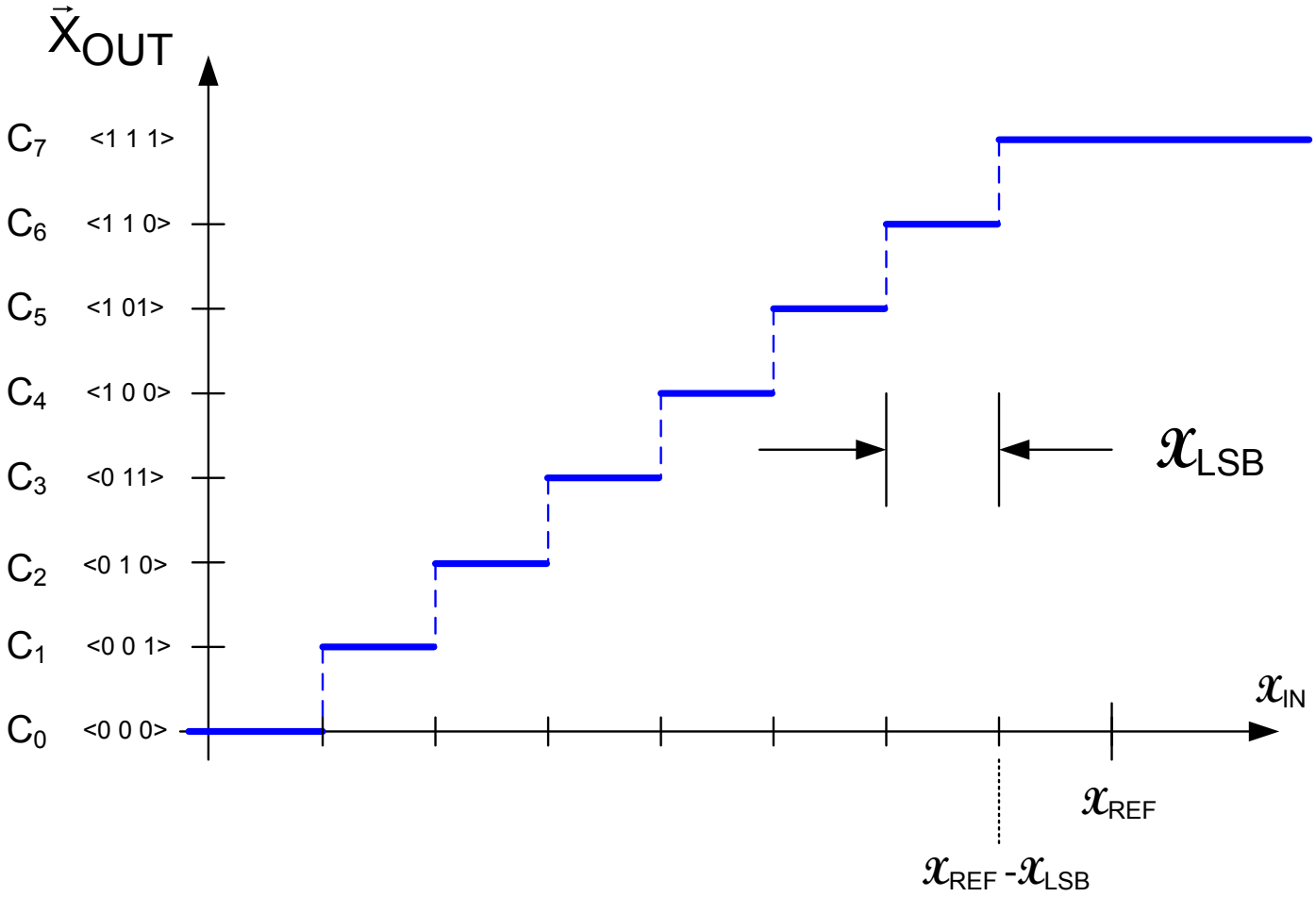
Notes:
Indexing notation reversed from what we used for DAC
some authors use different index notation

An Ideal ADC is characterized at low frequencies by its static performance

A/D Converters

An Ideal ADC transfer characteristic (3-bits)

$$\vec{X}_{OUT} = \langle d_{n-1}, d_{n-2}, \ldots d_0 \rangle$$

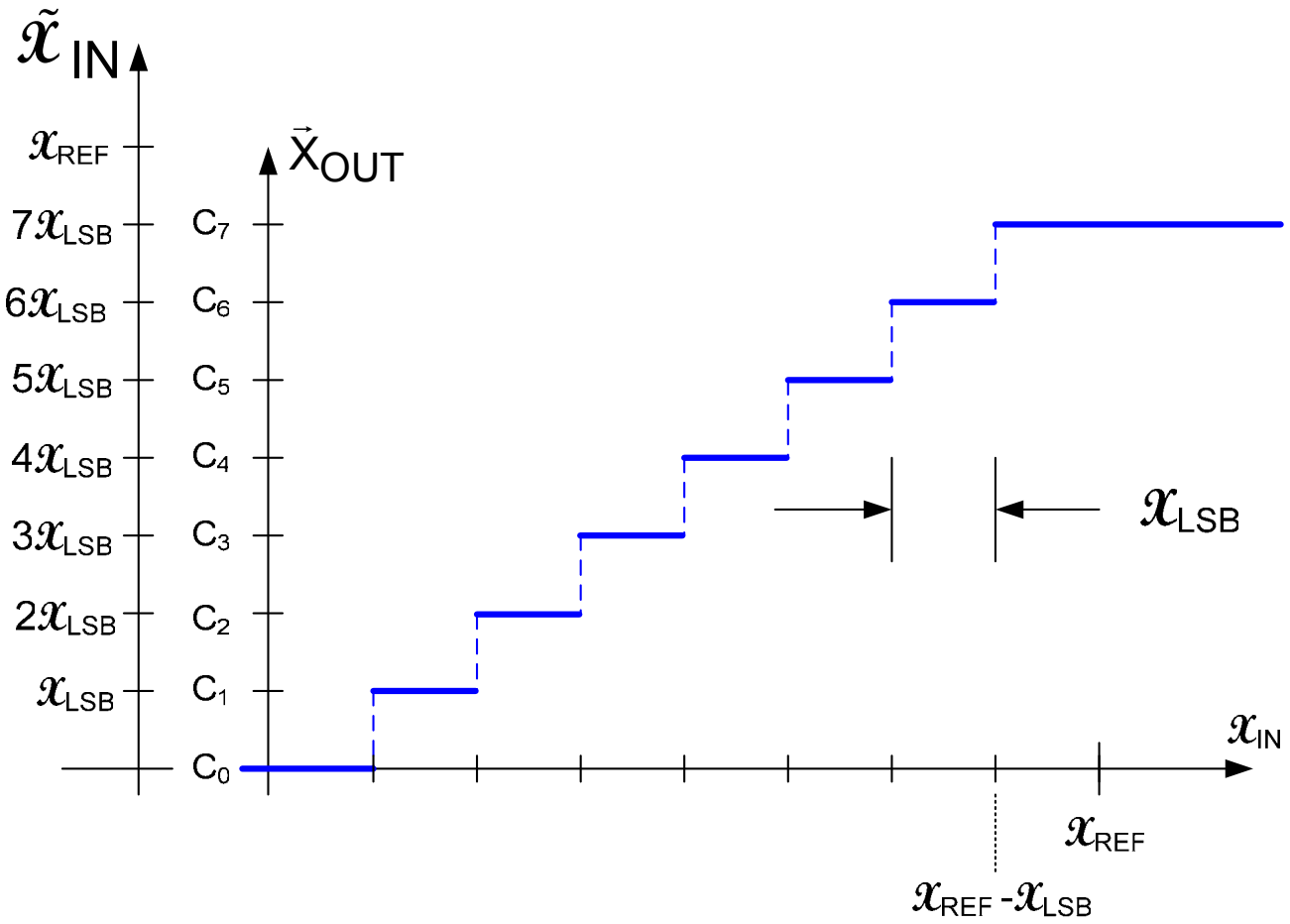


$$x_{LSB} = \frac{x_{REF}}{2^n}$$

A/D Converters

An Ideal ADC transfer characteristic (3-bits)

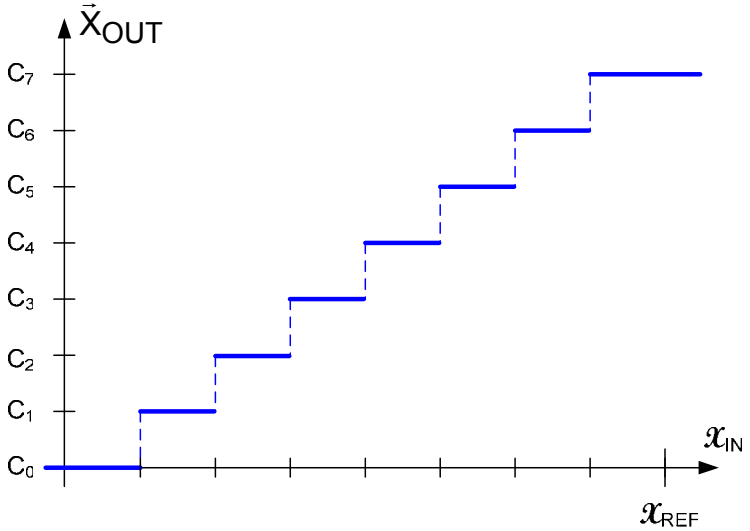
$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$



$$x_{LSB} = \frac{x_{REF}}{2^n}$$

The second vertical axis, labeled $\tilde{x}_{IN}$ is the interpreted value of x_{IN}

A/D Converters



For this ideal ADC

$$x_{IN} = x_{REF}\left(\frac{d_{n-1}}{2} + \frac{d_{n-2}}{4} + \frac{d_{n-3}}{8} + \ldots + \frac{d_1}{2^{n-1}} + \frac{d_0}{2^n}\right) + \varepsilon$$

where ε is small (typically less than 1LSB)

$$x_{IN} = x_{REF}\sum_{j=1}^{n}\frac{d_{n-j}}{2^j} + \varepsilon$$

- Number of bins gets very large for n large
- Spacing between break points is $x_{REF}/2^n$ and gets very small for n large

ε is the **quantization error** and is inherent in any ADC