EE 505

Lecture 12

DAC Design

- DAC Architectures
- Sring DACs

Review from last lecture

Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry

Review from last lecture

Summary of Offset Voltage Issues

- Random offset voltage is generally dominant and due to mismatch in device and model parameters
- MOS Devices have large V_{OS} if area is small
- σ decreases approximately with $1/\sqrt{A}$
- Multiple fingers for MOS devices offer benefits for common centroid layouts but too many fingers will ultimately degrade offset because perimeter/area ration will increase (A_W and A_L will become of concern)
- Offset voltage of dynamic comparators is often large and analysis not straightforward
- Offset compensation often used when low offsets important

MOS:

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTOn}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTOp}\right]$$

Bipolar:

$$\sigma^2_{V_{OS}} \cong 2V_t^2\left[\frac{A^2_{Jn}}{A_{En}} + \frac{A^2_{Jp}}{A_{Ep}}\right]$$

DAC Architectures

Types (Nyquist Rate)

- Voltage Scaling
  - Resistor String DACs (string DACs)
  - Interpolating
- Current Steering
  - Binary Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented
- Charge Redistribution
  - Switched Capacitor
- Serial
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined
- Integrating
- Resistor Switching
- MDACs (multiplying DACs)

Observations

- Yield Loss is the major penalty for not appropriately managing parasitics and matching and this loss can be ruthless
- The ultimate performance limit of essentially all DACs is the yield loss associated with parasitics and matching
- Many designers do not have or use good statistical models that accurately predict data converter performance
- If you work of a company that does not have good statistical device models
  - Convince model groups of the importance of developing these models
  - (or) develop appropriate test structures to characterize your process
- Existing nonlinear device models may not sufficiently accurately predict device nonlinearities for high-end data converter applications

DAC Architectures

Structures

- Hybrid or Segmented
- Mode of Operation
  - Current Mode
  - Voltage Mode
  - Charge Mode
- Self-Calibrating
  - Analog Calibration
    - Foreground
    - Background
  - Digital Calibration
    - Foreground
    - Background
  - Dynamic Element Matching
- Laser or Link Trimmed
- Thermometer Coded or Binary
- Radix 2 or non-radix 2
- Inherently Monotone

DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
    - Charge Redistribution
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored !
- Major challenge is in determining appropriate architecture and managing the parasitics

Nonideal Effects of Concern

- Matching
- Parasitic Capacitances

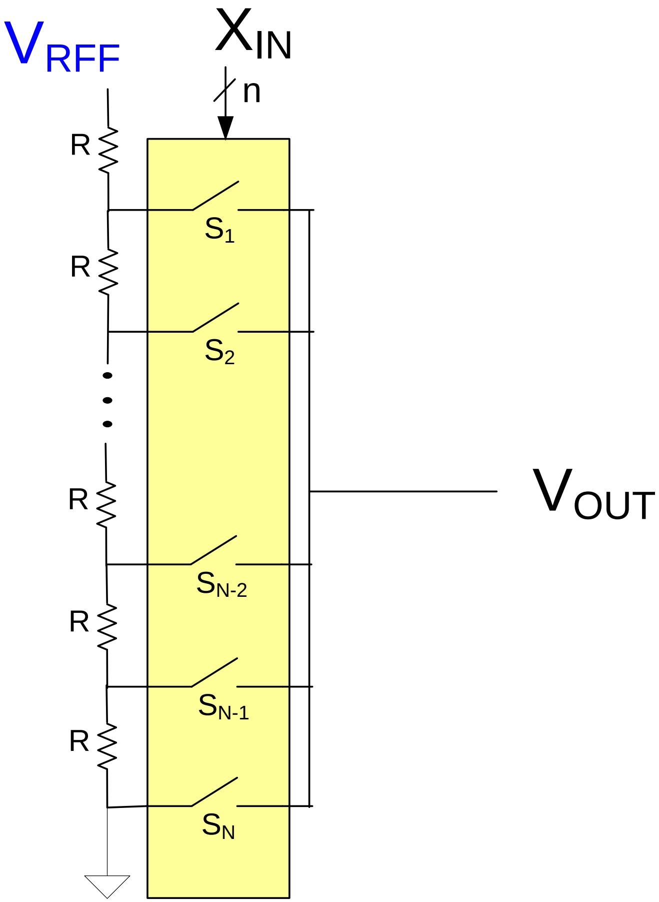
  (including Charge injection)
- Loading
- Nonlinearities
- Interconnect resistors
- Noise
- Speed
- Jitter
- Temperature Effects
- Aging
- Package stress

Observations

- Experienced Designers/Companies often produce superior data converter products
- Essentially all companies have access to the same literature, regularly reverse engineer successful competitors products and key benefits in successful competitors products are generally not locked up in patents
- High-end designs(speed and resolution) may get attention in the peer community but practical moderate performance converters usually make the cash flow
- Area (from a silicon cost viewpoint) is usually not the driving factor in high-end designs where attractive price/mfg cost ratios are common
- Considerable ongoing demand for data converter designers – particularly in ASICs where DAC optimized for specific application

DAC Architectures

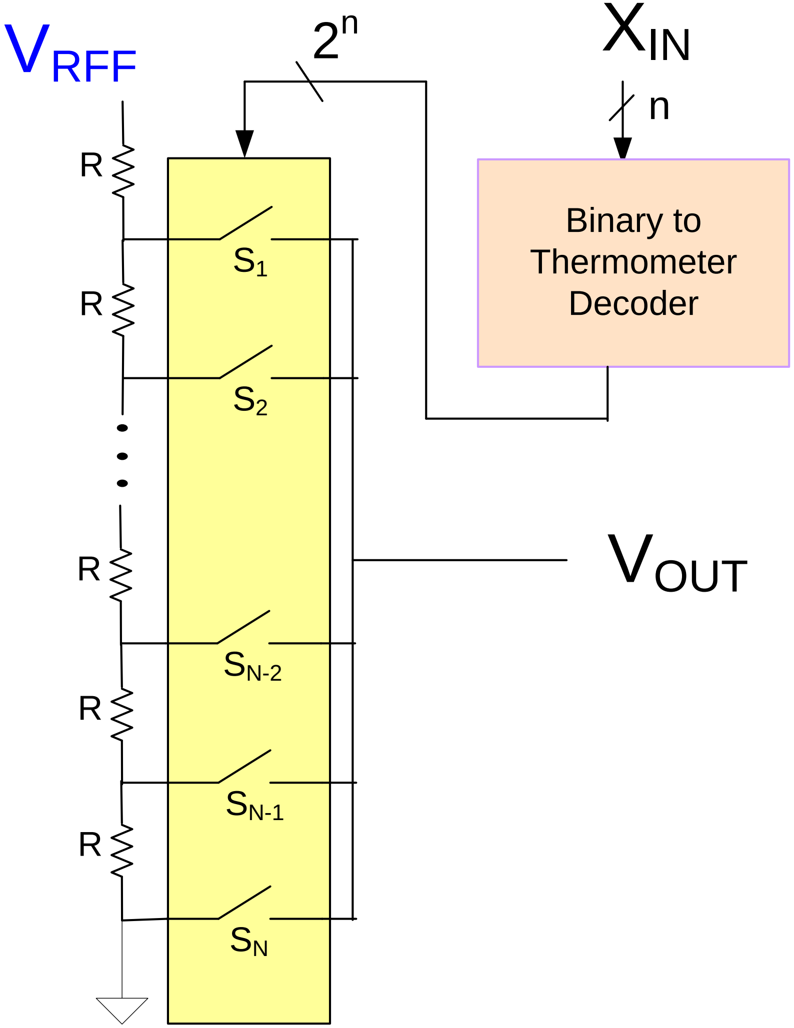
R-String



X_{IN} is decoded to close one switch

DAC Architectures

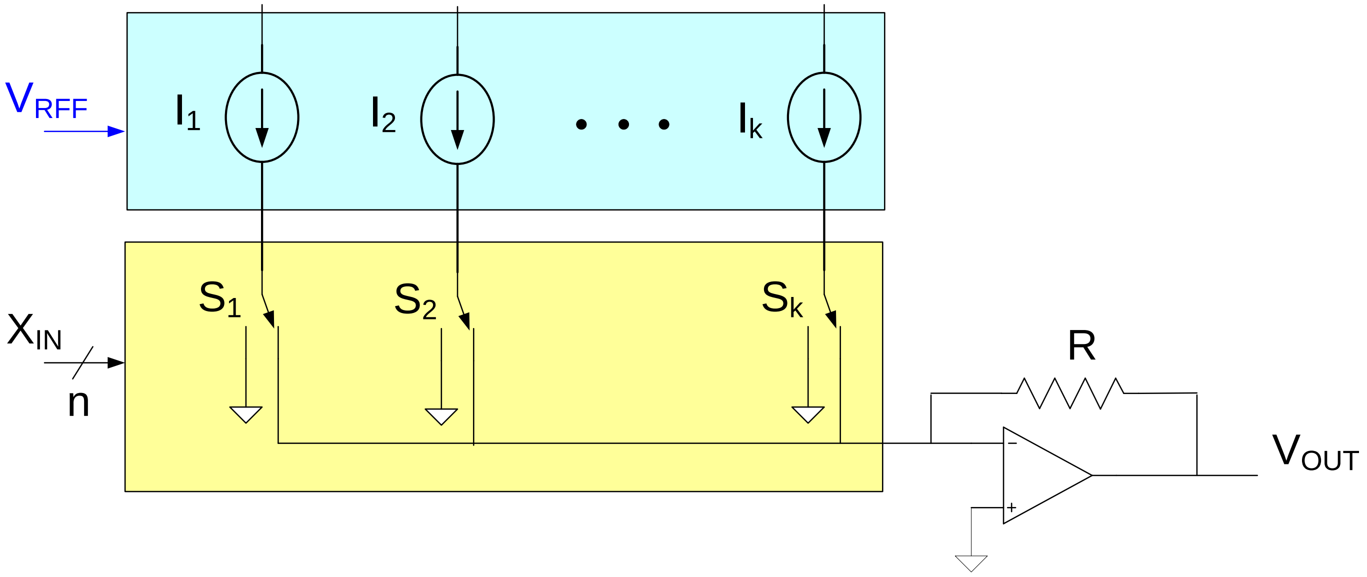
R-String



Basic R-String DAC including Logic to Control Switches

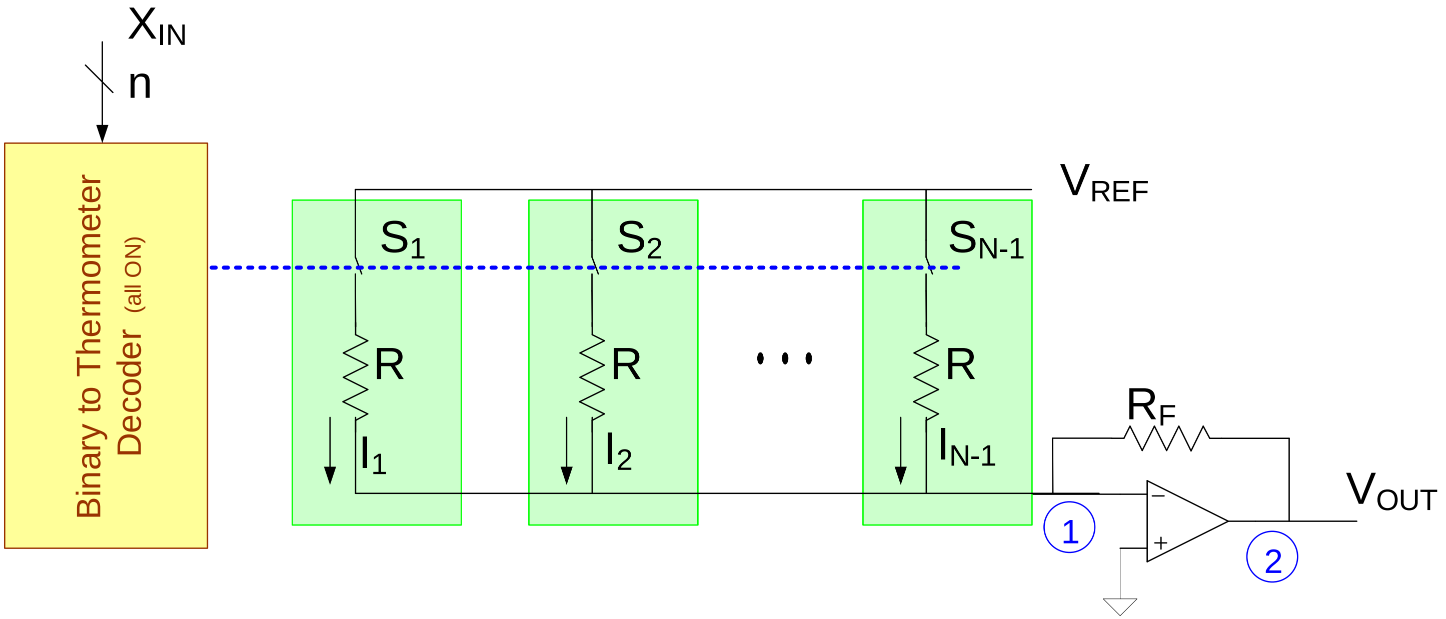
DAC Architectures

Current Steering



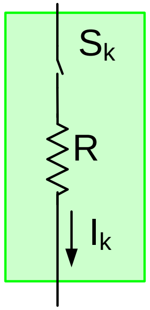
DAC Architectures

Current Steering



Inherently Insensitive to Nonlinearities in Switches and Resistors

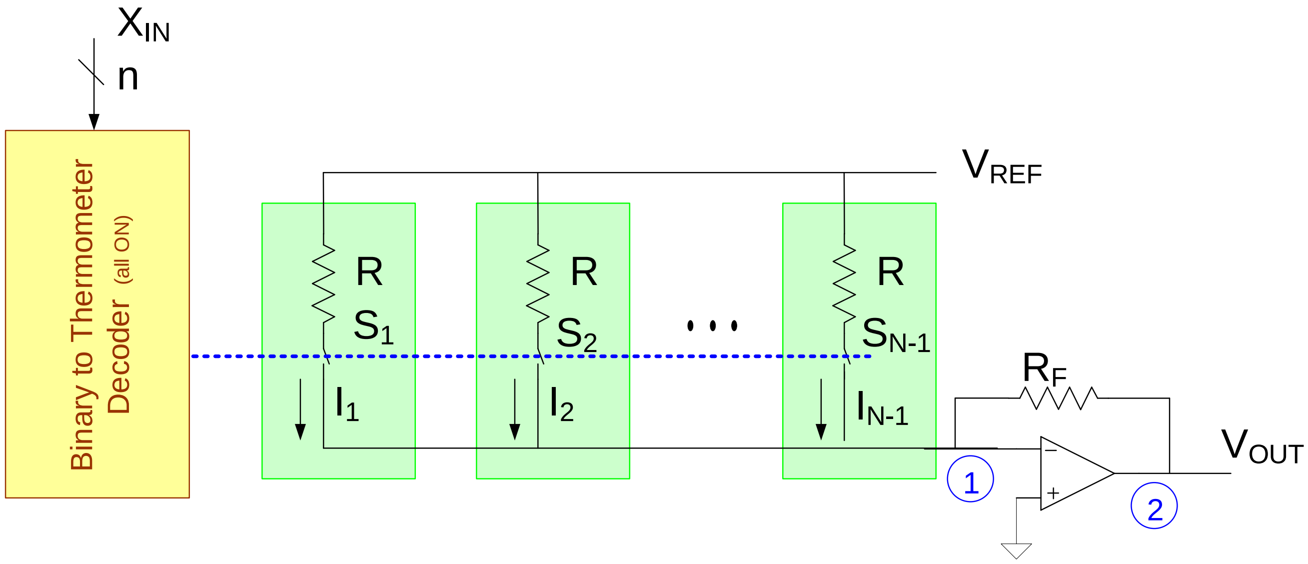
- Termed “top plate switching”
- Thermometer coded
- Based upon unary cell
- Speed limited by Op Amp and clock transients



Unary bit cell

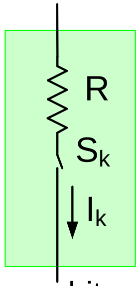
DAC Architectures

Current Steering



Inherently Insensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges

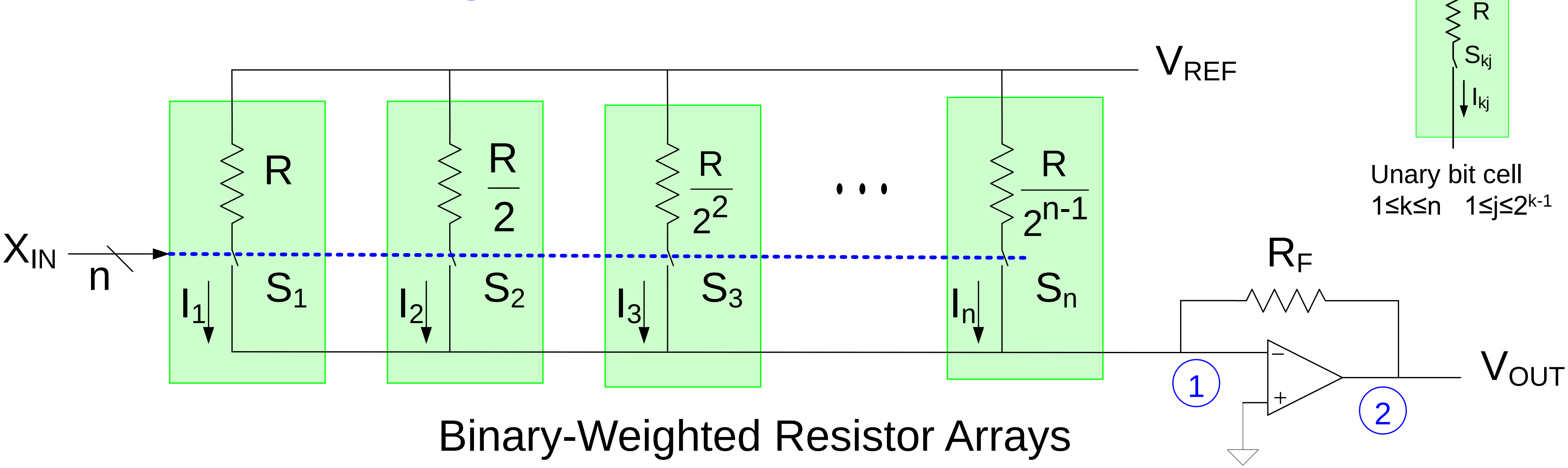
- Termed “bottom plate switching”
- Thermometer coded
- Based upon unary cell
- Speed limited by Op Amp



Unary bit cell

DAC Architectures

Current Steering



Unary bit cell

$1 \le k \le n \quad 1 \le j \le 2^{k-1}$

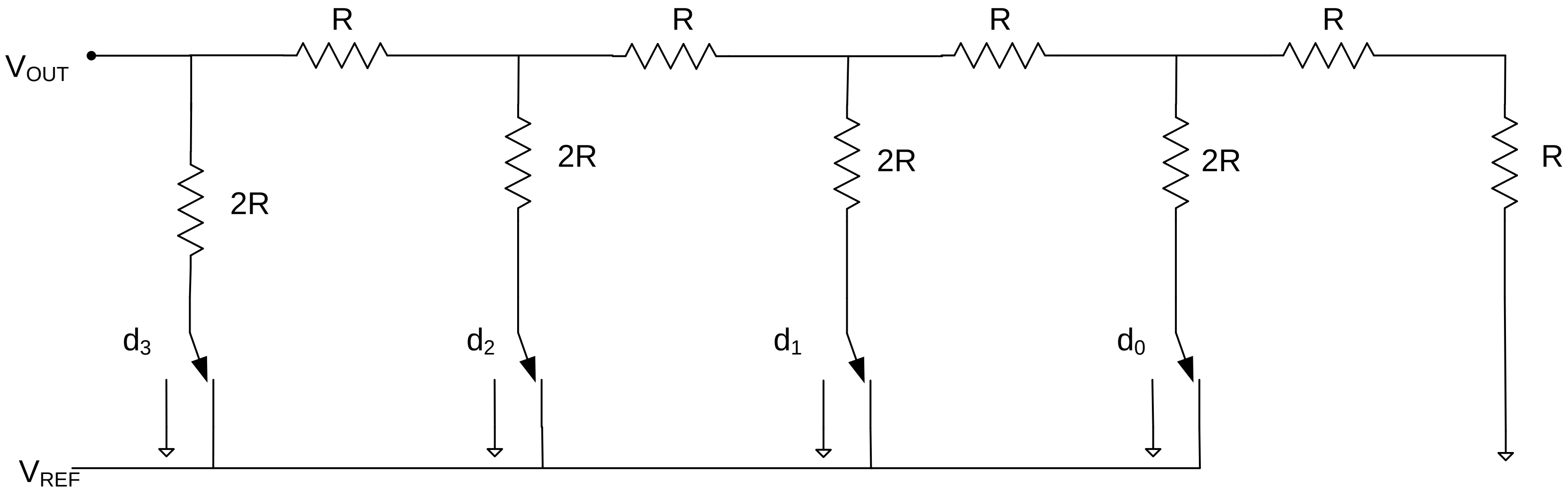
Binary-Weighted Resistor Arrays

- Unary bit cells usually bundled to make resistors
- Same number of unary cells needed as for thermometer coded structure
- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

DAC Architectures

R-2R (one variant) (4-bits shown)



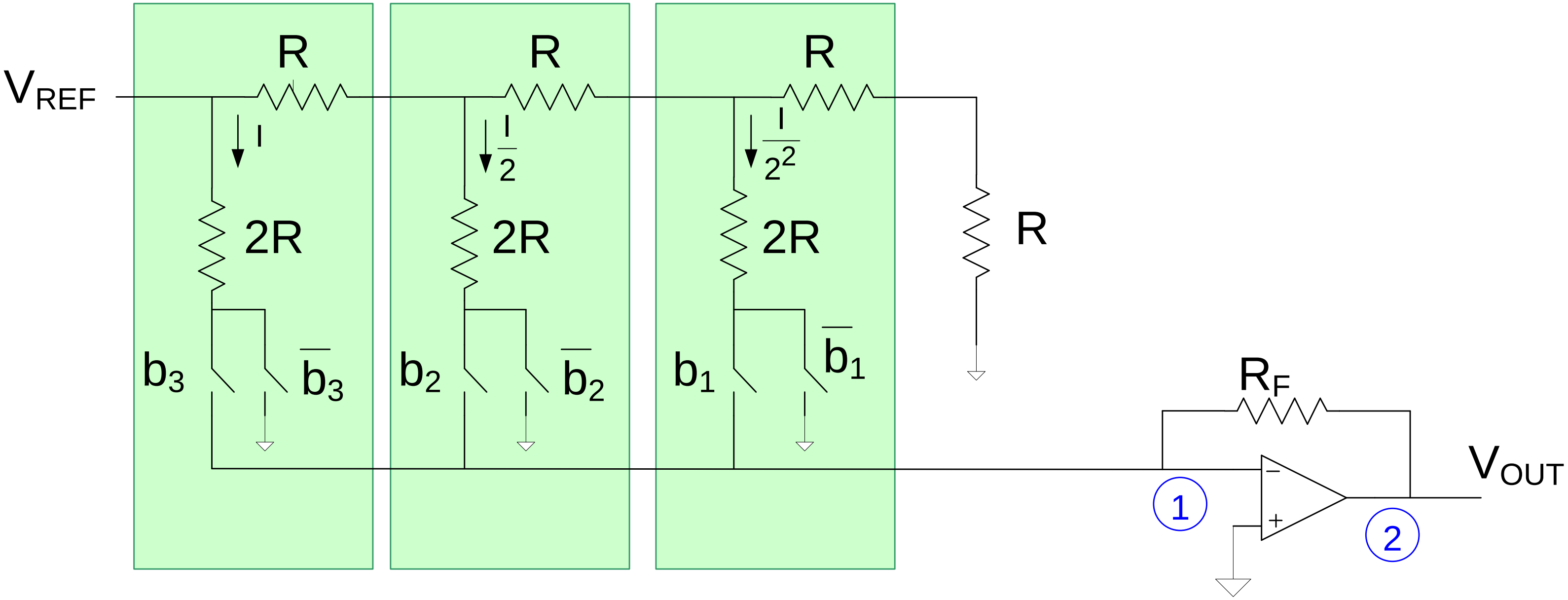
By superposition:

$$V_{OUT} = V_{REF} d_3 \bullet \frac{1}{2} + V_{REF} d_2 \bullet \frac{1}{4} + V_{REF} d_1 \bullet \frac{1}{8} + V_{REF} d_0 \bullet \frac{1}{16} = V_{REF} \sum_{k=0}^{3} \frac{d_k}{2^{4-k}} = V_{REF} \sum_{k=1}^{4} \frac{d_{4-k}}{2^k}$$

DAC Architectures

Current Steering

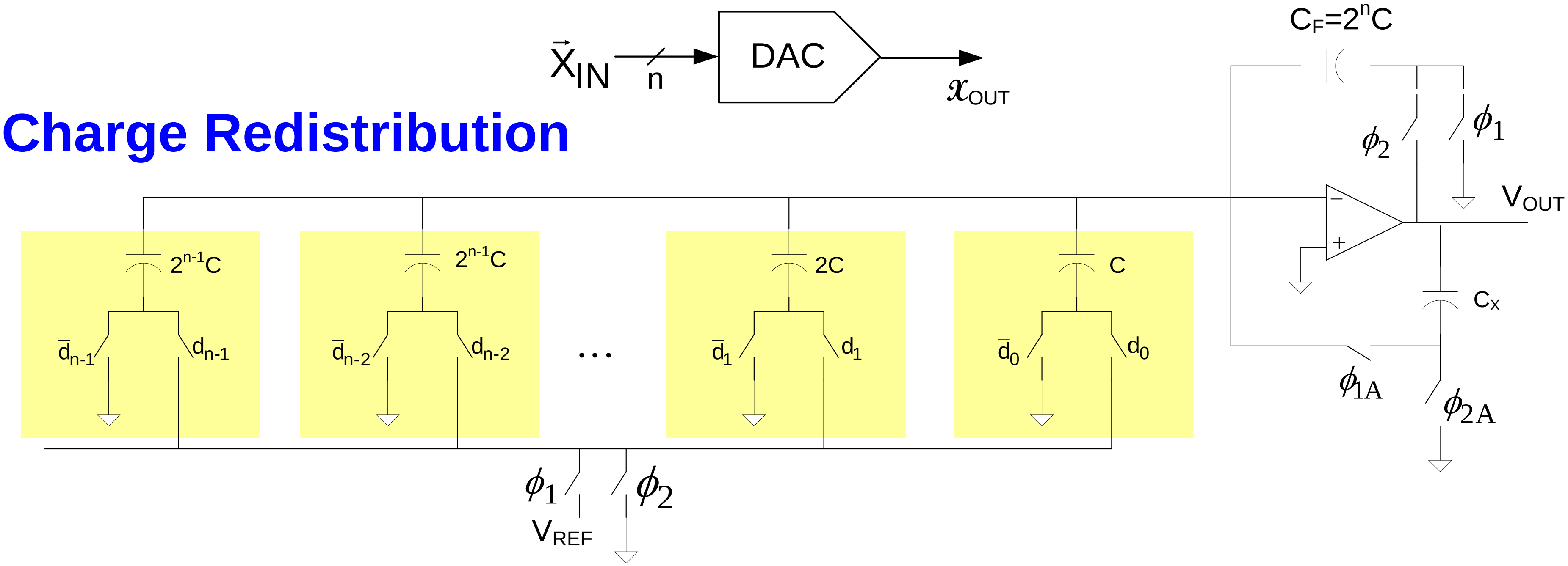
R-2R (another variant)

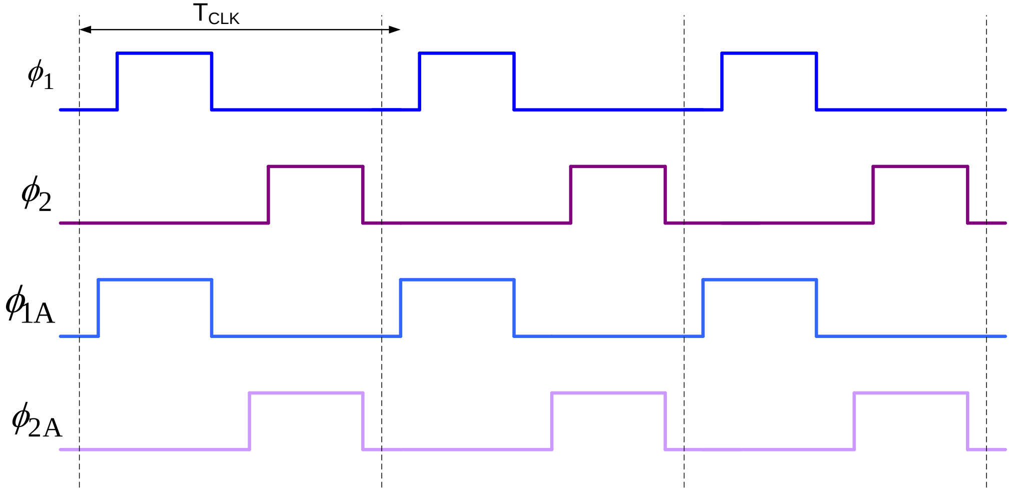


R-2R Resistor Arrays

DAC Architectures

Charge Redistribution





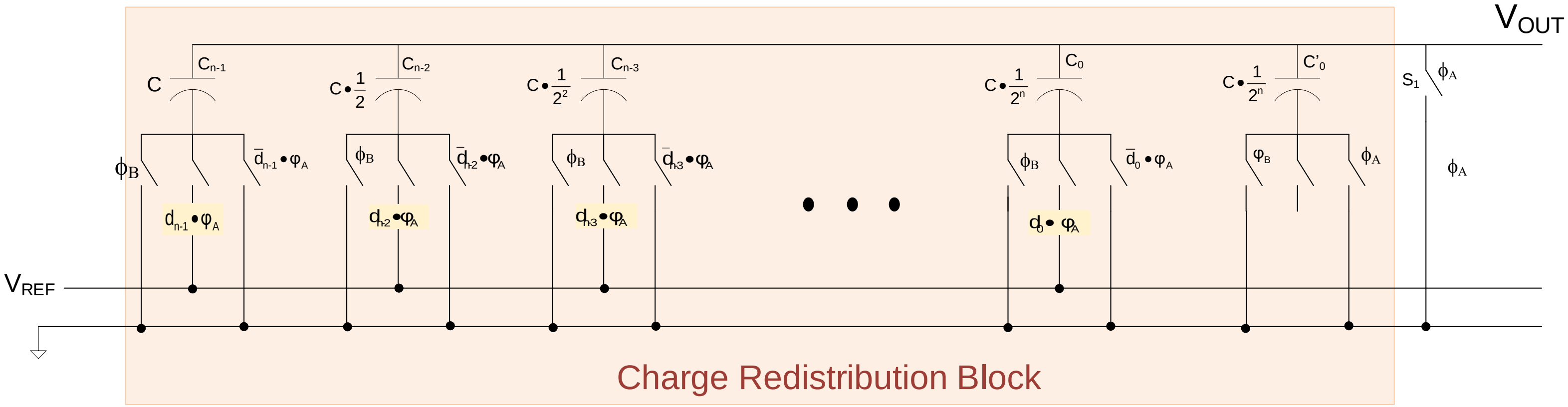
Unary cell used for capacitor array

C_X does some good things
(mitigates V_{OS}, 1/f noise and finite gain errors)

Will not consider C_X affects at this time

DAC Architectures

Charge Redistribution



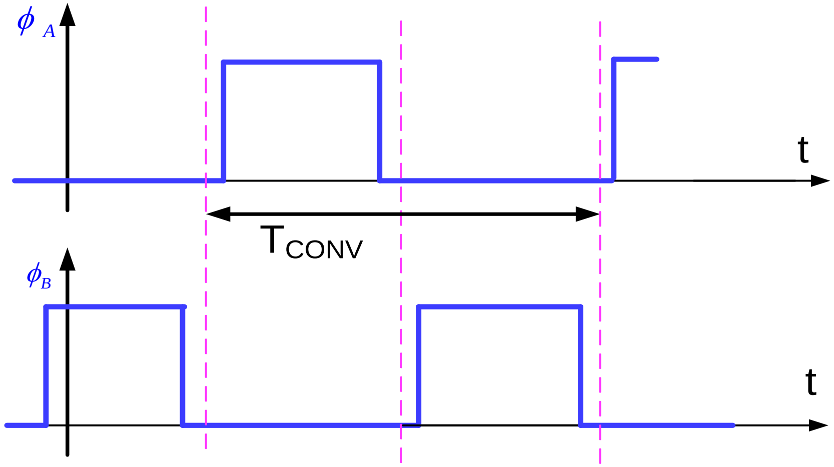
$$Q_{SET} = V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

$$Q_{RDIS} = V_{OUT}\left(\sum_{i=0}^{n-1} C_i + \left[C_0^{'}\right]\right) = V_{OUT}\left(\sum_{i=0}^{n-1}\frac{C}{2^{n-i}} + \left[\frac{C}{2^n}\right]\right) = V_{OUT}C$$

$$Q_{SET} = Q_{RDIS}$$

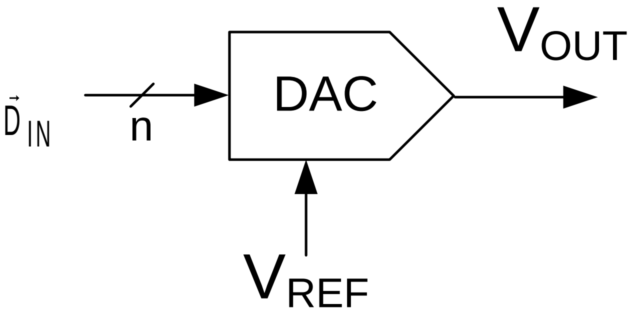
$$V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT}C$$

$$V_{OUT} = V_{REF}\sum_{i=0}^{n-1}\frac{d_i}{2^{n-i}}$$



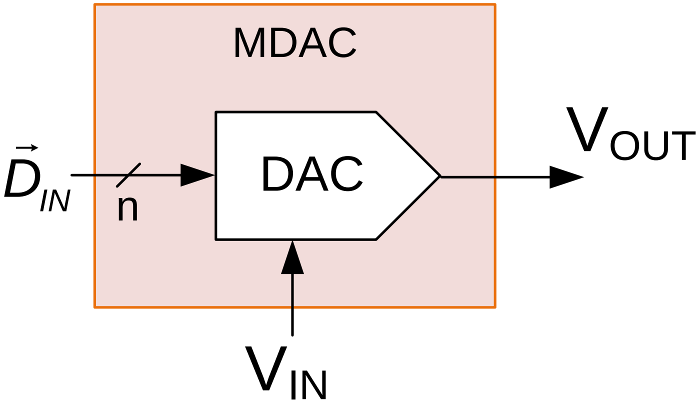
DAC Architectures

MDAC



V_{REF} fixed or limited range

$$V_{OUT} = V_{REF} \bullet \left[\vec{D}_{IN}\right]_{DECIMAL}$$



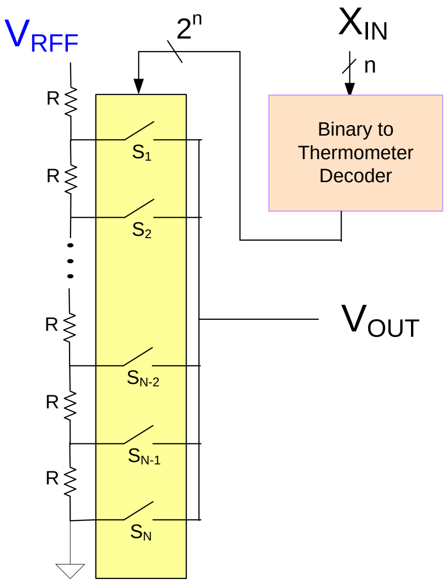
V_{IN} Variable, often positive or negative

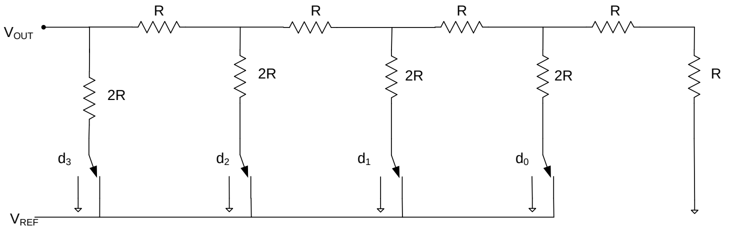
$$V_{OUT} = V_{IN} \bullet \left[\vec{D}_{IN}\right]_{DECIMAL}$$

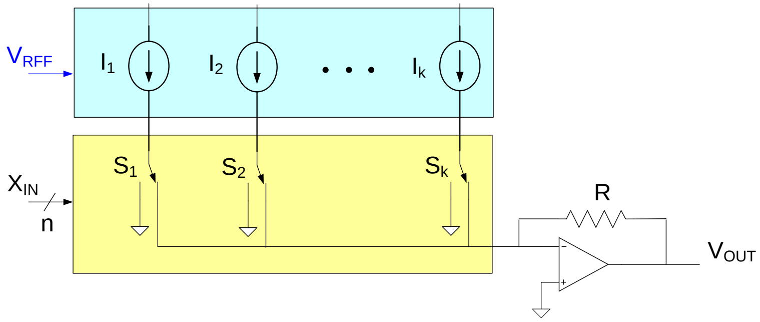
- Some define MDACs to be DAC structures that have current outputs
- Many DAC structures can perform well as a MDAC (possibly one quadrant)
- Performance of some DAC structures limited if V_{REF} is varied

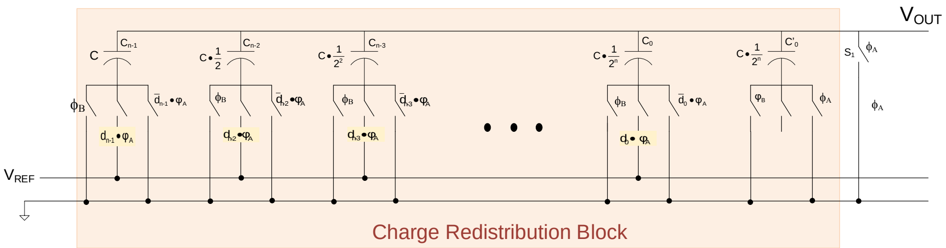
DAC Architectures

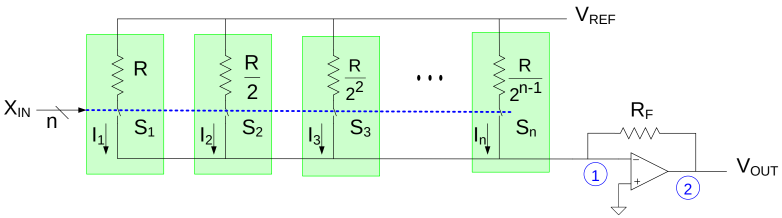
Suitable as MDAC?





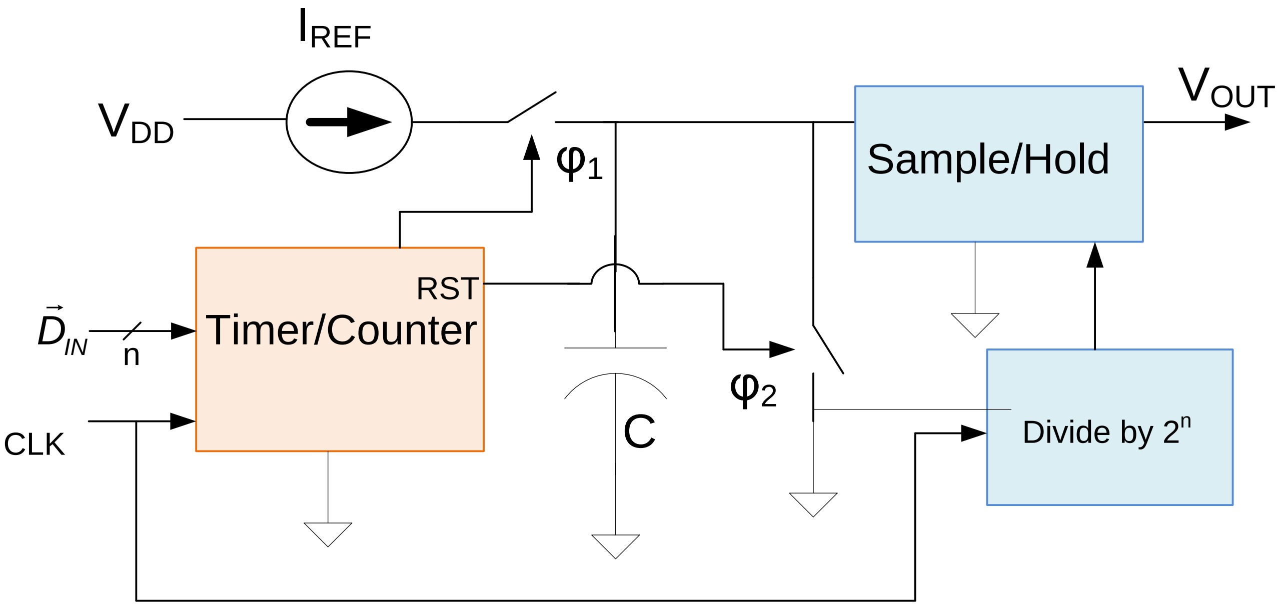






DAC Architectures

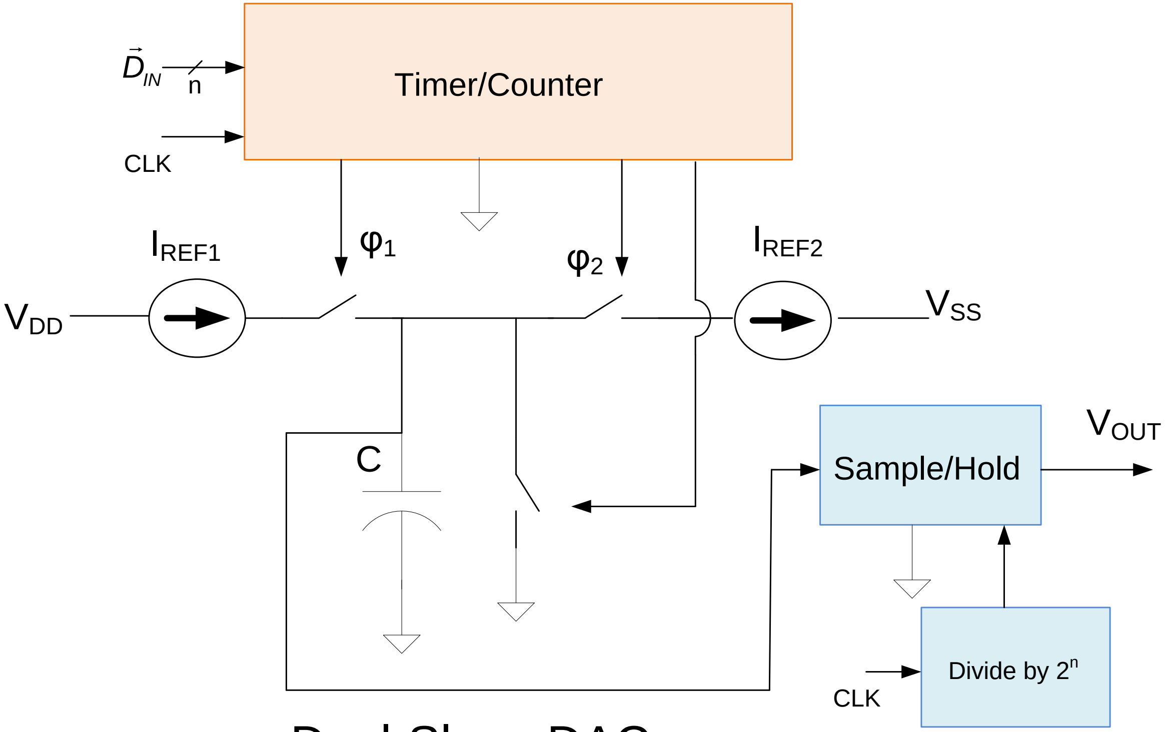
Single Slope



Single-Slope DAC

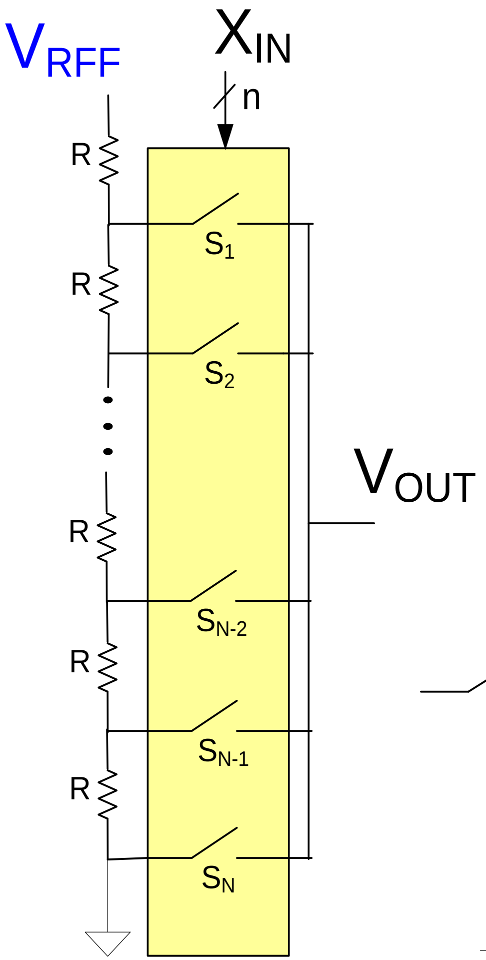
DAC Architectures

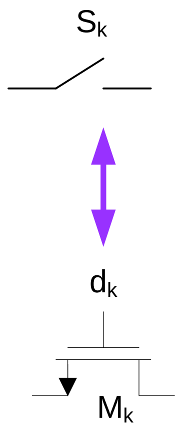
Dual Slope



Dual-Slope DAC

R-String DAC





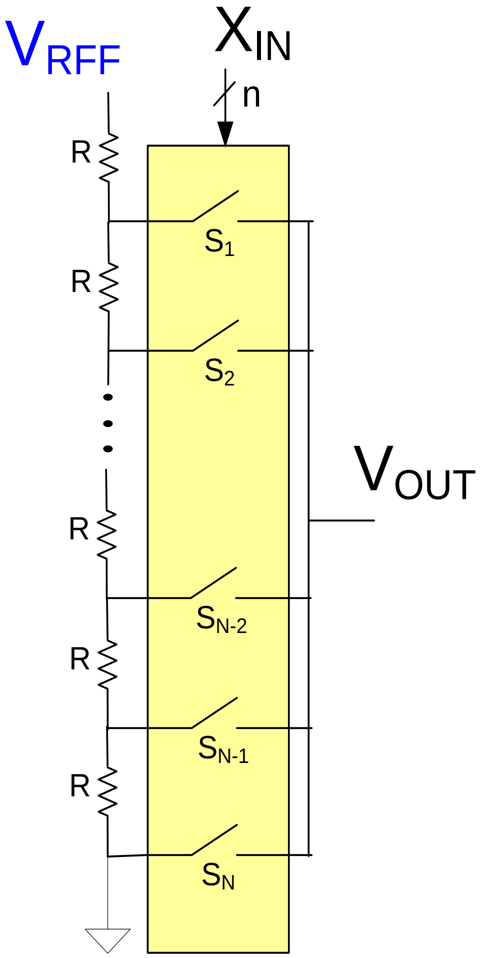
Conceptual

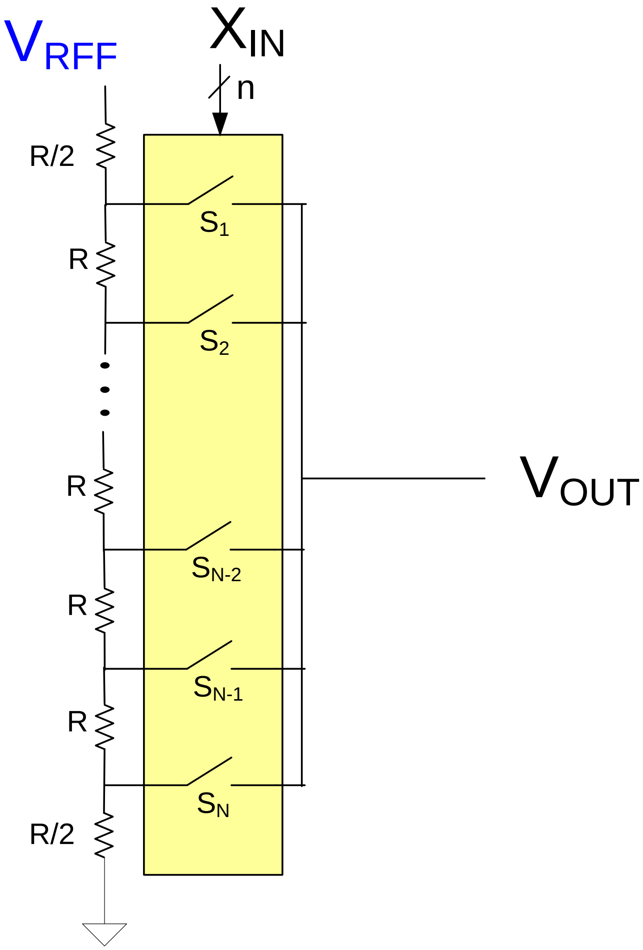
- ❑ Simple structure
- ❑ Inherently monotone
- ❑ Very low DNL
- ❑ Potential for being very fast
- ❑ Low Power Dissipation
- ❑ Widely Used Approach (with appropriate considerations)

Challenges:

- Managing INL
- Large number of devices for n large (2^n or 2^{n+1} lines)
- Decoder
- Routing thermometer/bubble clocks
- Transients during Boolean transitions
- Switch implementation
- Thevenin impedance facing V_{OUT} highly code dependent

R-String DAC

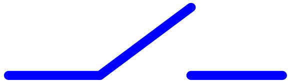




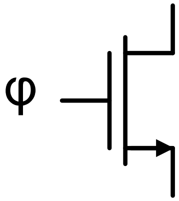
Practical level shift

Switch Implementation

Basic Switch

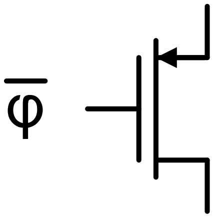


- Large number required for large resolution
- Simple structure often used



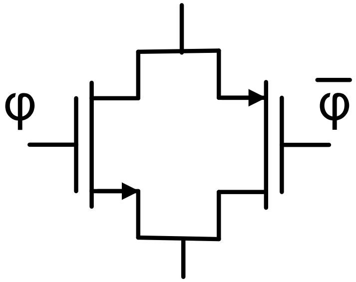
single n-channel device

- Good when switch terminals near gnd
- Will not turn on when terminals near V_{DD}



single p-channel device

- Good when switch terminals near V_{DD}
- Will not turn on when terminals near gnd

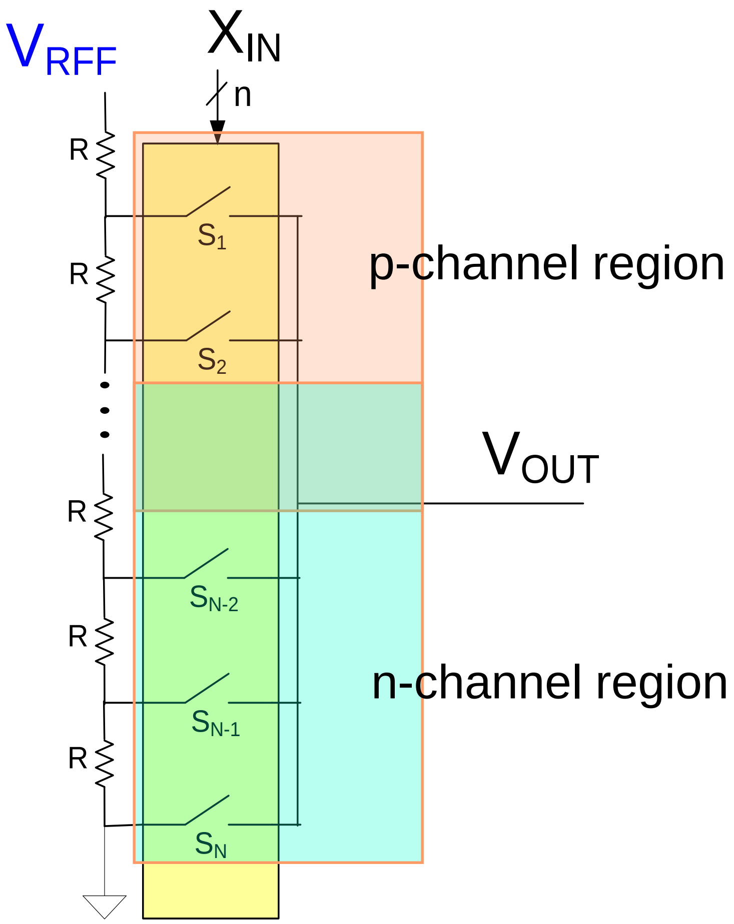


transmission gate switch

- Use devices where cross-over occurs
- Good for both high and low term voltages
- Extra clock signal required
- Try to avoid this complexity

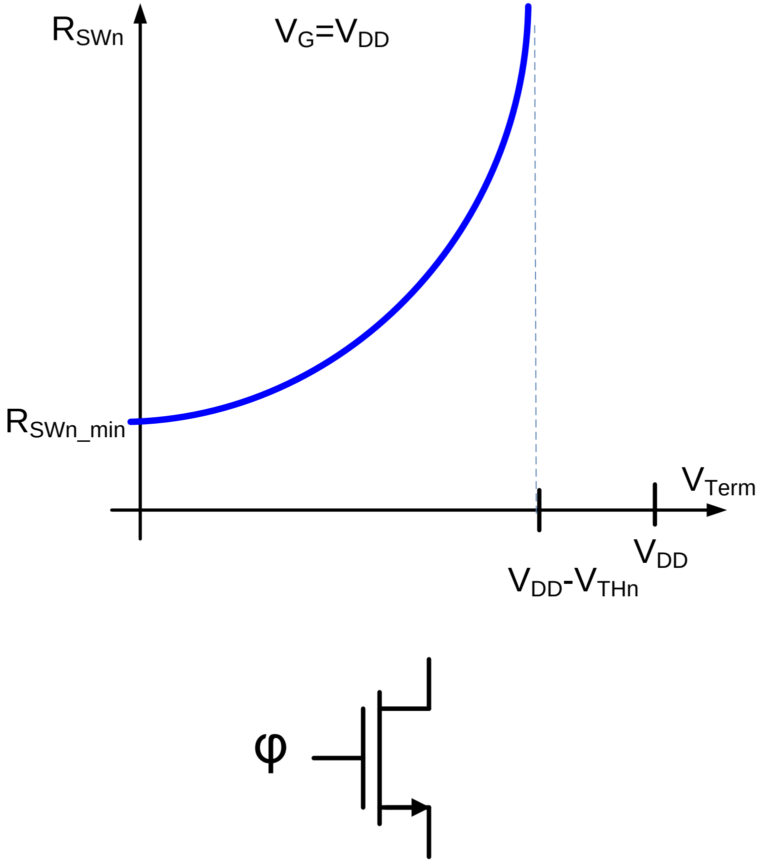
Other switch structures (such as bootstrapped switch) used but not for basic string DACs

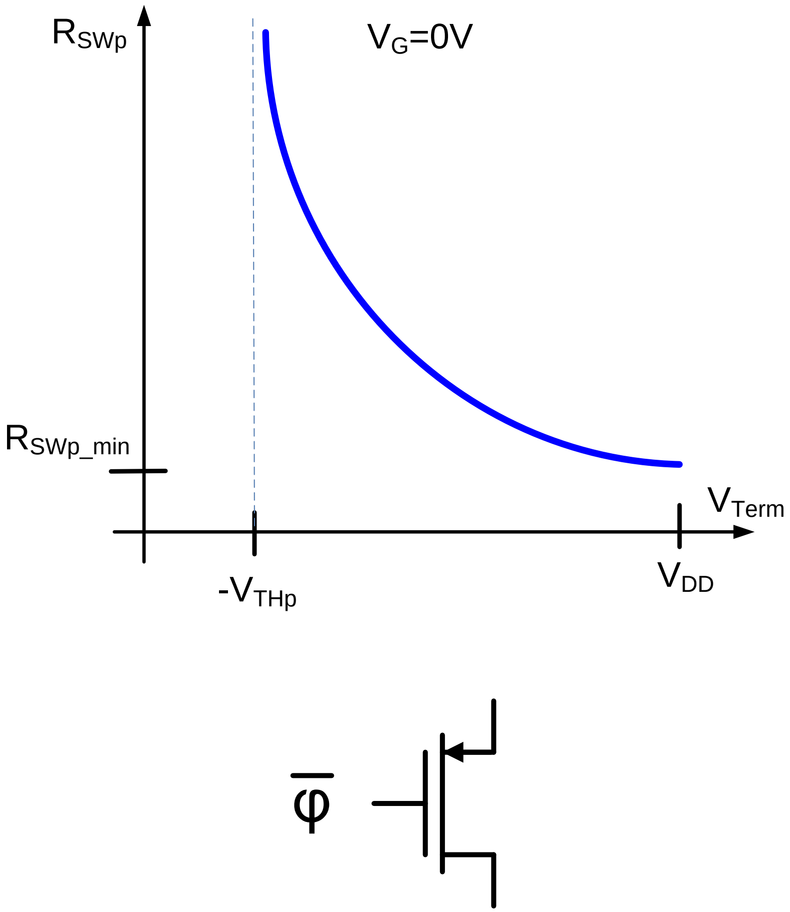
Switch Assignment



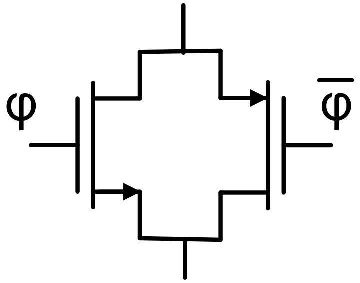
Challenges:

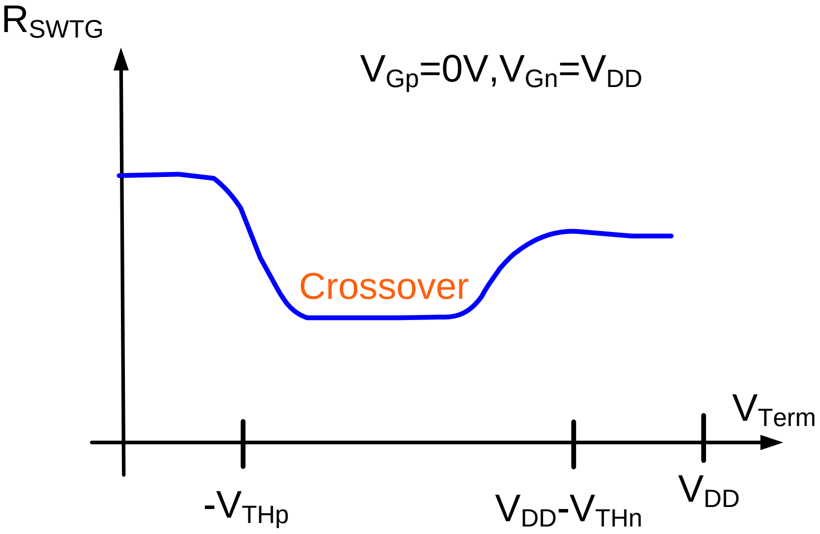
Switch Impedances

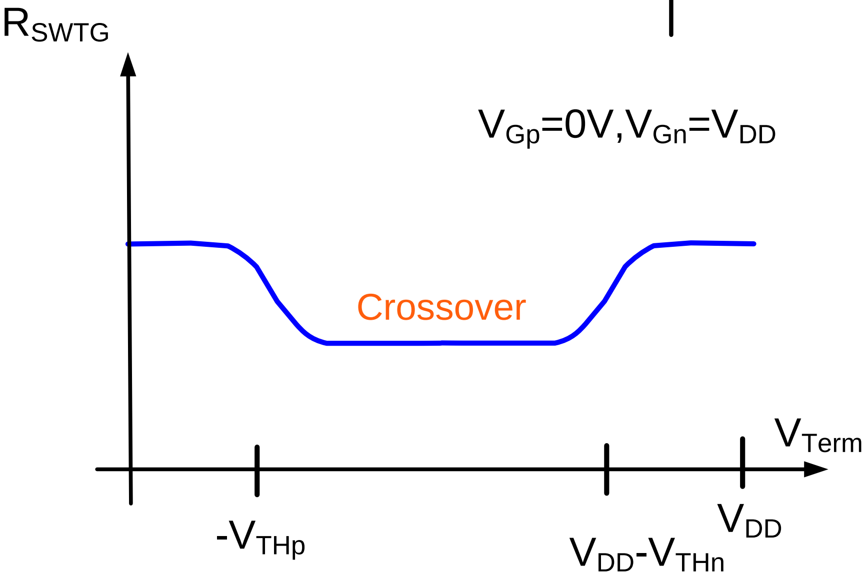


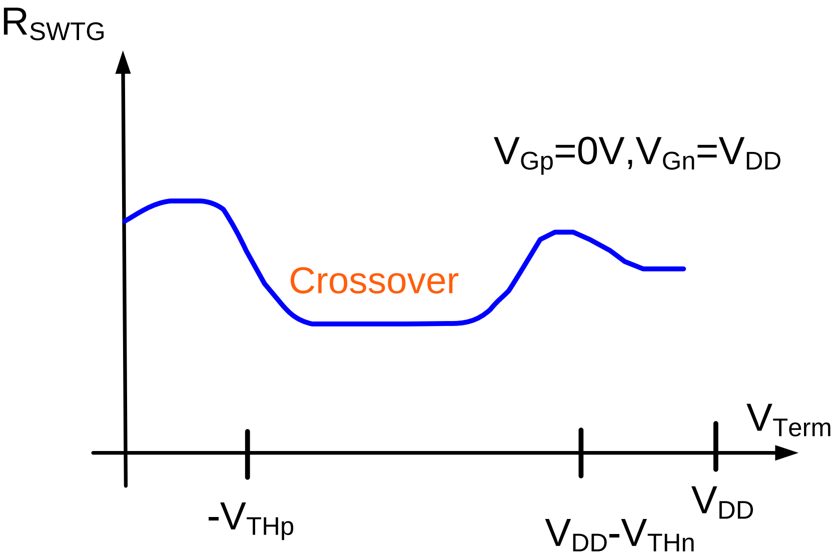


Switch Impedances



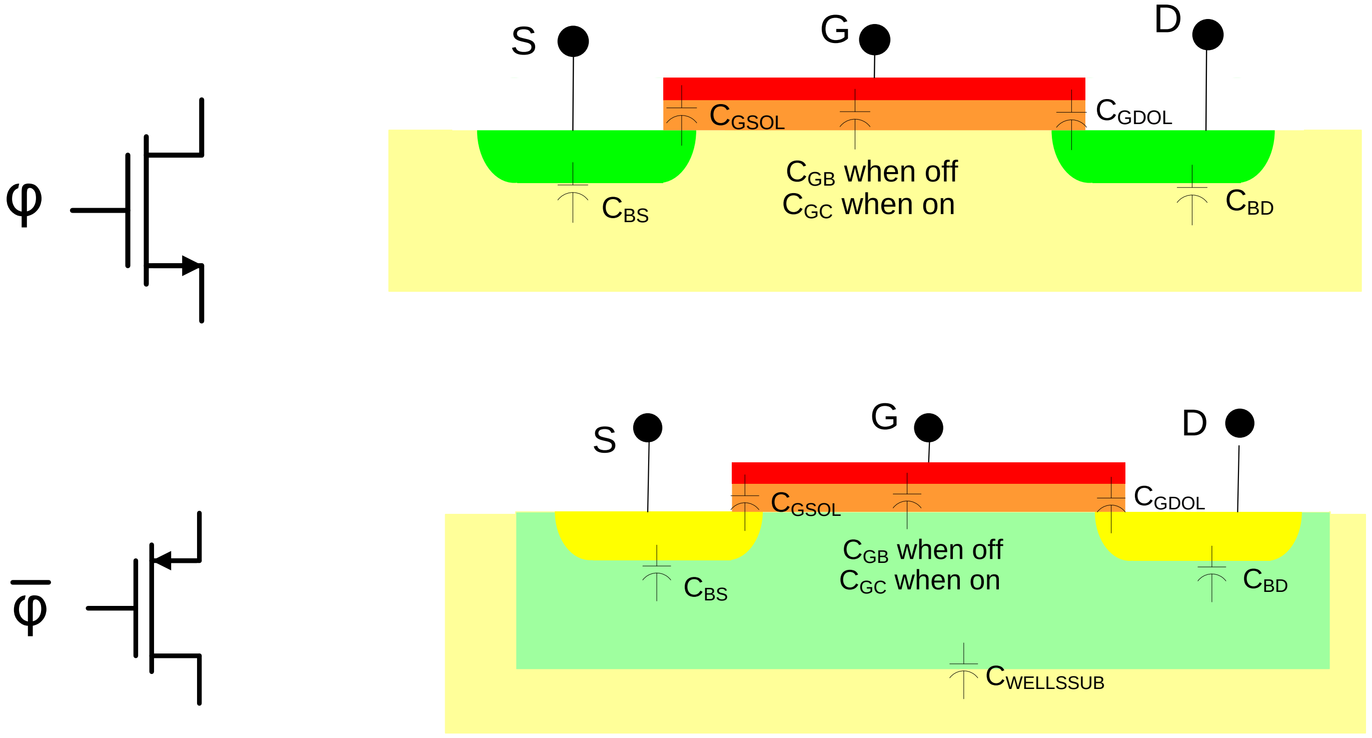






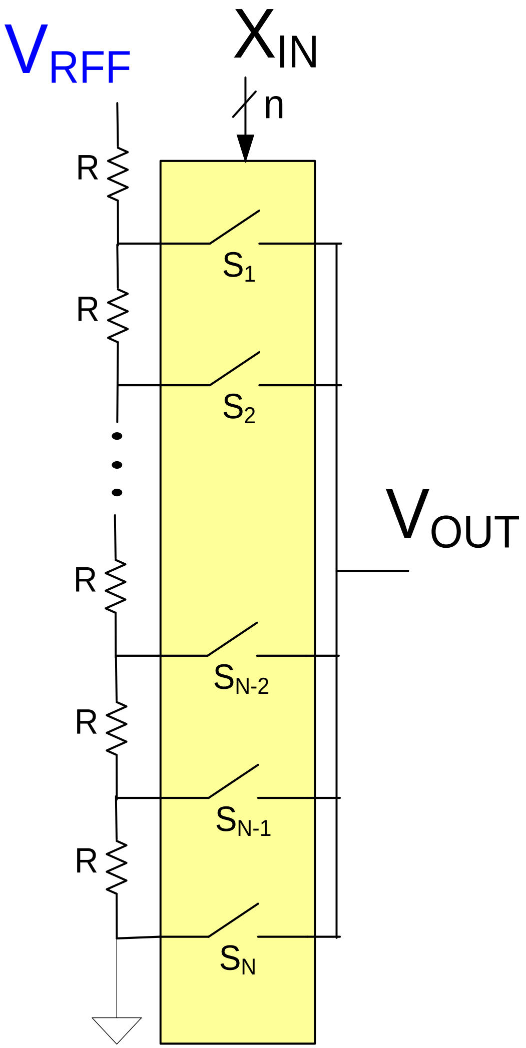
Switch impedance significantly both position and device size dependent

Switch Parasitics



- C_{BD} and C_{BS} can be significant and cause rise-fall times to be position dependent
- C_{GDOL} can cause “kickback” or feed-forward
- C_{GS} can slow turn-on and turn-off time of switch

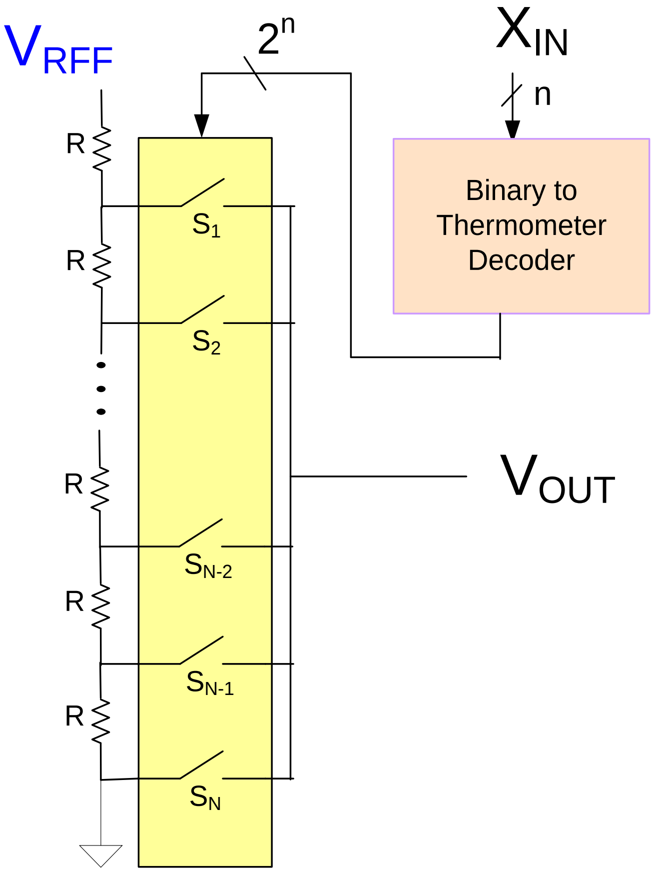
R-String DAC



Additional Challenges:

- Capacitance on V_{OUT} can be large
  - larger for p-channel devices
  - even larger for TG switches
- Switch impedances position dependent
- Kickback from switches to R-string
- Capacitance on each node (though small) of R-string from switch
- Thevenin impedance facing V_{OUT} highly code dependent

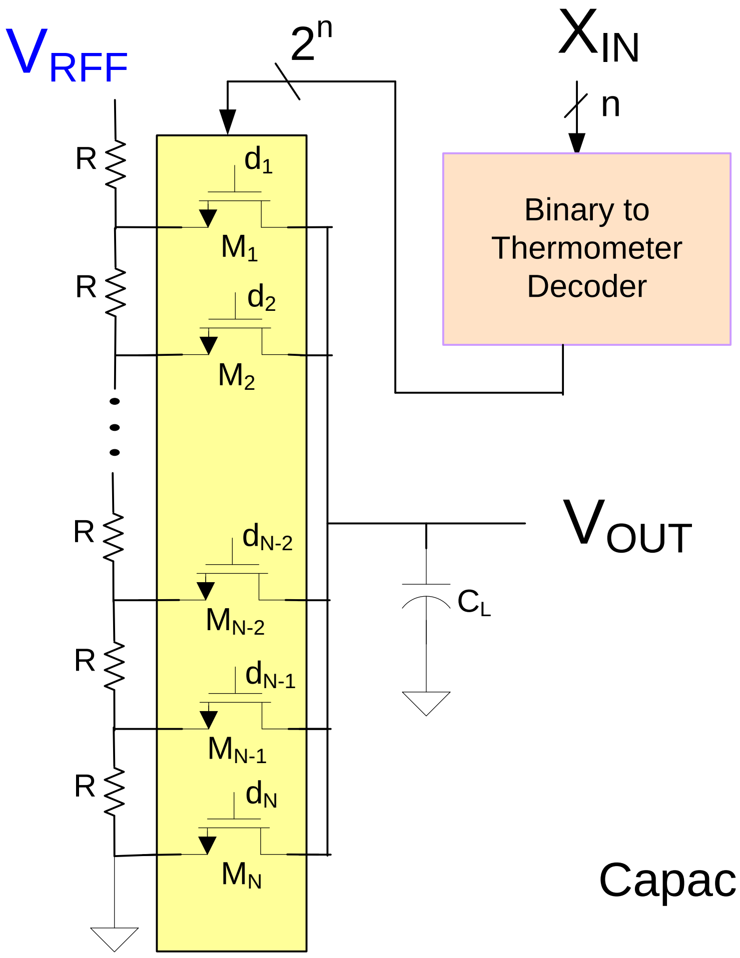
R-String DAC



Additional Challenges

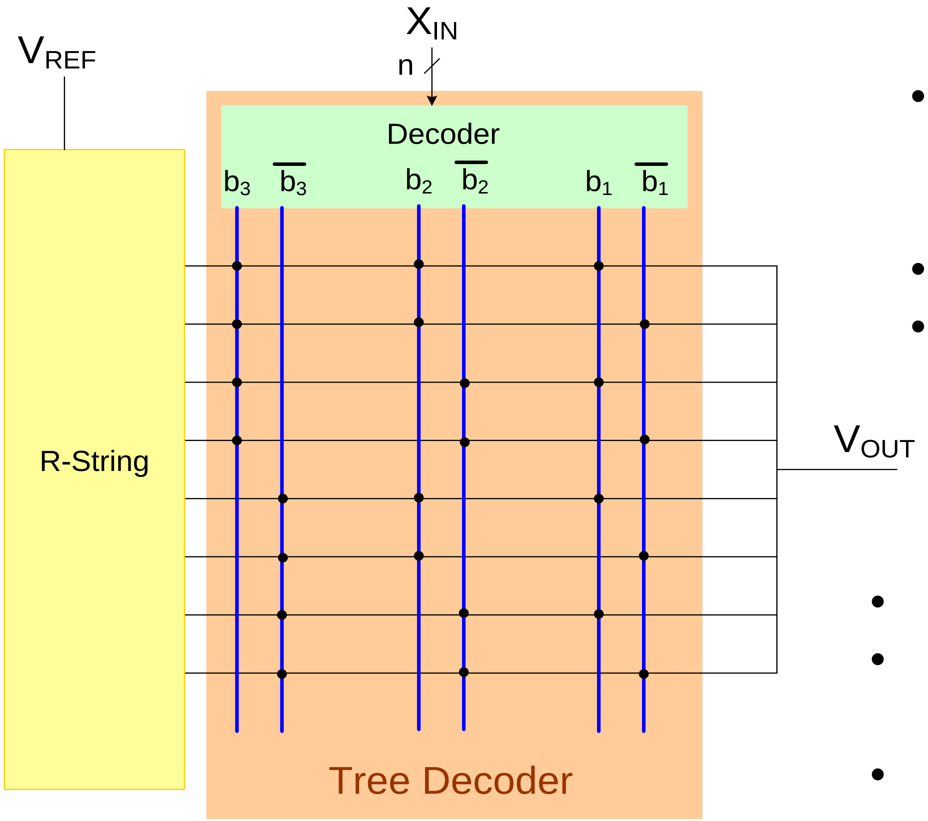
- Delay in Decoder may be significant
- Delay in Decoder may be previous code and current code dependent
- Intermediate undesired Boolean outputs may occur
  - These may cause undesired opening and closing of switches
  - Could momentarily short out taps on R-string
  - Could introduce transients on all nodes of R-string that are code and previous code dependent

R-String DAC



Capacitive loading due to switches

R-String DAC

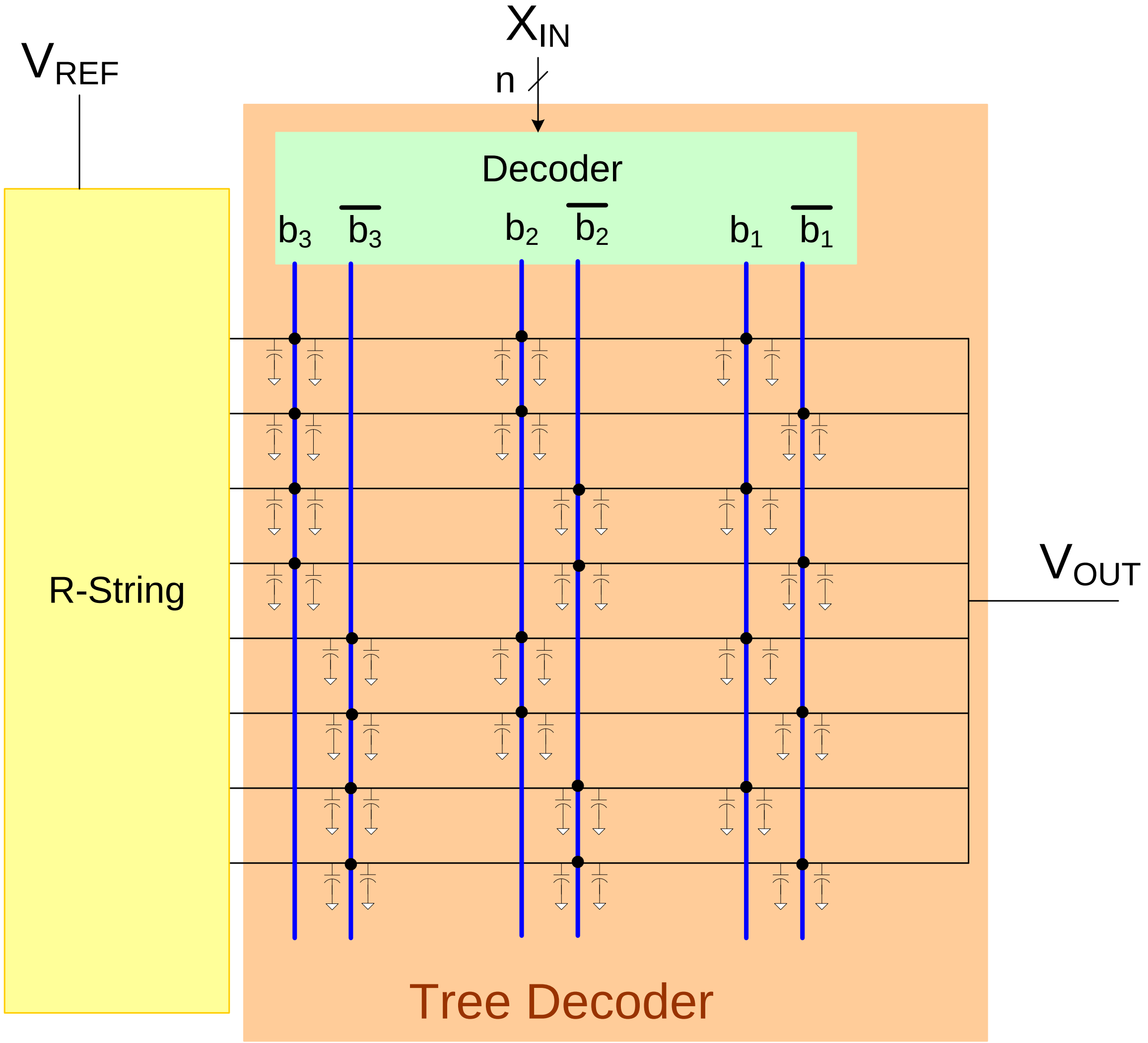


- Uses matrix decoder as analog MUX
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)

Challenges

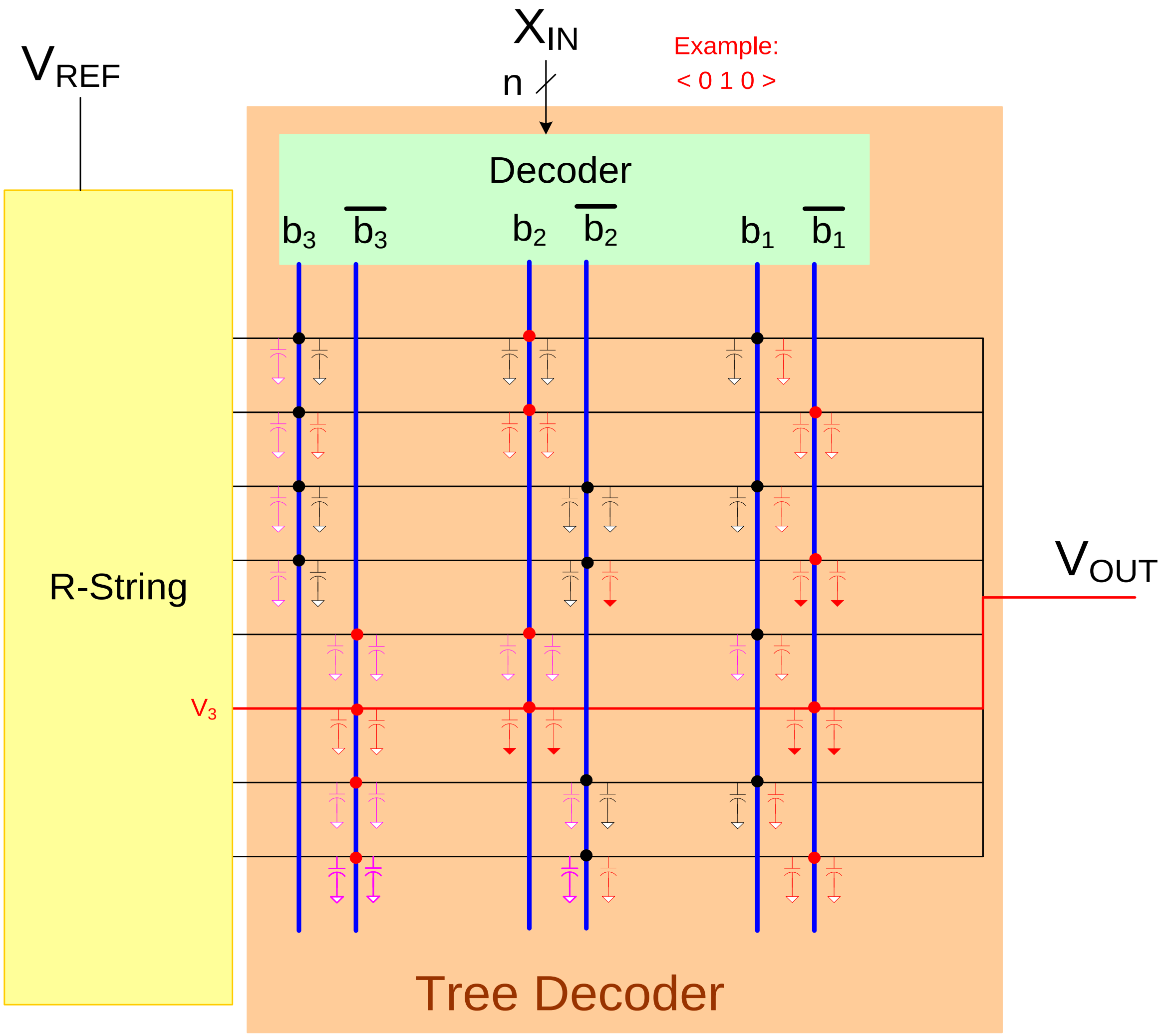
- Still many signals to route
- Large capacitance on V_{OUT} (over 2^{n+1} diff caps)
- Multiple previous code dependencies cause output transition time to be quite unpredictable
- Considerable transients introduced on R-string

R-String DAC



Parasitic Capacitances in Tree Decoder

R-String DAC



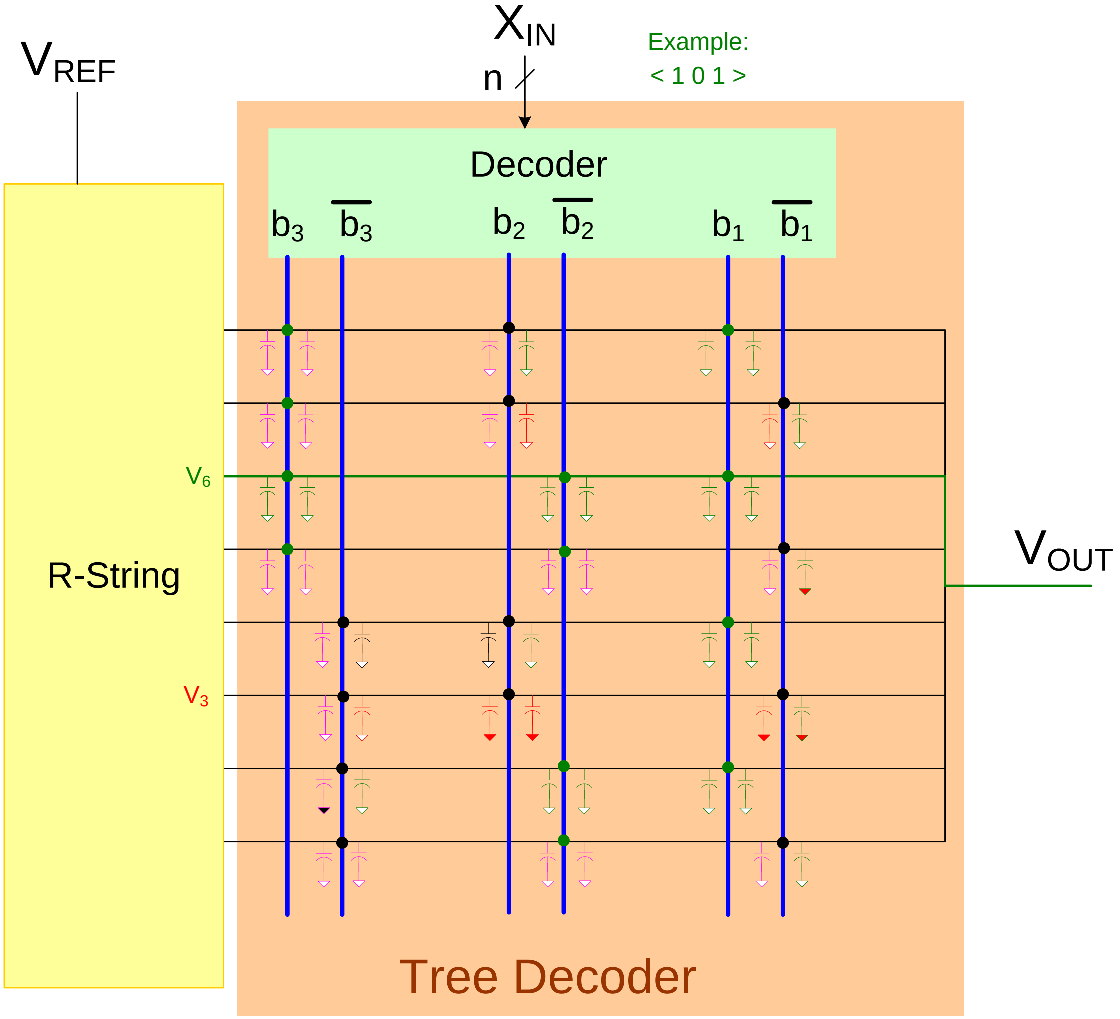
Previous-Code Dependent Settling

Assume all C's initially with 0V

Red denotes V_3, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>



Previous-Code Dependent Settling

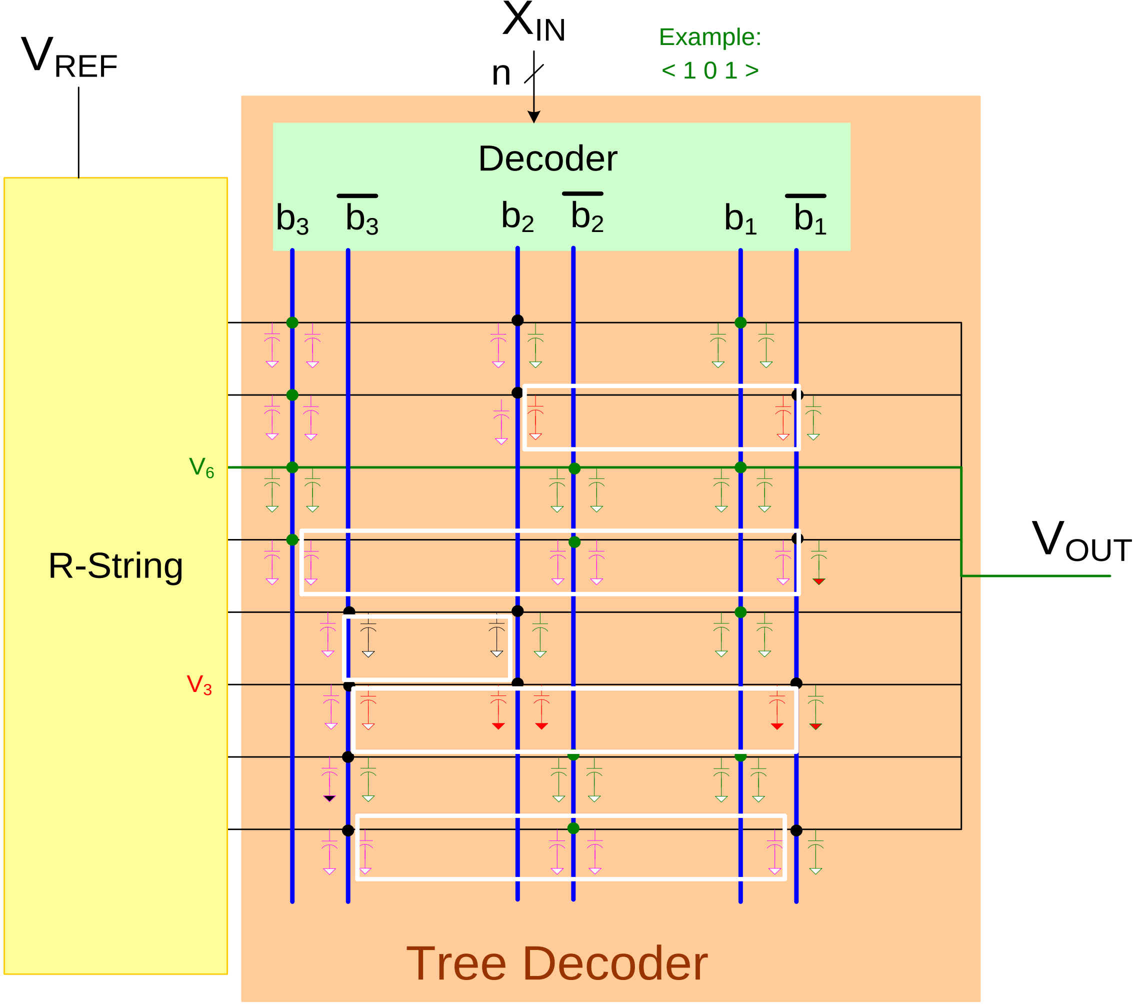
Assume all C’s initially with 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other v

R-String DAC

Transition from <010> to <101>

White boxes show capacitors dependen
upon previous code <010>



Previous-Code Dependent Settling

Assume all C’s initially with 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

End of Lecture 12