Switch Implementation

Basic Switch

- Large number required for large resolution
- Simple structure often used

\[ \phi \]

- Single n-channel device
  - Good when switch terminals near gnd
  - Will not turn on when terminals near \( V_{DD} \)

\[ \bar{\phi} \]

- Single p-channel device
  - Good when switch terminals near \( V_{DD} \)
  - Will not turn on when terminals near gnd

\[ \phi \quad \bar{\phi} \]

- Transmission gate switch
  - Use devices where cross-over occurs
  - Good for both high and low term voltages
  - Extra clock signal required
  - Try to avoid this complexity

Other switch structures (such as bootstrapped switch) used but not for basic string DACs
Switch Impedances

Review from Last Lecture
Switch Impedances

Review from Last Lecture

Switch impedance significantly both position and device size dependent.

\[ R_{SWTG} \]

\[ V_{Gp}=0V, V_{Gn}=V_{DD} \]

\[ V_{DD}-V_{THn} \]

\[ V_{DD}-V_{THp} \]

\[ V_{Term} \]
R-String DAC

• Uses tree decoder as analog MUX
• Implements binary to decimal conversion with pass transistor analog logic
• Very structured layout
• Interconnection points are switches (combination of n-channel and p-channel)
• Dramatically reduces capacitance on output and switching capacitances

Challenges
• Still many signals to route
• Multiple previous code dependencies cause output transition time to be quite unpredictable
R-String DAC

String DAC with Row-Column Decoder

- Dramatic reduction in decoder complexity
- Dramatic reduction of capacitive loading on output
- Changes decoder from a one-dimensional to a two-dimensional solution (can be thought of as folding)
- Logic gates could be placed at each node to eliminate analog row decoder

**Challenges** (most were present in earlier structures too)

- Some previous code dependence
- INL large
- Difficult to cancel gradient effects in layout
  - Switching sequencing can help a lot
- Switch impedances code dependent
- Settling times code dependent
R-String DAC

Can this concept be extended further?

- Dramatic reduction in decoder complexity
- Dramatic reduction of capacitive loading on output
- Changes decoder from a one-dimensional to a m-dimensional solution (folding)
- Logic gates could be placed at each node to eliminate analog row decoder

Review from Last Lecture
R-String DAC

What about this parallel R-string?

Review from Last Lecture

Added two resistors tapped at middle of original R-string
Note Dual Ladder is used!
Sometimes termed sub-divider, sub-range or dual-string DAC
R-String DAC

\[ n = n_1 : n_2 \]

\[ X_{\text{IN}} \]

\[ V_{\text{RFF}} \]

\[ V_{\text{OUT}} \]

Interpolator
R-String DAC

$X_{IN}$

$n = n_1 : n_2$

$V_{RFF}$

$R$

$S_{cN1}$

$S_{cN1}$

$S_k$

$S_{ck}$

$S_{c1}$

$S_{c2}$

$V_{OUT}$

$V_{DD}$

$S_{cN1}$

$S_{c1}$

Interpolator

$I_{INT}$

$V_{OUT}$
Basic R-String DAC

Latching Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion
Basic R-String DAC

For all $b_1$ and $b_2$, $R_U + R_L = R$

- Another Segmented DAC structure
- Can be viewed as a “dither” DAC
- Often $n_1$ is smaller than $n_2$
- Dither can be used in other applications as well
Current Steering DACs

Concept

\[ d_k = \begin{cases} 
1 & \text{if } S_k \text{ closed} \\
0 & \text{if } S_k \text{ open} 
\end{cases} \]

\[ V_{OUT} = \left[ \sum_{i=1}^{k} d_i I_i \right] (-R) \]
Current Steering DACs

Unary Current Sources

Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed “top plate switching”
- Thermometer coding (routing challenge!)
- Excellent DNL properties
- INL may be poor, typically near mid range
- Not suitable for use as MDAC
Current Steering DACs

Unary Current Sources

Inherently Insensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges

- Termed “bottom plate switching”
- Thermometer coded
- Can be used as MDAC
Current Steering DACs

Binary to Thermometer Decoder (all ON)

Transistor Implementation of Switches
Current Steering DACs

Transistor Implementation of Switches

β = \frac{R_{\text{CELL}}}{k} = \frac{k}{R_{\text{CELL}} + R_F}

\text{If } V_{\text{OUTFS}} = -\frac{V_{\text{REF}}}{N} \text{, then } R_{\text{CELL}} = \left(\frac{N}{N-1}\right)R_F

\frac{N}{2N-1} < \beta \leq 1 \\
0.5 < \beta \leq 1 \\
\text{approximately}

Phase-margin code dependent so distortion will be introduced if not fully settled
Current drawn from $V_{\text{REF}}$ changes with code (settling and issues if R0 is not 0)