EE 505

Lecture 15

Current Steering DACs
Charge Redistribution DACs
Review from Last Lecture

R-String DAC

\[ X_{IN} \]

\[ n = n_1 : n_2 \]

\[ V_{RFF} \]

\[ V_{OUT} \]

Interpolator
Current Steering DACs

Unary Current Sources

Binary to Thermometer Decoder (all ON)

\[ V_{OUT} = \left[ \sum_{i=1}^{N-1} d_i \right] \left( \frac{-V_{REF}}{R} \right) \]

Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed “top plate switching”
- Thermometer coding (routing challenge!)
- Excellent DNL properties
- INL may be poor, typically near mid range
- Not suitable for use as MDAC
Current Steering DACs

Unary Current Sources

Inherently Insensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges

- Termed “bottom plate switching”
- Thermometer coded
- Can be used as MDAC
Current Steering DACs

Transistor Implementation of Switches

\[ \beta = \frac{R_{\text{CELL}}}{k} + \frac{k}{R_{\text{CELL}} + kR_F} \]

\[ \frac{N}{2N-1} < \beta \leq 1 \]

Phase-margin code dependent so distortion will be introduced if not fully settled
Current drawn from \( V_{\text{REF}} \) changes with code (settling and issues if \( R_0 \) is not 0)
Current Steering DACs

Binary to Thermometer Decoder (all ON)

\[ \beta \text{ Compensation} \]
(Actually static \( \beta \) comp)

\[ C_P \text{ Compensation} \]
(to keep \( C_P \) from charging to \( V_{REF} \) when off)

\[ \text{Differential Output} \]
(inherent \( C_P \) compensation)
Current Steering DACs

Will β compensation double resistance of cells?
Will β compensation double area for cells?
Can $C_p$ and β compensation be used simultaneously?
Is the frequency-dependent β code dependent?
Spectral Characterization of DACs (a measure of linearity)

many more samples per DAC clock are often used (e.g. 64K samples, 31 periods would be approx 2114 samples/period)

Is this how we should characterize the spectral performance of a DAC?
Spectral Characterization of DACs (a measure of linearity)

one mid-period sample per DAC clock period (or maybe even less)

Assume Nyquist sampling rate is satisfied

Is this how we should characterize the spectral performance of a DAC?
Spectral Characterization of DACs (a measure of linearity)

one near-end sample per DAC clock period

Assume Nyquist sampling rate is satisfied

Is this how we should characterize the spectral performance of a DAC?
Spectral Characterization of DACs (a measure of linearity)

Assume Nyquist sampling rate is satisfied

Does it make a difference?

Yes! But depends on application which is useful
Spectral Characterization of DACs (a measure of linearity)

Does it make a difference?

- **Ideal**
- **Complete Linear Settling**
- **Incomplete Linear Settling**
- **Complete Nonlinear Settling**
- **Incomplete Nonlinear Settling**
- **Complete with glitch**
- **Incomplete with glitch**
- **Incomplete with big glitch**

Yes! But depends on application which is useful

- If entire DAC output is of interest, any nonlinearity including previous code dependence will degrade linearity.
- If DAC output is simply sampled, only value at sample point is of concern.
Current Steering DACs

Current Steering

Binary-Weighted Resistor Arrays

- Unary cells bundled to implement binary cells
- Need for decoder eliminated!
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical
- Large total resistance

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

Large DNL dominantly occurs at mid-code and due to ALL resistors switching together
Can unary cell bundling be regrouped to reduce DNL
Current Steering DACs

Reduced Resistance Structure

- Significant reduction in resistance possible
- Can be inserted at more than one place to further reduce resistance values
- Introduces a “floating node” but voltage on floating node does not change 😞
- Current drawn from $V_{REF}$ changes with code
- If inserted at each intersection becomes R-2R structure
Current Steering DACs

Reduced Resistance Structure
Current Steering DACs

Binary-Weighted Resistor Arrays

Actual layout of resistors is very important
End of Lecture 15