EE 505

Lecture 17

String DACs
Two much smaller decoders are needed.
Each node in R-string sees $2^{n/2}$ diffusions in switch matrix + those in the Analog MUX.
R-String Issues

- Placement & Staging of R-string
  - Sheet resistance & contact resistance variations
  - Gradient effects

- Architecture of R-string

Assume R-string comprised of
unit cells

Consider the placement issue
Since gradient direction is not controllable, this structure will have rather large INL for some directional gradients. Yield loss would be experienced, and this could be significant.
Dual Resistor String

Anti-parallel resistor layout

Dual String Layout
Dual Ladder,

\[ R_{eq} = \frac{R_{kA}}{R_{KB}} \]

The antiparallel layout provides a common centroid for all resistors in the R-string.
Sizing Issues

\[ R = R_{c1} + R_{c2} + R_{sh} \]

\[ R_{\text{nom}} = \frac{R_{cn}}{m} + \frac{R_{cn}}{m} + R_{on} \cdot \frac{L}{W} \]

\[ R = \sum_{k=1}^{m} \frac{1}{R_{c1k}} + \frac{1}{m} + \frac{1}{R_{c1k}} + \frac{1}{m} + \frac{L}{W} R_{on} \]

\[ \sigma_{\frac{R}{R_{\text{nom}}}} = \sqrt{\left( \frac{2 R_{cn}}{m \left( 2 R_{cn} + R_{\text{nom}} \right)} \right)^2 \sigma_{\frac{R_{cn}}{R_{cn}}}^2 + \left( \frac{R_{on} R_{\text{nom}}}{\left( \frac{2 R_{cn} + R_{\text{nom}}}{m} \right)^2} \sigma_{\frac{R_{on}}{R_{on}}}^2 \right) \left( \frac{R_{on} R_{\text{nom}}}{\left( \frac{2 R_{cn} + R_{\text{nom}}}{m} \right)^2} \sigma_{\frac{R_{on}}{R_{on}}}^2 \right)} \]
- Reduces (eliminates) previous output data dependence from decoder
- But previous output dependencies may still be present in the resistor switch segment.
Return to Zero Operation.

- Removes previous data dependencies in both decoder & switch string
- Reduces signal level
- Increases noise floor
- Data & Position Dependent Delays
Data Dependent Delays

(Appllicable to both DACs & ADCs)

\[ \text{Desired Output} \]

\[ \text{t}_{\text{des}} \quad \text{t}_{\text{ACT}} \]

\[ \text{delay} \]

\[ V_{\text{in}} \quad \phi \quad V_{\text{out}} \]

- \text{t}_{\text{ACT}} \text{ differs from } \text{t}_{\text{DES}} \text{ and this can be significant}

- \text{t}_{\text{delay}} \text{ is data dependent and causes nonlinearity limitations}
Position Dependent Delay

Position Dependent Delays also cause distortion
Managing Position Dependency

Delay

Example

end blk
- Layouts with either equal or near equal path lengths to each node of concern.
Settling Time

\[ V_0 = V \left( 1 - e^{-\frac{t}{RC}} \right) \]

**Example**

If .5 LSB settling at 10-bit level,

\[ V = V_{REF} \quad \Rightarrow \quad V_0 = 0.9995 \, V_{REF} \]

\[ V_{LSB} = 0.001 \, V_{REF} \]

\[ \frac{1}{2} V_{LSB} = 0.0005 \, V_{REF} \]

\[ 0.9995 \, V_{REF} = V_{REF} \left( 1 - e^{-\frac{t_s}{RC}} \right) \]

\[ 0.0005 = e^{-\frac{t_s}{RC}} \]

\[ t = 7.6 \, RC \]

Time to settle to 0.5 LSB at 10-bit level

\[ t_s = 9.9 \, RC \]

Time to settle to 0.05 LSB at 14-bit level

\[ t_s \approx 13 \, RC \]
A+ mid-tap

\[ R_{eq} = \frac{R_T}{4} \]

A+ 3/4 tap

\[ R_{eq} = \frac{R_T}{4} // \frac{3R_T}{4} \]

\[ = R_T \left( \frac{1}{4} \cdot \frac{3}{4} \right) \]

\[ = \frac{3}{16} R_T \]

A+ Last Tap on Top

\[ R_{eq} = R // R_T \]

\[ \approx R = \frac{R_T}{2^n} \]
Typical values for settling time in R-string DAC.

Consider: $V_{	ext{REF}} = 2V$

Ideal switches except for capacitance

$$\frac{W}{L} = 25$$

$$C_{\text{diff}} = \left(4 \cdot \frac{fF}{\mu^2}\right) (W \cdot 6L) + \left(34 fF/\mu^2\right) (2W + 12L)$$

If $L = .5 \mu$, $W = 12.5 \mu$, $2L \approx 0.5 \mu$
\[ C_{\text{diff}} = \left( \frac{0.4 \times 10^3}{\mu^2} \right) (12.5 \cdot \frac{1.5}{1.5}) + \left( \frac{0.34 \times 10^3}{\mu} \right) (25 + 3) \]

\[ = (0.4 \times 10^3)(12.5)(1.5) + (0.34)(28) \]

\[ = 17 \text{ pF} \]

\[ C_x = 2^n C_{\text{diff}} \approx 17 \text{ pF} \]

Settle to 0.05 LSB requires 10 times more

\[ t_{\text{settle}} = (10) R_{\text{string}} \left( 17 \text{ pF} \right) \]

\[ R_{\text{string}} = \begin{cases} 4 \Omega & \text{top p} \\ 750 \Omega & 3/4 \text{ p}, 1/4 \text{ p} \\ 1 \text{ k} & 1/2 \text{ p} \end{cases} \]

\[ R_T = 4 \text{ k} \]

\[ t_{\text{settle}} = (10)(1 \text{ k})(17 \text{ pF}) = 1.7 \times 10^{-7} \]

\[ \text{Note: The impact of } C_x \text{ is very significant on the } R\text{-string structure!} \]
A+ mid-tap.

\[ R_{sw} = \frac{5}{\mu \sigma_4 \omega (V_{GS} - V_T)} \]

\[ \approx \frac{1}{(25)(110 \times 10^{-6})(V_{DD} - V_S - V_T)} \]

If \( V_{DD} = 5 \, V \)

\( V_{REF} = 2 \, V \)

\( V_T = 1 \, V \)

<table>
<thead>
<tr>
<th>( \theta )</th>
<th>( R_{sw} )</th>
<th>( R_{string} )</th>
<th>( R_{total} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 T</td>
<td>86</td>
<td>0</td>
<td>86</td>
</tr>
<tr>
<td>¼ T</td>
<td>98</td>
<td>750</td>
<td>848</td>
</tr>
<tr>
<td>½ T</td>
<td>114</td>
<td>1k</td>
<td>1.14k</td>
</tr>
<tr>
<td>¾ T</td>
<td>135</td>
<td>750</td>
<td>885</td>
</tr>
<tr>
<td>T</td>
<td>165</td>
<td>4</td>
<td>169</td>
</tr>
</tbody>
</table>
Methods of Reducing Switch impedance

a) Increase \( W \)

\[
C_{\text{diff}} = C_{\text{diff bot}} (W \cdot (0A)) + C_{\text{diff sw}} (2W + 12A)
\]

\[
= \left( C_{\text{diff bot}} \cdot 6A + C_{\text{diff sw}} 2 \right) W
\]

\[
R_{\text{sw}} = \frac{L}{\mu_{\text{Cox}} W (B \cdot V_{Gx} - V_{T})}
\]

\[
R_{\text{sw}} (C_{\text{diff}} 2^n) = 2^n \frac{L}{\mu_{\text{Cox}} W (B \cdot V_{Gx} - V_{T})}
\]

\[
= 2^n \frac{L}{\mu_{\text{Cox}} (V_{Gx} - V_{T})}
\]

- it can reduce the non-linearities associated with signal dependence on \( R_{\text{sw}} \)
- no net improvement in settling time
b) Increase VDD
   - use a better process
     *Not directly practical*

c) use p/n switch cell

\[
\phi - 1 \quad \phi - 1
\]

\[
\phi
\]

\[
\phi
\]

d) concentric layouts

---

Sizing of p-channel device:

\[
R_{SWN} = R_{SUP} \text{ when driven to the extreme values,}
\]

\[
\frac{D}{\max Wn (VDD - VIP)} = \frac{1}{\max WP (VDD + VIP)}
\]

\[
WP = \frac{Wn \cdot Un}{WP}
\]
Concentric layouts