EE 505

Lecture 19

Comparison of String DACs
Noise in data converters
Dynamic Current Source Matching

Extra current source can be added to facilitate background calibration
Consider basic charge redistribution circuit

Review from Last Lecture

Clocks are complimentary non-overlapping
Review from Last Lecture

Basic charge redistribution circuit

During phase $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$\frac{Q_{\phi_1}}{C_F} = V_{OUT}$$

$$\frac{CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F}$$

Serves as a noninverting amplifier

Gain can be very accurate

Output valid only during $\Phi_2$
During phase $\phi_1$

$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

During phase $\phi_2$

Charge $Q_{SET}$ is all transferred to $C_F$

$$Q_{CF} = V_{OUT} C$$

but

$$Q_{SET} = Q_{CF}$$

$$V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C$$

$$V_{OUT} = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$
Another Redistribution DAC

\[ C_i = \frac{C}{2^i} \]

During phase \( \phi_1 \) selected switches set to \( V_{\text{REF}} \)

\[ Q_{\text{SET}} = V_{\text{REF}} \sum_{i=0}^{n} d_i C_i = V_{\text{REF}} \sum_{i=0}^{n} d_i \frac{C}{2^{n-i}} \]

During phase \( \phi_2 \) all switches connected to GND

Charge \( Q_{\text{SET}} \) is all redistributed among the capacitors

\[ Q_{\text{SET}} = V_{\text{OUT}} \left( \sum_{i=1}^{n} C_i + C_n \right) \]

but

\[ \sum_{i=1}^{n} C_i + C_n = \left( \sum_{i=1}^{n} \frac{C}{2^i} + C_n \right) = C \]

\[ Q_{\text{SET}} = V_{\text{OUT}} C \]

\[ V_{\text{REF}} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{\text{OUT}} C \quad \rightarrow \quad V_{\text{OUT}} = V_{\text{REF}} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}} \]
Relative Statistical Characterization of R-based DACs

\[ A = W L \]

\[ \frac{\sigma_R}{R_N} = \frac{A_{\rho R}}{\sqrt{A}} \]
Relative Statistical Characterization of R-based DACs

For the same total area and the same resolution, how do these structures compare from a statistical characterization viewpoint?
Relative Statistical Characterization of R-based DACs

For the same total area and the same resolution, how do these structures compare from a statistical characterization viewpoint?

Simulation environment:

Resolution = 10
$A_{\rho R} = 0.02\,\mu m$
$R_{\text{nom}} = 1000$
Area Unit Resistor = $2\,\mu m^2$
Resistor Sigma= 14.1421
INLtarget = 0.5000 LSB
Relative Statistical Characterization of R-based DACs

$\text{INL}_k$ for four random implementations

String DAC

\[ V_{\text{RFF}} \quad X_{\text{IN}} \quad n \]

\[ R \quad S_1 \quad R \]

\[ R \quad S_2 \quad R \]

\[ \cdots \]

\[ R \quad S_{N-2} \quad R \]

\[ R \quad S_{N-1} \quad R \]

\[ R \quad S_N \quad R \]

\[ \downarrow \quad V_{\text{OUT}} \]

\[ \text{INL}_k \] for four random implementations

Graphs showing INL behavior for different implementations.
Relative Statistical Characterization of R-based DACs

INL histogram for 100,000 random implementations

String DAC
Relative Statistical Characterization of R-based DACs

\[\text{INL}_{k\text{MAX}}\] histogram for 100,000 random implementations

String DAC
Relative Statistical Characterization of R-based DACs

DNL histogram for 100,000 random implementations

String DAC
Relative Statistical Characterization of R-based DACs

Summary

Resolution = 10
$A_{\rho R} = 0.02\mu m$
$R_{\text{nom}} = 1000$
Area Unit Resistor = $2\mu m^2$
Resistor Sigma = 14.1421
$\text{INL}_{\text{mean}} = 0.385$ LSB
$\text{INL}_{\sigma} = 0.118$ LSB
$\text{DNL}_{\text{mean}} = 0.049$ LSB
$\text{DNL}_{\sigma} = 0.0047$ LSB
Relative Statistical Characterization of R-based DACs

$\text{INL}_k$ for four random implementations

Binary Weighted DAC
Relative Statistical Characterization of R-based DACs

INL histogram for 100,000 random implementations

Binary Weighted DAC
Relative Statistical Characterization of R-based DACs

$\text{INL}_{k\text{MAX}}$ histogram for 100,000 random implementations

Binary Weighted DAC
Relative Statistical Characterization of R-based DACs

DNL histogram for 100,000 random implementations

Binary Weighted DAC
Relative Statistical Characterization of R-based DACs

Summary

Resolution = 10
$A_{pR} = 0.02 \mu m$
$R_{\text{nom}} = 1000$
Area unit resistor = $2 \mu m^2$
Resistor Sigma = 14.1421

$\text{INL}_{\text{mean}} = 0.367 \text{LSB}$
$\text{INL}_{\text{sigma}} = 0.128 \text{ LSB}$
$\text{INL}_{k\text{max_mean}} = 0.00013 \text{ LSB}$
$\text{INL}_{k\text{max_sigma}} = 0.226 \text{ LSB}$
$\text{DNL}_{\text{mean}} = 0.470 \text{ LSB}$
$\text{DNL}_{\text{sigma}} = 0.228 \text{ LSB}$
$\text{INL}_{\text{target}} = 0.500 \text{ LSB}$
Yield (%) = 84.9
Relative Statistical Characterization of R-based DACs

Popular Area Allocation Strategies

- Standard Series
- Standard Parallel
- Equal Area Series Parallel

R Block
- R

2R Block
- 2R

R-2R DAC
Relative Statistical Characterization of R-based DACs

$\text{INL}_k$ for four random standard series implementations
Relative Statistical Characterization of R-based DACs

INL histogram for 15,000 random implementations Standard Series

R-2R DAC
Relative Statistical Characterization of R-based DACs

DNL histogram for 15,000 random implementations Standard Series

R-2R DAC
Relative Statistical Characterization of R-based DACs

Summary  Standard Series

Resolution=10
A_R=0.02 µm
R_{nom} = 1000
Base Res Area(um^2)=2
Res Sigma=14.1421
INL_{mean} = 0.609 LSB
INL_{sigma} = 0.295 LSB
DNL_{mean} = 1.021 LSB
DNL_{sigma} = 0.610 LSB
INL_{kmax_mean} = 0.00017 LSB
INL_{kmax_sigma} = 0.566 LSB
Yield INL Bound=0.5 LSB
Yield= 41.4%
Relative Statistical Characterization of R-based DACs

\( \text{INL}_k \) for four random standard parallel implementations
Relative Statistical Characterization of R-based DACs

INL histogram for 100,000 random implementations Standard Parallel

R-2R DAC
Relative Statistical Characterization of R-based DACs

DNL histogram for 100,000 random implementations Standard Parallel

R-2R DAC
Summary Standard Parallel

Resolution = 10
\( A_{pR} = 0.02\mu m \)
\( R_{\text{nom}} = 1000 \)

Base Resistor Area(\( \text{um}^2 \)) = 2

Resistor Sigma = 14.1421

\( \text{INL}_{\text{mean}} = 0.737 \) LSB
\( \text{INL}_{\text{sigma}} = 0.357 \) LSB

\( \text{INL}_{\text{kmax_mean}} = 0.0045 \) LSB
\( \text{INL}_{\text{kmax_sigma}} = 0.680 \) LSB

\( \text{DNL}_{\text{mean}} = 1.225 \) LSB
\( \text{DNL}_{\text{sigma}} = 0.732 \) LSB

\( \text{INL}_{\text{target}} = 0.5 \) LS

Yield = 28.5%
Relative Statistical Characterization of R-based DACs

R-2R DAC

Standard Series Slice Area Scaled
Relative Statistical Characterization of R-based DACs

DNL histogram for 15,000 random implementations Standard Series Area Scaled
Scaling Factor: 1.7
Relative Statistical Characterization of R-based DACs

INL histogram for 15,000 random implementations Standard Series Area Scaled

Scaling Factor: 1.7
Relative Statistical Characterization of R-based DACs

Resolution = 10
$A_{\rho_R} = 0.02\mu m$
$R_{\text{nom}} = 1000$
Total Area $2048 \mu m^2$
Resistor Sigma = 14.1421
INL$_{\text{target}} = 0.5$ LSB
Yield = 28.5%

<table>
<thead>
<tr>
<th>Architecture</th>
<th>INL( LSB)</th>
<th>DNL( LSB)</th>
<th>INL Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mean</td>
<td>Sigma</td>
<td>Mean</td>
</tr>
<tr>
<td>String</td>
<td>0.385</td>
<td>0.118</td>
<td>0.049</td>
</tr>
<tr>
<td>Binary Weighted</td>
<td>0.367</td>
<td>0.128</td>
<td>0.470</td>
</tr>
<tr>
<td>R-2R Series</td>
<td>0.609</td>
<td>0.295</td>
<td>1.021</td>
</tr>
<tr>
<td>R-2R Parallel</td>
<td>0.737</td>
<td>0.357</td>
<td>1.225</td>
</tr>
<tr>
<td>Slice Scaled (1.7) Series R-2R</td>
<td>0.399</td>
<td>0.153</td>
<td>0.556</td>
</tr>
</tbody>
</table>
Calibration of DACs

- The area required to get acceptable performance of a DAC if often too large to be practical
- Large DAC area invariably increased power dissipation
- Large DAC area invariably limits speed of a DAC
- Calibration is often used to improve the linearity of a DAC
- Calibration requires area overhead but it is often less than the area overhead that is required to improve yield using area alone
  \[
  \sigma \frac{x}{x_N} = \frac{A_x}{\sqrt{A}}
  \]
- Benefits of using calibration are limited to the inherent noise in a DAC and calibration does not improve random noise (but can reduce quantization noise)
Calibration of DACs

- If CAL DAC is driven by appropriate information in RAM, it can correct for nonlinearities in ADC
- Resolution of CAL DAC can be small if IDAC is modestly linear
- Code in ROM can be programmed at test or during production
use a slow-speed ADC to determine actual output of IOAC & then add approp. output from CAI-IOAC to obtain desired result.

Dramatic reduction potential in area for higher-resolution ADCs.
Higher-resolution DACs make extensive use of calibration or self-calibration

- Calibration corrects for nonlinearities (either discontinuities or smooth nonlinearities)
- Better high frequency performance
- Smaller die area
- Lower power dissipation
- Often more practical to calibrate for combined effects of all nonlinearities rather than correct the source of individual nonlinearities
Recall the MDAC

\[ I_i = (D \cdot V_{\text{REF}})(K) \]

\[ V_0 = -I_i R \]

\[ V_0 = -R K D \cdot V_{\text{REF}} \]

\[ = D \left[ -R K J \right] V_{\text{REF}} \]
Dividing DACs

\[ I_2 = \frac{V_0}{2} D K \]

\[ V_x = -I_2 R \]

\[ V_i = -V_0 D K R \]

\[ V_0 = +V_i \left( \frac{1}{D} \right) \left( \frac{-1}{KR} \right) \]

Could call this \( \frac{MDAC}{\pi} \)}
Multiplying and Dividing DACs

\[
\begin{align*}
I_1 &= K_1 V_i D_1 \\
I_2 &= V_0 D_2 K_2
\end{align*}
\]

\[
V_0 = \frac{D_1}{D_2} \left[ -\frac{K_1 V_i}{K_2} \right]
\]

Can create various nonlinear relationships with MDACs and Op Amps
End of Lecture 19