Lecture 2
Data Converter Operation and Characterization
D/A Converters

\( \hat{X}_{\text{IN}} \rightarrow \text{DAC} \rightarrow X_{\text{OUT}} \)

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\( X_{\text{REF}} \)
D/A Converters

\[ \tilde{X}_{IN} = <b_{n-1}, b_{n-1}, \ldots b_1, b_0> \]

An Ideal DAC transfer characteristic (3-bits)

Code \( C_k \) is used to represent the decimal equivalent of the binary number \( <b_{n-1} \ldots b_0> \)
For this ideal DAC

\[ X_{\text{OUT}} = X_{\text{REF}} \left( \frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \frac{b_{n-3}}{8} + \ldots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n} \right) \]

\[ X_{\text{OUT}} = X_{\text{REF}} \sum_{j=1}^{n} \frac{b_{n-j}}{2^j} \]

- Number of outputs gets very large for n large
- Spacing between outputs is \( X_{\text{REF}}/2^n \) and gets very small for n large
A/D Converters

$X_{\text{IN}} \rightarrow \text{ADC} \rightarrow X_{\text{OUT}}$

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$X_{\text{IN}} \rightarrow \text{ADC} \rightarrow X_{\text{OUT}}$
A/D Converters

\[ \vec{X}_{\text{OUT}} = \langle d_{n-1}, d_{n-2}, \ldots, d_0 \rangle \]

- \( d_0 \) is the Least Significant Bit (LSB)
- \( d_{n-1} \) is the Most Significant Bit (MSB)

Notes:
- Indexing notation reversed from what we used for DAC
- Some authors use different index notation

An Ideal ADC is characterized at low frequencies by its static performance
A/D Converters

An Ideal ADC transfer characteristic (3-bits)

\[ \bar{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots, d_0> \]

\[ \chi_{LSB} = \frac{\chi_{REF}}{2^n} \]

\[ \chi_{REF} - \chi_{LSB} \]
A/D Converters

An Ideal ADC transfer characteristic (3-bits)

The second vertical axis, labeled $\tilde{X}_{IN}$, is the interpreted value of $X_{IN}$.
A/D Converters

For this ideal ADC

\[ x_{IN} = x_{REF} \left( \frac{d_{n-1}}{2} + \frac{d_{n-2}}{4} + \frac{d_{n-3}}{8} + \ldots + \frac{d_1}{2^{n-1}} + \frac{d_0}{2^n} \right) + \varepsilon \]

where \( \varepsilon \) is small (typically less than 1LSB)

\[ x_{IN} = x_{REF} \sum_{j=1}^{n} \frac{d_{n-j}}{2^j} + \varepsilon \]

- Number of bins gets very large for \( n \) large
- Spacing between break points is \( x_{REF}/2^n \) and gets very small for \( n \) large

\( \varepsilon \) is the **quantization error** and is inherent in any ADC
A/D Converters

Transition Points

- Actual values of $x_{IN}$ where transitions occur are termed transition points or break points.
- For an ideal n-bit ADC, there are $2^n$-1 transition points.
- Ideally the transition points are all separated by 1 LSB $\Delta$ $X_{LSB}=X_{REF}/2^n$.
- Ideally the transition points are uniformly spaced.
- In an actual ADC, the transition points will deviate a little from their ideal location.

Labeling Convention:

We will define the transition point $X_{Tk}$ to be the break point where the transition in the code output to code $C_k$ occurs. This seemingly obvious ordering of break points becomes ambiguous, though, when more than one break points cause a transition to code $C_k$ which can occur in some nonideal ADCs.
A/D Converters

Quantization Errors

\[ x_{T1} = x_{LSB} \]

\[ \varepsilon_Q = \tilde{x}_{OUT} - x_{IN} \]

Magnitude of \( \varepsilon_Q \) bounded by \( x_{LSB} \)
A/D Converters

Quantization Errors

Another Ideal ADC

\[ x_{T1} = \frac{x_{LSB}}{2} \]

\( \varepsilon_Q = \tilde{x}_{OUT} - x_{IN} \)

Magnitude of \( \varepsilon_Q \) bounded by \( \frac{1}{2} x_{LSB} \)
A/D Converters

Quantization Errors

$$\varepsilon_Q = \mathcal{X}_{\text{REF}} \left( \frac{d_{n-1}}{2} + \frac{d_{n-2}}{4} + \frac{d_{n-3}}{8} + \ldots + \frac{d_1}{2^{n-1}} + \frac{d_0}{2^n} \right) - \mathcal{X}_{\text{IN}}$$

- The only way to reduce p-p quantization errors is to increase number of levels
- A lower bound on the quantization errors in $0 < \mathcal{X}_{\text{IN}} < \mathcal{X}_{\text{REF}}$ is $\pm \frac{1}{2} \mathcal{X}_{\text{LSB}}$
- The static performance of an ADC is completely determined by the finite sequence of the transition points $< \mathcal{X}_{T_1}, \ldots, \mathcal{X}_{T_l}>$
Performance Characterization of Data Converters

- A large number of parameters are used to characterize a data converter
- Performance parameters of interest depend strongly on the application
- Very small number of parameters of interest in many/most applications
- “Catalog” data converters are generally intended to satisfy a wide range of applications and thus have much more stringent requirements placed on their performance
- Custom application-specific data converter will generally perform much better than a “catalog” part in the same
Performance Characterization of Data Converters

• Static characteristics
  – Resolution
  – Least Significant Bit (LSB)
  – Offset and Gain Errors
  – Absolute Accuracy
  – Relative Accuracy
  – Integral Nonlinearity (INL)
  – Differential Nonlinearity (DNL)
  – Monotonicity (DAC)
  – Missing Codes (ADC)
  – Low-f Spurious Free Dynamic Range (SFDR)
  – Low-f Total Harmonic Distortion (THD)
  – Effective Number of Bits (ENOB)
  – Power Dissipation
Performance Characterization of Data Converters

• Dynamic characteristics
  – Conversion Time or Conversion Rate (ADC)
  – Settling time or Clock Rate (DAC)
  – Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  – Dynamic Range
  – Spurious Free Dynamic Range (SFDR)
  – Total Harmonic Distortion (THD)
  – Signal to Noise Ratio (SNR)
  – Signal to Noise and Distortion Ratio (SNDR)
  – Sparkle Characteristics
  – Effective Number of Bits (ENOB)
Dynamic characteristics

- Degradation of dynamic performance parameters often due to nonideal effects in time-domain performance

- Dynamic characteristics often high resolution data converters often challenging to measure, to simulate, to understand source of contributions, and to minimize

Example: An n-bit ADC would often require SFDR at the 6n+6 bit level or better. Thus, considering a 14-bit ADC, the SFDR would be expected to be at the -90dB level or better. If the input to the ADC is a 1V p-p sinusoidal waveform, the second harmonic term would need to be at the $10^{-90dB/20dB} = 32\mu V$ level. A 32uV level is about 1 part in 30,000. Signals at this level are difficult to accurately simulate in the presence of a 1V level signal. For example, convergence parameters in simulators and sample (strobe) points used in data acquisition adversely affect simulation results and observing the time domain waveforms that contribute to nonlinearity at this level and relationships between these waveforms and the sources of nonlinearity is often difficult to visualize. Simulation errors that are at the 20dB level or worse can occur if the simulation environment is not correctly established.
Performance Characterization of Data Converters

What is meant by “low frequency”?

Operation at frequencies so low that further decreases in frequency cause no further changes in a parameter of interest.

Low frequency operation is often termed Pseudo-static operation.
Low-frequency or Pseudo-Static Performance

Parameter

Pseudo-Static Region

f
Performance Characterization

Resolution

- Number of distinct analog levels in an ADC
- Number of digital output codes in A/D
- In most cases this is a power of 2
- If a converter can resolve $2^n$ levels, then we term it an n-bit converter
  - $2^n$ analog outputs for an n-bit DAC
  - $2^{n-1}$ transition points for an n-bit ADC
- Resolution is often determined by architecture and thus not measured
- Effective resolution can be defined and measured
  - If N levels can be resolved for a DAC then
    \[ n_{EQ} = \frac{\log N}{\log 2} \]
  - If N-1 transition points in an ADC, then
    \[ n_{EQ} = \frac{\log N}{\log 2} \]
Performance Characterization

Least Significant Bit

Assume \( N = 2^n \)

Generally Defined by Manufacturer to be

\[ x_{\text{LSB}} = \frac{x_{\text{REF}}}{N} \]

Effective Value of LSB can be Measured

For DAC: \( x_{\text{LSB}} \) is equal to the maximum increment in the output for a single bit change in the Boolean input

For ADC: \( x_{\text{LSB}} \) is equal to the maximum distance between two adjacent transition points
Offset

For DAC the offset is

\[ X_{\text{OUT}} (\langle 0, \ldots, 0 \rangle) \]

- absolute

\[ X_{\text{OUT}} (\langle 0, \ldots, 0 \rangle) \]

- in LSB
Performance Characterization

Offset (for DAC)

- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data
Performance Characterization

*Offset* (for DAC)

\[ x_{\text{OUT}} \]

\[ x_{\text{REF}} \]

\[ \tilde{X}_{\text{IN}} \]

Offset relative to fit of data
Performance Characterization

**Offset**

For ADC the offset is

\[ X_{T1} - X_{LSB} \]

\[ \frac{X_{T1} - X_{LSB}}{X_{LSB}} \] - absolute

\[ X_{T1} - X_{LSB} \] - in LSB
Offset

For ADC the offset is

- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data
Performance Characterization

**Offset**

For ADC the offset is

Offset relative to fit of data
Performance Characterization

Gain and Gain Error

For DAC

\[ \mathbf{X}_{\text{REF}} \rightarrow \mathbf{X}_{\text{OUT}} \]

Ideal Output

Actual Output

Gain Error

C₀, C₁, C₂, C₃, C₄, C₅, C₆, C₇

\( \hat{X}_{\text{IN}} \)
Performance Characterization

**Gain and Gain Error**

For ADC

![Graph showing actual and ideal output with gain error](image-url)
Gain and Offset Errors

- Fit line would give better indicator of error in gain but less practical to obtain in test
- Gain and Offset errors of little concern in many applications
- Performance often nearly independent of gain and offset errors
- Can be trimmed in field if gain or offset errors exist.