EE 505

Lecture 20

ADC Design
Analog to Digital Converters

\[ x_{\text{IN}} \xrightarrow{\text{ADC}} x_{\text{OUT}} \]

\[ x_{\text{OUT}} \]

\[ \begin{align*}
C_0 & : 000 \\
C_1 & : 001 \\
C_2 & : 010 \\
C_3 & : 011 \\
C_4 & : 100 \\
C_5 & : 101 \\
C_6 & : 110 \\
C_7 & : 111
\end{align*} \]
Analog to Digital Converters

The conversion from analog to digital in ALL ADCs is done with comparators

ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects
Nyquist Rate

\[ X_{IN}(t) \rightarrow \text{Nyquist-Rate ADC} \rightarrow X_{OUT}(kT) \]

\[ X_{CL} \]

T_{SIG}

Sampling Clock
Nyquist Rate

Sampling Clock
Over-sampling ratios of 128:1 or 64:1 are common. Dramatic reduction in quantization noise effects are limited to relatively low frequencies.
Data Converter Type Chart

- **Resolution**:
  - 4
  - 8
  - 12
  - 16
  - 20
  - 24

- **Speed**:
  - 1K
  - 10K
  - 100K
  - 1M
  - 10M
  - 100M
  - 1G
  - 10G

- **Areas**:
  - **Oversampled**
  - **Nyquist**
ADC Types

Nyquist Rate
- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled
- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time
Nyquist Rate Usage Structures

Flash is the least used as a stand-alone structure but widely used as a subcomponent in SAR and Pipelined Structures.
ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

All have comparable conversion rates

Basic approach in all is very similar
Flash ADC

Thermometer to Binary Decoder

Thermometer to Binary Decoder

Vin

VREF

R

R

R

R

Vin

R/2

R/2

XOUT

n

XOUT

n
Flash ADC

Basic structure has thermometer code at output

Performance Issues:

+ Very fast
+ Simple architecture
+ Instantaneous (asynchronous) output

− Bubble vulnerability
− Input change during conversion
− Number of components and area (for large n)
− Loading of $V_{\text{REF}}$
− Propagation of $V_{\text{IN}}$
− Power dissipation (for large n)
− Offset and speed of comparators
− Layout of resistors
− Voltage and temperature dependence of R’s
− Matching of R’s
Flash ADC

Bubble Removal Approach
Flash ADC

Another Bubble Removal Approach
Flash ADC

Basic structure has thermometer code at output

Performance Issues:

+ Very fast
+ Simple architecture
+ Instantaneous (asynchronous output)
+ Good DNL with low comparator offsets

- Bubble vulnerability
- Input change during conversion
- Wide range of common-mode comparator inputs
- Number of components and area (for large n)
- Loading of \( V_{\text{REF}} \) and \( V_{\text{IN}} \)
- Propagation of \( V_{\text{IN}} \)
- Power dissipation (for large n)
- Offset and speed of comparators
- Layout of resistors
- Voltage and temperature dependence of R’s
- Matching of R’s
Input change during conversion

Flash ADC with Front-End S/H

- Speed of sample/hold of concern
- Noise of S/H
- Nonlinearity of S/H
- Input range of S/H
- Loose asynchronous operation of ADC (so can clock comparators)
Input change during conversion

Flash ADC with Front-End S/H
Input change during conversion

Front-End S/H and Clock of Comparators in Flash ADC

- Speed of sample/hold of concern
- Noise of S/H
- Nonlinearity of S/H
- Input range of S/H
- Loose asynchronous operation of ADC
Input change during conversion

Flash ADC with Front-End S/H

Input S/H with Clk

Input S/H with Clk and clocked comparators
Clocked Comparator with Regenerative Feedback

- Regenerative feedback often used to force decision when differential inputs are small
- Several variants of clocked comparators are available
- Important to not have trip point dependent upon previous comparison results
- Often one or more linear gain stages precede the regenerative stage
- Power dissipation can be small in regenerative feedback comparators
- Large offset voltage (100mV or more) common for regenerative feedback comparators
Clocked Comparator with Regenerative Feedback
Clocked Comparator with Regenerative Feedback

Lewis Gray Comparator

Sansen 92

Halonen Comparator

Katyal Comparator
Clocked Linear Comparator with Offset Compensation

Ideally removes all offset effects

May not have a large enough gain

Offset Compensation can be added to regenerative latch

Several variants of offset compensation circuits are available
End of Lecture 20