EE 505

Lecture 22

ADC Design
  – Folded
  – Multi-Step Flash
  – Pipeline
Review from last lecture

Interpolating Flash ADC

4 levels of interpolation
Preamp gain not critical
Common mode set at $V_{REF/2}$

Comparator Outputs:

- $V_k$ 0
- $V_{k1}$ 0
- $V_{k2}$ 1
- $V_{k3}$ 1
- $V_{k+1}$ 1

$V_{INX}$
Variants of Interpolating Flash

Patent Number: 5,867,116
Date of Patent: Feb. 2, 1999
Analog Devices

**Fig. 2**
(PRIOR ART)

**Fig. 11**
(PRIOR ART)

Standard Interpolator
Variants of Interpolating Flash

Patent Number: 5,867,116
Date of Patent: Feb. 2, 1999
Analog Devices

Flying Interpolator
Variants of Interpolating Flash

Standard R-String Interpolator

Interpolator can be based upon alternative DAC structures

- Current Steering
- Charge Redistribution
Flash ADC

Basic structure has thermometer code at output

**Performance Issues:**

- Very fast
- Simple architecture
- Instantaneous output
- Bubble vulnerability
- Input change during conversion
- Number of components and area (for large n)
- Speed of comparators
- Loading of $V_{\text{REF}}$ and $V_{\text{IN}}$
- Propagation of $V_{\text{IN}}$ and Kickback
- Power dissipation (for large n)
- Offset of comparators
- Layout of resistors
- Voltage and temperature dependence of R’s
- Matching of R’s
Flash ADC Summary

Flash ADC

- Very fast
- Simple structure
- Usually Clocked
- Bubble Removal Important
- Seldom over 6 or 7 bits of resolution

- Flash ADC has some really desirable properties (simple and fast)
- Wouldn’t it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

- Number of comparators increases geometrically --- $2^n$
- Too many comparators making non-critical decisions increases power
Premise: Folder provides large gain and is very fast

Similar in concept to interpolating flash ADC but

- Number of comparators has been reduced
- Thermometer to Binary decoder is eliminated
Folded ADC Architecture

- Provides gain in each fold region
- Effective input range increased from $V_{REF}$ to $N_2 V_{REF}$
- Reduces performance requirements of flash ADC by $N_2$
- Reduces number of comparators by factor of $N_2$
- Performance strongly dependent upon performance of folder
- With fast folders, speed comparable to that of a flash ADC
- Architecture of choice by Phillips (now NXP) for high-speed operation for many years (Rudy van de Plassche)
- Competes with pipeline for performance
Folded ADC Architecture

- Requires \( \frac{N_2}{2} \) differential amplifiers
- Basic Folder Circuit (8 level)
- Simple Differential Pair can be very fast
Folded ADC Architecture

- Usually implemented in differential form
- Differential output almost free
Nonlinearity in folder not a major problem since resolution nonlinearity affects primarily the LSBs and resolution of folded ADCs not large.
Multi-Step Flash Approaches

Goal with Multi-Step Flash Approach:
- Reduce number of comparators and sub DAC levels
- Reduce or eliminate unnecessary comparator decisions
Two-Step Flash ADC

- Can operate asynchronously after S/H
- If clocked, $C_{LK2}$ must be delayed from $C_{LK1}$
- Full-range of Residue signal is $V_{REF}/N_1$
- Reduces number of comparators by factor of $N_1$
- $V_{REF2}$ can be reduced by a factor of $N_1$ from $V_{REF}$

- No improvement in offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of $N_1$

$N_1 = 2^{n_1}$
$N_2 = 2^{n_2}$
Three-Step Flash ADC

\[ N_1 = 2^{n_1} \]
\[ N_2 = 2^{n_2} \]
\[ N_3 = 2^{n_3} \]

- Can operate asynchronously after S/H
- Full-range of Residue 2 signal is \( V_{\text{REF}}/(N_1 N_2) \)
- Reduces number of comparators by factor of \( N_2 \cdot N_1 \)
- \( V_{\text{REF3}} \) can be reduced by a factor of \( N_2 \) from \( V_{\text{REF2}} \)

- No improvement in offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of \( N_1 \)
Two-Step Flash ADC with Interstage Gain

\[ X_{IN} \rightarrow S/H \rightarrow C_{LK1} \rightarrow \text{Flash ADC}_1 \rightarrow V_{REF} \rightarrow \text{Residue} \rightarrow A \rightarrow \text{Digital Assembler} \rightarrow X_{OUT} \]

\[ n_1 \] MSB

\[ n_2 \] LSB
Two-Step Flash ADC with Interstage Gain and S/H
Three-Step Flash ADC with Interstage Gain and S/H

- S/H frees first stage to take another sample during second stage conversion
- This has a pipelining capability
- The pipelined approach dramatically improves speed (close to Flash)
- Significantly reduces the number of comparators
- Introduces latency but not of concern in most applications
End of Lecture 22