EE 505

Lecture 25

ADC Design

– Pipeline
Claim: If the Amplifiers are linear, settling is complete, and over-range protection is provided, the pipelined ADC makes no errors if the output of the DACs are correctly interpreted.

Implication: Flash ADC errors, offsets in comparators and amplifiers, and gain errors in amplifier and S/H do not degrade performance of a pipelined ADC structure!!
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

Review from last lecture

- Parameterization of Stage k
  - Amplifier
    - Closed-Loop Gain
      - From input – m1k
      - From DAC – m2k
      - From offset – m3k
    - Offset Voltage - $V_{OSk}$
  - DAC
    - $V_{DACki}$
  - ADC
    - Offset Voltages - $V_{OSAki}$
    - Out-Range Circuit (if used and not included in ADC/DAC)
      - DAC Levels - $V_{DACBki}$
      - Amplifier Gain – m4k
Solution of the 2n Linear Equations

\[ V_{in} = \left\{ d_1 \left[ \left( \frac{m_{21}}{m_{11}} \right) V_{DAC1} \right] + d_2 \left[ \left( \frac{m_{22}}{m_{11}m_{12}} \right) V_{DAC2} \right] + \ldots + d_n \left[ \left( \frac{m_{2n}}{m_{11}m_{12} \ldots m_{1n}} \right) V_{DACn} \right] + \frac{V_{REF}}{2^{n+1}} \right\} \]

\[ + \left\{ \frac{m_{31}}{m_{11}} V_{OS1} + \frac{m_{32}}{m_{11}m_{12}} V_{OS2} + \ldots + \left( \frac{m_{3n}}{m_{11}m_{12} \ldots m_{1n}} \right) V_{OSn} \right\} \]

\[ + \left\{ \frac{V_{RESn}}{m_{11}m_{12} \ldots m_{1n}} - \frac{V_{REF}}{2^{n+1}} \right\} \]

Term involving digital output codes

Code-independent offset term

Code-dependent but can be bounded by \( \frac{1}{2} \) LSB with out-range strategy
Review from last lecture

Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

\[ V_{\text{RES}k} = m \ V_{1k}^{\text{OUT}k} + m \left( \sum_{j=1}^{2^k-1} d_{kj} V_{\text{DAC}kj} \right) + m \ V_{3k}^{\text{OS}k} \]

If more than 1 bit/stage is used and DAC is binarily-weighted structure
Observations

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

form of \( \alpha_k : V_{DACk} \frac{m_{2k}}{\prod_{j=1}^{1} m_{1j}} \)

- Substantial errors are introduced if \( \alpha_k \) are not correctly interpreted!
- Some calibration and design strategies focus on accurately setting gains and DAC levels
- Analog calibration can be accomplished with either DAC level or gain calibration
- Digital calibration based upon coefficient identification does not require accurate gains or precise DAC levels
Observations (cont)

If nonlinearities are avoided, data conversion process with a pipelined architecture is extremely accurate.

Major challenge at low frequencies is accurately interpreting the digital output codes.

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

form of \( \alpha_k \):

\[ \alpha_k : V_{DAC_k} \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \]

- If nonlinearities are avoided, data conversion process with a pipelined architecture is extremely accurate.
- Major challenge at low frequencies is accurately interpreting the digital output codes.
Observations (cont)

If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable!

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

Form of \( \alpha_k \):

\[ \alpha_k : V_{DAC_k} \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \]

- If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable!
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

Over-range Protection

Extra comparator levels in ADC (2 extra comparators)

Review – preparing for calibration:

Review from last lecture
Amplifier Types used In Pipelined ADCs

- Two-stage
- Cascode
  - Telescopic
  - Folded
- Regulated Cascode (Gain-boosted Cascode)
  - Telescopic
  - Folded
- Regenerative Feedback Gain Enhancement
- Two-State Cascode
Amplifier Nonlinearity Becoming Increasingly Significant as $V_{DD}$ Reduced

Comparison of amplifiers at same power level and same $V_{EB}$

- Nonlinearity strongly architecture dependent
- Trade-Offs between Gain and Signal Swing

Drop in gain seriously degrades linearity and spectral performance
How Much Gain?

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in closed loop gain

Often see authors use

$$A_{dB} \approx 6n_{ST} + 12$$

- Gives no information about drop in gain at boundary of input/output window
- Maybe uses too much error budget on gain
- No indication how $A_{dB}$ relates to INL or DNL
- Gain requirements are large on the input buffer ($n_{ST}=n$) but will be significantly relaxed on latter stages in the pipeline when $n_{ST}$ decreases
## Pipelined Data Converter Design Guidelines

<table>
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<th>Issue</th>
<th>Strategy</th>
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| 1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate | 1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if $\alpha_k$’s correctly interpreted  
   a) Use Extra Comparators  
   b) Use sub-radix structures |
| 2. Correct interpretation of $\alpha_k$’s is critical                | 2. a) Accurately set $\alpha_k$ values  
   b) Use analog or digital calibration |
| 3. Op Amp Gain causes finite gain errors and introduces nonlinearity | 3. a) Select op amp architecture that has acceptable signal swing  
   b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors |

Review from last lecture
Performance Limitations
(consider amplifier, ADC and DAC issues)

- **ADC**
  - Break Points (offsets)
- **DAC**
  - DAC Levels (offsets)
    - Out-range (over or under range)
- **Amplifier**
  - Offset voltages
  - **Settling Time**
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Component mismatch
    - Inadequate open loop gain
  - Power Dissipation
  - kT/C switching noise
Amplifier Settling Time

- Can show that no distortion is introduced in pipelined ADC if the amplifier settling is linear (i.e. don’t worry about incomplete settling)
- But invariably slew rate and op amp nonlinearities will cause settling to be nonlinear
- Since can’t guarantee linear settling, must design for complete settling
Amplifier Settling Time

Worst Case Settling

- Neglect over-range protection (could be up against over-range limit)
- Occurs when input causes output to swing from 0 to $V_{REF}$

$V_{REF} = V_{R+} - V_{R-}$
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step on output in each stage

Note: This may not be quite good enough since allocating total error budget to settling of each stage

Compensated Operational Amplifier can be approximately modeled by

$$A_{ol}(s) \approx \frac{A_0 \cdot p_F}{s + p_F} = \frac{GB}{s + p_F}$$
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step in each stage

$$A_{OL}(s) \approx \frac{A_0 p_{OL}}{s+p_{OL}} = \frac{GB}{s+p_{OL}}$$

$$A_{FB}(s) \approx \frac{A_0 p_{OL}}{s+p_{OL} + \beta p_{OL}} = \frac{\theta \cdot GB}{s+\beta GB}$$

Step response (if slewing is neglected)

$$r(t) = F + (1-F)e^{-\beta GBt_s}$$

$$V_{REF}(1-\varepsilon) = V_{REF}(1-e^{-\beta GBt_s})$$

$$1-\varepsilon = 1-e^{-\beta GBt_s}$$

$$\varepsilon = e^{-\beta GBt_s}$$

$$V_{OUT} = (1-\varepsilon)V_{REF}$$

or, in terms of the time constant $\tau$ of closed loop amplifier

$$t_s = -\frac{\ln(\varepsilon)}{\beta GB}$$

$$t_s = -\tau \ln(\varepsilon)$$
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step in each stage

Define $n_{ST}$ to be the number of bits of resolution at the residue output of a stage

Step response (if slewing is neglected)

$$\varepsilon = \frac{1}{2^{n_{ST}+1}} \ln(\varepsilon) = -.693(n_{ST}+1)$$

$$t_s \approx 0.7 \left(n_{ST} + 1\right) \tau$$

- linear increase in settling requirements with $n_{ST}$
- $n_{ST}$ determined by accuracy requirements at residue output of a stage

Still need design requirements for GB of Op Amp

$$t_s \approx \frac{0.7(n_{ST}+1)}{\beta GB}$$
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step in each stage

Step response (if slewing is neglected)

Design requirements for GB of Op Amp

$$t_s \approx 0.7 \left( n_{st} + 1 \right) \frac{1}{\beta GB}$$

$$t_s = t_{AMP} \approx \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

$$GB_{RPS} \approx 1.4 \left( n_{st} + 1 \right) f_{CLK}$$

$$GB_{HZ} \approx 0.22 \left( n_{st} + 1 \right) f_{CLK}$$

Note: GB requirements drop from stage to stage
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step in each stage

Compensated Operational Amplifier can be approximately modeled by

$$A(s) \approx \frac{A_0 p_F}{s+p_F} = \frac{GB}{s+p_F}$$

What about high-impedance op amp?
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step at each stage

What about high-impedance op amp driving capacitive load (including $\beta$ network)?

\[
A_{OL} = -\frac{g_m}{g_o} \quad \text{BW} = \frac{g_o}{C_L} \quad \text{GB} = \frac{g_m}{C_L}
\]
Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step

What about high-impedance op amp?

\[ t = (1-\varepsilon)V_{\text{REF}} \]

\[ A_{\text{OL}} = -\frac{g_m}{g_o} \]

\[ \beta = \frac{g_m}{C_L} \]

\[ A_{\text{FB}} \approx \frac{g_m}{sC_L + g_o + \beta g_m} \approx \frac{g_m}{sC_L + \beta g_m} = \frac{GB}{s + \beta GB} \]

Note this is identical in form to that from the internally compensated op amp.
Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step

Step response (if slewing is neglected)

Design requirements for GB of Op Amp apply to both compensated two-stage structures and high output impedance single-stage structures

\[ t_s \approx \frac{0.7 (n_{ST} + 1)}{\beta \text{GB}} \]

\[ t_{s \text{ AMP}} = t_{\text{CLK}} = \frac{T_{\text{CLK}}}{2} = \frac{1}{2f_{\text{CLK}}} \]

\[ GB_{RPS} \approx \frac{1.4 (n_{ST} + 1)}{\beta f_{\text{CLK}}} \]

\[ GB_{HZ} \approx \frac{0.22 (n_{ST} + 1)}{\beta f_{\text{CLK}}} \]

Notes: May be over-using error budget
Slewing will modestly slow response
## Pipelined Data Converter Design Guidelines

### Issue

1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate

2. Correct interpretation of $\alpha_k$’s is critical

3. Op Amp Gain causes finite gain errors and introduces nonlinearity

4. Op amp settling must can cause errors

### Strategy

1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if $\alpha_k$’s correctly interpreted
   - a) Use Extra Comparators
   - b) Use sub-radix structures

2. a) Accurately set $\alpha_k$ values
    - b) Use analog or digital calibration

3. a) Select op amp architecture that has acceptable signal swing
    - b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors

4. Select GB to meet settling requirements (degrade modestly to account for slewing)
Performance Limitations
(consider amplifier, ADC and DAC issues)

- **ADC**
  - Break Points (offsets)
- **DAC**
  - DAC Levels (offsets)
    - Out-range (over or under range)
- **Amplifier**
  - Offset voltages
- **Settling Time**
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Component mismatch
    - Inadequate open loop gain
- **Power Dissipation**
  - $kT/C$ switching noise
Dominant source of power dissipation is in the op amps in S/H and individual stages
Power Dissipation

- Power dissipation strongly dependent upon op amp architecture and design
- Power budgets critical and even a net 5% savings in power is significant!

Consider a single stage in the pipeline

Consider single stage open-loop op amp structures (e.g. telescopic cascode)

\[ A_{OL} = - \frac{g_{mT}}{g_{oT}} \]

\[ P_{OP AMP} \approx 2I_{DQ} (V_{DD} - V_{SS}) \]

Power increases linearly with \( I_{DQ} \)

For MOS implementation with basic reference SE op amp

\[ A_{OL} = - \frac{2I_{DQ}}{V_{EB}} \frac{1}{2\lambda I_{DQ}} = - \frac{1}{\lambda V_{EB}} \]

No power implications on dc gain of op amp
  - Pick \( V_{EB} \) small to increase gain
  - Keep lengths larger than minimum to make \( \lambda \) small
Power Dissipation

\[ GB = \frac{g_{mT}}{C_L} \]

For MOS implementation (with ref SE op amp or telescopic cascade op amp)

\[ GB = \frac{2I_{DQ}}{V_{EB} C_L} = \left( \frac{1}{(V_{DD} - V_{SS}) C_L} \right) \frac{P}{V_{EB}} \]

For convenience, define

\[ V_{SUP} = V_{DD} - V_{SS} \]

- \( P \) increases linearly with \( GB \)
- Keep \( V_{EB} \) small, \( C_L \) as small as possible, \( GB \) as small as possible
- At high speeds, diffusion parasitics will cause \( P \) to increase more rapidly than \( GB \)
- Total amplifier power is sum of power in each stage
Power Dissipation

\[ GB = \frac{g_m}{C_L} \]

For single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

\[ P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB} \]

At high speeds, diffusion parasitics will cause \( P \) to increase more rapidly than \( GB \).
Power Dissipation

\[ GB = \frac{g_m}{C_L} \]

For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

\[ P = \begin{bmatrix} V_{SUP} & GB & C_L \end{bmatrix} \begin{bmatrix} V_{EB} \end{bmatrix} \]

Fixed by ADC requirements

Select architectures that minimize architecture-dependent term

Architecture Dependent
Power Dissipation

$P = \left[ \begin{array}{c} V_{SUP} \\
\cdot GB \\
\cdot C_L 
\end{array} \right] \left[ \begin{array}{c} V_{EB} \end{array} \right]
$

Fixed by ADC requirements

For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

$P = \left[ \begin{array}{c} V_{SUP} \\
\cdot GB \\
\cdot C_L 
\end{array} \right] \left[ \begin{array}{c} V_{EB} \end{array} \right]
$

$GB_{Hz} \cong \frac{0.22(n_{ST} + 1)}{\beta} f_{CLK}
$

• $n_{ST} = n$ for S/H thus S/H is a major power consumer
• Use energy efficient op amp architecture
• Power increases linearly with GB (even faster at high frequencies)
• Interleaving can reduce power dissipation at high frequencies (and extend effective clock speed)
• Power increases linearly with clock speed (or worse at high frequencies)
• Power can be scaled down in latter stages since $n_{ST}$ will decrease
• Amplifiers can be shared between stages or switched off when not used (factor of 2!)
• Using more than one bit/stage will reduce power since no of op amps will decrease (offsets decrease in $\beta$)
• Elimination of S/H will have dramatic effect on power reduction
Power Dissipation

For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

\[
P = \begin{bmatrix} V_{\text{SUP}} & \bullet & \text{GB} & \bullet & C_L \end{bmatrix} \begin{bmatrix} V_{EB} \end{bmatrix}
\]

Fixed by ADC requirements

\[
\text{GB}_{\text{Hz}} \approx 0.22 \left( n_{\text{ST}} + 1 \right) f_{\text{CLK}} / \beta
\]

Which op amp architectures are most energy efficient?

- Depends upon \( \beta \)
- For smaller \( \beta \), two-stage are more energy efficient for larger \( \beta \) single-stage are better
- Must optimize power in any given architecture
- Folding reduces efficiency (typically by 30% to 50%)

Power Dissipation

\[
P = X_F \left( n_{ST} + 1 \right) C_L
\]

Example: How do the op amp power requirements change from one-stage to the next with two bits per stage in a 16-bit pipeline. Assume a charge-redistribution gain stage and the size of the capacitors are scaled to keep the noise contributions the same in each stage. Assume the first stage has a total sampling capacitor of value \( C_1 \),

\[
V_{n1} = \sqrt{\frac{kt}{C_1}}
\]

\[
V_{n2} = 4V_{n1}
\]

Will keep the dc op amp gain for each stage the same

\[
P_1 = X_F \left( 14 + 1 \right) C_L
\]

\[
P_2 = X_F \left( 12 + 1 \right) \frac{1}{16} C_L \approx 0.05 \cdot P_1
\]
Power Dissipation

Example sol continued:

\[ P_1 = X_F (14+1)C_{L1} \]

\[ P_2 = X_F (12+1) \frac{1}{16} C_{L1} \]

\[ P_3 = X_F (10+1) \frac{1}{16^2} C_{L1} \]

\[ P_4 = X_F (8+1) \frac{1}{16^3} C_{L1} \]

\[ P_5 = X_F (6+1) \frac{1}{16^4} C_{L1} \]

\[ P_6 = X_F (4+1) \frac{1}{16^5} C_{L1} \]

\[ P_7 = X_F (2+1) \frac{1}{16^6} C_{L1} \]

- Power completely dominated by first stage
- Will likely not scale C so much so noise will be dominated by first stage
- No benefit from scaling power in latter stages
## Pipelined Data Converter Design Guidelines

### Issue

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2. Correct interpretation of $\alpha_k$'s is critical

3. Op Amp Gain causes finite gain errors and introduces nonlinearity

4. Op amp settling must can cause errors

5. Power dissipation strongly dependent upon GB of Op Amps

### Strategy

1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if $\alpha_k$'s correctly interpreted
   - a) Use Extra Comparators
   - b) Use sub-radix structures

2. a) Accurately set $\alpha_k$ values
   - b) Use analog or digital calibration

3. a) Select op amp architecture that has acceptable signal swing
   - b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors

4. Select GB to meet settling requirements
   (degrade modestly to account for slewing)

5. Minimize $C_L$, use energy efficient op amps, share or shut down op amp when not used, scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies
Power Efficiency and Settling Time Enhancement

Minimization of Power in Operational Amplifiers
- Reduce Power in Less Significant Stages
- Share Operational Amplifiers Between Stages
- Interleave Amplifiers Between Parallel Paths
- Power-Down Operational Amplifiers When Not Used
- Dynamically Bias Operational Amplifiers
- Use Operational Amplifier Architectures that are More Energy Efficient
Energy-Efficient Operational Amplifier Architectures?

• Settling Time Inversely Proportional to GB of an OP AMP (during linear settling)

• How does the energy efficiency of GB for various op amps compare?
Power Dissipation

\[ GB = \frac{g_m}{C_L} \]

For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

\[ P = \begin{bmatrix} V_{SUP} \cdot GB \cdot C_L \end{bmatrix} \begin{bmatrix} V_{EB} \end{bmatrix} \]

Fixed by ADC requirements

Select architectures that minimize architecture-dependent term

\[ GB = \begin{bmatrix} \frac{P}{V_{SUP} \cdot C_L} \end{bmatrix} \begin{bmatrix} \frac{1}{V_{EB}} \end{bmatrix} \]
Power Dissipation

\[ GB = \frac{g_m}{C_L} \]

For Single-stage MOS implementation (with ref FD op amp or telescopic cascade op amp)

\[ P = \left[ \begin{array}{c} V_{SUP} \cdot GB_2 \cdot C_L \end{array} \right] \left[ \begin{array}{c} V_{EB} \end{array} \right] \]

Fixed by ADC requirements

Select architectures that minimize architecture-dependent term

\[ GB = \left[ \frac{2P}{V_{SUP} C_L} \right] \left[ \frac{1}{V_{EB}} \right] \]
Figure of Merit for Comparing Energy Efficiency of Op Amps

For Single-stage MOS implementation (with ref FD op amp or telescopic cascade op amp)

\[ GB = \frac{2 \cdot P}{V_{DD} C_L} \cdot \frac{1}{V_{EB}} \]

Architecture Independent

Architecture Dependent

\[ FOM = \frac{GB \cdot V_{SUP}}{2P} \cdot \frac{C_L}{\sup \cdot L} \]

\[ "\text{Generic MOS Cascode-Type OpAmp}" \]

\[ FOM = \frac{1}{V_{EB1}} \]
Consider the Basic Single-State FD Op Amp

![Diagram of a basic single-state FD Op Amp].

- $V_{DD}$
- $V_{b1}$
- $V_{b2}$
- $V^{+}_{IN}$
- $V^{-}_{IN}$
- $V_{OUT}$
- $Q_1$, $Q_2$, $Q_3$, $Q_4$, $Q_9$

$C_L$ on Differential Outputs Not Shown

CMFB Not Shown
Consider the Basic Single-State FD Op Amp

**Differential Half-Circuit**

\[ V_{IN} = \frac{V_{IN}^+ - V_{IN}^-}{2} = \frac{V_{DIFF}}{2} \]

\[ A(s) = \frac{-g_m/2}{sC_L + [g_{o2} + g_{o1}]} \]

\[ A_o = \frac{g_m/2}{g_{o1} + g_{o2}} \]

\[ BW = \frac{g_{o1} + g_{o2}}{C_L} \]

GB = \[ \frac{g_m}{2C_L} = \frac{2I_Q}{2V_{EB}C_L} = \left[ \frac{P}{2V_{DD}C_L} \right] \frac{1}{V_{EB}} \]
Basic Single-Stage FD Op Amp

\[ FOM = \frac{1}{V_{EB1}} \]

C\textsubscript{L} on other output Not Shown

CMFB Not Shown
Consider the Basic Single-State FD Op Amp

Differential Half-Circuit

\[ \text{GB} = \left[ \frac{P}{2V_{DD}C_L} \right] \left[ \frac{1}{V_{EB}} \right] \]

Observations

- GB (settling time) improves linearly with P
- GB (settling time) improves with decreasing \( V_{EB} \)
Consider the Basic Single-State Op Amp

Differential Half-Circuit

\[
GB = \left[\frac{P}{2V_{DD}C_L}\right]\left[\frac{1}{V_{EB}}\right]
\]

Observations

- GB (settling time) improves linearly with \( P \).
  Is there any fundamental limit?
- GB (settling time) improves with decreasing \( V_{EB} \).
  Conflict with conventional wisdom that speed \((f_T)\) increases with \( V_{EB} \)?
- What assumptions implicit to draw these conclusions?
  \( C_L \) dominates parasitic capacitances
Energy Efficiency of Popular Op Amps

Assume parasitic capacitances on output negligible compared to external load capacitance
End of Lecture 25