EE 505

Lecture 27

ADC Design
  – Pipeline
If the ON impedance of the switches is small and it is assumed that $C_1 = C_2 = C$, it can be shown that

$$\hat{\psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{2C} + \frac{kTR_4GB}{4}}$$

Too much GB or too large of $R_{SW}$ can increase sampled noise voltage.

Too small of $R_{SW}$ will not derive any benefit and will increase power, area, and driving problems.
Sampling Noise

• Capacitors introduce no noise

• Noise is, however, present in switches that take samples

• This switch noise causes SNR problems in the amplifier if not correctly managed
Sampling Noise

(a) (b)
Sampling Noise

(a) $V_{IN}$ $C$ $V_{OUT}$ $S_1$ $C_{LK}$

(b) $V_{IN}$ $C$ $V_{OUT}$ $R_{SW}$

(c) $V_{IN}$ $C$ $V_{OUT}$

High

Low

$T_{CLK}$

TRACK

HOLD
Sampling Noise

$V_{\text{IN}}$

$V_{\text{OUT}}$

$C_{\text{LK}}$
Sampling Noise

$V_{\text{OUT}}(t)$

$V_{\text{OUT}}(kT)$

$C_{\text{LK}}$
Sampling Noise

$V_{OUT}(t)$

$V_{OUT}(kT)$

$C_{LK}$
Sampling Noise

Power spectral density of any resistor, $R_{SW}$, is given by

$$S_{VR} = 4kT R_{SW}$$

This is thermal noise and often termed “white” noise since the spectral dissipation is uniform for all $f$. 

$9$
Sampling Noise

Theorem 1  If $v_n(t)$ is a continuous-time zero-mean noise source with power spectral density $S_v$, then the spectral density of $v_{OUT}$ is given by the expression

$$S_{v_{OUT}} = |T(s)|^2 S_v$$

The RMS value of a continuous-time random variable $V(T)$ is defined to be

$$V_{RMS} = E\left(\sqrt{\lim_{T \to \infty} \left( \frac{1}{T} \int_0^T V^2(t) dt \right)} \right)$$

The RMS value of a random sequence $<V(kT)>$ is defined to be

$$\hat{V}_{RMS} = E\left(\sqrt{\lim_{N \to \infty} \left( \frac{1}{N} \sum_{k=1}^N V^2(kT) \right)} \right)$$

( the operator E is the expected value operator)

(these definitions apply to non-random signals as well)
Sampling Noise

Theorem 1  If $v_n(t)$ is a continuous-time zero-mean noise source with power spectral density $S_v$, then the spectral density of $v_{OUT}$ is given by the expression

$$S_{v_{OUT}} = |T(s)|^2 S_v$$

Theorem 2  If $v(t)$ is a continuous-time zero-mean noise voltage with power spectral density $S_v$, then the RMS value of the continuous-time noise is given by

$$V_{RMS} = \sqrt{\int_{f=0}^{\infty} S_v df}$$

Note: There are some parts of the hypothesis of this theorem that have not been stated such as stationary of the distribution and no correlation between samples spaced T seconds apart..
Sampling Noise

\[ S_{VR} = 4kTR_{SW} \]

\[ S_{VOUT} = 4kTR \left( \frac{1}{1 + (RC\omega)^2} \right) \]
Sampling Noise

\[
S_{V_{OUT}} = 4kTR \left( \frac{1}{1 + (RC\omega)^2} \right)
\]

\[
V_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1 + \omega^2 R^2 C^2} \, df}
\]

Recall:

\[
\int_{y=0}^{\infty} \frac{1}{1 + y^2} \, dy = (\tan^{-1} y) \bigg|_{y=0}^{\infty} = \frac{\pi}{2}
\]

\[
V_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \frac{kT}{\sqrt{C}}
\]

Key Result, Continuous-time noise at \(V_{OUT}\)
**Sampling Noise**

- Since noise is independent of $V_{REF}$, would like to make $V_{REF}$ as large as possible to minimize $C$ sizing

- Scaling to lower supply voltage has a negative impact on capacitor sizing (scaling supply by 2 requires increasing $C$ by factor of 4)
Sampling Noise

Capacitance vs Resolution ($V_{\text{REF}}=1V$, 1/2 LSB level)

Example: 14-bit ADC  $C=4.6\text{pF}$
Sampling Noise

**Theorem 3** If $V(t)$ is a continuous-time zero-mean noise voltage and $<V(kT)>$ is a sampled version of $V(t)$ sampled at times $T, 2T, \ldots$ then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as

$$V_{\text{RMS}} = \hat{V}_{\text{RMS}}$$

Note: There are some parts of the hypothesis of this theorem that have not been stated such as stationary of the distribution and no correlation between samples spaced $T$ seconds apart.
Sampling Noise

Theorem 4  If \( V(t) \) is a continuous-time zero-mean noise source and \( <V(kT)> \) is a sampled version of \( V(t) \) sampled at times \( T, 2T, \ldots \) then the standard deviation of the random variable \( V(kT) \), denoted as \( \sigma_{\hat{V}} \), satisfies the expression

\[
\sigma_{\hat{V}} = V_{\text{RMS}} = \hat{V}_{\text{RMS}}
\]

Theorem 5  The RMS value and the standard deviation of the noise voltage that occurs in the basic switched-capacitor sampler is related to the capacitor value by the expression

\[
\hat{V}_{\text{RMS}} = V_{\text{RMS}} = \sigma_{\hat{V}} = \sqrt{\frac{kT}{C}}
\]
Sampling Noise

Key Result, Continuous-time noise at $V_{OUT}$

$$V_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

Key Result, Discrete-time noise at $V_{OUT}$

$$\hat{V}_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$
Sampling Noise

But noise is actually a bit worse than simply $kT/C$

$$\beta_2 = \frac{C_2}{C_1 + C_2}$$
$$\beta_1 = 1$$
$$A_{FB2} = 1 + \frac{C_2}{C_1} = \frac{1}{\beta_2}$$

$$\beta = \frac{1 + \frac{C_2}{C_1}}{\beta_2}$$
Sampling Noise

RMS Noise Voltage on capacitors $C_1$ and $C_2$

\[
V_{n_{1,\text{RMS}}} = \sqrt{\frac{kT}{C_1}} \quad \text{and} \quad \hat{V}_{n_{1,\text{RMS}}} = \sqrt{\frac{kT}{C_1}}
\]

\[
V_{n_{2,\text{RMS}}} = \sqrt{\frac{kT}{C_2}} \quad \text{and} \quad \hat{V}_{n_{2,\text{RMS}}} = \sqrt{\frac{kT}{C_2}}
\]

$\beta_1 = 1$
Sampling Noise

\[ \beta_2 = \frac{C_2}{C_1 + C_2} \]

\[ V_{\text{out}} = V_{\text{in}} \left( 1 + \frac{C}{C_2} \right) - \delta V_{\text{ref}} \left( \frac{C}{C_2} \right) + \hat{V}_{\text{ref}} \left( \frac{C}{C_2} \right) + \hat{V}_{\text{r2}} \]

\[ \hat{V}_{\text{ref}} \left( 1 + R C_s \right) - \hat{V}_{\text{ref}} \left( \frac{C}{C_2} \left( 1 + R C_s \right) \right) \]

\[ + \frac{C}{C_2} + \frac{1}{\text{GB}} \left( 1 + \frac{C}{C_1} \right) + s' \frac{1}{\text{GB}} (R_1 + R_2) C_2 \]
Sampling Noise

If the ON impedance of the switches is small, it can be shown that

$$
\nu_{4-5\text{RMS}} = \sqrt{kT R_{\text{GB}}}
$$
Sampling Noise

If the ON impedance of the switches is small and it is assumed that \( C_1 = C_2 = C \), it can be shown that

\[
\begin{align*}
\nu_{\text{4-RMS}} & = \sqrt{kT R_4 G B} \\
\hat{\nu}_{\text{in-RMS}^2} & = \sqrt{\frac{2kT}{C} + kT R_4 G B} \\
\hat{\nu}_{\text{in-RMS}} & = \sqrt{\frac{kT}{2C} + \frac{kT R_4 G B}{4}}
\end{align*}
\]

\[ \beta_2 = \frac{C_2}{C_1 + C_2} \]
Sampling Noise

If the ON impedance of the switches is small and it is assumed that $C_1 = C_2 = C$, it can be shown that

$$\hat{\nu}_{IN-RMS} = \sqrt{\frac{kT}{2C} + \frac{kTR GB}{4}}$$

If size switches so that

$$R_{SW} = \frac{1}{Cf_{CLK} 2\ln(2)(n_{ST} + 1)}$$

$$\hat{\nu}_{IN-RMS} \approx \sqrt{\frac{kT}{2C}}$$
Sampling Noise

\[ \beta_2 = \frac{C_2}{C_1 + C_2} \]

If the ON impedance of the switches is small and it is assumed that \( C_1 = C_2 = C \), it can be shown that

\[ \hat{V}_{\text{IN-RMS}} = \sqrt{\frac{kT}{2C} + \frac{kTR^4GB}{4}} \]

Too much GB or too large of \( R_{SW} \) can increase sampled noise voltage.

Too small of \( R_{SW} \) will not derive any benefit and will increase power, area, and driving problems.
Sampling Timing

Even numbered stages sampled with $\phi_1$ and odd stages sampled with $\phi_2$
Quiet sampling is important
Sizing switches for constant input

Consider any first-order RC network

Target Settling: to $\frac{1}{2}$ LSB in time $T_{CLK}/2$ for worst-case transition
Switch Sizing

Target Settling: to $\frac{1}{2}$ LSB in time $T_{CLK}/2$ for worst-case transition

\[ V_{REF} \left( 1 - e^{-\frac{t}{RC}} \right) = V_{REF} - V_{REF} \frac{1}{2^{n_{ST} + 1}} \]

\[ e^{-\frac{t}{RC}} = \frac{1}{2^{n_{ST} + 1}} \]

\[ R = \frac{t}{(n_{ST} + 1)C\ln2} \]

\[ R_{SW} = \frac{1}{f_{CLK} (n_{ST} + 1)C2\ln2} \]
Switch Sizing

To settle to $\frac{1}{2}$ LSB in time $T_{\text{CLK}}/2$

$$R_{\text{sw}} = \frac{1}{C_{\text{H}} f_{\text{CLK}} 2 \ln(2)(n_{\text{st}} + 1)}$$

Recall minimum GB requirement (which is usually what will be designed for)

$$\text{GB} = \frac{(n_{\text{st}} + 1) 2 \ln 2}{f_{\text{CLK}} \beta}$$

Eliminating $f_{\text{CLK}}$ we obtain

$$R_{\text{sw}} C_{\text{H}} = \frac{1}{\beta \text{GB}}$$

Define excess switch sizing factor $\theta$ by

$$R_{\text{sw}} = \frac{\theta}{C_{\text{H}} \beta \text{GB}}$$
Sampling Noise

Summary of Flip-around SC gain stage

\[ \beta_2 = \frac{C_2}{C_1 + C_2} \]

\[ A_{FB} = 1 + \frac{C_1}{C_2} \]

\[ \hat{V}_{IN-RMS} = \sqrt{\frac{kT}{C_1 + C_2} + \left( \frac{C_2}{C_1 + C_2} \right)^2 \hat{V}_{4-5RMS}^2} \]

\[ R_4 = \frac{\theta}{C_1 \beta GB} \]

\[ \eta_4 = \sqrt{2kT \frac{\theta}{C_1 \pi \left( 1 + \left( \frac{\beta}{1-\beta} \right) \right)^2} \int_{\omega=0}^{\infty} \left( \omega^2 (2\theta \beta)^2 + \omega^2 \left[ \theta + \frac{\beta}{1-\beta} \right]^2 - \frac{4\theta \beta^2}{1-\beta} + \left( \frac{\beta}{1-\beta} \right)^2 \right) \, d\omega} \]

Often \( \theta \ll 1 \) even with minimum sized devices and in this case \( \eta_{4-5RMS} \) is negligible

\[ \hat{V}_{IN-RMS} = \sqrt{\frac{kT}{C_1 + C_2}} \]
Sampling Noise

Two popular SC gain stages
Sampling Noise

Basic SC gain stage

\[ A_{FB} = -\frac{C_1}{C_2} \]

\[ \beta = \frac{C_2}{C_1 + C_2} \]
Sampling Noise

Basic SC gain stage

It can be shown that

\[ V_{\text{OUT}} = \frac{C_1}{C_2} \left( V_{\text{IN}} + dV_{\text{REF}} + V_{n1} \right) + V_n \]

\[ + \frac{C_1}{C_2} \left( \frac{1}{1 + R_4 C_1 s + \frac{s}{GB} \left( 1 + \frac{C_1}{C_2} + R_4 C_1 s \right)} \right) \]
Sampling Noise

Basic SC gain stage

\[ \beta = \frac{C^2}{C_1 + C_2} \quad \text{R} = \frac{\theta}{C_1 \beta GB} \]

\[ V_{\text{OUT}} = \frac{C_1}{C_2} \left( V_{\text{IN}} + dV + V_{\text{n1}} \right) + V_4 \frac{C_1}{C_2} \left( \frac{1}{1 + R_4 C_1 s + \frac{s}{GB} \left( 1 + \frac{C_1}{C_2} + R_4 C_1 s \right) } \right) \]

\[ \Psi_{\text{OUT-nRMS}} = \sqrt{\frac{2kT \theta}{C_1 \pi} \left( \frac{1-\beta}{\beta} \right)^2} \int_{\omega=0}^{\infty} \frac{1}{1 + \omega^2 \left[ (1+\theta)^2 - 2\theta \beta \right] + \omega^4 (\theta \beta)^2} d\omega \]

\[ \hat{\Psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{C_1} + \left( \frac{C_2}{C_1} \right)^2 \Psi_{\text{OUT-nRMS}}^2} \]

\[ \hat{\Psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{C_1}} \]

\( \theta \ll 1 \)
Sampling Noise

Two popular SC gain stages

\[ A_{FB} = 1 + \frac{C_1}{C_2} \]

\[ \beta_2 = \frac{C_2}{C_1 + C_2} \]

\[ \hat{\psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{C_1 + C_2} + \left( \frac{C_2}{C_1 + C_2} \right)^2 \hat{\psi}_{\text{OUT4-RMS}}} \]

\[ \psi_{\text{OUT4-RMS}} = \sqrt{\frac{2kT \theta (1-\beta)^2}{C_1 \pi \left( \frac{1}{\beta} \right)}} \cdot \frac{1}{1 + \omega^2 \left( (1+\theta)^2 - 2\theta \beta \right) + \omega^2 (\theta \beta)^2} \]

\[ \theta \ll 1 \quad \hat{\psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{C_1 + C_2}} \]

\[ A_{FB} = -\frac{C_1}{C_2} \]

\[ \beta = \frac{C_2}{C_1 + C_2} \]

\[ \hat{\psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{C_1} + \left( \frac{C_2}{C_1} \right)^2 \hat{\psi}_{\text{OUT4-RMS}}} \]

\[ \psi_{\text{OUT4-RMS}} = \sqrt{\frac{2kT \theta (1-\beta)^2}{C_1 \pi \left( \frac{1}{\beta} \right)}} \cdot \frac{1}{1 + \omega^2 \left( (1+\theta)^2 - 2\theta \beta \right) + \omega^2 (\theta \beta)^2} \]

\[ \theta \ll 1 \quad \hat{\psi}_{\text{IN-RMS}} = \sqrt{\frac{kT}{C_1}} \]
Sampling Noise

When is the continuous-time SC noise really of concern?

Recall

\[
\begin{align*}
GB &= \frac{(n_{ST} + 1)2\ln2}{\beta f_{CLK}} \\
\sqrt{\frac{kT}{C}} &= \frac{1}{2^{n+1}} \\
R_4 &= \frac{1}{C_1\beta GB}
\end{align*}
\]

Eliminating GB and C

\[
R_4 = \frac{1}{kT2^{2n_{ST}+2}(n_{ST}+1)2\ln2f_{CLK}}
\]
# Sampling Noise

When is the continuous-time SC noise really of concern?

\[
R_{\text{MAX}}(f_{\text{CLK}}, n) = \frac{1}{kT2^{2n_{\text{ST}} + 2}(n_{\text{ST}} + 1)2\ln2_{\text{CLK}}}
\]

## Clock Speed

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**Sampling Noise**

When is the continuous-time SC noise really of concern?

\[
R_{\text{MAX}} = \frac{1}{kT2^{2n_{\text{ST}} + 2}(n_{\text{ST}} + 1)2\ln2_{\text{CLK}}}
\]

Where:
- \( k \) is the Boltzmann constant
- \( T \) is the temperature in Kelvin
- \( n_{\text{ST}} \) is the number of sampling instances
- \( f_{\text{CLK}} \) is the clock frequency

---

**Resolution**

- **10M**: 10,000,000
- **1G**: 1,000,000,000

---

**Clock Speed**

- **10**: 10
- **100**: 100
- **1K**: 1,000
- **10K**: 10,000
- **100K**: 100,000
- **1M**: 1,000,000
- **10M**: 10,000,000
- **100M**: 100,000,000
- **1G**: 1,000,000,000
Sampling Noise

What about this one?

Series-Parallel Structure

$$A_{FB} = ?$$

$$\beta = ?$$
Sampling Noise

Sampling noise from all stages must be referred back to input!

\[ \nu_{INRMS} = \nu_{IN1}^2 + \frac{1}{A_1^2} \nu_{IN2}^2 + \frac{1}{A_1^2 A_2^2} \nu_{IN3}^2 + \ldots + \frac{1}{A_1^2 A_2^2 \ldots A_{n-1}^2} \nu_{INn}^2 \]

\[ \nu_{INRMS} = \sqrt{\nu_{IN1}^2 + \sum_{k=2}^{n} \left( \frac{\nu_{INk}}{\prod_{i=1}^{k-1} A_i} \right)^2} \]

See Katyal, Lin and Geiger, ISCAS, for capacitor sizing for minimization of noise and power.
Sampling Timing

Even numbered stages sampled with $\phi_1$ and odd stages sampled with $\phi_2$

First Sample
- $S_1S$
- $S_1T$
- $S_2S$
- $S_2T$
- $S_3S$
- $S_3T$
- $S_4S$
- $S_4T$
- $S_5S$
- $S_5T$
- $S_6S$
- $S_6T$
- $S_7S$
- $S_7T$
- $S_8S$

Second Sample
- $S_1S$
- $S_1T$
- $S_2S$
- $S_2T$
- $S_3T$
- $S_3S$
- $S_4T$
- $S_4S$
- $S_5T$
- $S_5S$
- $S_6T$
- $S_6S$
Quiet sampling is important
Bootstrapped Switch

The ideal sampling operation

Should track $V_{IN}$ in the TRACK mode
Should accurately sample $V_{IN}$ at transition to HOLD mode
Bootstrapped Switch

The ideal sampling operation

Should track $V_{IN}$ in the TRACK mode
Should accurately sample $V_{IN}$ at transition to HOLD mode
Bootstrapped Switch

The ideal sampling operation

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{1 + R_{SW2} C_{L}s}{1 + (R_s + R_{SW1} + R_{SW2}) C_{L}s}
\]

For high frequency inputs, an attenuation error will occur

Affects absolute accuracy but not linearity

But, if switches are nonlinear, will introduce a nonlinear error that can be very substantial

Signal dependent \(R_{SW}\) or switch nonlinearity will introduce nonlinear errors
Bootstrapped Switch

Bootstrapping Principle

V_{DD} \quad C_X \quad \Phi_1 \quad \Phi_1 \quad \Phi_1 \quad \Phi_1
Bootstrapped Switch

Bootstrapping Principle

• May have difficult time turning on some switches
• May stress gate oxide!
Bootstrapped Switch

Bootstrapping Principle

From Galton, ISSCC 04
Bootstrapped Switch

Bootstrapping Principle

Fig. 7. Bootstrap circuit and switching device.

From Abo and Gray JSC 99
Bootstrapped Switch

Bootstrapping Principle

From Roberts MWSCAS 2000
Bootstrapped Switch

Bootstrapping Principle

Fig. 7. Transistor-level implementation of the bootstrapped switch.

From Kaiser JSC 2001
Bootstrapped Switch

Bootstrapping Principle

From Steensgaard  ISCAS 1999

Figure 5: Bootstrapped switch.
# Pipelined Data Converter Design Guidelines

## Issue

1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate

2. Correct interpretation of $\alpha_k$'s is critical

3. Op Amp Gain causes finite gain errors and introduces nonlinearity

4. Op amp settling must can cause errors

5. Power dissipation strongly dependent upon GB of Op Amps

6. Choice of FB Amplifier Architecture seriously impacts performance

## Strategy

1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if $\alpha_k$'s correctly interpreted
   a) Use Extra Comparators
   b) Use sub-radix structures

2. a) Accurately set $\alpha_k$ values
    b) Use analog or digital calibration

3. a) Select op amp architecture that has acceptable signal swing
    b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors

4. Select GB to meet settling requirements
   (degrade modestly to account for slewing)

5. Minimize $C_L$, use energy efficient op amps, share or shut down op amp when not used, scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies

6. Bottom plate sampling, bootstrapping, clock advance to reduce aperture uncertainty, critical GB, parasitic insensitivity needed, $\beta$ dependent upon architecture and phase, compensation for worst-case $\beta$, TG if needed
Pipelined Data Converter Design Guidelines

### Issue

7. Sampling operation inherently introduces a sampled-noise due to noise in resistors

8. Signal-dependent tracking errors at input introduce linearity degradation

### Strategy

7. Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage).

8. Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches.
Aperture Uncertainty

\[ V_{\text{in}} = \frac{V_{\text{REF}}}{2} (1 + \sin \omega t) \]

\[
\frac{\partial V_{\text{in}}}{\partial t} = \frac{V_{\text{REF}}}{2} \omega \cos \omega t \\
\left. \frac{\partial V_{\text{in}}}{\partial t} \right|_{\text{MAX}} = \frac{V_{\text{REF}}}{2} \omega \\
\Delta T < \left. \frac{\Delta V_{\text{MAX}}}{\partial V_{\text{in}}/\partial t} \right|_{\text{MAX}} = \frac{V_{\text{REF}}}{\omega V_{\text{REF}}/2} = \frac{2^{n+1}}{\omega V_{\text{REF}}} \\
\Delta T < \frac{1}{\omega 2^n} \]
Aperture Uncertainty

\[ V_{\text{in}} = \frac{V_{\text{REF}}}{2} (1 + \sin \omega t) \]

\[ \Delta T < \frac{1}{\omega 2^n} \]

Example: If \( f_{\text{CLK}} = 200\,\text{MHz} \), \( n = 14 \) determine the aperture uncertainty

\[ \Delta T < \frac{1}{2\pi (2\times10^8)2^{14}} = 4.86\times10^{-14} \approx 0.05\,\text{psec} \]

Aperture uncertainty requirements can be very stringent!
Elimination of Input S/H

Why is input S/H used?
Elimination of Input S/H

Why is input S/H used?

Conventional Wisdom:
Because want right sample at input
Because gain stages mess up when input is time varying

But what does an ADC error do to the Boolean output?

\[ V_{\text{in}} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

Absolutely nothing if over-range protection is provided!
Elimination of Input S/H

Why is input S/H used?

Conventional Wisdom:

Because want right sample at input
Because gain stages mess up when input is time varying
Elimination of Input S/H

Advance sampling clock a little so that sample is taken at quiet time but not too much to loose over-range protection
Fully Differential Architectures

Second-order spectral component is often most significant contributor to SFDR and THD limitations in single-ended structures

Noise from ADC and other components, coupled through the substrate, often source of considerable noise in an ADC

- All even-ordered spectral components are eliminated with fully-differential symmetric structures
- Common mode noise is rejected with fully-differential symmetric structures

Almost all implementations of Pipelined ADCs are fully-differential

Straightforward modification of the single-ended concepts discussed here

Authors often present structures in single-ended mode and then just mention that differential structure was used

Modest (but small) increase in area and power for fully differential structures
## Pipelined Data Converter Design Guidelines

### Issue

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Pipelined Data Converter Design Guidelines

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<td>9. Since latency usually of little concern, be sure that a clean clock is used to control all sampling.</td>
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<td>10. Input S/H major contributor to nonlinearity and power dissipation</td>
<td>10. Eliminate S/H but provide adequate over-range protection for this removal. Reduces power dissipation and improves linearity!</td>
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Layout Issues
Number of Bits/Stage
Cyclic (Algorithmic) ADCs

Cyclic (algorithmic) ADC
Reduces throughput but also area
Cyclic (Algorithmic) ADCs

Pipelined Assembler (Shift Register Array)
End of Lecture 27