Pipelined ADC Design

• Mathematical Model for Ideal Pipelined ADC

• Sources of Errors
Standard Pipelined ADC Architecture

\[ V_{in} \rightarrow \text{S/H} \rightarrow \text{Stage 1} \rightarrow \text{Stage 2} \rightarrow \text{Stage 3} \rightarrow \cdots \rightarrow \text{Stage k} \rightarrow \cdots \rightarrow \text{Stage m-1} \rightarrow \text{Stage m} \rightarrow \text{Pipelined Assembler} \]

\[ V_{ref} \text{ and } \text{CLK} \]

\[ D \rightarrow n \]
Pipelined Converter Stage

Clk \downarrow \quad V_{\text{ref}}

\begin{align*}
V_{\text{ink}} & \rightarrow \text{Stage } k \\
& \quad \downarrow n_k \\
& \quad \rightarrow V_{\text{resk}}
\end{align*}

\begin{align*}
V_{\text{IN}k} & \rightarrow \text{S/H} \\
& \quad \downarrow C_{\text{LK}} \\
& \quad \rightarrow \text{ADC} \\
& \quad \downarrow n_k \\
& \quad \rightarrow D_{\text{OUT}k} \\
& \quad \rightarrow \text{DAC} \\
& \quad \rightarrow \text{AMP} \\
& \quad \rightarrow V_{\text{RESk}} \\
& \quad \rightarrow V_{\text{REF}}
\end{align*}
Pipelined Converter Stage

Generally combined into one switched-capacitor gain stage
Simplified Pipelined Stage

Generally omitted on last stage
Modeling of a Pipelined ADC

• Assume all nonlinearities can be neglected
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

• Paramaterization of Stage k
  • Amplifier
    • Closed-Loop Gain
      • From input – m1k
      • From DAC – m2k
      • From offset – m3k
    • Offset Voltage - V\text{OS}_k
  • DAC
    • V\text{DAC}_k
  • ADC
    • Offset Voltages - V\text{OS}_A_k
    • Out-Range Circuit (if used and not included in ADC/DAC)
      • DAC Levels - V\text{DACB}_k
      • Amplifier Gain – m4k

![Diagram of a pipelined ADC system with an amplifier, DAC, ADC, input voltage \(V_{IN_k}\), output voltage \(V_{RES_k}\), and control signal \(D_{OUT_k}\).]
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

- Parameterization of Input S/H Stage

\[ V_{in1} = m_{10} V_{in} + m_{20} V_{OS0} \]
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

For notational convenience, assume 1 bit/stage

\[ V_{\text{RESk}} = m_{1k} V_{\text{ink}} + d_k V_{\text{DACk}} m_{2k} + m_{3k} V_{\text{OSk}} \]
Mathematical Representation of the n Pipelined Stages

\[ V_{RES1} = m_{11} V_{in1} + d_1 V_{DAC1} m_{21} + m_{31} V_{OS1} \]
\[ V_{RES2} = m_{12} V_{in2} + d_2 V_{DAC2} m_{22} + m_{32} V_{OS2} \]
\[ \cdots \]
\[ V_{RESk} = m_{1k} V_{ink} + d_k V_{DACk} m_{2k} + m_{3k} V_{OSk} \]
\[ \cdots \]
\[ V_{RESn} = m_{1n} V_{inn} + d_n V_{DACn} m_{2n} + m_{3n} V_{OSn} \]
Mathematical Representation of the Pipelined ADC

\[ V_{\text{in}1} = m_{10} V_{\text{in}} + m_{20} V_{OS0} \]

\[ V_{\text{RES}1} = m_{11} V_{\text{in}1} + d_1 V_{DAC1} m_{21} + m_{31} V_{OS1} \]

\[ V_{\text{RES}2} = m_{12} V_{\text{in}2} + d_2 V_{DAC2} m_{22} + m_{32} V_{OS2} \]

\[ \cdots \]

\[ V_{\text{RES}k} = m_{1k} V_{\text{in}k} + d_k V_{DACk} m_{2k} + m_{3k} V_{OSk} \]

\[ \cdots \]

\[ V_{\text{RES}n} = m_{1n} V_{\text{inn}} + d_n V_{DACn} m_{2n} + m_{3n} V_{OSn} \]
Mathematical Representation of the Pseudo-Static Pipelined ADC

\[ V_{in1} = m_{10} V_{in} + m_{20} V_{OS0} \]

\[ V_{RES1} = m_{11} V_{in1} + d_1 V_{DAC1} m_{21} + m_{31} V_{OS1} \]

\[ V_{RES2} = m_{12} V_{in2} + d_2 V_{DAC2} m_{22} + m_{32} V_{OS2} \]

\[ \cdots \]

\[ V_{RESk} = m_{1k} V_{ink} + d_k V_{DACk} m_{2k} + m_{3k} V_{OSk} \]

\[ \cdots \]

\[ V_{RESn} = m_{1n} V_{inn} + d_n V_{DACn} m_{2n} + m_{3n} V_{OSn} \]

\[ V_{RESk} = V_{in(k+1)} \quad \text{for} \quad k = 1 \ldots n-1 \]

2n equations, 2n-1 intermediate nodal voltages and \( V_{in} \)
Solution of the 2n linear equations

\[ V_{in} = \left\{ d_1 \left[ \left( \frac{m_{21}}{m_{11}} \right) V_{DAC1} \right] + d_2 \left[ \left( \frac{m_{22}}{m_{11} m_{12}} \right) V_{DAC2} \right] + \ldots + d_n \left[ \left( \frac{m_{2n}}{m_{11} m_{12} \ldots m_{1n}} \right) V_{DACn} \right] \right\} \]

\[ + \left\{ \frac{m_{31}}{m_{11}} V_{OS1} + \frac{m_{32}}{m_{11} m_{12}} V_{OS2} + \ldots + \left( \frac{m_{3n}}{m_{11} m_{12} \ldots m_{1n}} \right) V_{OSn} \right\} \]

\[ + \left\{ \frac{V_{ RESn}}{m_{11} m_{12} \ldots m_{1n}} \right\} \]
Solution of the 2n Linear Equations

\[ V_{in} = d_1 \left( \frac{m_{21}}{m_{11}} \right) V_{DAC1} + d_2 \left( \frac{m_{22}}{m_{11} m_{12}} \right) V_{DAC2} + \ldots + d_n \left( \frac{m_{2n}}{m_{11} m_{12} \ldots m_{1n}} \right) V_{DACn} + \frac{V_{REF}}{2^{n+1}} \]

Term involving digital output codes

\[ + \left\{ \frac{m_{31}}{m_{11}} V_{OS1} + \frac{m_{32}}{m_{11} m_{12}} V_{OS2} + \ldots + \left( \frac{m_{3n}}{m_{11} m_{12} \ldots m_{1n}} \right) V_{OSn} \right\} \]

Code-independent offset term

\[ + \left\{ \frac{V_{RESn}}{m_{11} m_{12} \ldots m_{1n}} - \frac{V_{REF}}{2^{n+1}} \right\} \]

Code-dependent but can be bounded by \( \frac{1}{2} \) LSB with out-range strategy
Solution of the 2n Linear Equations

\[
V_{in} = \left[ \sum_{k=1}^{n} d_k V_{DACk} \left( \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \right) + \frac{V_{REF}}{2^{n+1}} \right] + \sum_{k=1}^{n} V_{OSk} \frac{m_{3k}}{\prod_{j=1}^{k} m_{1j}} + \left[ \frac{V_{RESn}}{\prod_{k=1}^{n} m_{1k}} - \frac{V_{REF}}{2^{n+1}} \right]
\]

\[
m_{ij} = 2, \ V_{DACk} = V_{REF}/2, \ V_{OSk} = 0
\]

\[
V_{in} = \frac{V_{REF}}{2} \sum_{k=1}^{n} d_k \frac{2^k}{2^{k-1}} + \frac{V_{REF}}{2^{n+1}} + \left( \frac{V_{RESn}}{2^n} - \frac{V_{REF}}{2^{n+1}} \right)
\]
Solution of the 2n Linear Equations

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

\[ \alpha_k = V_{DAC_k} \frac{m_{2k}}{\prod_{j=1}^{m_{1j}}} \]

- \( f(\text{offset}) \) is code-independent, ideally zero, and causes only overall offset error in ADC

- \( f(\text{residue}) \) is code-dependent but can be bounded by 1 lsb (causing at most \( \frac{1}{2} \) LSB error) with out-range protection

- No errors causing spectral distortion or INL degradation if \( \alpha_k \) are correctly determined
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

If more than 1 bit/stage is used and DAC is binarily-weighted structure

\[ V = m_{RESk} V + m_{1k} V_{INK} + m_{2k} \left( \sum_{j=1}^{2^k-1} d_{kj} V_{DACj} \right) + m_{3k} V_{REF} \]
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

If DAC is characterized by

\[ f \left( V_{REF}, \left\langle d_{kj} \right\rangle_{j=1}^{n_k} \right) \]

Then

\[ V = m V_{RESk} + m V_{1k} + m \left( f \left( V_{REF}, \left\langle d_{kj} \right\rangle_{j=1}^{n_k} \right) \right) + m V_{3k} \]
Solution of the 2n Linear Equations

If more than 1 bit/stage is used and DAC is binarily-weighted structure

\[
V_{in} = \left[ \sum_{k=1}^{n} \left( \sum_{j=1}^{h=n_{kj}} d_{kj}^{DAC_{kj}} \right) \left( \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \right) + \frac{V_{REF}}{2^{n+1}} \right] + \sum_{k=1}^{n} V_{OSk} \frac{m_{3k}}{\prod_{j=1}^{k} m_{1j}} + \left[ \frac{V_{REF}}{\prod_{k=1}^{n} m_{1k}} - \frac{V_{REF}}{2^{n+1}} \right]
\]

If DAC is characterized by

\[
f_{\frac{k}{k}} \left( V_{REF}, \langle d_{kj} \rangle_{j=1}^{n_{kj}} \right)
\]

\[
V_{in} = \left[ \sum_{k=1}^{n} \left( f_{\frac{k}{k}} \left( V_{REF}, \langle d_{kj} \rangle_{j=1}^{n_{kj}} \right) \right) \left( \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \right) + \frac{V_{REF}}{2^{n+1}} \right] + \sum_{k=1}^{n} V_{OSk} \frac{m_{3k}}{\prod_{j=1}^{k} m_{1j}} + \left[ \frac{V_{REF}}{\prod_{k=1}^{n} m_{1k}} - \frac{V_{REF}}{2^{n+1}} \right]
\]

No errors causing spectral distortion or INL degradation if terms involving \(d_{kj}\) are correctly determined
Pseudo-Static Characterization of Pipelined ADC with Arbitrary Bits/Stage and Out-Range Protection

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

- \( d_k \) are boolean output variables from stage ADCs (including out-range protection if included)
- the \( \alpha_k \) are functions of DAC levels and amplifier gains
- \( f(\text{offset}) \) is code-independent, ideally zero and causes only overall offset error in ADC
- \( f(\text{residue}) \) is code-dependent but can be bounded by 1 lsb (causing at most \( \frac{1}{2} \) LSB error) with out-range protection
- Equation applies to both sub-radix2 and extra comparator out-range protection
- No errors causing spectral distortion or INL degradation if \( \alpha_k \) are correctly determined
Observations

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

form of \( \alpha_k : V_{DACk} \frac{m_{2k}}{\prod_{j=1}^{m} m_{1j}} \)

- Substantial errors are introduced if \( \alpha_k \) are not correctly interpreted!
- Some calibration and design strategies focus on accurately setting gains and DAC levels
- Analog calibration can be accomplished with either DAC level or gain calibration
- Digital calibration based upon coefficient identification does not require accurate gains or precise DAC levels
Observations (cont)

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

form of \( \alpha_k : V_{DAC_k} \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \)

- If nonlinearities are avoided, data conversion process with a pipelined architecture is extremely accurate
- Major challenge at low frequencies is accurately interpreting the digital output codes
Observations (cont)

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

form of \( \alpha_k : V_{DAC_k} \frac{m_{2k}}{\prod_{j=1}^{m_{1j}}} \)

- If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable!