Pipelined ADC Design
Part 5

• Sources of Errors

• Robust Performance of Pipelined ADCs
Review

Standard Pipelined ADC Architecture

\[ C_{LK} \]

\[ X_{IN} \rightarrow \text{S/H} \rightarrow \text{Stage 1} \rightarrow r_1 \rightarrow \text{Stage 2} \rightarrow r_2 \rightarrow \ldots \rightarrow \text{Stage k} \rightarrow r_k \rightarrow \ldots \rightarrow \text{Stage m} \rightarrow r_m \rightarrow n \rightarrow X_{OUT} \]

Pipelined Assembler
(Shift Register Array)

\[ X_{INK} \rightarrow \text{ADC}_k \rightarrow \text{DACK} \rightarrow \text{Amp} \rightarrow X_{OUTK} \]

\[ C_{LK} \]

\[ d_k \rightarrow V_{REF} \]
Review

Pseudo-Static Characterization of Pipelined ADC with Arbitrary Bits/Stage and Out-Range Protection

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

• \(d_k\) are boolean output variables from stage ADCs (including out-range protection if included)
• The \(\alpha_k\) are functions of DAC levels and amplifier gains
• \(f(\text{offset})\) is code-independent, ideally zero and causes only overall offset error in ADC
• \(f(\text{residue})\) is code-dependent but can be bounded by 1 lsb (causing at most \(\frac{1}{2}\) LSB error) with out-range protection
• Equation applies to both sub-radix2 and extra comparator out-range protection
• No errors causing spectral distortion or INL degradation if \(\alpha_k\) are correctly determined and last residue is variability bounded
• Substantial errors are introduced if \(a_k\) are not correctly interpreted or \(f(\text{residue})\) is not bounded!
Observations (cont)

\[ V_{in} = \sum_{k=1}^{n} \alpha d_k + f(\text{offset}) + f(\text{residue}) + \varepsilon \ (\text{nonlinear}) \]

- If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable!

Two major types of nonlinearities

1. Saturating nonlinearities (cause information loss in residue path)
2. Continuous nonlinearities

- Most successful designers have methods for addressing the first type
- Few know how to address the second type but fortunately these can be relatively small in many good designs (but not small enough to practically meet high-end performance requirements)
Amplifier Types used In Pipelined ADCs

- Two-stage
- Cascode
  - Telescopic
  - Folded
- Regulated Cascode (Gain-boosted Cascode)
  - Telescopic
  - Folded
- Regenerative Feedback Gain Enhancement
- Two-State Cascode
Amplifier Nonlinearity Becoming Increasingly Significant as $V_{DD}$ Reduced

Comparison of amplifiers at same power level and same $V_{EB}$

- Nonlinearity strongly architecture dependent
- Trade-Offs between Gain and Signal Swing

Drop in gain seriously degrades linearity and spectral performance
How Much Gain?

Conventional Approach: Assume want to make at most \( \frac{1}{2} \) LSB error in closed loop gain

Often see authors use

\[
A_{\text{dB}} \approx 6n_{ST} + 12
\]

- Gives no information about drop in gain at boundary of input/output window
- Maybe uses too much error budget on gain
- No indication how \( A_{\text{dB}} \) relates to INL or DNL
- Gain requirements are large on the input buffer (\( n_{ST} = n \)) but will be significantly relaxed on latter stages in the pipeline when \( n_{ST} \) decreases
Settling Time

Conventional Approach: Assume want to make at most $\frac{1}{2}$ LSB error in settling for worst-case step

Step response (if slewing is neglected)

Design requirements for GB of Op Amp apply to both compensated two-stage structures and high output impedance single-stage structures

$$t_s \approx \frac{0.7(n_{ST} + 1)}{\beta GB}$$

$$t_{s_{AMP}} = t_{CLK} \approx \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

$$GB_{RPS} \approx \frac{1.4(n_{ST} + 1)}{\beta f_{CLK}}$$

$$GB_{HZ} \approx \frac{0.22(n_{ST} + 1)}{\beta f_{CLK}}$$

Notes: May be over-using error budget
Slewling will modestly slow response
Dominant source of power dissipation is in the op amps in S/H and individual stages
Which op amp architectures are most energy efficient?

- Depends upon $\beta$
- For smaller $\beta$, two-stage are more energy efficient for larger $\beta$
- Single-stage are better
- Must optimize power in any given architecture
- Folding reduces efficiency (typically by 30% to 50%)

## Pipelined Data Converter Design Guidelines

### Issue

1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate

2. Correct interpretation of $\alpha_k$'s is critical

3. Op Amp Gain causes finite gain errors and introduces nonlinearity

4. Op amp settling must can cause errors

5. Power dissipation strongly dependent upon GB of Op Amps

### Strategy

1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if $\alpha_k$'s correctly interpreted  
   a) Use Extra Comparators  
   b) Use sub-radix structures

2. a) Accurately set $\alpha_k$ values  
   b) Use analog or digital calibration

3. a) Select op amp architecture that has acceptable signal swing  
   b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors

4. Select GB to meet settling requirements  
   (degrade modestly to account for slewing)

5. Minimize $C_L$, use energy efficient op amps, share or shut down op amp when not used, scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies
Performance Limitations
(consider amplifier, ADC and DAC issues)

• ADC
  – Break Points (offsets)
• DAC
  – DAC Levels (offsets)
    • Out-range (over or under range)
• Amplifier
  – Offset voltages
• Settling Time
  – Nonlinearity (primarily open loop)
    • Open-loop
    • Out-range
  – Gain Errors
    • Component mismatch
    • Inadequate open loop gain

Power Dissipation
  – kT/C switching noise
Power Efficiency and Settling Time Enhancement

Minimization of Power in Operational Amplifiers

- Reduce Power in Less Significant Stages
- Share Operational Amplifiers Between Stages
- Interleave Amplifiers Between Parallel Paths
- Power-Down Operational Amplifiers When Not Used
- Dynamically Bias Operational Amplifiers
- Use Operational Amplifier Architectures that are More Energy Efficient
Energy-Efficient Operational Amplifier Architectures?

- Settling Time Inversely Proportional to GB of an OP AMP (during linear settling)
- How does the energy efficiency of GB for various op amps compare?
Power Dissipation

\[ GB = \frac{g_m}{C_L} \]

For MOS implementation

\[ P = \begin{bmatrix} V_{SUP} \cdot GB \cdot C_L \end{bmatrix} \begin{bmatrix} V_{EB} \end{bmatrix} \]

Fixed by ADC requirements

Select architectures that minimize architecture-dependent term

\[ GB = \begin{bmatrix} \frac{P}{V_{SUP}} \cdot \frac{1}{C_{L}} \end{bmatrix} \begin{bmatrix} \frac{1}{V_{EB}} \end{bmatrix} \]

Architecture Dependent
Figure of Merit for Comparing Energy Efficiency of Op Amps

\[ GB = \begin{bmatrix} \frac{2 \cdot P}{V_{C_{L}}} \\ \frac{1}{V_{EB}} \end{bmatrix} \]

Architecture Independent

Architecture Dependent

\[ \text{FOM} = \frac{GB \cdot V_{SUP}}{2P} \]

"Generic MOS Cascode-Type OpAmp"

\[ \text{FOM} = \begin{bmatrix} \frac{1}{V_{EB1}} \end{bmatrix} \]
Consider the Basic Single-State Op Amp

C\textsubscript{L} on Differential Outputs Not Shown

CMFB Not Shown
Consider the Basic Single-State Op Amp

Differential Half-Circuit

\[ V_{IN} = \frac{V_{IN}^+ - V_{IN}^-}{2} = \frac{V_{DIFF}}{2} \]

\[ A(s) = \frac{-g_m/2}{sC_L + [g_{o2} + g_{o1}]} \]

\[ A_O = \frac{g_m/2}{g_{o1} + g_{o2}} \]

\[ BW = \frac{g_{o1} + g_{o2}}{C_L} \]

\[ GB = \frac{g_m}{2C_L} = \frac{2I_Q}{2V_{EB}C_L} = \left[ \frac{P}{2V_{DD}C_L} \right] \left[ \frac{1}{V_{EB}} \right] \]
Basic Single-Stage Diff Amp

\[ FOM = \frac{1}{V_{EB1}} \]

- \( C_L \) on other output Not Shown
- CMFB Not Shown
Consider the Basic Single-State Op Amp

Differential Half-Circuit

\[
\begin{align*}
\text{GB} &= \frac{P}{2V_{DD}C_L} \left[ \frac{1}{V_{EB}} \right] \\
\end{align*}
\]

Observations

- GB (settling time) improves linearly with P
- GB (settling time) improves with decreasing \( V_{EB} \)
Consider the Basic Single-State Op Amp

Differential Half-Circuit

V_{DD} \quad V_{b1} \quad V_{OUT} \quad C_L \quad V_{IN} \quad Q1 \quad Q2

\[
GB = \begin{bmatrix}
P \\
2V_{DD}C_L \\
V_{EB}
\end{bmatrix}
\]

Observations

- GB (settling time) improves linearly with P
  Is there any fundamental limit?

- GB (settling time) improves with decreasing $V_{EB}$
  Conflict with conventional wisdom that speed ($f_T$) increases with $V_{EB}$?

- What assumptions implicit to draw these conclusions?
  $C_L$ dominates parasitic capacitances
Energy Efficiency of Popular Op Amps

Assume parasitic capacitances on output negligible compared to external load capacitance
Energy Efficiency of Popular Single-Stage Op Amps

- Basic Single-Stage Diff Amp
- Current Mirror Op Amp
- Telescopic Cascode
- Folded Cascode
- Gain-Boosted Telescopic Cascode
- Gain-Boosted Folded Cascode
- $-gm$ Compensated Single-Stage
- Telescopic Cascode Positive Feedback
Basic Single-Stage Diff Amp

\[ \text{CMFB Not Shown} \]

\[ \text{CL on other output Not Shown} \]

\[ \text{FOM} = \left[ \frac{1}{V_{EB1}} \right] \]
Current Mirror Op Amp

\[
\text{FOM} = \begin{bmatrix} \frac{M}{M+1} \\ \frac{1}{V_{EB1}} \end{bmatrix}
\]
Telescopic Cascode

\[ \text{FOM} = \left[ \frac{1}{V_{EB1}} \right] \]
Folded Cascode

\[ I_{D3Q} = \theta I_{D1Q} \]

\[ \text{FOM} = \left[ \frac{1}{1 + \theta} \right] \left[ \frac{1}{V_{EB1}} \right] \]
Gain-Boosted Telescopic Cascode

\[
P_{Ai\text{Total}} = \theta P_{\text{Telescopic Cascode}}
\]

\[
\text{FOM} = \left[ \frac{1}{1+\theta} \right] \left[ \frac{1}{V_{EB1}} \right]
\]
Gain-Boosted Folded Cascode

\[ P_{Ai\text{Total}} = \theta_1 P \text{ Folded Cascode} \]

\[ \text{FOM} = \left[ \frac{1}{1+\theta_1} \right] \left[ \frac{1}{1+\theta_2} \right] \left[ \frac{1}{V_{EB}\theta_3} \right] \]
-gm Compensated Single-Stage

\[
\text{FOM} = \left[\frac{1}{V_{EB1}}\right]
\]
Telescopic Cascode Positive Feedback Op Amp

\[ A_v \approx \frac{-g_{m1} \cdot g_{m2} \cdot g_{m3}}{g_{o1} \left( g_{o2} \cdot g_{m3} - g_{o3} \cdot g_{m2} \right)} \]

\[ \text{FOM} = \left[ \frac{1}{V_{EB1}} \right] \]
Energy Efficiency of Popular Op Amps

• All of the Op Amps in the comparison have an energy efficiency for a given settling requirement that is, at best, as good as that of the basic simple structure if the parasitics are small compared to $C_L$

• The settling of most of the amplifiers decreases linearly with $P$

• The linear settling time is minimized if $V_{EB1}$ is minimized!
Settling Energy Efficiency of Popular Op Amps

Questions:

• Are there any structures that are more settling energy efficient than than of the basic amplifier?

• Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

• Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?
Settling Energy Efficiency of Popular Op Amps

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- Are there any structures that are more settling energy efficient than than of the basic amplifier?

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Improved Energy Efficiency Op Amps

\[
\text{FOM} = \left[ \frac{1}{V_{EB1}} \right] + \left[ \frac{1}{V_{EB3}} \right]
\]
Improved Energy Efficiency Op Amps

Another was presented at ISCAS 2001 - Amourah
Settling Energy Efficiency of Popular Op Amps

Questions:

• Are there any structures that are more settling energy efficient than the basic amplifier?

• Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

• Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?
Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

Layout of simple MOS Transistor

Assumption: $W \gg d_1$

for TSMC 0.25u

$C_{Xn} = .83$

$C_{Xp} = .90$

Define $C_X$ by

$$C_X = \frac{(C_{SW} + C_{BOT} \cdot d_1)}{L_{MIN} \cdot C_{OX}}$$

$$\omega_T = 2\pi f_T = \frac{\mu V_{EB}}{L_{MIN}^2}$$

Where:

- $C_{SW}$ is the sidewall capacitance density
- $C_{BOT}$ is the bottom diffusion capacitance density
- $L_{MIN}$ is the minimum gate length
- $d_1$ is the minimum spacing from poly to diffusion

Note: $C_X$ is a dimensionless process parameter
Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

Differential Half-Circuit for Basic Op Amp

\[
\begin{align*}
\text{DOF} &= \{V_{EB1}, V_{EB3}, P\} \\
\text{GB} &= \frac{P}{2V_{DD} V_{EB1} C_L + P \left(2L_{\text{MIN}}^2\right) \left[ \frac{C_{Xn}}{\mu_n V_{EB1}} + \frac{C_{Xp}}{\mu_p \left(\frac{V_{EB1}}{V_{EB3}}\right)} \right]} \\
\text{GB} &= \frac{P}{2V_{DD} V_{EB1} C_L + 2P \left[ \frac{C_{Xn}}{\omega_{Tn}} + \frac{C_{Xp}}{\omega_{Tp}} \left(\frac{V_{EB1}}{V_{EB3}}\right) \right]}
\end{align*}
\]
Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

**Differential Half-Circuit for Basic Op Amp**

\[ \text{DOF} = \{ V_{EB1}, V_{EB3}, P \} \]

\[ GB = \frac{P}{2V_{DD}V_{EB1}C_L + 2P \left[ \frac{C_{Xn}}{\omega_{Tn}} + \frac{C_{Xp}}{\omega_{Tp}} \left( \frac{V_{EB1}}{V_{EB3}} \right) \right]} \]

\[ \text{FOM} = \frac{1}{V_{EB1} + \frac{P}{V_{DD}C_L} \left[ \frac{C_{Xn}}{\omega_{Tn}} + \frac{C_{Xp}}{\omega_{Tp}} \left( \frac{V_{EB1}}{V_{EB3}} \right) \right]} \]
Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

\[
GB = \frac{P}{2V_{DD} V_{EB1} C_L + 2P\left[\frac{C_{Xn}}{\omega_{Tn}} + \frac{C_{Xp}}{\omega_{Tp}} \left(\frac{V_{EB1}}{V_{EB3}}\right)\right]}
\]

\[
GB_{MAX} = \frac{\omega_{Tn}}{2\left[C_{Xn} + C_{Xp} \left(\frac{\omega_{Tn}}{\omega_{Tp}}\right)^2 \frac{\mu_p}{\mu_n}\right]} = \frac{\omega_{Tn}}{2\left[C_{Xn} + C_{Xp} \left(\frac{V_{EB1}}{V_{EB3}}\right)^2 \frac{\mu_n}{\mu_p}\right]}
\]
Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

No – reach a point of diminishing returns as power is increased

What is a practical point of diminishing returns?

\[
GB_{\text{crit}} = \frac{GB_{\text{max}}}{2} = \frac{\omega}{2} \left[ 4C_{Xn} + C_{xp} \left( \frac{V_{EB1}}{V_{EB3}} \right)^2 \frac{\mu_n}{\mu_p} \right]^{-1}
\]
Settling Energy Efficiency of Popular Op Amps

Questions:

• Are there any structures that are more settling energy efficient than the basic amplifier?

• Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

• Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?
Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?

Recall:

$$\omega_T = \frac{\mu V_{EB}}{L_{MIN}^2}$$

Implication:

Speed increases with $V_{EB}$
Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?

$$GB = \frac{P}{2V_{DD}V_{EB1}C_L + P(2L_{MIN}^2)\left[\frac{C_{Xn}}{\mu_n V_{EB1}} + \frac{C_{xp}}{\mu_p \left(\frac{V_{EB1}}{V_{EB3}^2}\right)}\right]}$$

$$DOF = \{V_{EB1}, V_{EB3}, P\}$$

To maximize GB, want to make $V_{EB3}$ as large as possible without causing signal swing problems.
Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?

No – but an optimal value of $V_{EB1}$ can be obtained

$$V_{EB1, \text{MAX}} = \sqrt{\frac{P(C_{x_n} L_{\text{MIN}}^2)}{\mu_n V_{DD} C_L + P \left( \frac{C_{x_p} L_{\text{MIN}}^2}{V_{EB3}^2} \right) \frac{\mu_n}{\mu_p}}}$$
Is the strategy of minimizing $V_{EB1}$ to minimize settling time justifiable even if parasitics are considered?

For large $P$, obtain

$$V_{EB1,\text{MAX}} = V_{EB3} \sqrt[2]{\frac{C_{Xn}}{C_{Xp}}} \frac{\mu_p}{\mu_n}$$

$$GB_{\text{MAX}} = \frac{\mu_n V_{EB3}}{4L_{\text{MIN}}^2 \sqrt{C_{Xn}C_{Xp}}} \sqrt[2]{\frac{\mu_p}{\mu_n}} = \frac{\omega_{Tp}}{4 \sqrt{C_{Xn}C_{Xp}}} \sqrt[2]{\frac{\mu_p}{\mu_n}}$$
Settling Energy Efficiency of Popular Single-Stage Op Amps

- Other single-stage op amps have settling performance properties similar to those considered here
- Increasing power improves settling time but a point of diminishing returns will limit the benefits
- Maintain large $V_{EB3}$ to minimize effects of parasitics associated with p-channel transistor
- Set $V_{EB1}$ at critical point to maximize GB for a given power dissipation
Energy Efficiency of Popular Single-Stage Op Amps

- Basic Single-Stage Diff Amp
- Current Mirror Op Amp
- Telescopic Cascode
- Folded Cascode
- Gain-Boosted Telescopic Cascode
- Gain-Boosted Folded Cascode
- \(-gm\) Compensated Single-Stage
- Telescopic Cascode Positive Feedback

What about the 2-stage structures?
Energy Efficiency of Popular Two-Stage Op Amps

- Basic Two-Stage
- Cascode-Cascade
- Cascode-Cascode
- Telescopic Positive Feedback Cascode-Cascade
- -gm gain enhancement

What about the 2-stage structures?
Two-Stage

Single-Ended Output
Two-Stage

Fully Differential
Two-Stage

Fully Differential
Two-Stage Cascode/Cascade

[Park – ISSCC 2001]
Telescopic Cascode Two-Stage Positive Feedback Op Amp

\[
A_v \approx \left[ \frac{-g_{m1} \cdot g_{m2} \cdot g_{m3}}{g_{o1} \left( g_{o2} \cdot g_{m3} - g_{o3} \cdot g_{m2} \right)} \right] \cdot \left[ \frac{g_{m7}}{g_{o7} + g_{o8}} \right]
\]

CMFB Not Shown
Two-Stage Negative R Compensation
Enhanced-Gain Two-Stage Negative R Compensation

Diagram showing the circuit with transistors Q1-Q10, resistors, capacitors, and voltage sources.
Performance Limitations  
(consider amplifier, ADC and DAC issues )

- **ADC**
  - Break Points (offsets)
- **DAC**
  - DAC Levels (offsets)
    - Out-range (over or under range)
- **Amplifier**
  - Offset voltages
- **Settling Time**
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Component mismatch
    - Inadequate open loop gain

Power Dissipation
- kT/C switching noise
I/O Power Dissipation

• Driving the output pads can consume considerable power

For a single bit line

\[ P = f_{CL} V^2 C_L \]

For an n-bit ADC

\[ P = n \cdot f_{CL} V^2 C_L \]

Example: if \( n=14 \), \( V_{SUP}=3.3V \), \( C_L=5pF \), \( f_{CL}=100MHz \), 50% change

\[ P = 14 \cdot 10^8 \cdot 3.3^2 \cdot 5E-12 = 70mW \]
I/O Power Dissipation

• Driving the output pads can consume considerable power

For a single bit line

\[ P = f_{CL} V_{SUP}^2 C_L \]

\[ P \approx 2 f_{CL} V_{SUP}^2 C_L \]

For an n-bit ADC

\[ P = n \cdot f_{CL} V_{SUP}^2 C_L \]

\[ P \approx 2n \cdot f_{CL} V_{SUP}^2 C_L \]

Example: if \( n=14, V_{SUP}=3.3V, C_L=5pF, f_{CL}=100MHz, 50\% \) change

\[ P = 70mW \]

\[ P \approx 140mW \]
Interstage Amplifiers

Typical Finite-Gain Inter-stage Amplifier
(shown single-ended with 1-bit/stage)

Ideally

\[ V_{OUT} = V_{IN} \left(1 + \frac{C_1}{C_2}\right) - d_1 \left(\frac{C_1}{C_2}\right)V_{REF} \]

\[ V_{OUT} = 2V_{IN} - dV_{REF} \]

Gain = 2.00000