Pipelined ADC Design
Part 7

• Sources of Errors
  – Sampling Noise
  – Aperature Uncertainty

• Robust Performance of Pipelined ADCs
  – Fully Differential Operation

• Cyclic ADCs
Review

Standard Pipelined ADC Architecture

\[ C_{LK} \]

\[ X_{IN} \rightarrow S/H \rightarrow \text{Stage 1} \rightarrow r_1 \rightarrow \text{Stage 2} \rightarrow r_2 \rightarrow \cdots \rightarrow \text{Stage } k \rightarrow r_k \rightarrow \cdots \rightarrow \text{Stage } m \rightarrow r_m \rightarrow X_{OUT} \]

Pipelined Assembler
(Shift Register Array)
Pseudo-Static Characterization of Pipelined ADC with Arbitrary Bits/Stage and Out-Range Protection

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

- \( d_k \) are boolean output variables from stage ADCs (including out-range protection if included)
- The \( \alpha_k \) are functions of DAC levels and amplifier gains
- \( f(\text{offset}) \) is code-independent, ideally zero and causes only overall offset error in ADC
- \( f(\text{residue}) \) is code-dependent but can be bounded by 1 lsb (causing at most \( \frac{1}{2} \) LSB error) with out-range protection
- Equation applies to both sub-radix2 and extra comparator out-range protection
- No errors causing spectral distortion or INL degradation if \( \alpha_k \) are correctly determined and last residue is variability bounded
- Substantial errors are introduced if \( a_k \) are not correctly interpreted or \( f(\text{residue}) \) is not bounded!
Observations (cont)

\[ V_{in} = \sum_{k=1}^{n} \alpha d_k + f(\text{offset}) + f(\text{residue}) + \varepsilon (\text{nonlinear}) \]

- If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable!

Two major types of nonlinearities

1. Saturating nonlinearities (cause information loss in residue path)
2. Continuous nonlinearities

- Most successful designers have methods for addressing the first type
- Few know how to address the second type but fortunately these can be relatively small in many good designs (but not small enough to practically meet high-end performance requirements)
Sampling Noise

• Capacitors introduce no noise

• Noise is, however, present in switches that take samples

• This switch noise causes SNR problems in the amplifier if not correctly managed
Theorem 4  If $V(t)$ is a continuous-time zero-mean noise source and $<V(kT)>$ is a sampled version of $V(t)$ sampled at times $T$, $2T$, ..., then the standard deviation of the random variable $V(kT)$, denoted as $\sigma_\hat{V}$ satisfies the expression

$$\sigma_\hat{V} = V_{RMS} = \hat{V}_{RMS}$$

Theorem 5  The RMS value and the standard deviation of the noise voltage that occurs in the basic switched-capacitor sampler is related to the capacitor value by the expression

$$\hat{V}_{RMS} = V_{RMS} = \sigma_\hat{V} = \sqrt{\frac{kT}{C}}$$
Sampling Noise

Key Result, Continuous-time noise at $V_{OUT}$

$$V_{rms} = \sqrt{\frac{kT}{C}}$$

Key Result, Discrete-time noise at $V_{OUT}$

$$\hat{V}_{rms} = \sqrt{\frac{kT}{C}}$$

Review
Sampling Noise

"kT/C" Noise at T=300K

Example: $\frac{1}{2}$ LSB for $V_{\text{REF}}$ in a 16-bit ADC is 7.63uV
Sampling Noise

Capacitance vs Resolution (1/2 LSB level)

Example: 14-bit ADC  C=4.6pF
Sampling Noise

If the ON impedance of the switches is small, it can be shown that
\[ \hat{V}_{\text{IN-RMS}} = \sqrt{\frac{kT}{2C} + \frac{kTR_G B}{4}} \]

If size switches so that
\[ R_{\text{sw}} = \frac{1}{Cf_{\text{CLK}} 2 \ln(2) (n_{\text{ST}} + 1)} \]
\[ \hat{V}_{\text{IN-RMS}} \cong \sqrt{\frac{kT}{2C}} \]

\[ \beta = \frac{C_2}{C_1 + C_2} \]
Sampling Noise

If the ON impedance of the switches is small and it is assumed that $C_1 = C_2 = C$, it can be shown that

$$V_{\text{IN-RMS}} = \sqrt{\frac{kT}{2C} + \frac{kT R}{4 \beta}}$$

Too much GB or too large of $R_{\text{SW}}$ can increase sampled noise voltage

Too small of $R_{\text{SW}}$ will not derive any benefit and will increase power, area, and driving problems
Sampling Noise

How should switches be sized?

Consider any first-order RC network

To settle to \( \frac{1}{2} \) LSB in time \( T_{CLK}/2 \)

\[
R_{SW} = \frac{1}{C_H f_{CLK} 2 \ln(2)(n_{ST} + 1)}
\]

12
Sampling Noise

How should switches be sized?

To settle to \( \frac{1}{2} \) LSB in time \( T_{\text{CLK}}/2 \)

\[
R_{\text{sw}} = \frac{1}{C f_{\text{CLK}} 2 \ln(2)(n_{\text{st}} + 1)}
\]

Recall minimum GB requirement (which is usually what will be designed for)

\[
\text{GB} = \frac{(n_{\text{st}} + 1) 2 \ln 2}{f_{\text{CLK}}} \beta
\]

Eliminating \( f_{\text{CLK}} \) we obtain

\[
R_{\text{sw}} C_h = \frac{1}{\beta \text{GB}}
\]

Define excess switch sizing factor \( \theta \) by

\[
R_{\text{sw}} = \frac{\theta}{C_h \beta \text{GB}}
\]
Sampling Noise

Summary of Flip-around SC gain stage

\[ \beta_2 = \frac{C_2}{C_1 + C_2} \]

\[ A_{FB} = 1 + \frac{C_1}{C_2} \]

\[ \hat{V}_{IN-RMS} = \sqrt{\frac{kT}{C_1 + C_2} + \left( \frac{C_2}{C_1 + C_2} \right)^2 \hat{V}_{^4-5RMS}^2} \]

\[ R_4 = \frac{\theta}{C_1 \beta GB} \]

\[ \hat{V}_{4-5RMS} = \sqrt{2kT \frac{\theta}{C_1 \pi} \left( 1 + \frac{\beta}{1 - \beta} \right)^2} \sqrt{\int_0^{\infty} \left( \frac{1 + \theta^2 \omega^2}{\omega^2(2\beta^2) + \omega^2 \left( \frac{\theta + \beta}{1 - \beta} - 4\theta^2 \beta^2 + \left( \frac{\beta}{1 - \beta} \right) \right)} \right) d\omega} \]

Often \( \theta \ll 1 \) even with minimum sized devices and in this case \( V_{4-5RMS} \) is negligible

\[ \hat{V}_{IN-RMS} = \sqrt{\frac{kT}{C_1 + C_2}} \]
Sampling Noise

Two popular SC gain stages
Sampling Noise

Basic SC gain stage

\[ A_{FB} = -\frac{C_1}{C_2} \]

\[ \beta = \frac{C_2}{C_1 + C_2} \]
Sampling Noise

Basic SC gain stage

It can be shown that

\[
V_{\text{OUT}} = \frac{C_1}{C_2} \left( V_{\text{IN}} + dV_{\text{REF}} + V_{n1} \right) + \frac{V}{n4} \frac{C_1}{C_2} \left( \frac{1}{1 + R_4 C_s + \frac{s}{GB} \left( 1 + \frac{C_1}{C_2} + R_4 C_s \right)} \right)
\]
Sampling Noise

Basic SC gain stage

\[ \beta = \frac{C_2}{C_1 + C_2} \]

\[ R = \frac{\theta}{C_1 \beta GB} \]

\[ V_{\text{OUT}} = \frac{C_1}{C_2} \left( V_{\text{IN}} + dV_{\text{REF}} + \frac{V}{n} \right) + V_n \frac{C_1}{C_2} \left( \frac{1}{1 + R^4 C_s + \frac{s}{GB} \left( 1 + \frac{C_1}{C_2} + R^4 C_s \right)} \right) \]

\[ \hat{V}_{\text{OUT RMS}} = \sqrt{\frac{2kT\theta \left( 1 - \beta \right)}{C_1 \pi \beta}} \left[ \int_{0}^{\infty} \frac{1}{1 + \omega^2 \left[ (1+\theta)^2 - 2\theta \beta \right] + \omega^4 (\theta \beta)^2} d\omega \right]^{1/2} \]

\[ \hat{V}_{\text{IN RMS}} = \sqrt{\frac{kT}{C_1} + \left( \frac{C_2}{C_1} \right)^2 \hat{V}_{\text{OUT RMS}}^2} \]

\[ \hat{V}_{\text{IN RMS}} = \sqrt{\frac{kT}{C_1}} \]

\[ \theta << 1 \]
Sampling Noise

Two popular SC gain stages

\[ A_{FB} = 1 + \frac{C_1}{C_2} \]

\[ \beta = \frac{C_2}{C_1 + C_2} \]

\[ \hat{V}_{IN-RMS} = \sqrt{\frac{kT}{C_1 + C_2}} \hat{V}^2 \]

\[ \hat{V}_{OUT-RMS} = \sqrt{\frac{kT}{C_1}} \hat{V}^2 \]

\[ \hat{V}_{IN-RMS} = \sqrt{\frac{kT}{\theta C_1}} \hat{V}^2 \]

\[ \hat{V}_{OUT-RMS} = \sqrt{\frac{kT}{\theta C_1}} \hat{V}^2 \]

\[ \theta \ll 1 \]

\[ \theta \ll 1 \]
Sampling Noise

When is the continuous-time SC noise really of concern?

Recall

\[ GB = \frac{(n_{ST} + 1) 2 \ln 2}{\beta f_{CLK}} \]

\[ \sqrt{\frac{kT}{C}} = \frac{1V}{2^{n+1}} \]

\[ R_4 = \frac{1}{C_i \beta GB} \]

Eliminating GB and C

\[ R_4 = \frac{1}{kT 2^{n_{ST} + 2} (n_{ST} + 1) 2 \ln 2 f_{CLK}} \]
## Sampling Noise

When is the continuous-time SC noise really of concern?

\[
R_{\text{MAX}} = \frac{1}{kT2^{2n} + 1)2\ln2f_{\text{CLK}}}
\]

\(R_{\text{MAX}}(f_{\text{CLK}},n)\)

| Resolution | 10  | 100 | 1K  | 10K | 100K | 1M  | 10M | 100M | 1G
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Sampling Noise

What about this one?

Series-Parallel Structure

\[ A_{FB} = ? \]

\[ \beta = ? \]
Sampling noise from all stages must be referred back to input!

\[
V_{\text{IN RMS}} = V_{\text{IN1}}^2 + \frac{1}{A_1^2} V_{\text{IN2}}^2 + \frac{1}{A_1^2 A_2^2} V_{\text{IN3}}^2 + \cdots + \frac{1}{A_1^2 A_2^2 \cdots A_{n-1}^2} V_{\text{INn}}^2
\]

\[
V_{\text{IN RMS}} = \sqrt{V_{\text{IN1}}^2 + \sum_{k=2}^{n} \left( \frac{V_{\text{INk}}}{\prod_{i=1}^{k-1} A_i} \right)^2}
\]

See Katyal, Lin and Geiger, ISCAS, for capacitor sizing for minimization of noise and power.
Sampling Timing

Even numbered stages sampled with $\phi_1$ and odd stages sampled with $\phi_2$
Sampling Timing

Quiet sampling is important
Bootstrapped Switch

The ideal sampling operation

Should track $V_{IN}$ in the TRACK mode
Should accurately sample $V_{IN}$ at transition to HOLD mode
Bootstrapped Switch

The ideal sampling operation

Should track $V_{IN}$ in the TRACK mode
Should accurately sample $V_{IN}$ at transition to HOLD mode
Bootstrapped Switch

The ideal sampling operation

\[ \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{1 + R_{\text{SW2}} C_{\text{S}}}{1 + (R_{\text{S}} + R_{\text{SW1}} + R_{\text{SW2}})} \]

If linear

For high frequency inputs, an attenuation error will occur

Affects absolute accuracy but not linearity

But, if switches are nonlinear, will introduce a nonlinear error that can be very substantial

Signal dependent \( R_{\text{SW}} \) or switch nonlinearity will introduce nonlinear errors
Bootstrapped Switch

Bootstrapping Principle

\[ V_{DD} \]

\[ C_x \]

\[ \varphi_1 \]

\[ \overline{\varphi}_1 \]

\[ \varphi_1 \]

\[ \overline{\varphi}_1 \]
Bootstrapped Switch

Bootstrapping Principle

Conceptual Realization

- May have difficult time turning on some switches
- May stress gate oxide!
Bootstrapped Switch

Bootstrapping Principle

From Galton, ISSCC 04
Bootstrapped Switch

Bootstrapping Principle

From Abo and Gray JSC 99
Bootstrapped Switch

Bootstrapping Principle

From Roberts MWSCAS 2000
Bootstrapped Switch

Bootstrapping Principle

Fig. 7. Transistor-level implementation of the bootstrapped switch.

From Kaiser JSC 2001
Bootstrapped Switch

Figure 5: Bootstrapped switch.

From Steensgaard  ISCAS 1999
# Pipelined Data Converter Design Guidelines

## Issue

1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate

2. Correct interpretation of $\alpha_k$'s is critical

3. Op Amp Gain causes finite gain errors and introduces nonlinearity

4. Op amp settling must can cause errors

5. Power dissipation strongly dependent upon GB of Op Amps

6. Choice of FB Amplifier Architecture seriously impacts performance

## Strategy

1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if $\alpha_k$'s correctly interpreted

   a) Use Extra Comparators

   b) Use sub-radix structures

2. a) Accurately set $\alpha_k$ values

   b) Use analog or digital calibration

3. a) Select op amp architecture that has acceptable signal swing

   b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors

4. Select GB to meet settling requirements

   (degrade modestly to account for slewing)

5. Minimize $C_L$, use energy efficient op amps, share or shut down op amp when not used, scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies

6. Bottom plate sampling, bootstrapping, clock advance to reduce aperture uncertainty, critical GB, parasitic insensitivity needed, $\beta$ dependent upon architecture and phase, compensation for worst-case $\beta$, TG if needed
## Issue

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<table>
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<tr>
<td>7.</td>
<td>Sampling operation inherently introduces a sampled-noise due to noise in resistors</td>
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<tr>
<td>8.</td>
<td>Signal-dependent tracking errors at input introduce linearity degradation</td>
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## Strategy

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<tr>
<td>7.</td>
<td>Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage).</td>
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<tr>
<td>8.</td>
<td>Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches</td>
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Aperture Uncertainty

\[ V_{in} = \frac{V_{REF}}{2} (1 + \sin \omega t) \]

\[ \frac{\partial V_{in}}{\partial t} = \frac{V_{REF}}{2} \omega \cos \omega t \]

\[ \frac{\partial V_{in}}{\partial t}_{\text{MAX}} = \frac{V_{REF}}{2} \omega \]

\[ \Delta T < \frac{\Delta V_{\text{MAX}}}{\partial V_{in}} = \frac{V_{REF}}{\omega V_{REF}} / 2^{n+1} \]

\[ \Delta T < \frac{1}{\omega 2^n} \]
Aperture Uncertainty

\[ V_{in} = \frac{V_{\text{REF}}}{2} (1 + \sin \omega t) \]

\[ \Delta T < \frac{1}{\omega 2^n} \]

Example: If \( f_{\text{CLK}} = 200 \text{MHz} \), \( n = 14 \) determine the aperture uncertainty

\[ \Delta T < \frac{1}{2\pi (2\times10^8) 2^{14}} = 4.86\times10^{-14} \approx 0.05 \text{psec} \]

Aperture uncertainty requirements can be very stringent!
Elimination of Input S/H

Why is input S/H used?
Elimination of Input S/H

Why is input S/H used?

Conventional Wisdom:

Because want right sample at input
Because gain stages mess up when input is time varying

But what does an ADC error do to the Boolean output?

\[ V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue}) \]

Absolutely nothing if over-range protection is provided!
Elimination of Input S/H

Why is input S/H used?

Conventional Wisdom:

Because want right sample at input
Because gain stages mess up when input is time varying
Elimination of Input S/H

Advance sampling clock a little so that sample is taken at quiet time but not too much to loose over-range protection
Fully Differential Architectures

Second-order spectral component is often most significant contributor to SFDR and THD limitations in single-ended structures.

Noise from ADC and other components, coupled through the substrate, often source of considerable noise in an ADC

- All even-ordered spectral components are eliminated with fully-differential symmetric structures
- Common mode noise is rejected with fully-differential symmetric structures

Almost all implementations of Pipelined ADCs are fully-differential.

Straightforward modification of the single-ended concepts discussed here.

Authors often present structures in single-ended mode and then just mention that differential structure was used.

Modest (but small) increase in area and power for fully differential structures.
Pipelined Data Converter Design Guidelines

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   (degrade modestly to account for slewing)

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<tr>
<td>7. Sampling operation inherently introduces a sampled-noise due to noise in resistors</td>
<td>7. Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage).</td>
</tr>
<tr>
<td>8. Signal-dependent tracking errors at input introduce linearity degradation</td>
<td>8. Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches</td>
</tr>
<tr>
<td>9. Aperature uncertainty can cause serious errors</td>
<td>9. Since latency usually of little concern, be sure that a clean clock is used to control all sampling.</td>
</tr>
<tr>
<td>10. Input S/H major contributor to nonlinearity and power dissipation</td>
<td>10. Eliminate S/H but provide adequate over-range protection for this removal. Reduces power dissipation and improves linearity!</td>
</tr>
</tbody>
</table>
Layout Issues
Number of Bits/Stage
Cyclic (Algorithmic) ADCs

Cyclic (algorithmic) ADC
Reduces throughput but also area
Cyclic (Algorithmic) ADCs

\[ X_{\text{IN}} \rightarrow \text{S/H} \rightarrow \text{Stage 1} \rightarrow \text{Pipelined Assembler} \rightarrow n \]

\[ C_{\text{LK}} \]

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