CprE583 Paper Presentation

“Dynamic FPGA Routing for Just-In-Time FPGA Compilation”

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JIT FPGA Compilation

Introduction

• Just In Time (JIT) compilation used to dynamically compile software from a “standard format” binary, to a target-specific binary.
  – x86 to binaries converted to RISC or VLIW
  – Java bytecode to run on native processor instead of Java Virtual Machine

• Propose extending to FPGA architectures.
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Introduction

- There are no “standard” binaries for FPGA designs.
  - Netlists are generated for a specific FPGA architecture (even within an FPGA family).
  - There are many FPGA architectures.
- Propose developing JIT compiler for FPGA
  - Small processor on FPGA would do placement and routing from supplied “Standard” binary.
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Mapping Considerations

• When performing FPGA mapping, “routing” takes the most time and resources.

• Current mapping algorithms work well, but are timely and resource intensive.
  – Time and resources are scarce in Embedded Designs.

• Propose new “Lean Routing Algorithm”.
  – Riverside On-Chip Router (ROCR)
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FPGA Fabric Considerations

• Current FPGA fabrics not suited for JIT.
  – Current FPGA fabrics contain complex CLBs, labyrinth routing, and varied resources — requiring sophisticated mapping tools.

• Redevelop FPGA fabric for JIT routing.
  – Simple Configurable Logic Fabric (SCLF).
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FPGA Fabric Considerations

Figure 2: (a) Simple configurable logic fabric (b) configurable logic block (CLB), and (c) switch matrix (SM) architecture.
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Lean Routing Algorithm

- Riverside On-Chip Router aims to be lean.
  - Borrows ideas from traditional “Versatile Place and Route (VPR)” algorithms, including overuse of resources up-front which get pruned later.
  - Also borrows basic “cost routing” accounting technique.
  - Using the JIT-oriented fabric, ROCR performs routing with less resources than VPR… thus being lean.
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Lean Routing Algorithm

Figure 3: Riverside On-Chip Router (ROCR) algorithm overview.

1. Start Routing
2. Initialize SCLF routing costs
3. Greedily route all unrouted nets
   - Illegal routes exists?
     - yes: Rip-up illegal routes
     - no: Build/Update routing conflict graph
4. Assign route channels (Brelaz’s vertex coloring)
   - Illegal channel assignments?
     - yes: Adjust SCLF routing costs
     - no: Done!
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Implementation Results

Figure 4: Critical path (nanoseconds) for several MCNC benchmark circuits using VPR routability-driven (RD) and timing-driven (TD) router and ROCR.

Figure 5: Total wire segments required to route several MCNC benchmark circuits using VPR routability-driven (RD) and timing-driven (TD) router and ROCR.
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Conclusions And Future Work

- JIT FPGA routing an interesting idea, with results that show promise.
- Work is being done to further address timing consideration and timing optimizations, increasing the potential.
- The work to date is smaller scale, with ambitions towards more complicated devices in the works.
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Analysis Of Proposal
(Bryan and Bill’s Opinions)

• The proposed idea of JIT routing is interesting, and the idea has attractive aspects. However, despite the attractions, some obvious problems exist.

  – JIT seems tailored for the domain of the internal CLBs; at least this paper doesn’t discuss the issue of signal-to-pin assignment.

  – Even if signal-to-pin could be identified, JIT seems capable of simple LVTTL interface standards and not anything more complicated, like LVDS, etc.
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Analysis Of Proposal
(Bryan and Bill’s Opinions)

- The standard programming file (and implied “standard programming interface”) is a terrific idea, but for the JIT routing to be usable in industry, the routing algorithm needs to be guaranteed deterministic. That is, for a given programming file, and a given chip, you need to be guaranteed the same routing every time. No exceptions.

- Further, for certain markets, design over temperature is a must. The JIT router needs to understand (and be provided information from the programming file) as to what temperature ranges its routing solution needs to meet and how that part’s timing reacts to temperature.
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Analysis Of Proposal
(Bryan and Bill’s Opinions)

- The routing performance results show a dramatic improvement in processing time and resources with their routing algorithm. However, it is stated that the same processor was used for obtaining the results. Yet the proposed system will use a small embedded processor, which will most likely not provide the same performance.

- The paper does not mention how resource utilization issues are to be resolved. For example, meeting timing parameters, or CLB usage. Not every chip that supports this architecture will have the same number of resources, and there was no mention of how something like that would be handled.
Questions? Comments?

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