SWITCHED RESISTOR FILTERS

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Abstract

A new technique using switched resistors to implement high frequency analog filters is presented. This approach is compatible with MOS technology and has the effective RC time constants determined by capacitor ratios. The technique involves periodically pretuning a MOSFET which is biased in the ohmic region. Once pretuned, the circuit behaves as a continuous time filter and can be used at frequencies beyond that of switched-capacitor filters. Results for both a discrete and integrated version of this filter are discussed.

I. INTRODUCTION

The inability to accurately determine RC products in existing semiconductor processes has impeded the development of monolithic active RC filters. This problem has been recently circumvented by using switched-capacitor techniques in which the effective RC products are determined by capacitor ratios which can be accurately determined (to .1% or better [1]) in existing popular NMOS processes. The switched-capacitor (SC) filters, however are discrete-time in nature and thus introduce aliasing and hence require additional input and output continuous-time filters. SC filters are also subject to frequency warping, require cumbersome analysis and modeling, and are often limited to low frequency applications due to the limitations of the switches and active devices imposed by the high clock rates generally required.

The switched-resistor (SR) technique presented here employs FETs biased in the ohmic region as resistors. All FET resistors are periodically switched out of the filter and into a pretune circuit which maintains the resistance of the FET at the prescribed value by establishing the gate to source voltage on a holding capacitor. The continuous-time nature of the filter, however, is maintained by alternately switching other properly pretuned FET resistors into the filter during the pretune states. Since the resistors are memoryless elements, additional requirements such as the rapid transfer of charge at switching times generally required in switched-capacitor circuits are not made on the active devices.

The use of FETs as voltage-controlled resistors in the design of compensated filters has been discussed in the literature. Rao and Srinivasan [2] used JFETs to compensate for power supply effects on the GB of the OP AMPs. Master and slave filters are employed in [3] and [4] where the master is phase-locked to a reference signal source to generate a dc voltage which simultaneously controls both the master and slave filters. Unfortunately the "Master-Slave" approach requires matched FET characteristics in [3] and matched programmable operational amplifiers and FET characteristics in [4] since the "Master" filter rather than the desired "Slave" filter is compensated. The matching of the FET resistances for a common gate to source voltage are strongly dependent upon the matching of threshold voltages which cannot be controlled as accurately as capacitor ratios [5]. Furthermore, only a single characteristic of the master filter, ω_o, is controlled by the phase-lock technique which is in general not sufficient to guarantee proper operation of the slave filters.

Another "Master-Slave" approach using voltage-controlled integrators instead of the FETs directly was presented recently [6] but it too requires matching of FETs employed in the integrators for proper operation.

The Switched-Resistor approach presented in this paper pretunes each resistor in the actual filter so that the component values of the actual filter are compensated. The effective RC products of the filter are proportional to a ratio of capacitors (which may realistically be monolithic as in the switched-capacitor approach) which can be typically controlled to about .1% in existing MOS processes. It is actually preferable to accurately determine RC products rather than absolute resistor or capacitor values since present manufacturing tolerances on absolute resistor and capacitor values are still quite large. The pretune circuit compensates for changes of temperature and for FET mismatch, thus eliminating the need of matching the less controllable FET characteristics.

A comparison of SR designs with the popular SC approach is justifiable since both are manufacturable with the same basic MOS process. Although the

filter characteristics for both approaches are determined by capacitor ratios, the SR designs are capable of higher frequency operation and less subject to frequency warping and aliasing due to the inherently continuous-time nature of the filter response.

II. SWITCHED-R STRUCTURE

The basic switched-resistor structure is shown in Fig. 1 where the resistor R of Fig. 1(a) is ideally equivalent to the SR structure of Fig. 1(b). The FETs Q_1 and Q_2 are biased to operate in the ohmic region by appropriately restricting the magnitude of the drain to source voltage. The voltage on the gate-source capacitors is established by the pretune circuit so that ideally $R_{FET1} = R$ during clock phase ϕ_1 and $R_{FET2} = R$ during clock phase ϕ_2. The clocks ϕ_1 and ϕ_2 are assumed complementary and nonoverlapping. The clock frequency, f_c, determines the refresh rate but does not affect circuit performance provided $\frac{1}{f_c}$ is much larger than the RC time-constant of the gate-source capacitance and the FET input impedance which can be practically established in the .1 sec - 10 sec. range and higher.

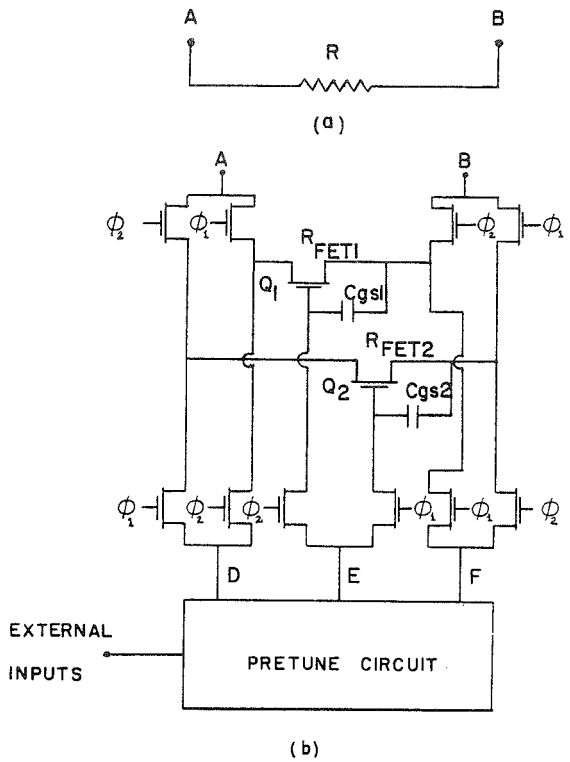

Figure 1. Basic Switched-Resistor Process
a) Fixed Resistor b) Switched-Resistor

Many options exist for the design of the pretune circuit, the choice of which strongly affects the characteristics of circuits employing the switched-resistors. Emphasis here will be placed upon precharge designs which will accurately determine the effective RC time-constants of passive or active RC filters employing the switched resistors. With this goal, one such precharge scheme will be discussed.

Assume a passive or active RD filter is to be transformed to a switched-resistor structure by replacing all resistors by SR equivalents. Assume C_u is the unit capacitance for all capacitors in the original filter design and that α is a positive real number. A precharge circuit using a basic phase-lock approach is shown in Fig. 2a.

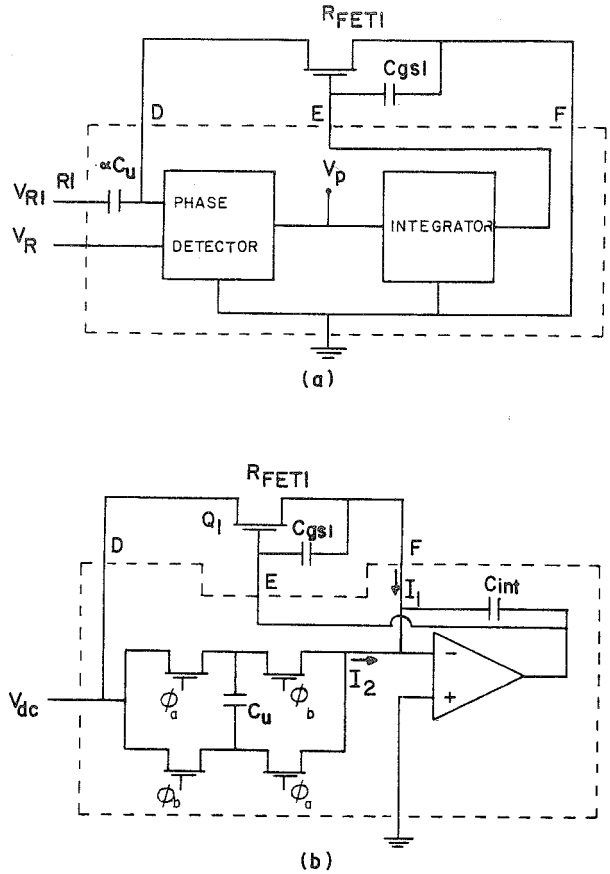

Figure 2. Typical Pretune Circuits During Clock Phase ϕ_1 a) Phase-Locked
b) Switched-Capacitor

along with Q_1 (which is in the precharge state during clock phase ϕ_1). V_R is an external reference signal of frequency ω_R and 0° reference phase. The reference voltage V_{R1} is of the same frequency as V_R but shifted in phase by θ_R. The phase detector has a time average output voltage,

V_P, that relates monotonically in a sufficiently large interval about the zero crossing, θ_{Do}, to the phase at node D such as shown in Fig. 3. The phase detector drives an integrator which in turn determines the gate-source voltage stored on the gate-source capacitor C_{gs1}. This pretune circuit will force the first-order $R_{FET1} - \alpha C_u$ circuit to have a phase shift of θ_{Do} between nodes R_1 and D. It thus follows that during lock the value of $R_{FET1}C_u$ is given by

$$R_{FET1}\, C_u = \frac{\tan(90° - \theta_{Do} + \theta_R)}{\alpha\omega_R} \quad . \qquad (1)$$

Since the product of R_{FET1} and the unit capacitance is dependent only upon accurately controllable parameters (θ_{Do}, θ_R, and ω_R) and the capacitor ratio α it follows that the effective product of R_{FET1} and any capacitor in the filter is likewise dependent only upon θ_{Do}, θ_R, ω_R, and a ratio of capacitors as desired. Although specific details about phase comparator designs will not be presented, one such scheme can be obtained by placing high-speed comparators at both inputs of the phase detector and using the outputs of these phase comparators to drive an "exclusive-or" gate between two appropriately determined voltage levels while making $V_{R1} = V_R$ (i.e. $\theta_R = 0$). The choice of α, ω_R, and θ_{Do} remains to be made. If the original filter has equal R's and operates around ω_o, a practical choice of these parameters might be $\omega_R = \omega_o$, and $\theta_{Do} = 45°$. Note that this

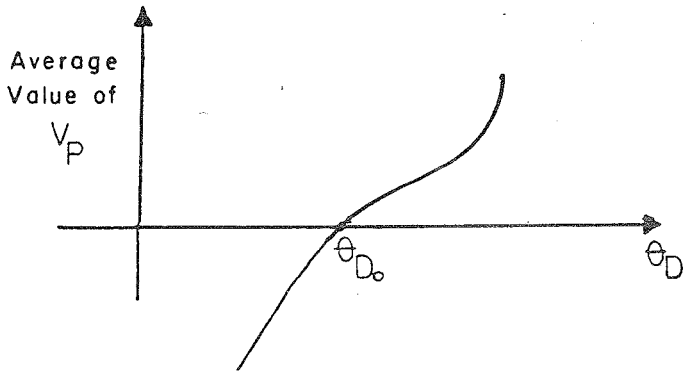

Figure 3. Typical Transfer Characteristics of Phase Detector

scheme actually requires only the reference V_R since V_{R1} has been chosed to equal to V_R. Another similar phase comparator scheme appears in the following example. Phase comparator circuits like these are quite popular and used for many applications. They are similar to those used in the Master-Slave schemes discussed earlier. A switched-capacitor pretune circuit appears in Fig. 2b.

In filters involving a large number of switched-resistors, the area devoted to the pretune circuits must be considered. A single pretune circuit, however, can be used to pretune several resistors since the time required to pretune a single MOS resistor will typically be much less than the period of the switching clock ϕ_A.

The frequencies range over which these switched-resistor filters can operate is quite large since the filter itself behaves as a continuous-time circuit except at the switching times of the pretune circuit which can be realistically selected in the .1Hz to 10Hz range. If a passive circuit is realized, operation should extend into the MHz range and if active devices are employed they will generally determine the high frequency limitations.

The filter topology selection/ synthesis problem will parallel that of the well-researched active RC approach. Many of the active RC filters should be directly applicable to switched-resistor techniques. It may prove desirable to consider minimum resistor and/or equal resistor and/or grounded resistor active RC filters as the starting point for switched-resistor filter synthesis.

III. EXAMPLE

A simple first-order highpass switched-resistor filter is shown in Fig. 4(b) along with the parent analog circuit of Fig. 4(a). The pretune circuit is shown in the dashed box. For this circuit, assume

V_R	$V_m \sin \omega_R t$
V_{R1}	$V_{m1} \sin (\omega_R t + 45°)$
A_1 & A_2	are high speed comparators
A_3	is an OP AMP
G_1	is an exclusive-or digital gate with symmetric output voltage levels

$R_I C_I \gg \frac{1}{\omega_R}$.

If the additional assumptions that all active devices are ideal and that the time-constants of the gate capacitor - FET input impedance is much larger than the period ϕ_2 if follows from (1) that the circuit of Fig. 4(b) behaves like the circuit of Fig. 4(a) with an equivalent resistance of

$$R_{FEQ} = \frac{\tan(90° - 0° - 45°)}{C_R\,\omega_R} = \frac{1}{C_R\omega_R} \quad . \qquad (2)$$

Stated alternately, the 3dB cutoff frequency of the circuit of Fig. 4(b) is given by

$$\omega_{3db} = \frac{C_R\omega_R}{C_F} \qquad (3)$$

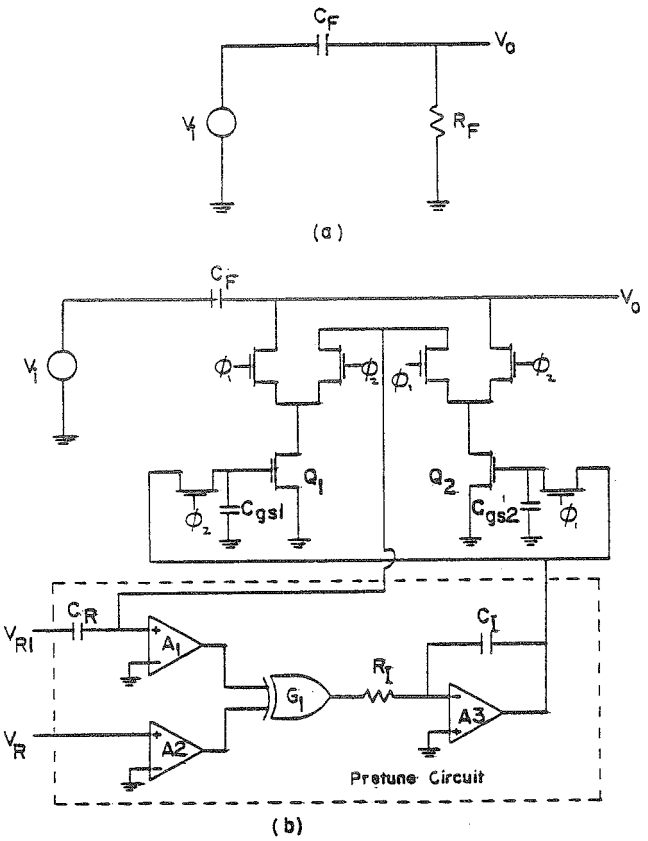

Figure 4. Example of Switched-Resistor High-pass Filter a) Parent Passive Structure b) Switched-Resistor

Note that the filter performance is essentially independent of R_I, C_I, C_{gs1}, C_{gs2}, period of clocks, V_m, and V_{m1}. If the ratio of C_R to C_F is accurately controlled, as can be currently accomplished in standard monolithic processes, it follows that the characteristics of the filter are accurately controllable.

V. EXPERIMENTAL RESULTS

The circuit of Fig. 4b was evaluated in the laboratory using discrete active and passive components. The measured values for the components are listed in Table 1 for three different test frequencies at which the filter was evaluated. Relatively large valued capacitors were used in this evaluation so that instrumentation and switch parasitics would be negligible. Comparators A_1 and A_2 were of type LM361. The "exclusive-or" gate was constructed from a T^2L 7486 followed by a 7404 and two analog switches to drive R_I (which was duplicated) by the well defined voltages of either +5V or -5V. The amplifier A_3 was a LF356. The FETs were ECG465 devices that were intentionally significantly mismatched.

Table 1

Text Conditions and Experimental Performance for Circuit of Fig. 4b

	Test 1	Test 2	Test 3
C_F	100. nf	9.999 nf	10.107 nf
R_{FEQ}	1.59 KΩ	1.59 KΩ	1.44 KΩ
T	10 sec.	10 sec.	10 sec.
ω_r	(2π)1.0 K rad/sec.	(2π)0.996K rad/sec.	(2π)99.93 K rad/sec.
ϕ_r	45°	45°	45°
C_R	100. nf	9.999 nf	1.106 nf
C_{g1}, C_{g2}	10 nf	10 nf	10 nf
f_o	1.999 KHz	10.00 KHz	99.93 KHz
f_o, ϕ_1	1.003 KHz	10.38 KHz	102.4 KHz
f_o, ϕ_2	1.003 KHz	10.16 KHz	99.63 KHz

The steady-state cutoff frequencies during the states ϕ_1 and ϕ_2 (f_o, ϕ_1 and f_o, ϕ_2 respectively) are also compared in Table 1 with the theoretical (f_o) obtained assuming $R_{FET}(t) = R_{FEQ}$. As can be seen the percent error between the theoretical cutoff frequency and that obtained during either ϕ_1 or ϕ_2 is less than 4% at all test frequencies. The observed change in the frequency response during either phase ϕ_1 and ϕ_2 was quite negligible as expected since T_g (>1000 sec.) was quite large compared to T. Considerably better accuracy can be expected in monolithic form.

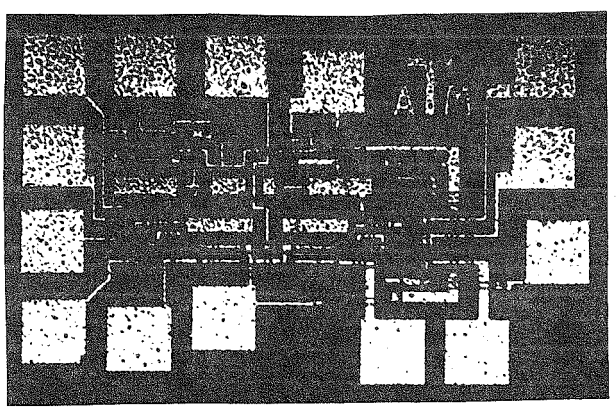

Figure 5. Microphotograph of Integrated Switched-Resistor Building Block

An integrated version of a switched-resistor pair was designed and fabricated in a double-poly NMOS process. A microphotograph of the die of this building block is shown in Fig. 5. This building block was used to investigate the effects of the gate holding capacitor and switch mismatch. The gate-holding capacitor was approximately 1pf. For a refresh rate of .5Hz a few percent droop in Vgs

was observed. Switch mismatch effects appear negligable. Additional details will be presented in the near future.

Design Considerations for Switched-Resistor Networks

In this section we will attempt to outline some of the practical considerations and limitations of the switched-resistor approach.

(1) The L/W ratios of the MOS switches should be selected so that the switch "on" impedance is small compared to the switched-resistor impedances in the circuit.
(2) The dynamic range is limited by the linearity of the MOSFET in the ohmic region. This can be increased with depletion devices and/or large gate to source voltages.
(3) C_{gs} should be large enough so that parasitic switch and poly capacitances to the gates do not cause a significant change in the gate to source voltage when the MOSFET is switched from the pretune circuit to the filter circuit. It should be pointed out, however, that cancellation of clock feedthrough effects to the gate-holding capacitor occur if identical switches are used to connect R_{FET} to the pretune circuit.
(4) The parasitic capacitance associated with the switched-resistors should be considered when designing the filter if the pretuned resistance is large.
(5) The clock controlling the gate-holding capacitor should be nonoverlapping.
(6) In a circuit employing a large number of switched-resistors, one must consider the tradeoffs between using a single pretune circuit with relatively complicated clocking schemes compared to multiple pretune circuits and very simple clocking.

IV. CONCLUSIONS

A new method of designing MOS compatible active filters has been presented which employs switched-resistor techniques. The characteristics of these filters were shown to be dependent upon ratios of capacitors as in switched-capacitor designs and hence the filter characteristics are largely independent of process paramenters.

One of the major advantages of using switched-resistor structures instead of switched-capacitor designs is the capability of designing monolithic high-frequency filters since the filter is essentially continuous-time in nature rather than sampled-data.

Switched-resistor techniques may well offer a superior alternative to switched-capacitor configurations in the design of monolithic filters in some applications. A combination of switched-resistor and switched-capacitor designs on a single chip also seems practical and should provide a significant increase in flexibility for the circuit designer.

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