

# LASER TRIMMABLE TEMPERATURE COMPENSATION TECHNIQUE FOR MONOLITHIC MOS RESISTORS

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## ABSTRACT

A laser trimmable resistor-switch (RS) technique which compensates for temperature and process variations in monolithic MOS resistors is discussed. A temperature-to-digital converter is used to sense temperature and through a RS technique compensate for temperature variations. Laser trimming fine tunes the resistors to the desired values compensating for process variations. Details of the design, practical implementation and applications of this technique using a standard double poly NMOS process are discussed.

## PROBLEM STATEMENT

Large-scale integrated circuits for many analog and combined analog-digital circuit functions are proving feasible in single channel and complementary metal-oxide-semiconductor (MOS) technologies. The key elements in these MOS circuits have been precision-ratioed MOS capacitors, MOS transistor analog switches, internally compensated operational amplifiers (op amps), low offset comparators and charge-coupled devices (CCD) (1). Digital signal processors, CCD's, switched-capacitor (SC) filters, switched resistor (SR) filters and active RC filters are readily integrable design approaches that use the above key elements but each have draw-backs.

The temperature and process variations of monolithic resistors and capacitors make RC active filter design quite impractical. In addition, the GB effects of the op amp severely limit the operating frequency range of these filters (2)(3)(4). Resistor manufacturing tolerances of  $\pm 30$  percent combined with a typical temperature coefficient of  $+0.1$  percent/degC (5) creates up to  $\pm 40$  percent deviation in the desired resistance value over a 100 degC operating range. Combining this with the temperature and process variations of capacitors ( $+0.25\%/100\text{degC}$  and a few percent respectively (1)(5)) produces RC product variation in excess of  $\pm 50\%$ . The op amp GB can cause a  $\pm 20\%$  variation of center frequency from a calculated center frequency if the GB is not taken into

account during design (3). The presented technique focuses on varying the resistor values to simultaneously compensate for all of the above problems.

## TEMPERATURE TO DIGITAL CONVERTER

### Block Diagram

The temperature and process compensation technique described here employs the three stages shown in the block diagram of Figure 1.

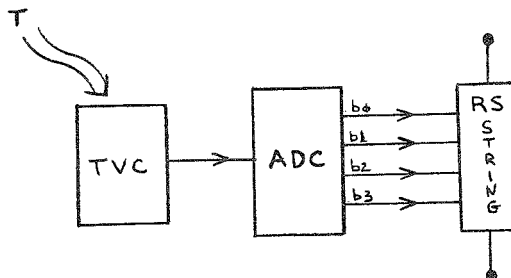


Figure 1 - Block diagram of laser trimmable compensation technique

The temperature-to-voltage converter (TVC) produces an output voltage proportional to the environmental temperature. This analog voltage is converted to a binary signal through the ADC which controls resistor-switch (RS) strings. Once fabricated, the TVC and RS strings are laser trimmed.

### Temperature Sensor

The threshold voltage  $V_t$  of MOS transistors is nearly linearly dependent on temperature (6)(7). A temperature sensor which utilizes this threshold voltage temperature dependence is shown in Figure 2.

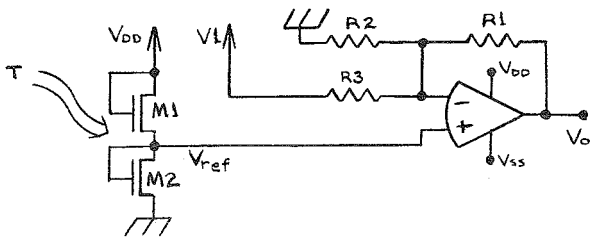


Figure 2 - TVC with laser trimmable gain and offset

The two n-channel enhancement mode devices, M1 and M2, are forced into saturation by tying the gates and drains together. By using Sah's equation and equating the current through the two devices, an expression for Vref is found:

$$V_{ref} = \frac{V_{DD} - V_{t1} + V_{t2} \sqrt{W_2 L_1 / L_2 W_1}}{\sqrt{1 + W_2 L_1 / L_2 W_1}} \quad (1)$$

By making the device's geometrical widths and lengths,  $W_2/L_2$  much greater than  $W_1/L_1$ , the threshold voltage of device M1,  $V_{t1}$ , can be neglected yielding:

$$V_{ref} \approx \frac{V_{DD}}{\sqrt{W_2 L_1 / L_2 W_1}} + V_{t2} \quad (2)$$

Since  $V_t$  is linearly dependent on temperature

$$V_t(T) = V_t + aT \quad (3)$$

where  $a$  is the threshold voltage temperature coefficient and

$$V_t = V_{t0} + \gamma [\sqrt{\phi - V_{s0}} - \sqrt{\phi}] \quad (4)$$

where  $\phi$  is the surface potential at strong inversion,  $\gamma$  is the bulk threshold parameter and  $V_{t0}$  is the zero bias threshold voltage. From equations (2) and (3) it follows that  $V_{ref}$  is nearly linearly dependent on temperature.

#### Laser Trimmable TVC

The amplifier portion of the TVC provides a laser trimmable gain and offset. See Figure 2. Assuming an ideal amplifier and solving nodal equations one obtains an output voltage which is a function of  $V_{ref}$  and thus of temperature:

$$V_o = V_{ref}(1 + R_1/R_3 + R_1/R_2) - V_1 R_1/R_3 \quad (5)$$

$$\approx (R_1/R_3)[V_{ref}(1 + R_3/R_2) - V_1] \quad (6)$$

for  $R_1 \gg R_3$

By laser trimming resistors  $R_2$  and  $R_3$ , the offset of the output  $V_o$  is zeroed. Then adjusting  $R_1$  sets the gain so the desired  $V_o$  vs temperature slope is achieved.

#### Experimental Circuit

The TVC of Figure 2 was fabricated using a double-poly NMOS process and trimmed with an Electro Scientific Industries model-44 laser trimming system. The circuit layout of the fabricated TVC is shown in Figure 3.

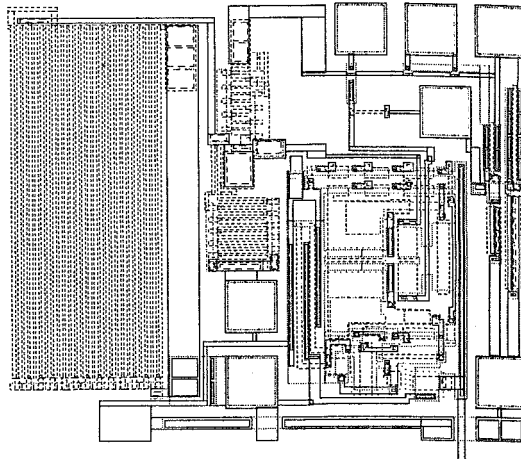


Figure 3 - Layout of the fabricated TVC.

Approximately 50% of  $R_3$  was trimmed using a Q-switch Nd:YAG laser of wavelength 1.06 microns adjusted for an average power of 1.25mW. The laser controller was set for a pulse width of 70nsec, a speed of 2mm/sec and a Q-switch repetition rate of 1KHZ. Approximately 20% of  $R_1$  was trimmed using all the above settings except trim speed which was reduced to 1mm/sec. This resulted in an approximate offset of 0.5volts at 70degC and slope of -5volts/100degC. The resulting  $V_o$  vs temperature plot is graphed in Figure 4.

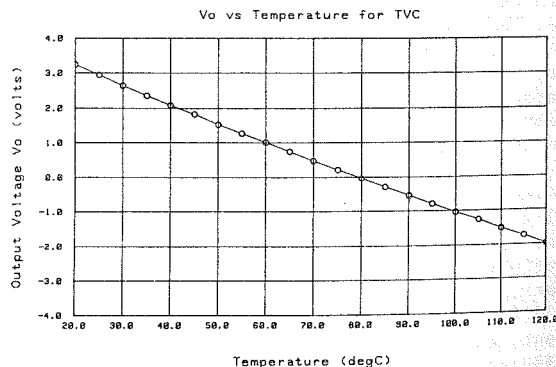


Figure 4 -  $V_o$  vs temperature after laser trimming.

The trim was accomplished in two steps with only a slight error of 0.47mV offset at 70 degC and a slope within +2% of linearity. This can be

corrected with additional trimming steps or through the use of a tuning algorithm that predicts the error before trimming, allowing correction of error during the first two trim steps. Further design modifications are being made to increase linearity, to more accurately zero the offset and to decrease the dependence of Vref on VDD.

### Other Considerations

Performance of the op amp used is not critical since the effects of input offset voltages and temperature variations in gain are trimmed out. The common mode effects of the op amp are minimized by maintaining the op amp inputs within 1 volt of ground. This is done through biasing the devices M1 and M2 in the TVC so that Vref is approximately 1.0volts. Output current drive of the op amp is minimal since the feedback resistors and input impedance of the ADC are kept high.

Since thermal time constants are generally very long, speed of the analog-to-digital converter (ADC) is not of major concern. Thus numerous techniques are available for designing the ADC in an area efficient manner. No major comments about the ADC will be made since several good ADC design techniques are available. It should be emphasized that the TVC and ADC blocks are not dependent upon filter topologies. A well designed and tested pair can be stored in a data-base and placed when needed on the circuit layout. The number of bits in the ADC determines the precision of the active filter. Linearity of the ADC binary output is not critical since the laser trimming will adjust the RS strings as will be discussed in the following section.

### RESISTOR-SWITCH STRINGS

A 4-bit RS string is shown in Figure 5.

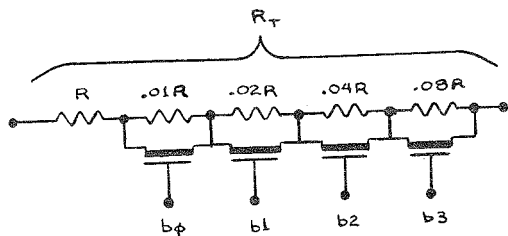


Figure 5 - Laser trimmable binary weighted RS strings

The total resistance,  $R_t$ , is broken into five smaller resistors, four which can be shorted by switches. The resistors are binary weighted such that:

$$R_t = R + 0.01b_0R + 0.02b_1R + 0.04b_2R + 0.08b_3R \quad (6)$$

where the coefficients  $b_0$  through  $b_3$  can only take

on the values 0 and 1. This allows a 16% adjustment of the RS strings by simply shorting or opening the switches across the resistors. These RS strings replace the controlling resistors in a given circuit. The switches are made as wide as area permits to minimize ON resistance.

The laser trimmable compensation scheme works as follows. Assume that as temperature increases the output  $V_o$  of the TVC increases causing the binary output of the ADC to increase. Since a high bit output causes a switch to close, the total RS string resistance  $R_t$  will decrease with temperature. This will compensate for the positive temperature coefficient of the resistor. The resistance can be trimmed to be exact at 5 different temperatures as illustrated in Figure 6.

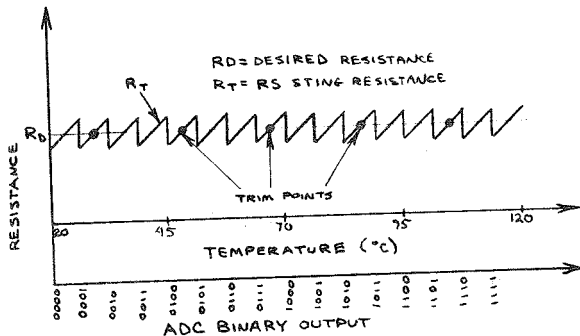


Figure 6 - Resistance vs temperature after laser trimming

If the resistance of the RS string varies linearly with temperature and if the RS string varies linearly due to switching, then the resistance will be exact at 16 points. Since resistive temperature effects usually dominate in for example, an RC active filter, the trimming scheme just discussed will provide "exact" filter performance at trim temperatures and "close to exact" at intermediate temperatures even if some other temperature coefficients are somewhat nonlinear. If the resistors are binary weighted, a theoretical accuracy of approximately  $\pm 1/2^{n-1}\%$  over an 80 degC temperature range is expected.

### LASER TRIMMING

Three laser trimming techniques have been considered for trimming the passive components. Heating polysilicon resistors with low-power laser pulses decreases resistance by increasing grain size. This technique is called laser annealing and can be used for fine trims. Metal or polysilicon links can be severed with the laser or portions of resistors removed to change component values. A third technique still under development fuses two layers of polysilicon with a high power laser pulse to short portions of resistors together. These techniques can be used simultaneously for coarse and fine up/down trims.

## CONCLUSIONS

Although initial emphasis has been on temperature compensation of the resistors, a functional trimming of the resistors in a filter structure will simultaneously compensate for temperature, resistor, capacitor, GB, and parasitic limitations on filter characteristics.

Application of this scheme is presently being tested with an NMOS active filter using an ESI Model-44 laser. Characteristics of the compensated resistors and performance of the monolithic filter structure will be reported when the results are available.

## REFERENCES

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