MONOLITHIC, FREQUENCY REFERENCED, DIGITALLY SELF-TUNED FILTERS

Jeffrey Fincher and Randall Geiger

Department of Electrical Engineering

Texas A & M University

College Station, Texas 77843

ABSTRACT

A method is presented for designing monolithic filters which uses an external frequency reference and digitally controlled resistor arrays. This method produces a filter whose W_o and Q can be tuned to better than 1% of their desired values. The technique is applicable at both low and high frequencies.

INTRODUCTION

Monolithic filters are smaller than discrete component filters and are less expensive to manufacture in quantity. Present techniques for designing these filters suffer from several drawbacks which make discrete component filters preferable in many applications where space is not important. The approach to monolithic filter design presented in this paper greatly reduces these drawbacks.

In the two most common approaches toward monolithic filter design, either resistor-capacitor products or capacitor ratios are used to determine the filter characteristics. Monolithic resistor-capacitor products are difficult to maintain with an accuracy greater than plus or minus 30% due to process parameter variations. Capacitor ratios can be held to reasonably tight tolerances on single substrates, but the switched capacitor circuits which utilize these ratios suffer from aliasing and do not currently produce good results at frequencies much above 10 kHz. Another approach being investigated is the Switched-Resistor [1] technique in which FET resistors are alternately and repeatedly adjusted to maintain an accurate resistance. The Switched-Resistor technique involves slowly switching a resistor between a filter circuit and pretune circuit in such a manner that the effective RC products are proportional to a ratio of two capacitors and inversely proportional to an external reference frequency.

THE DIGITALLY SELF-TUNED FILTER

As in the Switched-Resistor method, R-C products are controlled in the proposed technique to determine the filter characteristics, but instead of utilizing resistors which require repeated refreshment, each adjustable resistor consists of a digitally controlled array of resistors and switches. The resistance of each array is determined by a binary input signal which controls the switches and thus the resistance of the array. The array is designed so that its nominal resistance approximates that required to give the filter a certain characteristic. Once established, the binary inputs are latched to maintain the required values.

For tuning, signals of known frequencies are applied to the input. A phase comparator is used to determine the phase shift of the filter at different frequencies near W_o. A control circuit uses the information provided by the phase comparator to adjust the variable resistors until the filter characteristics (e.g. W_o and Q) converge to the desired values.

The tuning procedure always occurs at power-up. The tuning algorithm can be implemented at other times, if necessary, such as when a significant temperature change is detected. With clever tuning schemes, the time it takes to trim the filter is in the millisecond range. Since the adjustment of the filter is based on measured performance, the filter characteristics are insensitive to GB variations and parasitic effects. A standard NMOS process can be used to produce filters which operate in the 100kHz range.

The resistance of the array shown in Figure 1 is adjustable from $R_t/2$ to R_t, where R_t is the maximum resistance of the array. The resistors in the array are sized so that the series combination of the resistor and on-impedance of the switch for each section on the right side of the array equals the corresponding resistance on the left side of the array. This allows for approximately a +/- 25% change in resistance about the nominal value of $3R_t/4$ which should be adequate to adjust for process variations, parasitics, and GB effects in many applications.

A block diagram of the general filter structure is shown in Figure 2. A graph of the transfer function of the resistor array is shown in Figure 3.

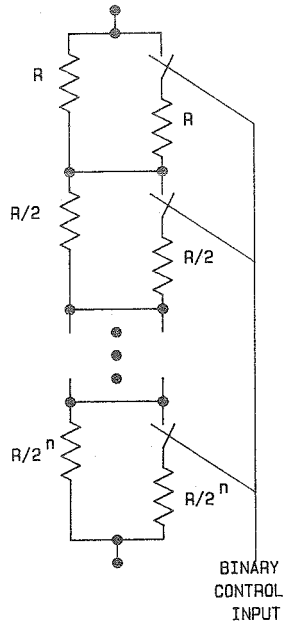

Figure 1: Schematic of Resistor Array

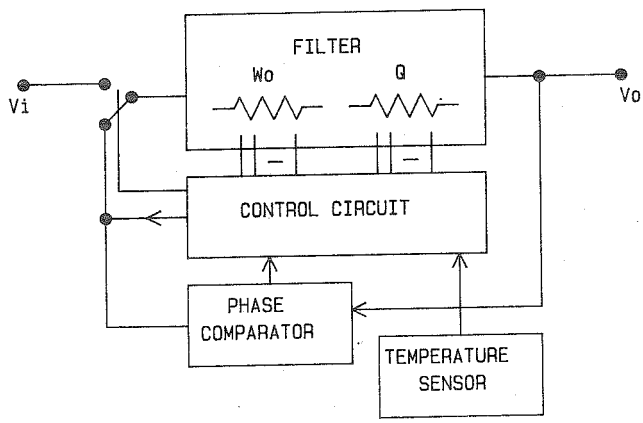

Figure 2: Block Diagram of Filter Structure

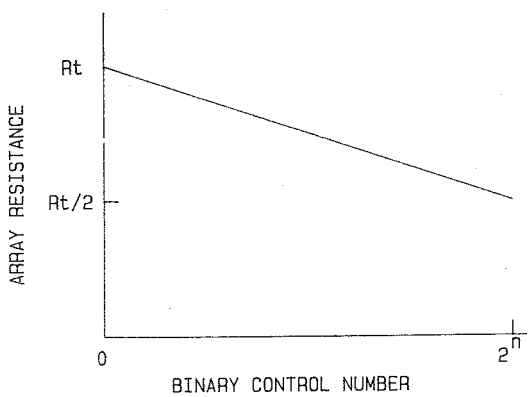

Figure 3: Graph of Resistor Array Transfer Function

THE CONTROL CIRCUIT

The control circuit itself plays a major role in the performance of the filter. It must be capable of electrically isolating the actual filter from the input signal for the short amount of time necessary for tuning. It must then be able to apply reference frequencies for the adjustment of the filter characteristics. (For practical reasons, the reference frequencies should be chosen as fractional multiples of a single clock frequency. They should also be spaced to give an adequately measurable change in filter characteristics.)

For the block diagram shown in Figure 2, the filter is tuned by establishing the correct phase response. By knowing what the duty cycle of the output of the phase comparator should be for the appropriate input frequency, the control circuit must be able to adjust the binary control input to the appropriate resistor array until the duty cycle converges to the desired value. The control circuit may take the form of hardware, both hardware and software, or it may be a micro-processor structure responsible for tuning and adjusting the components of a larger system of which the filter is only a part. The filter and controller may be produced as a single chip or as a 2-chip set where the controller chip may be capable of tuning several different filters individually.

The control circuit may also add flexibility to the filter design by switching in different capacitor values from a capacitor bank to achieve different filter characteristics. This allows for post fabrication circuit design.

THE PHASE COMPARATOR

Figure 4 shows a block diagram of a phase comparator that can be used for the corresponding block in Figure 2. The test frequency clock input to the phase comparator is a square wave which is also used as the test input to the actual filter during tuning. When the output of the filter is applied to the phase comparator, an output pulse whose duty cycle is proportional to the phase shift between the input and the output of the filter is generated. The control circuit measures this duty cycle and adjusts the appropriate resistor array until it converges to the desired value.

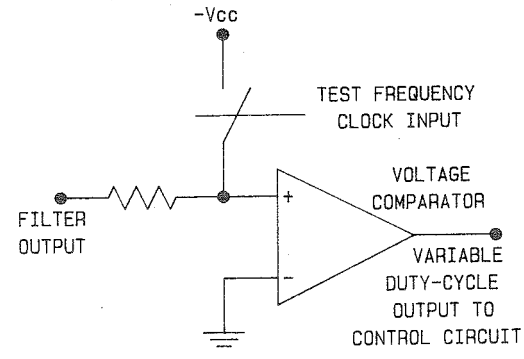

Figure 4: Schematic of Phase Comparator

FILTER DESIGN EXAMPLE

For the purpose of demonstrating the proposed technique, an example filter design is presented in this section. The topology for the second-order bandpass filter [2] shown in Figure 5 was selected because it allows for independent adjustment of W_o and Q, as illustrated by equations (1) and (2).

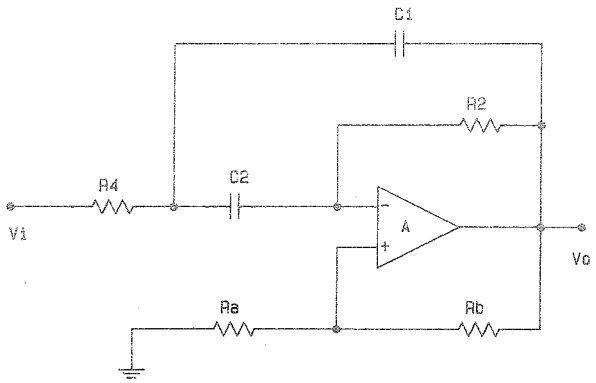

Figure 5: Schematic of Example Filter

$$W_o = \sqrt{\frac{1}{R_2 R_4 C^2}} \qquad (1)$$

$$Q = \frac{R_b \sqrt{R_2/R_4}}{R_a R_2/R_4 - 2R_b} \qquad (2)$$

The resistor arrays R_2 and R_a are used to adjust W_o and Q respectively. For this example it is assumed that W_o = 50 kHz +/- 1% and Q = 10 +/- 5%. The following calculations show that 6 bits are required to attain this resolution, provided that R_2 and R_b can be maintained to within +/- 33% of their nominal values over temperature and process variations.

The sensitivity of W_o wrt R_2 is:

$$\int_{R_2}^{W_o} = -\frac{1}{2}$$

By definition:

$$\frac{dW_o}{W_o} = \int_{R_2}^{W_o}\Big|_{\substack{\text{nom}\\ \text{val}}} \frac{dR_2}{R_2}$$

For a 1% change in W_o:

$$\frac{dW_o}{W_o} = .01$$

The nominal resistance of the type of binary array shown in Figure 1 is:

$$R_{2nom} = \frac{3}{4} R_{t2}$$

Where R_{t2} is the maximum resistance of the array. Then:

$$.01 = -\frac{1}{2}\frac{dR_2}{R_{2nom}}$$

By substitution:

$$dR_2 = -.015R_{t2}$$

Thus:

$$\frac{R_{t2} - \frac{1}{2} R_{t2}}{.015R_{t2}} = 33.3 \text{ steps}$$

Rounding up, this requires 6 bits.

The sensitivity of Q wrt R_b is:

$$\int_{R_b}^{Q} = \frac{2Q}{\sqrt{h}} + 1 \; ; \; h = \frac{R_2}{R_4}$$

By definition:

$$\frac{dQ}{Q} = \int_{R_b}^{Q}\Big|_{\substack{\text{nom}\\ \text{val}}} \frac{dR_b}{R_2}$$

For a 5% change in Q:

$$\frac{dQ}{Q} = .05$$

The nominal resistance of the type of binary array shown in Figure 1 is:

$$R_{bnom} = \frac{3}{4} R_{tb}$$

Where R_{tb} is the maximum resistance of the array.

Then for Q = 10 and h = 49:

$$.05 = 3.857 \frac{dR_b}{R_{bnom}}$$

By substitution:

$$dRb = .013 R_b$$

Thus:

$$\frac{R_{tb} - \frac{1}{2} R_{tb}}{.013 R_{tb}} = 38.6 \text{ steps}$$

Rounding up, this requires 6 bits.

It is important to know how much offset voltage can be tolerated in the voltage comparator used in the phase comparator and still maintain the desired accuracy. For example, for the second-order bandpass filter shown in Figure 3, and using the equation:

$$\theta = 90^o - \tan^{-1} \frac{W - \sqrt{1 - \frac{1}{4Q^2}}\ W_o}{W_o/2Q}$$

$$- \tan^{-1} \frac{W + \sqrt{1 - \frac{1}{4Q^2}}\ W_o}{W_o/2Q}$$

where θ is the phase shift of the filter, a 1% variation in W_o at W_o causes a phase shift of 11.26^o. For a 1V peak input signal, this corresponds to a voltage shift of sin 11.26 - sin 0.0 = 195.26mV. Assuming no error in W_o, a 5% variation in a Q of 10 at $W=1.05W_o$ causes a phase shift of 1.40^o. This corresponds to a voltage shift of sin -44.31 - sin -45.71 = 17.27mV. If the maximum error of 3% introduced by six bits of resolution on the Q adjustment were to occur, this would leave 2% allowable error remaining. This corresponds to an allowable offset voltage of sin -44.31 - sin -44.88 = 7.08mV on the voltage comparator. If the resolution were increased to 8 bits, an adjustment accuracy of 0.76% could be achieved, leaving 4.24% remaining for the phase comparator and allowing an offset voltage of sin -44.31 - sin -45.50 = 14.71mV. The error in the expected phase shift for the Q measurement is very large for a 1% error in W_o. The control circuit will have to compensate for this error by measuring the phase shift at W_o and adjusting the expected phase shift for the Q measurement accordingly. These characteristics are a function of the filter topology, and may vary for a different filter design.

CONCLUSIONS

Not only does the monolithic filter design technique presented in this paper offer improvements in the accuracy and frequency range available in a monolithic filter, it also lends itself well to applications in harsh environments where large temperature variations cause significant changes in component values. It is process independent. Modest process parameter variations will not affect the accuracy of the filter. The ultimate frequency range is limited by the GB's and slew rates of the OP AMP's and the speed of the phase comparator. If W_o is within the operating range of the OP AMP's, variations in the GB's will not affect filter accuracy, which is also insensitive to parasitics. Since switching and tuning are only performed at power-up or after significant temperature changes, the noise characteristics are greatly superior to the characteristics of those techniques which require constant high-speed switching. The dynamic range is very good, and is comparable to that reported by Banu and Tsividis [3].

REFERENCES

[1] J. Bass, "The Design and Characterization of Switched-Resistor Filters" Master of Science Thesis, Texas A&M University, to be awarded August 1983.

[2] J. J. Friend, "A single operational-amplifier biquadratic filter section," 1977 IEEE ISCT Dig. Tech. Papers, pp. 189-190.

[3] M. Banu, Y. Tsividis, "Fully Integrated RC Filters in MOS Technology", IEEE International Technology, IEEE International Solid-State Circuits Conference, pp. 244-246, February 25, 1983.