PERFORMANCE CHARACTERISTICS OF SWITCHED RESISTOR FILTERS

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1.0 Abstract

The performance characteristics and practical limitations of switched resistor filters are investigated. The dominant parasitic capacitances, FET nonlinearities, and op amp limitations are considered. Design techniques for reducing the parasitic limitations are discussed. Experimental results obtained from a switched-resistor integrator test cell are presented.

2.0 Introduction

One of the major factors limiting the development of practical monolithic filters is the inability to accurately establish the RC time constants associated with the integral passive components. Resistor deviations of ± 30% due to process variations and capacitor deviations of ±10% are common. The corresponding variations in the effective RC products are too large for most applications. Even if the process dependent variations in R and C were ignored, temperature effects and variations of the gain-bandwidth product (GB) of the operational amplifiers (op amps) typically cause unacceptable deviations of several percent in the effective RC products.

Several approaches to monolithic filter design have appeared in recent years which reference the effective RC products to an external reference frequency rather than to an actual resistor-capacitor product. These include the switched-capacitor (SC), master-slave [1-3] and switched-resistor (SR) [4] approaches. These approaches all require matching of active or passive components for proper operation but are essentially independent of the nominal process values of the resistors and capacitors. Since matching of components can be controlled much more accurately than the absolute value of the components, significant improvements in performance are attainable. One of the major sources of error in all of these frequency referenced approaches is caused by the parasitic capacitors and/or resistances inherent in any existing monolithic process.

Considerable success has been attained in minimizing the parasitic effects in SC filters as evidenced by both the literature addressing the problem as well as the widespread industrial application of SC filters in demanding applications. The accuracy attainable with SR filters is ideally comparable to that of the SC approaches. The SR filters, however, are essentially continuous time in nature and thus are not affected by aliasing and show potential for high frequency applications. It is the purpose of this paper to investigate some of the major parasitic effects which limit the performance of SR filters.

3.0 Switched Resistor Integrator Test Structure

The basic switched-resistor technique is depicted in Fig. 1. MOSFETs biased to operate in the ohmic region are used for all resistors in a filter structure. The value of the MOSFET impedance, R_{FET}, is established in a pretune

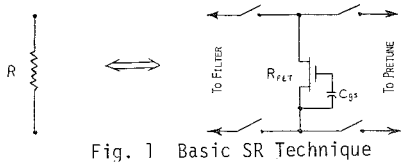

Fig. 1 Basic SR Technique

circuit by charging a capacitor connected between gate and source to the proper value. Once established, R_{FET} is switched into the filter circuit. Since the voltage on the gate holding capacitor droops with time, it is necessary to periodically switch R_{FET} back and forth between the filter circuit and the pretune circuit. This switching rate, fs, can be very low due to the small losses associated with the gate holding capacitor.

The characteristics of SR filters are strongly dependent upon the characteristics of the pretune circuit. A simplified schematic of a switched capacitor pretune circuit [4] is shown in Fig. 2. If C_f is any capacitor in the filter, it can be easily shown that ideally

$$R_{FET}\, C_f = \frac{C_f\, h}{C_s\, f_R} \qquad (1)$$

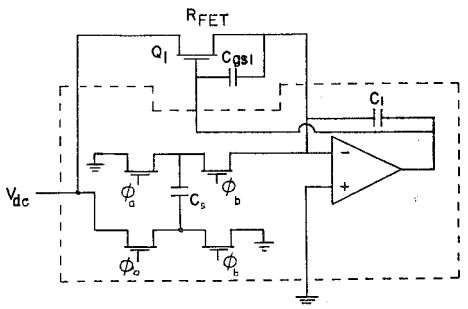

Fig. 2. Simple Pretune Circuit

where f_R is the frequency of the pretune clock and h is a temperature, time, and process invariant constant. The ability to accurately control the effective RC time constants of the filter using an external frequency reference is apparent from (1).

The lossy SR integrator of Fig. 3 is used here as a vehicle for evaluating the performance features and limitations of SR filters [5]. The circuit of Fig. 4 is used to pretune the MOSFET resistors.

It can be readily shown that the equivalent FET impedance is given by

$$R_{FET} = \frac{\theta}{C_s\, f_R} \qquad (2)$$

where θ is the duty cycle of the clock ϕ_c and f_R is the frequency of the clock on the switched capacitor. The frequency of the ϕ_c and f_R clocks are assumed identical. The duty cycle of ϕ_c, which can be accurately controlled, is used as a design variable to minimize area requirements for the pretune capacitor, C_s.

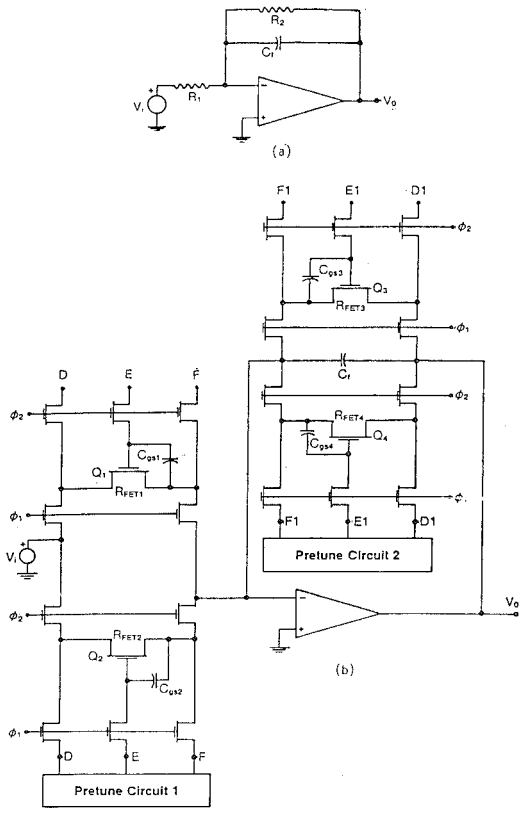

Fig. 3. Lossy SR Integrator; (a) continuous time structure, (b) SR equivalent

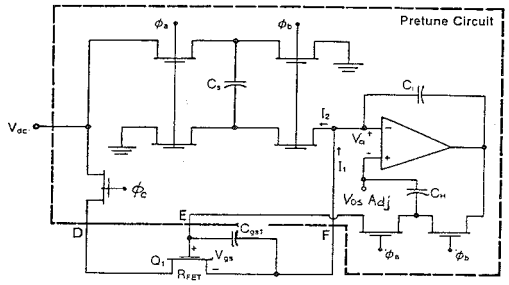

Fig. 4. Practical SC Pretune Circuit

Ideally the lossy integrator has a transfer function given by

$$I(s) = \frac{-R_2/R_1}{1+R_2C_f s} \qquad (3)$$

At high frequencies, the finite GB of the op amp will degrade the performance of the integrator. In order to separate associated performance deviations with the SR process itself from those attributable to the characteristics of the op amp, the op amp effects will be singled out. If the op amp is modeled with a single pole by the expression

$$A(s) = \frac{GB}{s} \qquad (4)$$

then the gain of the integrator is given by (assume $R_1=R_2=R$)

$$I_A(s) = \frac{1}{RC + 1\,\frac{s}{GB}\,(2+RC} \qquad (5)$$

4.0 Performance Evaluation

The structure of Fig. 3 and Fig. 4 can be used to investigate the effects of the pretune input voltage, ϕ_c duty cycle, bulk voltage, offset voltage, pretune frequency, and filter signal amplitude on dynamic range. In general, the affects of these designer controllable parameters on performance of the filter are determined by the parasitics in the circuit itself.

The test structure was sized for operation around 45 KHz (a 3dB cutoff frequency of 45 KHz) although operation at lower and higher frequencies is possible by changing the duty cycle of ϕ_c and/or the pretune clock frequency, f_R. Large changes from the nominal design value will cause deterioration in performance attributable due to a decrease in gate to source voltage.

A summary of the theoretical and experimental dc gain and 3dB cutoff frequency for this lossy integrator appears in Fig. 5 for several different

Test Conditions	Theoretical 3 dB Freq. (Ideal op amps)	Theoretical 3 dB Freq. (GB=1MHz)	Measured 3 dB Freq.	% Error in 3dB Freq. (Relative to Theoretical GB=1MHz case)	ERROR in DC Gain (in DB)
Vdc = 400mv fs= 1Hz f_c = 30KHz θ = 1/15	45KHz	43.03 KHz	42.8 KHz	-.5%	-0.17
Vdc = 600mv fs= 1Hz f_c = 30KHz θ = 1/15	45KHz	43.03 KHz	42.7 KHz	-.7%	-.022
Vdc = 800mv fs= 1Hz f_c = 30KHz θ = 1/15	45KHz	43.03 KHz	43.3 KHz	+.6%	-.016
Vdc = 400mv fs= 1Hz f_c = 20KHz θ = 1/15	30KHz	29.07 KHz	30.0 KHz	3%	.011
Vdc = 600mv fs= 1Hz f_c = 20KHz θ = 1/15	30KHz	29.07 KHz	30.2 KHz	3.3%	.013
Vdc = 800mv fs= 1Hz f_c = 20KHz θ = 1/15	30KHz	29.07 KHz	31.05 KHz	6.8%	-.005
Vdc = 100mv fs= 1Hz f_c = 60KHz θ = 1	6KHz	5.96 KHz	6.0 KHz	.7%	.135
Vdc = 300mv fs= 10Hz f_c = 60KHz θ = 1	6KHz	5.96 KHz	7.5 KHz	26%	-.056

Fig. 5. Experimental Performance of lossy SR integrator; fs is the resistor switch rate, fc the pretune clock frequency and θ the duty cycle of θ_c.

test conditions. The experimental results were obtained from a double poly NMOS die fabricated by Texas Instruments as part of a recent multiproject chip. The error percentages shown are with respect to that predicted with an op amp which has a bandwidth product of 1 MHz. The offset voltage of the op amps was manually nulled out in both the filter and pretune circuits prior to taking measurements. The sinusoidal input amplitude to the filter was maintained at 50 mv. Although the accuracy is not comparable with that currently attainable with switched capacitor techniques, the results do show promise. It must be emphasized that although the % deviation from ideal for the intended 45 KHz case is very favorable, it is

premature to claim this type of accuracy is characteristic of the SR technique. The measurements taken, however, do suggest that even if parasitic effects remain uncompensated, effective RC time constant accuracy of + or - 4 % appears to be practically attainable for reasonable signal levels. The sources of some of the performance deviations and methods to reduce their effects are discussed in the following section.

Sources of error can be split into two groups, those associated with the pretune circuit and those associated with the filter. The errors associated with the pretune circuit will be considered first. If the pretune voltage (V_{dc}) is large, the pretune circuit will not lock on the correct value of V_{gs}. The error is a result of the non-linear IV characteristics of the FET when biased in the ohmic region. When located the average charge transfered by R_{FET} is equal to the average charge transfered by C_s. The percent error in the drain current of R_{FET} is given by the expression:

$$\% \text{ error} = - \frac{2V_{os}/V_{DS}}{1+V_{os}/V_{DS}} \qquad (6)$$

The resulting error in R_{FET} will be of the same order of magnitude the For small values of V_{GS} and large values of V_{DS} the errors can become quite large.

The offset voltage (V_{os}) of the pretune op amp is another source of error. It can be shown that the error in ω_{3dB} due to V_{os} is given by

$$\% \text{ error} = \frac{V_{DS}}{2(V_{GS}-V_T)} \qquad (7)$$

Since well known schemes exist to null the offset voltage, the error due to V_{os} do not appear to be of major concern in SR filters.

The gate of the duty cycle switch (ϕ_c) has a parasitic capacitance from the gate to drain and source of the switch. Switch feedthrough will be more significant for the on-off transition than the off-on transition since C_{gs} is larger when the FET is active. The calculations to determine the magnitude of the error due to switch feedthrough have not been performed; however, experimental results suggest the error is small.

When R_{FET} is conducting and the switched capacitor in the pretune circuit is discharging, the voltage at the null port (V_a) of the pretune op amp is not zero. For low duty cycles the capacitor nearly completely discharges after R_{FET} stops conducting as the op amp output settles to its nominal value. An error in the pretune circuit is, however, introduced since the voltage across R_{FET} differs from the desired value, V_{dc}, by V_a. The time varying magnitude of V_a has not been determined. Preliminary calculations indicate the error in ω_{3D} due to V_a is of the same order of magnitude or less than the other sources of error mentioned above.

The errors associated with the filter circuit itself will now be considered. The FETs which switch R_{FET} between the pretune circuit and the filter have an on resistance of 500Ω. Since the switches are not ideal, all the switches will not have the same on resistance. The switch mismatch will create an error in R_{FET}, but a 20 % switch mismatch creates a ω_{3dB} error of less than .1 % for the circuit presented in this paper.

In active SR filters, the GB of the op amp will affect the frequency response of the filter. These effects become quite significant at high frequencies as can be seen from (5). At lower frequencies the effects become negligable.

The designer must avoid crossing clock and signal lines in the filter. In particular, no clock lines should cross the signal line at the null port of the op amp since this serves a charge summing node. The fundamental amplitude will not be affected but the THD of the signal will increase due to clock crossings.

5.0 Limitations

Although switched resistor filters are essentially continuous-time circuits, there are some limitations. The signal amplitude must be small in order to operate in the linear region. This limits the dynamic range.

The pretune circuit required approximately 1500 mil^2. If the pretune circuit is repeated for every resistor in a high-order active filter, the area required makes the filter impractical. However, one pretune circuit can be used for all of the resistors. This results in an area-efficient high-order filter.

While high frequency filters are possible using switched-resistor techniques, the op amp GB causes an error in the desired cutoff frequency. This will limit the range of cutoff frequencies for active SR filters. Passive SR filters, however, are applicable at higher frequencies.

Finally, the limitations in accuracy imposed by the parasitics discussed in the previous section must be considered. Clever design techniques, however, will likely reduce these parasitic effects.

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