ISCAS'84

A TEMPERATURE STABLE AND PROCESS COMPENSATED MOS ACTIVE FILTER

Mathew A. Rybicki
Motorola, Inc.
Austin, Texas

and

Randall L. Geiger
Texas A&M University
College Station, Texas

ABSTRACT

A new method of designing temperature stable and process compensated MOS active filters is discussed. An on-chip temperature transducer drives an analog-to-digital converter that digitally selects binary weighted resistors to compensate for temperature variations in an RC active filter. Laser trimming fine tunes the filter resistors to the desired values and compensates for process variations. Details about building these filters supported with experimental results of a fabricated NMOS bandpass filter are discussed.

INTRODUCTION

Extensive research has been performed in the area of MOS active filter design to desensitize the filter characteristics from temperature and process variations. Some of the more successful techniques include; switched-capacitor [1], switch-resistor [2], CCD [3] and master-slave [4] approaches. Each has its advantages and disadvantages, however, none of these are simultaneously compensated for both temperature and process variations. The method presented in this paper compensates for paracitic capacitances and resistances along with temperature and process variations of the passive components and op-amp gain-bandwidth product (GB) in an active filter.

COMPENSATION TECHNIQUE

The technique presented here compensates the frequency response parameters of an MOS RC active filter structure by laser trimming the passive components in a temperature controlled compensation scheme. This temperature and process compensation technique employs the three stages shown in the block diagram of Figure 1. The temperature transducer produces an output voltage proportional to the die temperature. This D.C. control voltage is converted to a binary signal through the analog-to-digital converter (ADC) which digitally selects binary valued resistances in series connected resistor and switch strings. These binary selectable resistors replace judiciously chosen filter resistors that directly control the frequency response parameters of the filter being compensated. Once fabricated, the temperature transducer, binary resistors and compensated filter are functionally laser trimmed at various temperatures to obtain the desired performance.

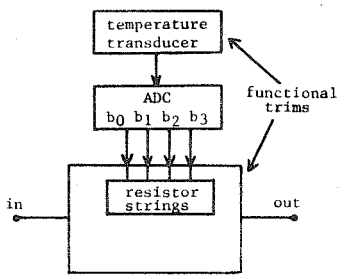

Figure 1 - Block diagram illustrating the temperature and process compensation scheme.

The compensation accuracy of this scheme over temperature is dependent upon the % change in the parameter of interest over the desired temperature range and the number of bits in the ADC. Assuming no errors are associated with either the temperature sensor or ADC and that the parameter of interest, P, varies linearly with temperature by ΔP over the temperature range of interest, then the % deviation in P from ideal over the temperature range is bounded by:

$$\pm \frac{\Delta P}{P} \times \frac{1}{2^{n+1}} \times 100\% = \text{maximum possible deviation in percent}$$

where n is the number of bits in the ADC.

A second-order bandpass active filter, fabricated with a double-poly NMOS process and trimmed with an Electro Scientific Industries (ESI) Nd:YAG Q-switched laser, is used here to demonstrate the above temperature and process compensation scheme.

Temperature Transducer

A temperature transducer is needed to sense die temperature. The experimental temperature transducer is broken into two sections: 1) the temperature sensor which generates a voltage that varies linearly with die temperature and 2) the transducer amplifier which provides for laser trimmable gain and offset. The following sections describe the temperature sensor and laser trimmable transducer amplifier.

Temperature Sensor. Two basic mechanisms are available in the MOS technology for sensing temperature. They are the temperature variations of both polysilicon resistance and MOS threshold voltage. The variation of polysilicon resistance with temperature is positive and somewhat linear though it displays some second-order effects. The variation of the MOS threshold voltage (V_T) with temperature is negative and offers increased linearity [5]-[8]. A V_T temperature reference was used in this work.

CH1993-5/84-0000-0940 $1.00

The V_T temperature dependence (slope of V_T vs. temperature) was about -1.1mv/°C for the process used to fabricate the test vehicle. Experimental data obtained from a 1mil/1mil enhancement transistor over the 5°C to 125°C range is shown in Figure 2. The V_T dependence on temperature

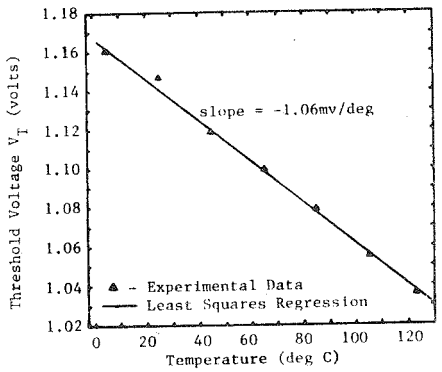

Figure 2 - Threshold voltage (V_T) vs. temperature for a 1mil/1mil enhancement transistor.

can be expressed as:

$$V_T(T) = V_{TR} + \alpha(T - T_R)$$

where V_{TR} is the value of the threshold voltage at the reference temperature T_R, and α is the temperature coefficient of $V_T(T)$ in mv/°C.

A temperature sensor that generates a voltage (V_R) that is linearly dependent on temperature is shown in Figure 3. The two enhancement transistors

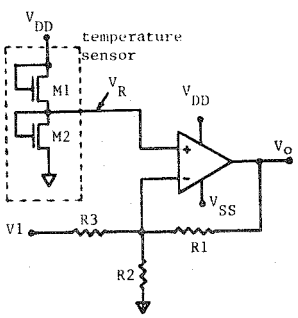

Figure 3 - MOS temperature transducer including; 1) temperature sensor 2) laser trimmable transducer amplifier

that make up the temperature sensor are kept in saturation by tying gates and drains together. By setting the currents in the two devices equal, it follows from Sah's equation that:

$$V_R = \frac{SV_{DD} - SV_{T1} + V_{T2}}{S + 1} \quad (1)$$

$$\simeq SV_{DD} + V_{T2} \quad (2)$$

where: $S = (W1L2/W2L1)^{1/2} << 1$

and V_{T1} and V_{T2} are the enhancement threshold voltages for M1 and M2 respectively. Note that V_R is approximately linear with V_{T2}, and since V_{T2} is linearly dependent on temperature, V_R is nearly linearly dependent on temperature. The threshold voltage (V_T) and its temperature dependence discussed above are strongly process dependent creating wide variations in the D.C. bias value and temperature slope for the transducer of Figure 3. It was necessary to devise a post processing scheme to adjust for these variations and to buffer the V_R node since it has limited current drive capability.

Laser Trimming. Three laser trimming techniques are available for trimming the passive components. Fine trims are accomplished by laser annealing polysilicon resistors with low-power laser pulses which decrease resistance by increasing grain size [9]-[10]. With high-power laser blasts metal or polisilicon links can be severed with the laser or portions of resistors or capacitors can be removed to change component values. A third technique, still under developement, fuses two layers of polysilicon with high power laser pulses to short capacitor plates or portions of resistors. This technique can be used for both course and fine trims. If two of these techniques are combined, up-down trims of a single component can be achieved.

Transducer Amplifier. An amplifier with laser trimmable gain and offset was designed to adjust for process variations and provide tunable output swings. The complete circuit is shown in Figure 3. Assuming an ideal amplifier and solving nodal equations, an equation for the output voltage, which is a function of V_R and thus of temperature, is obtained.

$$Vo = V_R(1 + R1/R3 + R1/R2) - V1(R1/R3) \quad (3)$$

$$\simeq (R1/R3)(V_R(1 + R3/R2) - V1) \quad (4)$$

for: R1 >> R3

By laser trimming R2 (to increase offset) or R3 (to decrease offset) the offset of the output (Vo) can be zeroed at the mid-point of the two temperature extremes. Annealing R1 reduces the gain so the desired Vo vs. temperature curve is achieved.

Analog-to-Digital Converter

Since thermal time constants are generally very long, speed of the ADC is not of major concern. However, the number of bits are of concern since they determine the precision of the compensated active filter. Numerous economical techniques are available for designing the ADC in an area efficient manner. However, a flash 4-bit ADC was used in this design because it was readily available and its characteristics were well known.

It should be noted that the temperature transducer TVC and ADC blocks are not dependent upon filter topologies. A well designed and tested pair can be stored in a data-base and placed when needed on the circuit layout.

Compensated Resistors

The temperature compensation scheme presented here revolves around the idea of adjusting the value of a resistor that directly controls the

center frequency (f_o). Temperature changes in the center frequency can be directly compensated by adjusting this controlling resistor as temperature varies. This idea is demonstrated in Figure 4. The total resistance RT is broken into

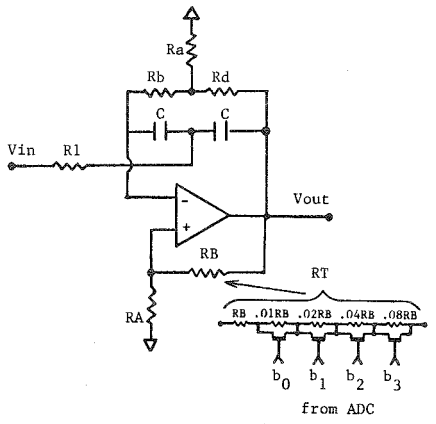

Figure 4 Temperature compensation applied to a second-order bandpass active filter.

five smaller resistors, four which can be shorted by switches. The resistors are binary weighted such that:

$$RT = RB + 0.01RBb_0 + 0.02RBb_1 + 0.04RBb_2 + 0.08RBb_3$$

This allows a 15% increase in RT over RB with a 1% of RB resolution by simply shorting or opening the switches across the resistors. For a linear variation in RT, each switch should have an "ON" resistance that is a fixed percentage smaller than the resistor in parallel with it. This percentage should be identical for all switches. This resistor string was used to replace the filter resistor that controls f_o.

RC Active Filter

For the purpose of demostrating the laser trimmable compensation technique, the SAB second-order band-pass filter in Figure 4 was used. Process and temperature compensation of the filter center frequency was performed to demonstrate the effectiveness of this technique. The expressions for the transfer function (Vout/Vin) and the center frequency (w_o) of the filter are as follows:

$$\text{Vout/Vin} = \frac{s/CR1(h-1)}{s^2 + \frac{s}{C}[2/R2 + h/(h-1)R1] + 1/R1R2C} \quad (5)$$

$$w_o = \frac{1}{C(R1R2)^{1/2}} \quad (6)$$

where R2 and h are given in equations (7) through (10) below and the op amp d.c. gain and GB are assumed to be infinite.

$$R2 = \frac{Rb(h-1)}{h-k} \quad (7)$$

$$\text{where: } h = \frac{RA}{RA + RB} \quad (8)$$

$$k = (1/Rd + h/Rb)RT \quad (9)$$

$$RT = \frac{1}{1/RA + 1/Rb + 1/Rd} \quad (10)$$

Resistor RB was chosen for compensation since it had a positive sensitivity with respect to w_o of approximately 3/2 for the component values chosen to set the nominal center frequency at 13khz. This allows for full compensation of w_o over a 100°C temperature range. The size of resistor RB is such that the internal binary resistors are large in comparison to the "ON" resistance of the parallel switches.

Computer simulations revealed that f_o varied from approximately 14khz to 12khz over a 100°C temperature range. For an RB variation of approximately 15% (all 16 combinations of the 4-bit binary signal) and a fixed temperature of 50°C, the center frequency varied from approximately 12khz to 14khz. Thus, by superposition, a full variation in RB, should provide compensation of w_o over a 100°C temperature range.

EXPERIMENTAL RESULTS

The filter and compensation scheme were fabricated using a double-poly NMOS process and laser trimmed using a hot/cold chuck mounted upon an Electro Scientific Industries Q-switched Nd:YAG laser trimming system of 0.53 microns laser light wavelength (green). A microphotogragh of the fabricated die is shown in Figure 5. A compensation

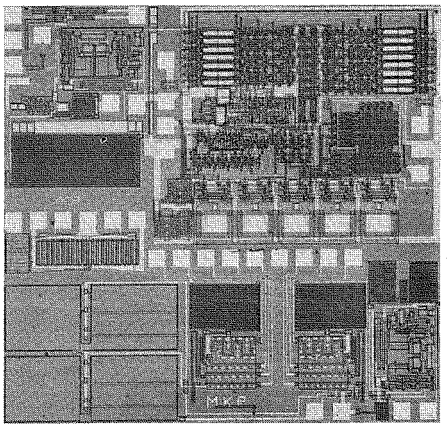

Figure 5 - Microphotograph of fabricated die with: the temperature transducer (upper left), ADC (upper right), and filter (bottom)

temperature range of 10°C to 90°C was chosen since the ADC was found to fail beyond these temperatures.

The circuit was laser trimmed over the desired 10°C to 90°C temperature range. The temperature was initially set to 50°C with the input voltage range of the ADC set to ±2 volts. The resistance of R3 of the temperature transducer was reduced 8% (approximately 25% of the resistor was trimmed) to adjust the output offset to a slight overtrimmed value of 200mv. This voltage generated a binary 8 (1000) at the output of the ADC. At this time, the resistance of R1 of the filter was reduced by 10%

(approximately 30% of the resistor was trimmed) to set the filter center frequency at 12.92khz. (The definition of center frequency used here is; that frequency at which the magnitude of the gain is a maximum.) This value was chosen so that the nominal center frequency would be 13khz. The temperature was then increased to 80°C. Resistor R1 of the temperature transducer was trimmed until the transducer output forced the ADC binary signal to fully compensate f_o to 13khz.

The resulting temperature transducer output and center frequency vs. temperature plots, for this post-trimmed filter, are shown in Figure 6 and 7. The dotted line in Figure 6 is the actual

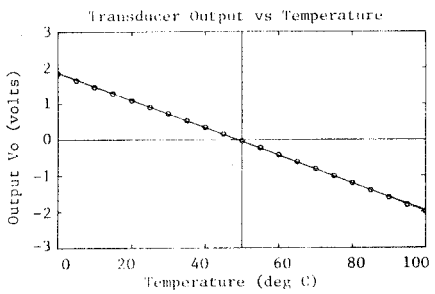

Figure 6 - Output voltage (Vo) vs. temperature for the NMOS temperature transducer after laser annealing

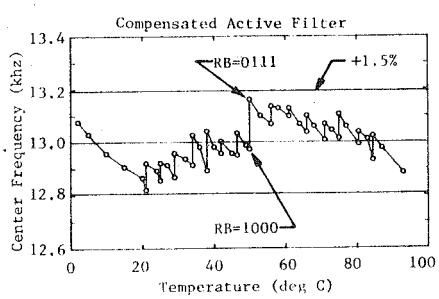

Figure 7 - Experimental post-trimmed f_o vs. temperature plot for the active filter

measured curve and the solid line is a least-squares linear regression fit to the experimental data points. The experimental circuit exhibits a deviation from linear of less than ±0.74% over the entire 4 volt operating range with a small offset error of 30mv at 50°C.

All values of f_o fall within ±1.5% of 13khz over a 10°C to 90°C temperature range. The curve is somewhat "bowed" with some differences in f_o at the ADC trip points being greater than others. This can be attributed to mismatches in the binary resistor ratios and inaccurate sizing of switches.

CONCLUSIONS

A second-order band-pass filter has been successfully laser trimmed and compensated against process and temperature variations. The filter exhibits a center frequency of 13khz ±1.5% (compared to ±0.5% ideally) over a temperature range of 10°C to 90°C. Laser annealing of polysilicon resistors adjusted the filter to the desired center frequency at two temperatures. The main errors in the filter center frequency were due to switch "ON" resistances and resistor mismatches that were assumed negligable during design.

The heart of the compensation scheme, an on chip temperature transducer with laser trimmable gain and offset, was laser trimmed to a ±2 volt swing and zero volt offset. The transducer sensed temperature through the linear variation of the MOS threshold voltage with temperature. A linearity of better than ±0.74% over full scale was achieved.

The functional trims were performed in two steps at two temperatures using an Electro Scientific Industries model-44 laser trimming system. The laser was equiped with a computer driven controller and 0.53 micron wavelength, Q-switch, Nd:YAG laser. Laser annealing was used for all trims in this research, however, a much wider trim range was possible through link cutting and link fusing.

REFERENCES

[1] P.E. Allen and E. Sanchez-Sinencio, Switched-Capacitor Circuits, Van Rostrand Reinhold Co. Inc., New York, N.Y., Jan. 1983.

[2] R.L. Geiger, P.E. Allen and D.T. Ngo, "Switched-Resistor Filters - A Continuous Time Approach to Monolithic MOS Filter Design", IEEE Transactions on Circuits and Systems, vol. CAS-29, No. 5, May 1982.

[3] H.J. Whitehouse, "Signal Processing with Charge Transfer Devices", IEEE Transactions on Electron Devices, vol. ED-23, No.2, Feb. 1976, pp.132-133.

[4] K. Rao, V. Sethuraman and P. Neclakantan, "A Novel Follow the Master Filter", Proceedings IEEE, vol. 65, pp.1725-1726, Dec. 1977.

[5] R. Wang, J. Dunkley, T.A. DeMassa and L.F. Jelsma, "Threshold Voltage Variations with Temperature in MOS Transistors", IEEE Transactions on Electron Devices, June 1971, pp.386-388.

[6] B. Song, P.R. Gray, "Threshold-Voltage Temperature Drift in Ion-Implanted MOS Transistors", IEEE Journal of Solid-State Circuits, vol. SC-17, No.2, April 1982, pp.291-298.

[7] R.A. Blauschild, P.A. Tucci, R.S. Muller and R.G. Meyer, "A New NMOS Temperature-Stable Voltage Reference", IEEE Journal of Solid-State Circuits, vol. SC-13, No. 6, December 1978, pp. 767-773.

[8] F.P. Heiman and H.S. Miiller, "Temperature Dependence of n-Type MOS Transistors", IEEE Transactions on Electron Devices, March 1965, pp.142-148.

[9] W.F. Tseng and J.W. Mayer, "Grain Size Dependence in a Self-Implanted Silicon Layer on Laser Irradiation Energy Density", Appl. Phys. Lett., vol 32, No.12, pp.824-826, 15 June 1978.

[10] N.C.C. Lu, L. Gerzberg and J.D. Meindl, "A Quantitative Model of the Effect of Grain Size on the Resistivity of Polycrystalline Silicon Resistors", IEEE Electron Device Letters, vol. EDL-1, No.3, pp.38-41, March 1980.