TRADEOFFS BETWEEN PASSIVE SENSITIVITY, OUTPUT

VOLTAGE SWING AND TOTAL CAPACITANCE IN SC FILTERS

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ABSTRACT

Design guidelines for SC filters taking into consideration passive sensitivity, output voltage swing and total capacitance area are described. In this paper, we discuss the tradeoffs between these three parameters. A popular SC topology with additional positive feedback is used to illustrate the tradeoffs involved in the design of SC filters.

I. INTRODUCTION

A number of SC filters have been published which realize general biquadratic transfer functions [1]-[4]. In particular, SC topologies that have partial positive feedback are capable of significantly reducing the total capacitance [5], [6]. However, attempts to minimize total capacitance in filter structures are often accompanied by an increase in Q sensitivity and/or a reduction in the corresponding output voltage swing of the op amps. Conversely, when the designer only concentrates on minimizing the sensitivities large capacitor areas typically result.

In this paper, we show the tradeoffs between total capacitance and Q sensitivities for a certain output voltage swing of the op amps. Using information presented here the designer can specify the maximum Q sensitivity value permitted and obtain the minimum total capacitance, $C_{\rm T}$, under certain op amp output voltage swing conditions, or vice versa the designer can specify the op amp output voltage swing $C_{_{\mathbf{T}}}$, and determine the resultant Q sensitivity.

II. SECOND-ORDER FILTER WITH POSITIVE FEEDBACK

Figure 1 shows a popular general SC filter structure which includes a local positive feedback loop [5]-[6]. This filter, without the positive feedback capacitor b_oC reduces to the popular Fcircuit reported by Fleisher and Laker [3]. We focus attention here on the positive feedback and the effects of b₂C on the pole frequency and polequality factor, Q, sensitivities.

III. DESIGN AND POLE EQUATIONS

The loop equation defining the pole locations for the circuit of Figure 1 is given by

$$D(z) = 1 - z^{-1}(2+b_1+b_2-a_1a_2)/(1+b_1)+z^{-2}(1+b_2)/(1+b_1).$$

From this equation we can identify (2)

$$r^2 = \frac{1 + b_2}{1 + b_1}$$

and

$$2r\cos\theta = \frac{2+b_1+b_2-a_1a_2}{1+b_1}$$
 (3)

This work was supported, in part, by the Organization of American State (PIT/EE/OEA/81/1670).

where r and θ correspond to the pole radius and angle respectively.

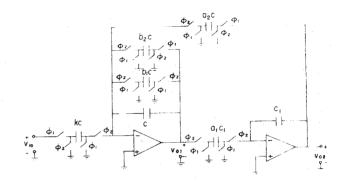


Figure 1. A popular switched-capacitor filter

Assuming r and θ are given. The following algorithmic design strategy can be used.

Solving (2) we obtain the expression

$$b_1 = (1+b_2-r^2)/r^2 (4)$$

$$a_2 a_1 = \frac{1+b}{r^2} 2 (1+r^2-2r\cos\theta).$$
 (5)

It can be seen that \mathbf{b}_2 is a design parameter that can be used to judiciously 2 tailor either sensitivity or total capacitance. Since only the a,a, product is fixed, the designer also has flexibility in specifying one of these parameters. Next, in order to relate the s- and z-plane, we arbitrarily use for purposes of example the impulse invariant response[1] to derive the sensitivity expressions. It can be shown [1] that

 $f_0 = \frac{fs}{2\pi} [\theta + \ln^2 r]^{\frac{1}{2}}$ (6)

and

$$Q = -\frac{2\pi fo}{f \sin^2 2}$$
 (7)

where f is the sampling (clock) frequency and f is the center (cutoff) frequency.

If p is any capacitor ratio in the circuit of

Figure 1, it follows from (2), (6) and (7) that
$$S_{p}^{f} \circ = \left(\frac{f}{\omega}\right)^{2} \left[\ln r + \theta / \tan \theta S_{p}^{r}\right] - V \tag{8}$$

where $V = (\theta/\tan\theta) S_n^{2r\cos\theta}$

$$S_{p}^{Q} = \left(\frac{f_{s}}{\omega_{o}}\right)^{2} \left[\frac{-\theta^{2} + \theta(\ln r)/\tan\theta}{2 \ln r}\right] S_{p}^{r^{2}} - V$$
 (9)

The sensitivities of $2r\cos\theta$ and r^2 that appear in these expressions can be obtained from (2) and (3).

IV. PRACTICAL DESIGN CONSIDERATIONS

There is a tradeoff, in designing SC filters, between the total capacitance $\mathbf{C}_{_{\mathbf{T}}}$, Q sensitivity and the op amp output voltage swings. It is particularly important to consider these tradeoffs in SC filter topologies which involve both positive and negative feedback. The tradeoffs for the circuit of Figure 1 are illustrated in Table 1 in terms of the sensitivity measure

$$S_{\text{average}} = \frac{1}{2} \left(\left| S_{b_1}^Q \right| + \left| S_{b_2}^Q \right| \right)$$
 (10)

for a particular set of design specifications i.e., $f_{O/S} = 1/50$ and Q = 10. Two cases are simultaneou-

sly considered for comparison purposes. In one case the op amp outputs are unbalanced, that is $\rm V_{o2}$ is fixed to OdB and $\rm V_{o1}$ is variable. In the other case both outputs are scaled (by the choice of the parameter $\rm a_1)$ to OdB. $\rm C_{TU}$ and $\rm C_{TB}$ are the total capacitances for the unbalanced and balanced outputs, respectively.

b ₂	V ₀₁ (dB)	Saverage	c _{TU}	c _{TB}	
0	.02726	0.49844	114.91	114.97	
.025	.1345	2.42720	81.214	81.416	
.05	.23916	4.2641	54.725	55.013	
.1	.44119	7.6875	41.953	42.416	
.2	.81907	13.678	49.252	46.369	
.4	1.4885	23.09	83.28	72.793	
.8	2.5800	35.64	162.76	125.0	

Table 1. Balanced and unbalanced outputs versus $Q \ \text{sensitivity and } C_T, \ \text{with } V_{O_2} = 0 \text{dB}.$

The tradeoff between C $_{\rm T}$ and Q sensitivity for balanced op amp outputs will now be considered. The total capacitance C $_{\rm T}$ can be expressed as [3]:

$$C_{T} = [(a_{2}C+b_{2}C+b_{1}C+kC+C) / C_{min1}]$$

$$+[(a_{1}C+C_{1}) / C_{min2}] Cu,$$
(11)

where ${\rm C_{min1}}$ and ${\rm C_{min2}}$ are the smallest capacitors in the sets{C, kC, b₁C, b₂C, a₂C}and{C₁, a₁C1} respectively. Since the variable a₁ has been used to obtain balanced outputs, it follows from (4) and (5) that ${\rm C_T}$ is actually only a function of the single variable b₂. The nonlinear nature of ${\rm C_T}$ in terms of b₂ is illustrated in Figure 2 for a family of different f_s/f_o and a fixed Q = 10.

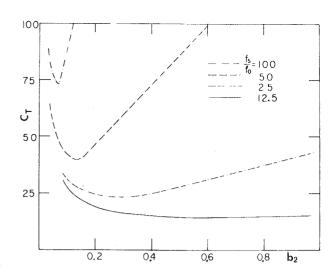


Fig. 2. Total capacitance versus the capacitor ratio ${\rm b_2}$ for a fixed Q=10, and different ${\rm f_0/f_S}$ values.

Two practical solutions are now considered.

i) Figure 2 3 illustrates the compromise between the total capacitance $^{\rm C}$ C, and $^{\rm S}$ average for a family of $^{\rm f}$ o/ $^{\rm f}$ s values. Note that for this plot Q is fixed, in this case Q = 10. Another set of curves can be easily generated for any desired Q value. These curves can be used to obtain the tradeoff between the $^{\rm C}$ C and $^{\rm S}$ s average for a given $^{\rm f}$ o/ $^{\rm f}$ s value. These curves also can be used to obtain the minimum $^{\rm C}$ C for a given maximum permissible sensitivity value or a minimum sensitivity for a given total capacitance.

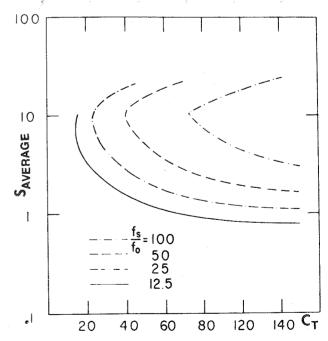


Fig. 3. Average Q sensitivity versus total capacitance for a fixed Q=10, and different f_0/f_s values

² Figs. 3 and 4 already include the scaling of both op amp outputs for V₀₁=V₀°

 $^{^{}l}\text{We do not present results on }\mathbf{S}_{p}^{f}\text{o}$ since they are around 0.5, therefore not critical

ii) For a given value of Q, we can determine the compromise between S average and C . This is shown in Figure 4 for a family of Q values and a fixed ratio of $f_{\rm o}/f_{\rm s}=1/10$. In either case considered, once the desired operating point is determined the required value of b can be obtained from Figure 2. It is important to emphasize that in Figures 2, 3, and 4, C is bi-valued and the value of S average is not unique. b should be chosen to render the minimum S average

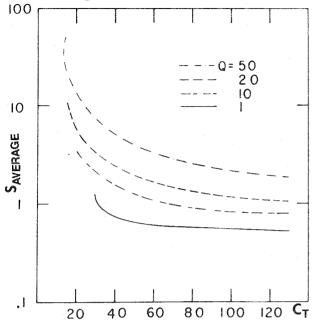


Fig. 4. Average Q sensitivity versus total capacitance for a fixed $f_{o}/f_{s} = 1/10$, and different Q values.

V. EXAMPLES

The following examples illustrate the use of Figures 2, 3, and 4. First, assume the design specifications are $\rm f_o/f_s$ = 1/50, Q = 10 and a center frequency gain of OdB and that the maximum S average

is 11. The problem is to determine C_T and the value of b_2 to satisfy the above conditions. By using Figure 3, we find that C_T = 40 Cu, $b_2 \in \{0.12, 0.15\}$.

Additional flexibility is available through the parameter a_1 if the requirement of unbalanced op amp outputs is relaxed. This is illustrated in Table 2, where the case of no positive feedback, $b_2 = 0.12$, yields a smaller $S_{\rm average}$ than the case of $b_2 = 0.15$. For a very small $S_{\rm average}$, i.e., when $b_2 = 0$, the total capacitance increases by nearly a factor of 3.

	Output	V _{o2} (dBs)	b ₁ .	a ₁	a ₂	k	c _T	Saverage
b ₂ = 0	Unbalanced	.02726	.01264	.12598	.12598	.20147	114.91	0.4981
	Balanced	0	.01264	.12558	.12638	.20147	114.97	
b ₂ = .12	Unbalanced	. 15944	.13416	.13332	.13332	2.3893	39.95	8.9712
	Balanced	0	.13416	.12556	.14154	2.3893	40.504	
b ₂ * .15	Unbalanced	.63424	.16454	.13509	.13509	3.008	41.40	10.813
	Balanced	0	.16454	.12558	.14533	3.008	39.712	

Table 2. C_T and Q sensitivities for example 1).

Consider for the second example the design specifications f $_{\rm o}/{\rm f}_{\rm s}$ = 1/25, Q = 10 and a center frequency peak gain of OdB. Assume that the maximum permitted value of ${\rm C}_{\rm T}$ is 40 Cu. The problem is to determine S $_{\rm average}$ and b $_{\rm f}$ for the above data. By

using Figure 4, the corresponding value of S average

becomes 2.9. Then b_2 ϵ {0.07, 0.90} from Figure 2. The smallest b_2 gives the smallest $S_{average}$ of the two choices. Table 3 describes all the component values for the balanced and unbalanced output cases. The particular case of b_2 = 0 is included in the Table. It is observed in the latter case that $S_{average}$ is reduced by a factor of about 6, however the total capacitance is increased by nearly a factor of 2.

		V _{o2} (dBs)	b ₁ .	a _l	a ₂	k	c _T	Saverage
b ₂ = 0	Unbalanced	.054683	.025451	.25225	.25225	.2008	63.056	.4969
	Balanced	0	.025451	.25067	.25384	.2008	63.143	
b ₂ = .07	Unbalanced	.34852	.097233	.26093	.26093	.81472	36.87	3.0675
	Balanced	0	.097233	.25067	.27161	.81472	37.183	

Table 3. ${\rm C}_{\overline{1}}$ and ${\rm Q}$ sensitivities for example 2).

VI. CONCLUSIONS

We have presented design guidelines that consider the tradeoffs between the op amp voltage swings, Q sensitivity and total capacitance. We illustrated the approach using plots for certain particular design specifications. It can be seen that the advantage of using positive feedback is the reduced capacitance area at the expense of increased Q sensitivity. General equations are given which are suitable for any desired design specification.

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