CMOS OTA STRUCTURES WITH IMPROVED LINEARITY

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ABSTRACT

Methods of designing OTAs with improved common-mode and differential-mode input characteristics are discussed. Performance comparisons of new designs with conventional source-coupled differential input stages are made. These structures are shown to be useful for voltage controlled and monolithic designs. Characteristics of a filter structure using the new OTAs are investigated.

INTRODUCTION

The operational transconductance amplifier (OTA) has recently received increased attention for use as an active device in continuous-time filter structures [1],[2]. This interest is due in part to the reduced filter complexity, voltage control capabilities, potential applications in continuous-time monolithic filter structures, and potential uses at high frequencies.

Most existing OTA structures suffer from severe nonlinear distortion unless the differential input voltage is restricted to very low levels. The input voltage restriction has limited the dynamic range of ensuing circuit structures, and limited the development of OTA applications in the literature.

The input voltage restriction of existing OTA structures is inherently associated with the use of a conventional source-coupled (emitter-coupled in bipolar technology) differential amplifier as the input stage. Some work on improving the linearity of the input stage has been recently reported in the literature [1],[2]. A simple means of improving the source-coupled differential input stage by using source degradation is presented here. Although this discussion is limited to MOS structures, similar improvements in bipolar OTAs using the corresponding emitter degradation can be attained.

The performance of the new OTA is then discussed. The use of the OTA in a simple continuous-time biquad filter structure is investigated. Results of a computer simulation of a monolithic CMOS version of this filter which predicts less than 1% THD for 7.8 Vpp inputs to the filter (biased with +/- 5 volt supplies) are presented.

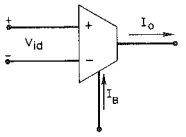

Fig.1 - OTA model

OTA MODEL

The symbol of an OTA is shown in Fig. 1. An ideal OTA has infinite input and output impedances, and is characterized by a transconductance parameter, Gm = Io/Vid , which should remain valid over a large range of input voltages.

OTA DESIGN

A block diagram of a typical OTA structure is shown in Fig. 2. A conventional source-coupled differential amplifier which is typically used as the first stage of a OTA is shown in Fig. 3. M1 and M2 are geometrically identical with channel widths and lengths of W and L respectively. It is further assumed that both devices are operating in the saturation region , and are modeled by the standard saturation region expression:

$$I_d = \frac{K'W}{L}(Vgs - V_T)^2 \tag{1}$$

It follows [3] that an upper bound on the differential input voltage occurs when all of the bias current (Iss) is directed to one of the two input transistors by the differential input voltage , Vid = V2-V1. This corresponds to a maximum differential input voltage of:

$$Vid_{max} = \pm 2\sqrt{\frac{I_{SS}L}{2K'W}} \tag{2}$$

It has been reported [3] that this typically varies from 300mV to several

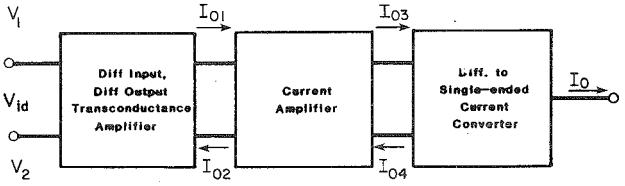

Fig.2 - Block diagram of an OTA

volts. However, if reasonably good linearity in the transconductance gain is required, the maximum differential input voltage is considerably less than predicted by (2). A routine analysis of the diff amp of Fig. 3 using the saturation region model of (1) yields the following expression for the differential output current , $\Delta Io = Io2 - Io1$:

$$\Delta I_o = \frac{-K'W}{L} Vid\sqrt{\frac{2I_{SS}L}{K'W} - Vid^2} \tag{3}$$

which for small V1 and V2 reduces to (4).

$$\Delta I_o = -Vid\sqrt{\frac{2K'WI_{SS}}{L}} \tag{4}$$

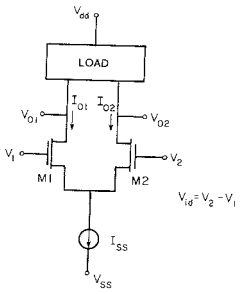

Fig.3 - Source-coupled diff amp

The transconductance gain of this differential input, differential output differential amplifier is thus approximated by:

$$g_m = \frac{\Delta Io}{Vid} = 2\sqrt{\frac{K'W I_{SS}}{2L}} \qquad (5)$$

Eq. (3) is plotted in Fig. 4 for the process parameters listed in Table 1 for Iss = 30 uA , W = 20u , and L = 5u. The nonlinearity in the transfer characteristics is apparent. A SPICE2 simulation for the same circuit which includes channel modulation effects (λ = .01 and Vd1=Vd2=5 volts) gives data which appears essentially coincident on the axis chosen (maximum error $\leq$ 2% of full scale). If we define the 1% linear range to be the range of input voltages where the output differs by at most 1% from the tangent to the transconductance curve at Vin=0 ; then it follows that to remain within the 1% linear range, the input (Vin) must be restricted to +/- 131 mV (λ = 0). This is significantly lower than the upper bound (1118 mV) given by (2). Both of these values, however, are considerably better than the ranges specified for the commercial bipolar OTAs. The linear input range for bipolar OTAs is in the vicinity of +/- 30 mV [4]. Resistive attenuators of approximately 500:1 are advised to reduce the input to acceptable levels with commercial OTAs such as the LM13600, with a subsequent 54 dB loss in dynamic range !

The differential input stage of Fig. 3 is incorporated into a simple OTA in Fig. 5 [5]. The Iss bias generator for the differential amplifier consists of MOSFET MI biased to operate in the saturation region. The drain currents (Io1 and Io2) are used to drive balanced loads ML1 and ML2. ML1 and ML2 serve as inputs to separate current mirrors which ultimately mirror the currents to MD2 and MS2 respectively. The difference in the drain currents of the two output transistors becomes the single-ended output current (Io). Thus from (3) and the gains of the current mirrors (neglecting λ effects), the output current of the OTA of Fig. 5 is given by (6) when the current mirror gain from ML1-MD2 is equal to the mirror gain from ML2-MS2.

$$Io = K'(\frac{W}{L})_{M1} Vid \sqrt{\frac{2I_{SS}}{K'}(\frac{L}{W})_{M1} - Vid^2}\ (\frac{W}{L})_{MS2}(\frac{W}{L})_{ML2} \qquad (6)$$

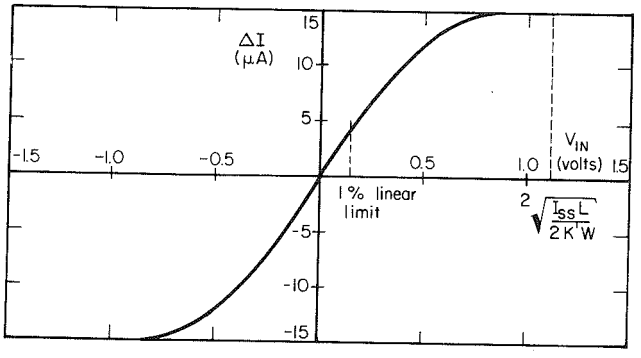

Fig.4 - Diff amp dc transfer curve

And for small input signals, the differential transconductance gain is given by:

$$G_M = \frac{Io}{Vid} = K'(\frac{W}{L})_{M1}\sqrt{\frac{2I_{SS}}{K'}(\frac{L}{W})_{M1} - V_{id}^2}\ \ (\frac{W}{L})_{MS2}(\frac{W}{L})_{ML2} \qquad (7)$$

The limits on the differential-mode (DM) input of the OTA are essentially determined by the characteristics of the diff amp which has been previously described. The maximum and minimum common-mode (CM) input voltages are determined by MI and the ML1-ML2 combination respectively. For the bias voltages, device sizes, and process parameters used in the design of the OTA of Fig. 5, the maximum symmetric CM input voltage limit about V1=V2=0 volts is determined by MI. As the common-mode excitation (VCM=V1=V2) increases, Vds(MI) decreases to Vds,sat(MI) causing MI to enter the ohmic region, and thereby causing a serious degradation of MI's output impedance.

$$V_{CM} = V_{dd} - |V_{Tp}| - \sqrt{\frac{I_{SS}}{2K'}(\frac{L}{W})_{M1}} - \sqrt{\frac{I_{SS}}{K'}(\frac{L}{W})_{MI}} \qquad (8)$$

It can be readily shown that the maximum CM input voltage allowable to maintain saturated operation of MI is given by (8).

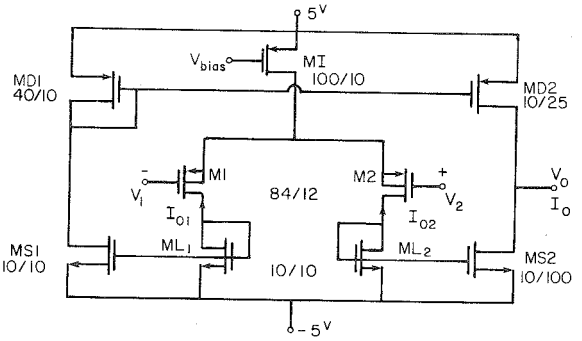

Fig.5 - Simple OTA design

IMPROVED OTA DESIGN

A good OTA should have good common-mode and differential-mode input voltage ranges, high input and output impedances, and low common-mode transconductance gain. An additional constraint is imposed on audio frequency OTA-based monolithic active filter structures due to the low capacitance density of monolithic capacitors. Since large C/gm ratios are required for audio frequency applications, and since C is bounded by practical silicon area constraints, it is necessary to design structures with low transconductance gain (Gm).

Improvements in DM range as well as reductions in gain (Gm) can be obtained by adding source degradation loads to the differential input stage. To avoid consuming excessive silicon area, the use of active loads must be considered for most standard processes. The effects of device nonlinearities are of major concern with active loads

Table 1 - Process/SPICE2 Parameters

Device Type:		n ch.-enh	n ch.-depl	p ch.-enh
Parameter				
K '	(μA/V^2)	12.0	12.0	3.0
V_{To}	(V)	.80	-3.4	-.60
λ	(V^{-1})	.01	.01	.01
γ	($\sqrt{V}$)	.55	.55	.70
ϕ	(V)	.60	.60	.60
LD	(μ)	.75	.75	.75

since the large signal I-V characteristics of the MOSFET are far from linear.

Consider the general active load shown in Fig. 6a. and assume that the current (I) is a function of the voltage (V) independent of Va and Vb - which can be expressed in a power series as:

$$I = \sum_{i=1}^{\infty} a_i V^i \tag{9}$$

If two identical devices are connected in an inverted-parallel structure as shown in Fig. 6b, it follows that:

$$I = I_1 - I_2 = \sum_{i=1}^{\infty} (a_i V_1^i - a_i V_2^i)$$

$$I = \sum_{i=1}^{\infty} a_i V_1^i [1 - (-1)^i] = 2\sum_{i=1}^{\infty} a_{2n-1} V_1^{2n-1} \tag{10}$$

and thus that all even powers have been cancelled.

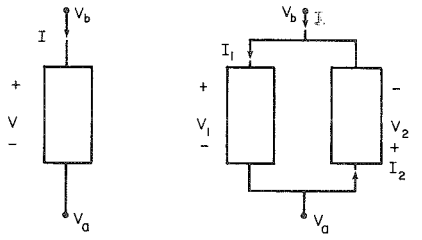

Fig.6 Active loads ; a) General ,b) Inverted-parallel

A particularly useful inverted-parallel structure is the depletion inverted-parallel load shown in Fig. 7. If Vr is kept small enough to maintain operation in the ohmic region (Vr < Vtd), then this device is quite linear. Using the device model given by (1), the resistance of the depletion inverted-parallel load is calculated to be:

$$R_{load} = \frac{-1}{4K'V_t(\frac{W}{L})} \tag{11}$$

By adding this device as a source degradation resistor, the portion of the input signals that appears as input to the input transistors of the differential amplifier is reduced, thus improving linearity, decreasing transconductance gain, and improving differential input swing

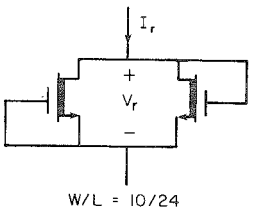

Fig.7 - Depletion inverted-parallel load

capabilities. The principle disadvantage is that the source degradation also reduces the CM range because of the voltage drop across the source degradation loads. Depending on the number of source degradation loads placed in the source leads, the designer may tradeoff between achieving a large DM range or a large CM range. Fig. 8 shows the CM/DM tradeoff and the OTA transconductance as a function of the number of series inverted-parallel loads.

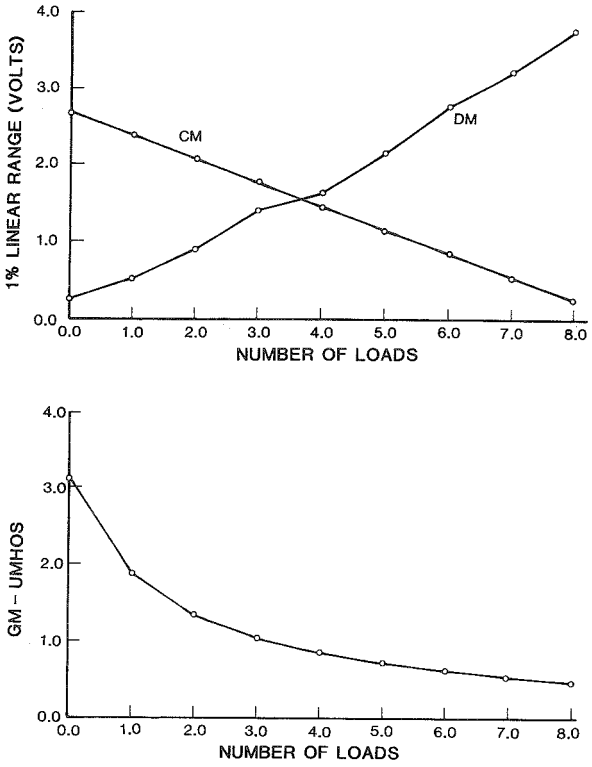

Fig.8 OTA characteristics ; a) CM/DM ranges , b) Gm variation

Analytically, the differential transconductance gain of the source-degenerated differential amplifier is given by:

$$g_m = \frac{1}{R_{source} + \frac{1}{g_{m1}}} \tag{12}$$

where Rsource is the series resistance in each source lead, and gm1 is the transconductance of M1.

An OTA structure incorporating the source degradation loads is shown in Fig. 9. This differs from the structure of Fig. 5 in the addition of the pass transistors of the output to increase the output impedance [6]. The OTA of Fig. 9 was incorporated into the second order lowpass filter of Fig. 10 [7]. A computer simulation using SPICE2 with level 2 device models was made using the process parameters of Table 1, the device sizes of Table 2 and capacitors C1,C2 of values 1.66 pf and 41.4 pf respectively (Q=5 , fo=20 kHz). The frequency response of the filter assuming ideal OTAs and capacitors is shown as a the solid curve (a) in Fig. 11. The dotted curve (b) shows the stimulated response for the filter with the OTAs of Fig. 9. The shift to the left is caused by MOSFET model parasitics and the non-zero Gm(common-mode). Finally, adjusting the bias current to both OTAs simultaneously to trim the Gm's causes the simulation to shift back right as shown by the dashed curve (c). Simulations also showed < 1% THD (measured at 1 kHz) for a 7.8 Vpp input with the OTAs biased from +/- 5 volt supplies.

Table 2 - Device sizes (W/L in microns)

M1,M2	84/12	MB6	10/15
ML1,ML2	10/10	MS1	10/10
ML3-ML6	10/24	MD1	40/10
MB1,MI	100/10	MD2	10/25
MB2	21/10	MS2	10/100
MB3,MB5	50/5	MR0D	40/5
MB4	5/50	MR0S	50/5

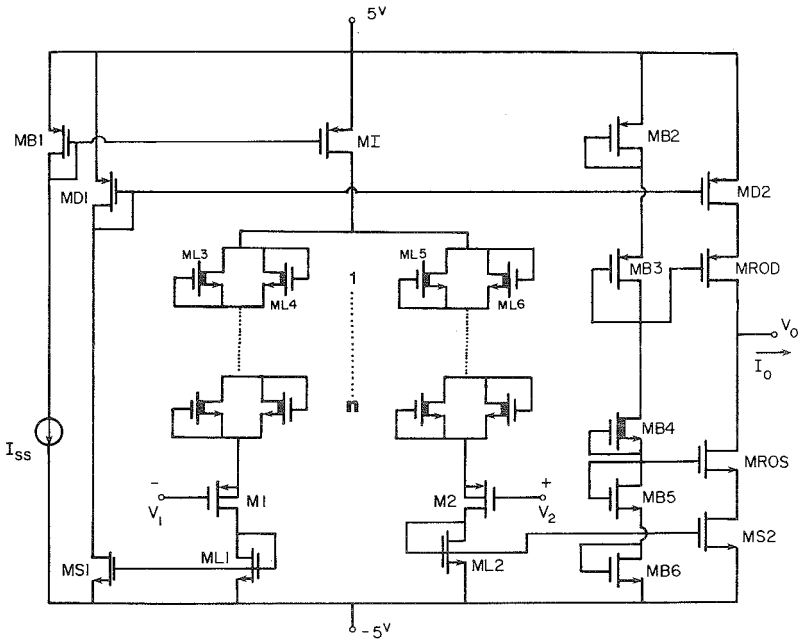

Fig.9 - Complete OTA schematic

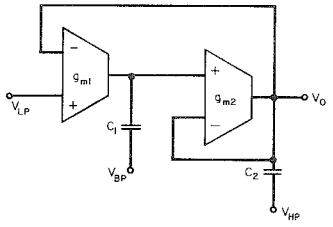

Fig.10 - OTA-based biquad

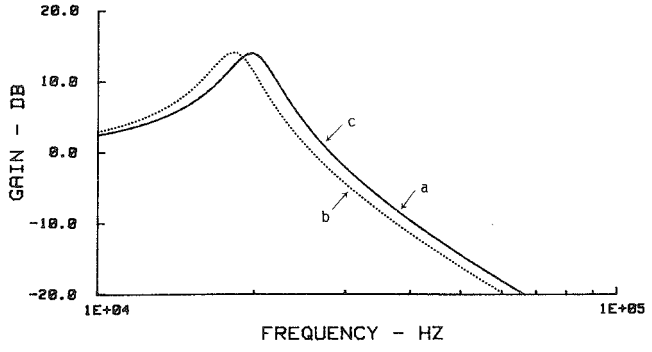

Fig.11 - LP filter response

Through the use of voltage or current control, the characteristics of these OTA-based filters can be adjusted or locked to an external reference.

CONCLUSION

The performance limitations of existing OTA structures have been investigated. One of the major limitations has been the common differential stage which introduces nonlinearities and severely limits input voltage swing.

A modified OTA structure which offers improvements in the differential input voltage range is presented. Methods for trading off common-mode range for differential-mode range are discussed.

The new OTA structure was employed in a second order biquadratic filter structure suitable for monolithic fabrication. The structure shows potential for voltage controlled and master-slave applications in which the cutoff frequency can be adjusted to compensate for process variations. Computer simulations of the circuit using SPICE2 which include the level 2 MOS model parasitics show good agreement with theoretical predictions.

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