A CMOS OTA for Voltage-Controlled Analog Signal Processing

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ABSTRACT

A new CMOS architecture is presented. The structure offers a wide linear differential input capability and an extended g_m adjustment range for voltage-controlled applications. The device is suitable for discrete or monolithic applications and operates at both low and high frequencies. Applications in voltage controlled filter structures are addressed.

Introduction

The ideal operational transconductance amplifier (OTA) is a versatile building block that offers potential in a host of linear and nonlinear applications. Specifically, the OTA is attractive because it can be conveniently current controlled (alt. voltage controlled), structures utilizing the OTA can be very simple [1], and the high frequency performance of the OTA is good.

The OTA finds applications in both discrete and monolithic applications. In discrete applications, it offers one of the simplest methods of obtaining either voltage or current control of the desired characteristics of the circuit 2 .

Unfortunately, the evolution of practical OTA based circuit structures, since the introduction of the OTA in 1969 [3], has been very slow primarily due to the severe practical limitations of commercially available OTAs. The major practical limitation of existing bipolar OTAs [2] is a very limited input voltage capability (tens of milivolts).

The major limitations of existing or published MOS OTAs are a limited input voltage capability due primarily to the use of a standard source-coupled pair as the input stage which becomes very nonlinear with large differential inputs. The g_m adjustment range in existing MOS OTA's is typically proportional to the square root of a bias current making wide-range adjustment impractical due to the extreme control current values required. Deterioration of both common mode and difference mode input voltage capabilities are also associated with large control current changes.

In this paper, emphasis will be placed upon modifying the input stage of MOS OTAs to improve the signal handling capabilities. Methods of increasing the g_m adjustment range by changing the dependence on the control current from quadratic to linear will also be discussed.

A new CMOS OTA structure is presented which offers both a large differential input voltage capability and a wide g_m adjustment range. Computer simulations of the performance of the OTA are presented.

Conventional OTAs

An OTA is ideally a differential voltage controlled current source with infinite input impedance characterized by the equation

$$I_o = g_m Vid \tag{1}$$

where the variables in (1) are as defined in Fig. 1.

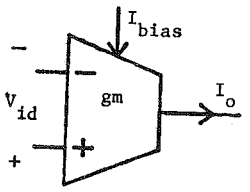

Fig. 1. OTA Symbol and variable convention

With both MOS and Bipolar OTA's, the transconductance gain, g_m, can be practically controlled by a dc control current, I_{bias}. Whenever it is necessary to emphasize the control current capabilities, the I_{bias} input is included in the symbol of the OTA as shown in Fig. 1.

A basic OTA architecture is shown in Fig. 2. It is comprised of a source-coupled (or emitter-coupled) pair and four current mirrors with current gains A_{1-4}.

Assuming the current mirrors are ideal (zero input impedance and infinite output impedance) and that M_1 and M_2 are matched, a standard analysis yields the dc relationship between I_o and $V_1 - V_2$

$$I_0 = A_2(V_2 - V_1)\sqrt{\frac{K'W}{L}}\sqrt{2I_{bias} - \frac{K'W}{L}(V_2 - V_1)^2} \tag{2}$$

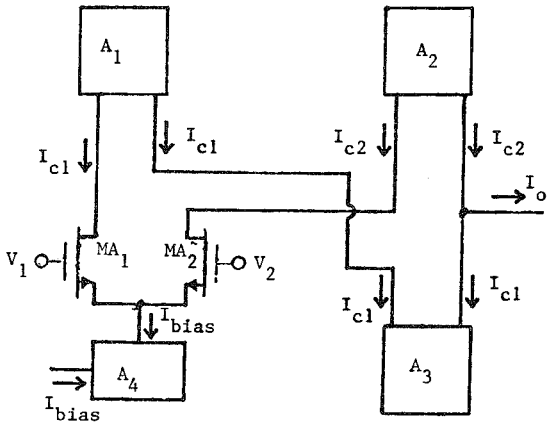

Fig. 2 Basic OTA Architecture

and the small signal relationship

$$i_0 = g_{m1}(A_2 - A_1A_3)(v_2 - v_1) \qquad (3)$$

where g_{m1} is the transconductance gain of the source-coupled pair and K' is the transconductance parameter of the MOSFETs. The inherent nonlinearites for large differential input voltages is apparent from the presence of the $(V_2 - V_1)^2$ term in (2). Since $g_{m1} = \sqrt{\frac{I_{bias}A_4}{2}}\sqrt{\frac{K'W}{L}}$, the quadratic dependence of g_{m1} on I_{bias} is also apparent.

Improved OTA Architecture

Two methods have been discussed in the literature for increasing the input swing capabilities of an OTA by reducing the effects of the nonlinearities in (2) for MOS structures. Both focus on modification of the basic source-coupled pair. Peterson [4] added linear source degradation resistors. Nedungadi [5] has used a linearization compensation scheme. A third approach has been recommended for discrete bipolar OTA applications [2]. It involves using a passive resistive attenuator to precede the basic differential amplifier. Although the resistive attenuator could be used in conjunction with any of the other schemes to obtain further improvements in signal swing, it is impractical due to the unavailability of good resistors in a typical MOS process, area required for resistors is large, *and* the input impedance of the resistive attenuator would be unacceptably small. The quadratic dependence of g_m on the bias current has been addressed in a related application by Soo and Meyer [6]. They adjusted two bias currents simultaneously to obtain a linear rather than quadratic relationship between bias current and g_m.

An improved OTA architecture is shown in Fig. 3. It employs a new active attenuator with essentially infinite input impedance along with a g_m adjustment extension stage (Differential Voltage Amplifier) that gives a linear relationship between bias current and g_m.

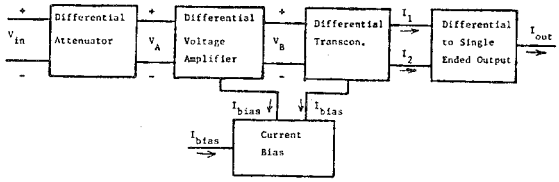

Fig. 3 Improved OTA Architecture

Defining the small signal attenuation of the first stage by $\eta = v_A/v_{in}$, the small signal gain of the differential voltage amplifier by $A_V = v_B/v_A$, the small signal transconductance of the differential transconductance stage by the expressions $i_1 = g_{m1}v_B$ and $i_2 = -g_{m1}v_B$ and the small signal current gain of the differential to single ended output stage by $A_I = i_0/(i_2 - i_1)$, it follows that the overall transconductance gain is given by the expression

$$g_m = \frac{i_0}{v_{in}} = \eta A_v g_{m1} A_I$$

The strategy is to make both A_v and g_{m1} proportional to $\sqrt{I_{bias}}$ whereas η and A_I are to be independent of I_{bias} thus rendering an overall transconductance gain which is linearly dependent on I_{bias}. With the exception of the input and output nodes of the overall OTA, *all* blocks will be designed to have *no* internal high impedance nodes to eliminate the need for external compensation and maintain a good high frequency response. The differential voltage amplifier will be designed to have a low gain (preferably around 1).

Active Attenuator

An active attenuator is shown in Fig. 4. The circuit is designed to operate with transistor M_2 in the ohmic region and transistor M_1 in the saturation region. Separate wells are used for M_1 and M_2 to enable matching of threshold

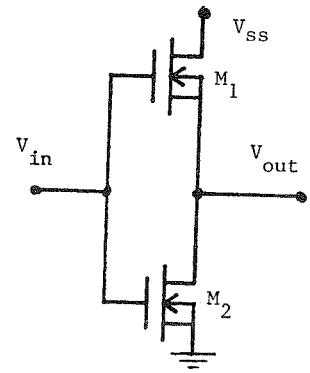

Fig. 4 Active Attenuator

voltages. It can be readily shown that M_1 and M_2 will be operating in the required regions provided.

$$V_t < V_i < V_{ss} + V_t \qquad (4)$$

The relationship between V_0 and V_i is linear but the derivation is somewhat tedious. Neglecting λ effects, the drain currents of M_1 and M_2 can be equated to yield the expression

$$I_{D2} = \frac{K'W_2}{L_2}\Big(2(V_i - V_0 - V_{T1})(0) - (V_0 - V_{ss})\Big)(V_0 - V_{ss})$$

$$= \frac{K'W_1}{L_1}(V_i - V_0 - V_{T1}) = I_{D1} \qquad (5)$$

This represents a *quadratic* equation in V_0 which can be solved by the quadratic equation to yield the perfectly *linear* equation

$$V_O = (V_i - V_t)\left(1 - \sqrt{\frac{1}{1+B}}\right) \qquad (6)$$

where

$$B = \frac{W_1L_2}{W_2L_1} \qquad (7)$$

The attenuation of the attenuator is defined to be η where

$$\eta = 1 - \frac{1}{\sqrt{1+B}} \qquad (8)$$

The differential active attenuator shown in Fig. 3 is obtained by using two identical non-interacting active attenuators. The offset terms in (6) cancel in the overall OTA structure since the output current is proportional to the difference of two inputs with identical offsets. If matching is not perfect, a small residual offset voltage for the differential attenuator will result in a small dc offset current in the resultant OTA.

A plot of the deviation from linear versus the differential input voltage as obtained from the SPICE simulation is shown in Fig. 5. The deviation from linear is relative to full scale where full scale is defined to be the differential input voltage which corresponds to a 5% deviation from a straight line relating I_0 to the differential voltage input.

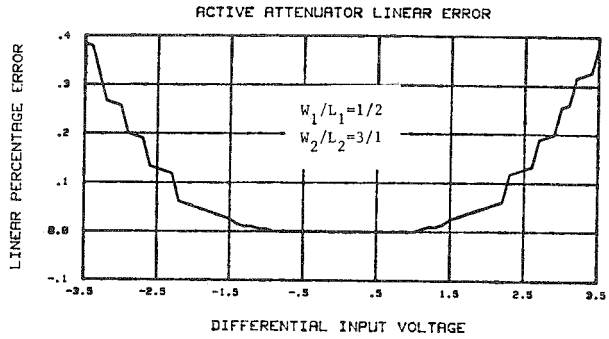

Fig. 5 Nonlinearities in Active Attenuator

Differential Voltage Amplifier

The differential voltage amplifier shown in Fig. 6 was added to obtain a voltage gain proportional to $\sqrt{I_{BIAS}}$. A pair of constant current biasing sources, I_{c3} and $I_{c4}(I_{c4} = I_{c3})$. are used to bias $MA3$ and $MA4$ in a manner which makes the effective load impedance of $MA3$ and $MA4$ independent of I_{bias}. A small signal analysis (neglecting λ effects) of this circuit yields a differential small signal voltage gain of the form

$$\frac{V_{B2} - V_{B1}}{V_{A2} - V_{A1}} = \frac{g_{m1}}{g_{m3}}$$

where

$$g_{m1} = \sqrt{\frac{I_{bias}}{2}}\sqrt{\frac{K'W_1}{L_1}}$$

and

$$g_{m3} = \sqrt{\frac{I_{c3}}{2}}\sqrt{\frac{K'W_3}{L_3}}$$

Differential Transconductance Amplifer and Output Stage

The differential transconductance amplifier is a standard two-transistor source-coupled pair.The output stage is a standard 3-mirror structure with output current given by the expression

$$i_0 = i_{01} - i_{02}$$

The Wilson current mirrors were used to improve the over all output impedance.

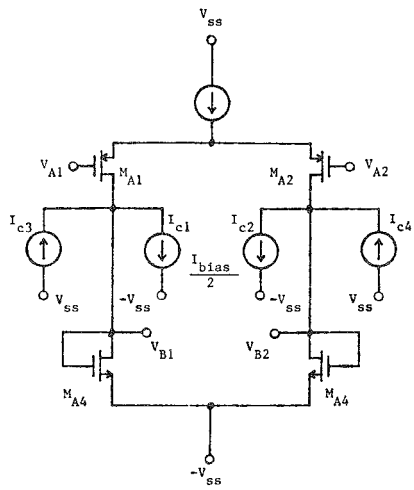

Fig. 6 Differential Voltage Amplifier

Improved OTA

The schematic of the improved OTA is shown in Fig. 7. Device sizing information used in a computer simulation of the overall OTA is listed in Table 1. The device was designed to operate with $V_{ss} = 7.5V$ and a 4V attenuator reference. Process parameters of $K'_p = 8uA/V^2, K'_n = 28uA/V^2$, $V_{TON} = .7V$ and $V_{TOP} = -.7V$ were used in the simulation.

A plot of the % deviation from linear vs. differential bias currents appears in Fig. 8.

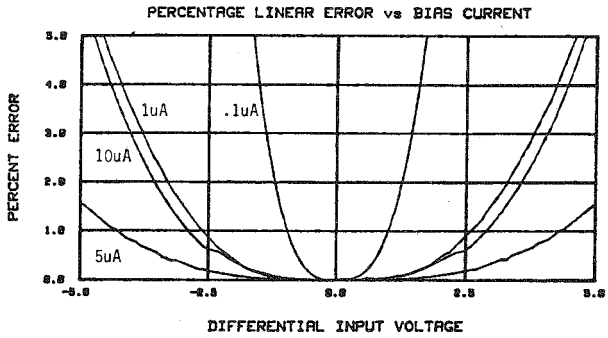

Fig. 8 Linearity of OTA Structure

Conclusions

A new CMOS OTA structure has been presented which offers a large differential input voltage capability and a wide g_m adjustment range. The improvements in the DIV characteristics were atttained primarily through the use of a linear active attenuator which should find use in other applications.

References

[1] R. L. Geiger and E. Sanchez-Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," *IEEE Circuits and Devices*, vol. v-1 number 2, pp 20, March,1985.

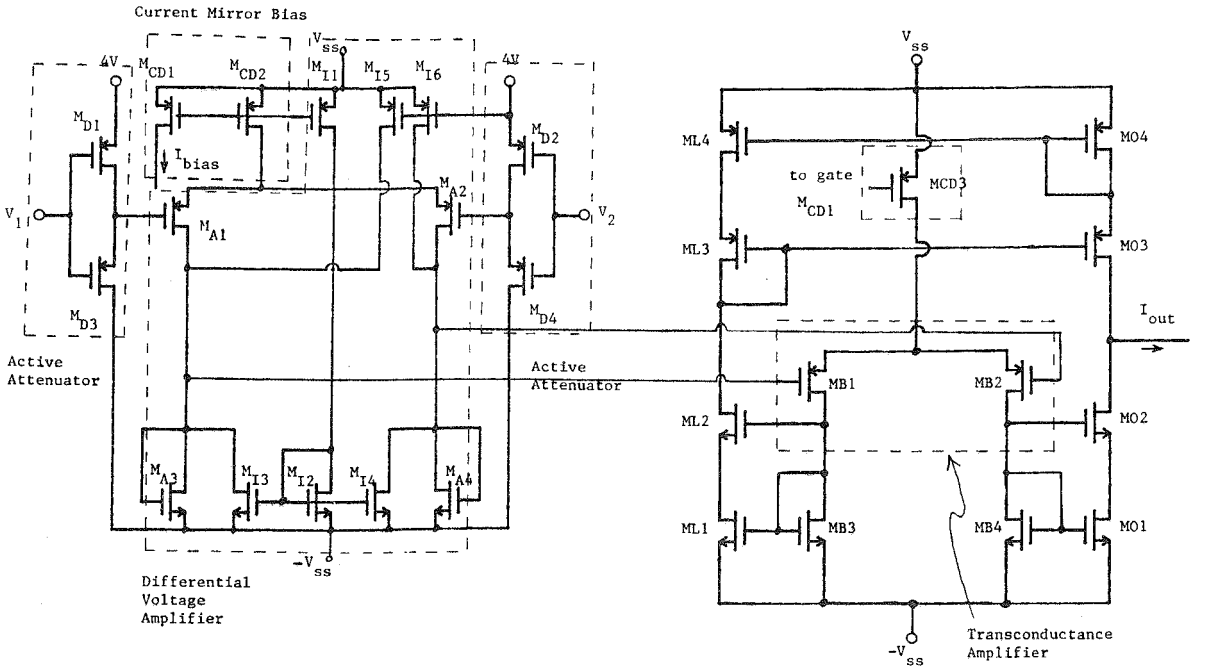

Fig. 7 Improved OTA Circuit Schematic

Transistor	W/L	Transistor	W/L	Transistor	W/L
MD1	30u/10u	MD2	30u/10u	MD3	10u/20u
MD4	10u/20u	MCD1	25u/10u	MCD2	250u/10u
MCD3	250u/10u	MA1	70u/10u	MA2	70u/10u
MA3	10u/30u	MA4	10u/30u	MI1	25u/10u
MI2	10u/110u	MI3	20u/45u	MI4	20u/45u
MI5	25u/20u	MI6	25u/20u	MB1	20u/10u
MB2	20u/10u	MB3	60u/10u	MB4	60u/10u
ML1	60u/10u	ML2	60u/5u	ML3	120u/5u
ML4	200u/10u	MO1	60u/10u	MO2	60u/5u
MO3	120u/5u	MO4	200u/10u		

Table 1 Device Sizing for OTA Structure

[2] C.F. Wheatley and H.A. Whittlinger, "OTA Obsoletes OP-Amp," in *Proc. Nat. Electronics Conference*, Chicago, Illinois, 1969.

[3] National Semiconductor, *Linear Applications Handbook*. National Semiconductor: , July, 1978.

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[6] D.C. Soo and R.G. Meyer, "A Four-Quadrant NMOS Analog Multiplier," *IEEE Journal of Solid State Circuits*, vol. Sc-17, pp. 1174, Dec. 1982.

[7] Mark Van Horn, *CMOS Operational Transconductance Amplifier Building Block for Tunable Filters,MS Thesis*. Department of Electrical Engineering Texas A&M University: College Station, Texas, August, 1985.