A 1-MHZ VOLTAGE-CONTROLLED CONTINUOUS-TIME BANDPASS/LOWPASS FILTER USING LINEARIZED CMOS OTAs

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ABSTRACT

The design and implementation of a continuous-time bandpass/lowpass filter with voltage-controlled center frequency and $Q$ is presented. The circuit uses a linearized CMOS transconductance element as the basic integrating block. A voltage-controlled phase-adjusting scheme is employed in the integrator to compensate for excess phase in the transconductance at high frequencies. The fabricated filter readily achieves the nominal design-center frequency of 1 MHz with $Q = 10$, and provides output signal swings up to $4V_{p-p}$ with 1% distortion.

INTRODUCTION

Recently, there has been considerable interest in the design and implementation of fully monolithic continuous-time analog signal-processing circuits [1-3]. Such circuits overcome certain inherent limitations of switched-capacitor networks arising due to their sampled-data nature [4]. In particular, the advantages of continuous-time processing become increasingly apparent as operating frequencies are raised well beyond the audio range. A basic requirement for realizing accurate and stable continuous-time filters is a filter block having time-constants that are controllable using a voltage or current, thereby allowing the realized filter to be tuned on chip against process and temperature variations. This paper describes the design and implementation of a voltage-tunable filter block capable of realizing cut-off frequencies in excess of 1 MHz. The circuit is a second-order bandpass/lowpass structure using a CMOS operational transconductance amplifier (OTA) as the basic active element. The OTA employs a linearized input stage which dynamically adjusts the bias current of a differential pair to cancel out nonlinearities of the MOSFETs over a wide input voltage range. A voltage-controlled phase adjusting scheme is employed in the OTA integrators to compensate for the excess phase of the OTAs at high frequencies.

PHASE COMPENSATED OTA INTEGRATOR

Fig. 1 shows the schematic diagram of a phase compensated integrator using an OTA whose transconductance $g_m$ is adjustable by a control voltage $V_C$. It is as-

\[
g_m(s) = \frac{g_{mo}}{1 + \frac{s}{\tau}}
\]

(1)

where $g_{mo}$ is the transconductance value at low frequencies and $\tau$ is a high-frequency time constant. This model is fairly accurate at normal operating frequencies where $|s| < \tau$. The resulting transfer function of the integrator is obtained as

\[
A_I(s) = \frac{g_{mo}}{sC} \left(1 + \frac{sCr_d}{1 + \frac{s}{\tau}}\right)
\]

(2)

where

\[
r_d = \frac{\mu_nC_{ox}W}{L} (V_P - V_T)
\]

(3)

is the small-signal drain resistance of $MP$ in Fig. 1. In the above equation, $W$ and $L$ are, respectively, the channel width and length of device $MP$, while the parameters $\mu_n$, $C_{ox}$ and $V_T$ have their usual significance [5]. Note that transistor $MP$ introduces a high-frequency zero in the transfer function of the integrator. Since $r_d$ depends on the gate-source voltage $V_p$, the location of this zero is voltage-adjustable. The phase lead due to this zero can then be used to compensate for the excess phase lag within the OTA itself. That is, if $V_P$ is adjusted to make $Cr_d = \tau$, exact phase compensation is achieved. Assuming that the initial phase error is not large, the zero frequency required for compensation is much higher than the unity-gain bandwidth of the compensated integrator. Therefore, at frequencies of interest, the signal voltage across the compen-

![Fig. 1 Phase compensated OTA integrator](image-url)
sating device $MP$ is very small, resulting in negligible distortion due to the nonlinearity of this device [6].

Fig. 2 shows a CMOS realization of the complete integrator. It employs a linearized transconducance circuit ($M_1 - M_{22}$) which provides a voltage-controlled low-frequency transconductance given by the relation

$$g_m = K(V_C - V_T)$$  

where $K$ is a constant dependent on process parameters and the geometries of the input and biasing devices [6]. The quantity $V_T$ is a constant bias voltage. Details of circuit design and the linearization scheme employed are discussed elsewhere [6,7] and are not repeated here. The integrator in Fig. 2 was fabricated using a standard $3\mu$ double-poly p-well CMOS process [8]. Fig. 3 depicts the nonlinearity in the measured $i - v$ characteristics of the OTA as a percentage of a 2 V (peak) full-scale value. The observed nonlinearity is less than 1 % for input voltages in the range between -2.4 V and + 2.4 V. The circuit consumes 10 mW with the nominal bias values, and exhibits a short-circuit 3-dB bandwidth of 15 MHz.

**FILTER REALIZATION**

The schematic diagram in Fig. 4 shows the proposed test filter structure. It is simply a version of the well known two-integrator loop using the OTA integrator of Fig. 2 as a basic building block. OTAs $g_{m1}$ and $g_{m2}$ along with capacitors $C_1$ and $C_2$ form the integrators, while an additional OTA $g_{m3}$ provides the required loss to obtain finite Q. With an input signal $V_i$ the outputs $V_{OBP}$ and $V_{OLP}$ provide second-order band-pass and low-pass responses respectively. Assuming that $|s| < \tau$ and $|s| >> C \tau$ in the frequency range of interest, a straightforward analysis using (1) and (2) gives the following relations for the bandpass center frequency $\omega_c$ and quality factor $Q$ of the filter

$$\omega_c \approx \omega_0$$  

$$Q \approx \frac{\hat{Q}}{1 - \hat{\omega}_0 \hat{Q}(r_1 + r_2 - C_1 r_2 - C_2 r_2)}$$  

where

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}}$$  

![Fig. 4 Second-order bandpass/lowpass filter](image)
\[ \dot{Q} = \frac{\sqrt{g_{m1}g_{m2}}}{g_{m0}} \sqrt{\frac{C_1}{C_2}} \]  

are, respectively, the ideal center frequency and quality factor obtained without high-frequency parasitic effects \( r_1 = r_2 = 0 \) and without phase compensation \( r_{d1} = r_{d2} = 0 \).

It is evident from (6) that, without compensation, the parasitic time-constants \( r_1 \) and \( r_2 \) can cause significant Q enhancement, especially for large values of \( \dot{Q} \). Exact compensation \( Q = \dot{Q} \) is achieved if \( r_{d1} \) and \( r_{d2} \) are adjusted to satisfy the condition \( C_1 r_{d1} + C_2 r_{d2} = r_1 + r_2 \). Since these drain resistances depend on the phase control voltage \( V_p \) according to (3), this scheme provides a convenient method for voltage-tuning the realized \( Q \) of the filter. Note from (8) and (7) that \( \omega_c \) is independent of this Q adjustment.

The voltage-control of \( \omega_c \) is achieved by adjusting \( V_C \) which modifies all the transconductance values according to (4). Since the same control voltage is applied to all OTAs, the ratio of transconductances in (8) is constant implying that \( \dot{Q} \) is independent of \( V_C \). The realized Q in turn is also largely independent of changes in \( \dot{\omega}_c \) since the corresponding term in the denominator of (6) is small. This feature greatly simplifies the task of tuning the overall response of the filter. In practice, however, due to effects neglected in the approximate relations derived here, a small degree of coupling between \( \omega_c \) and \( Q \) is present.

**EXPERIMENTAL RESULTS**

The filter of Fig. 4 was designed to have a nominal bandpass center frequency \( f_0 = \omega_c / 2\pi = 1 \text{ MHz} \), and \( \dot{Q} = 10 \). In order to simplify design, identical integrators were used with \( g_{m1} = g_{m2} = g_{m0}, C_1 = C_2 \) and \( r_{d1} = r_{d2} \). The required value for the third transconductance is then \( g_{m3} = g_{m0}/\dot{Q} = g_{m0}/10 \). This was obtained by scaling down the gains of the output current mirrors in the OTA (Fig. 2) by a factor of ten. In this way, the linearity of the input stage is preserved. Capacitances \( C_1 \) and \( C_2 \) had nominal values of 4.5 pF, while \( MP_1 \) and \( MP_2 \) had \( W/L = 25 \). The substrates of these devices were short-circuited to their sources. The entire filter, including on-chip output buffers, was fabricated using the process already mentioned [8], and occupies an area of approximately \( 1000 \times 700 \mu\text{m}^2 \).

All measurements were made using \( \pm 5 \text{ V} \) power supplies with \( V_B = -2.5 \text{ V} \). Fig. 5 shows the measured response of the filter at its bandpass output for three different values of \( V_C \) corresponding to \( f_0 \) ranging from 500 kHz to 2 MHz. In each case, \( V_P \) was adjusted slightly to maintain the required value \( Q = 10 \). The relationship between center frequency and control voltage is essentially linear for values of \( f_0 \) up to 1.7 MHz as expected from the linear dependence of \( g_{m0} \) on \( V_C \) in (4). Above this frequency, the large \( V_C \) required drives \( M_4 - M_{11} \) in the OTAs into their ohmic regions of operation, resulting in a decreased sensitivity of the OTA bias currents to \( V_C \). This causes a nonlinear dependence of \( f_0 \) on \( V_C \), and, for this particular design, limits the maximum obtainable value of \( f_0 \) to 2.3 MHz. The effectiveness of the phase control scheme was tested by first tuning the filter to the desired specifications \( f_0 = 1 \text{ MHz}, Q = 10 \) and then varying \( V_P \) while keeping \( V_C \) fixed. Fig. 6 shows the measured bandpass response for three different values of \( V_P \) corresponding to \( Q \) values of 5, 10, and 20. The maximum shift in \( f_0 \) was less than 1 % in this case. The distortion characteristics of the filter were studied. Since the filter has a passband gain equal to \( Q \), signal swings are limited at the output of the filter. Fig. 7 shows the output spectrum obtained for the 1 MHz bandpass filter \( Q = 10 \) for a 4\( V_p-p \) signal at its output. The total harmonic distortion is approximately 1 %. This value is reduced to 0.2 % for a 1.5\( V_p-p \) output. The measured inband noise at the bandpass output is approximately 70\( \mu \text{V}_{\text{rms}} \).
CONCLUSION

The design and implementation of a second-order continuous-time filter with voltage-controlled center frequency and Q has been presented. Experimental results demonstrate the viability of continuous-time processing in the MHz range using a standard 3μ CMOS technology. The voltage-control feature allows this filter to be tuned on-chip against process and temperature variations using known tuning schemes [3, 9]. The implementation of higher-order filters obtained by cascading the proposed second-order block is presently under investigation.

REFERENCES