A Fully Balanced CMOS OTA for High Frequency Monolithic Filters

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ABSTRACT

A fully balanced CMOS OTA (operational transconductance amplifier) designed for high frequency continuous–time filters is described. Computer simulations show the OTA has less than .6% nonlinearity over a ± 1 V range. The transconductance is adjusted using a novel CMOS voltage source with an output resistance that is less than 180 Ω. A fully balanced monolithic filter biquad with lowpass and bandpass outputs at 400 kHz shows THD of .30% and .70% respectively.

INTRODUCTION

The continuous–time filter presented in this paper utilizes fully balanced OTA's in a fully balanced filter structure. The benefits of fully differential (balanced) designs have recently been exploited in several switched capacitor filters [1],[2]. Reported advantages of fully balanced structures include improved power supply rejection ratio (PSRR), simpler gain block design, higher signal–to–noise ratio, improved linearity [3], and less gain–bandwidth induced filter characteristic shifts. These benefits are obtained at the expense of increased silicon area. The tradeoff has proven justifiable in many switched capacitor applications, and should be justifiable in corresponding continuous–time applications as well.

Transconductance based gain blocks provide post– fabrication tunability, a superior frequency response, and possibly an area advantage over the convertional op amp RC integrator.The traditional gain block for low–medium frequency discrete active filters has been the operational amplifier (op amp). For high frequency filter gain blocks, transconductors (OTA's) offer advantages over the traditional op amp, which suffers from excess phase. The improved performance of the OTA at high frequencies can be attributed to the fact that the OTA has no internal high impedance nodes. Any excess phase in the OTA is primarily due to the internal current mirrors [5]. In the 100 kHz – 1 MHz range the OTA integrator excess phase is adequately modeled by a single parasitic pole ($\gg f_o$). A traditional op amp integrator model with comparable accuracy includes 2 high frequency poles. The higher order op amp model contributes more excess phase.

Recent op amp designs (cascode and folded–cascode op amps) offer significant improvements in high frequency performance, since they have no internal high impedance nodes and thus require no separate compensation capacitor. However, these recent high frequency op amps are actually transconductance amplifiers with very large output resistances [5]. As such, these devices are not general purpose op amps, but are rather designed specifically to drive capacitive loads. In particular, the capacitive load itself is used for frequency compensation. These new high speed op amps are superior choices for applications with low current drive requirements, like switched capacitor circuits. Traditional op amp RC active filter designs, however, can not use these new op amps (even with their superior frequency performance) because of their large output resistance. Monolithic high frequency active filters based upon conventional op amps are recognized as impractical due to both the high frequency op amp limitations and the inability to practically and accurately control the passive component values.

It is our intent to exploit the improved high frequency performance of the OTA in the design of high frequency monolithic filters. Emphasis will be placed upon the design of a high performance general purpose OTA. A block diagram of a basic fully balanced OTA is shown in Fig. 1 . The design problem can be decomposed into the design of a differential input stage followed by the design of the appropriate current mirrors.

INPUT STAGE

OTA's in active filter structures typically experience input/output size signals across the OTA inputs [6]. For low distortion and good dynamic range the OTA input must remain linear over a wide input voltage range. This is a problem not encountered in op amp design since the differential input is ideally zero.

The circuit of Fig. 2 is a fully balanced OTA input circuit. It differs from a conventional source coupled pair differential amplifier in that the high impedance tail current

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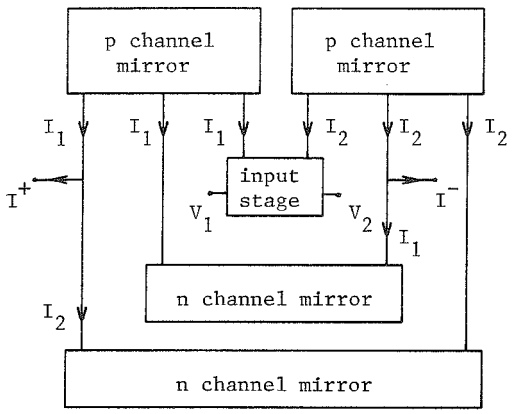

Fig. 1. Fully Balanced OTA Block Diagram.

source has been replaced by a voltage source. Both devices are assumed operating in the saturation region and modeled by Sah's equation :

$$I_1 = \beta(V_1 - V_{ee} - V_T)^2 \tag{2}$$

$$I_2 = \beta(V_2 - V_{ee} - V_T)^2 \tag{3}$$

where $\beta \equiv \frac{1}{2}\mu C_{ox}\frac{W}{L}$ and V_T is the threshold voltage. The differential output is defined as:

$$\begin{aligned} I_{out} &= I_2 - I_1 \\ &= \beta[(V_2^2 - V_1^2) - 2(V_T + V_{ee})(V_2 - V_1)] \end{aligned} \tag{4}$$

If the devices see purely differential input signals ($V_1 = -V_2$), the output expression simplifies to :

$$I_{out} = 4\beta(V_T + V_{ee})V_2 \tag{5}$$

and the transconductance gain is given be the expression:

$$g_m = \frac{I_{out}}{V_2 - V_1} = 2\beta(V_T + V_{ee}) \tag{6}$$

With differential inputs, the output current is a purely linear function of the difference mode input voltage, given that Sah's equation is an accurate model of MOSFET large signal behavior. Extensive SPICE2G.6 simulations using the full MOSIS 3μ CMOS models (25 Level 2 parameters) and device sizes listed in Table 1 have validated the excellent linearity.

OTA STRUCTURE

One of the largely unexplored advantages of OTA's is their topological and structural simplicity. The previous section has shown a very simple input stage that produces a linear output current given balanced (purely differential mode) inputs. A method of obtaining the difference in drain currents, I_{out}, is shown in Fig. 1. The OTA does not require internal compensation like a conventional op amp, because there are no internal high impedance nodes.

Specification of current mirrors almost completes the OTA design. Consideration is given to the desired output resistance, current matching, frequency response and to the common mode output. The fully balanced input stage of Fig. 2 is combined with Wilson p–channel mirrors and cascode n–channel mirrors to form the OTA of Fig. 3. The p–channel mirrors were chosen for their superior frequency response. Very strict 1:1 current gain (and good frequency response) motivated the choice of the n–channel mirrors.

Fig. 4 shows the % full scale deviation from linear for both balanced output currents (I^+ and I^- on Fig. 3). The OTA is designed for a nominal g_m of 12.3μmhos and shows a maximum nonlinearity of .57% over ± 1 V full scale. Global parameter shifts and statistical (individual) parameter variations will cause the fabricated OTA's behavior to deviate slightly from the simulations. Nonlinearity degradation caused by global parameter shifts has been investigated by repeating the initial simulations with $\pm 25\%$ variations in each model parameter. The worst case nonlinearity was for a 25% decrease in K_n', when the maximum full scale linear deviation became .94%. This large K_n' variation is outside the range of acceptable MOSIS fabrication parameters, so global parameter shifts should cause less severe nonlinearity. Statistical deviations were investigated for worst case β mismatches of $\pm 5\%$ and V_T mismatches of ± 20mV. The maximum nonlinearity occured for a 5% β mismatch in the input devices and was .77%. These simulated values appear a bit pessimistic based on measurements of a recently fabricated OTA with a similar topology.

Modest device mismatches can lead to large common-mode offsets unless common–mode feedback is used for Q–point stabilization [1]. The common–mode feedback is provided by the ME devices on the V_{ss} rail.

CMOS VOLTAGE SOURCE

The OTA transconductance is controlled by adjustment of V_{ee} as shown by Eq. 6. The final filter structure is designed to be readily adaptable to either Master–Slave tuning [7] or digital sensing/control [8]. An adjustable CMOS voltage source is used to buffer the tuning struc-

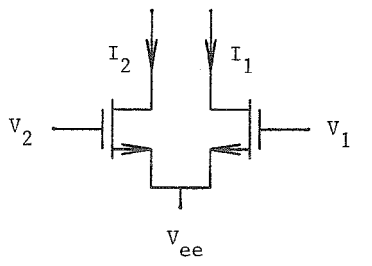

Fig. 2. Fully Balanced OTA Input Stage.

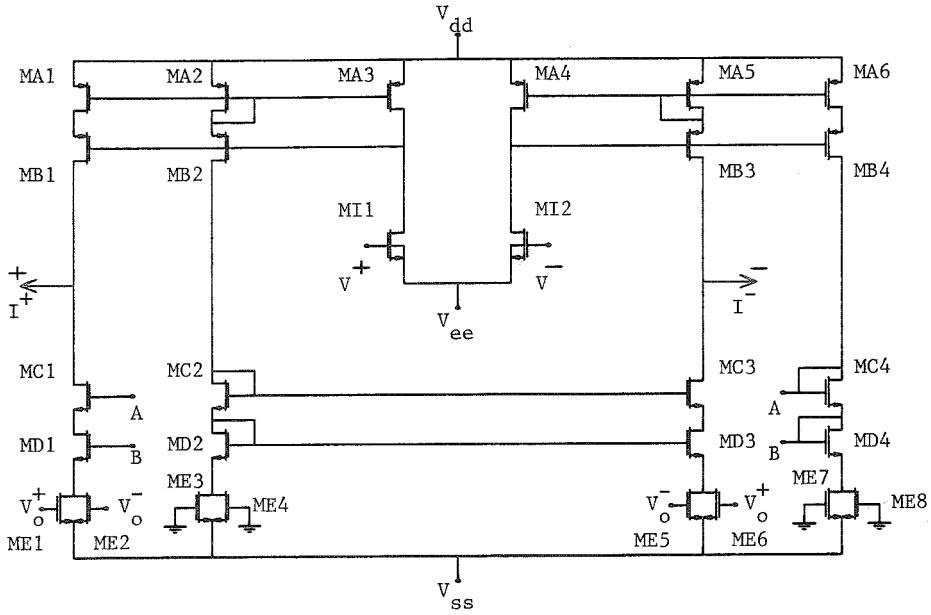

Fig. 3. Complete OTA Schematic.

ture control lines from the OTA V_{ee} current requirements. Fig. 5 shows an adjustable CMOS voltage source. A current mirror feedback loop senses V_{ee} and adjusts V_{GS} of a wide output device. A small (.36 pf) compensation capacitor is used to keep the output resistance low over a reasonable frequency range and to insure stability. The output resistance is nominally 180Ω. As V_{adj} varies from −4.0 V to −2.4 V the voltage source output V_{ee} varies from −4.15 V to −2.85 V, giving an OTA g_m adjustment range from 15.4μmhos to 8.85μmhos.

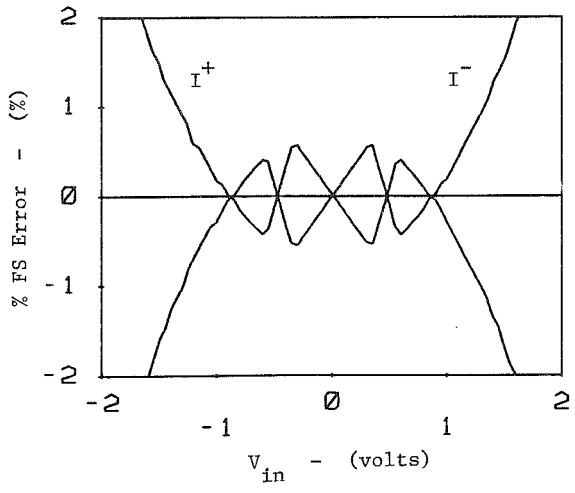

Fig. 4. Nonlinearity in balanced output currents.

INTEGRATOR

The integrator is the fundamental circuit element in many filter structures. An OTA integrator is shown in Fig. 6. For high frequency filter applications the deviations from ideal phase (90°) are critical. A parasitic pole 2 decades above the filter critical frequency (40 MHz for this filter) will contribute .57° excess phase. This modest amount of excess phase can cause substantial deviations from the nominal Q and critical frequency gain.

A simple phase compensation scheme obtained by the addition of a small "resistor" below the OTA integrator capacitor is shown in Fig. 6. This "resistor" introduces a phase–lead zero. An external voltage (V_Z) sets the gate voltage of a grounded n–channel transistor operating in the ohmic region. The gate voltage can be used to adjust the resistance value and the zero location which offsets the excess phase due to a parasitic pole(s). Since the compensation zero is at a high frequency, the required equivalent

Devices	W/L (microns)
MAx	100/6
MBx	10/8
MIx	8/60
MCx	10/8
MDx	50/8
MEx	14/7

Table 1. OTA Device Sizes.

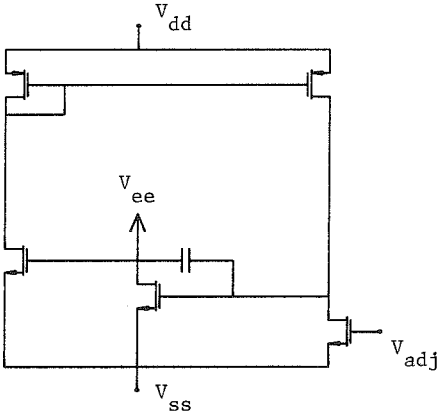

Fig. 5. CMOS Voltage Source Schematic.

resistance is low, and consequently the portion of the signal voltage appearing across the ohmic device is small. Therefore, distortion caused by the ohmic device is negligible. The integrator phase response simulation with $C = 16.96$pf shows negligible phase error at $f_o = 400$ kHz, and less than .25° within an octave of f_o for $V_Z = 1.25$ V.

FILTER TOPOLOGY

A fully balanced OTA based biquad is shown in Fig. 7 . The topology is similar to that used by the op amp Tow–Thomas filter. In the conversion of the Tow–Thomas structure the op amp integrator(s) were replaced with OTA integrators, and the other resistors with OTA's.

This filter topology has been simulated with the OTA of Fig. 3, $C_1 = 16.96$pf and $C_2 = 1.06$pf. Because the C_2's are fairly small, calculation of the filter critical frequency and Q must include an estimate of the capacitive loading of C_2 by the gate (input) of OTA 3. For $V_{adj} = -3.8$ V, ± 5 V supplies, and a 2 V_{p-p} input signal; the filter exhibits a 400 kHz center frequency, $Q = 3.8$, and THD of .30% and .70% for the lowpass and bandpass outputs respectively.

Silicon is currently being fabricated to verify this design and to test design feasibility at higher frequencies. The OTA appears well suited to higher frequency applications,

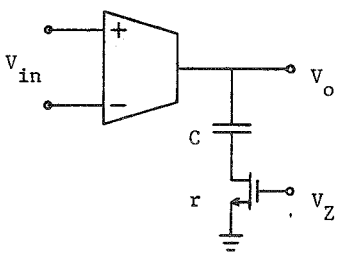

Fig. 6. (Compensated) OTA Integrator.

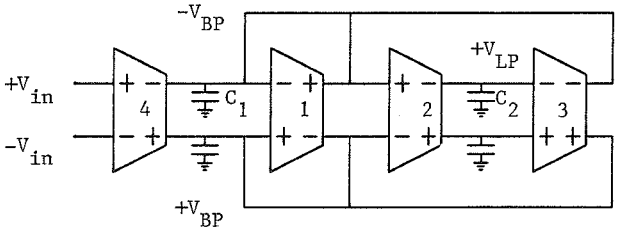

Fig. 7. OTA Filter Topology.

the input devices are fairly long (W/L = $8\mu/60\mu$) for operation at 400 kHz. Simulations show that decreasing the input device length (L) to achieve larger OTA transconductances provides working designs above 1 MHz.

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