Digitally Controlled Analog Signal Processing

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Introduction

Many signal processing applications involving continuous-time input and/or output signals exist. These applications are both linear and nonlinear, vary from low to high frequencies, and have specifications ranging from very lax to very stringent. Monolithic continuous-time signal processors have largely eluded IC designers for the past decade. This can be attributed primarily to the inability of researchers to solve many of the numerous technological challenges associated with analog signal processing.

Digital signal processing techniques have been successfully applied in a very useful but limited class of analog signal processing applications. The digital signal processing techniques have offered flexibility and simplicity but have been accompanied by high system costs and restricted to relatively low frequency and/or non-real-time applications. Aliasing, quantization, warping, and algorithimic performance and sensitivity limitations pose continual challenges.

It is well known that monolithic continuous-time analog integrated circuits can ideally provide sophisticated signal processing capabilities in an area efficient manner over a very wide frequency range. This extends from the low audio range to frequencies well beyond 100 MHz where conventional circuits such as a simple digital inverter behave much as a lowpass filter.

Initially, the major practical limitations which have limited the development of monolithic analog integrated circuits are identified and quantified in this paper. Existing approaches and their fundamental limitations are discussed.

An architecture for a system which inherently compensates for the major factors which have limited the development of monolithic continuous-time integrated circuits is introduced. The architecture utilizes a precisely controllable analog signal path and a sophisticated digital controller in a control loop and is termed a Digitally Controlled Analog Signal Processor (DCASP). Within a predetermined range, both the functional characteristics and specifications of the analog signal processor can be established via software input after silicon processing and packaging are complete. The structure is amenable for self-checking/self-correcting requirements as well as adaptive applications. Self testing features are also practical. The structure is applicable from low frequencies to very high frequencies. The DCASP is compatible with and scales with existing VLSI technologies.

The major emphasis in this paper is placed upon the DCASP architecture itself and on how this architecture can be used to simultaneously overcome the major technological limitations currently impeding the development of monolithic real-time continuous-time signal processing circuits.

Technological Challenges Facing the IC Designer

Numerous practical limitations are responsible for seriously limiting the evolution of monolithic analog integrated circuits. The major passive factors limiting the performance of these circuits are listed in Table 1. In addition to the passive factors, electrical noise of the passive and active devices and device nonlinearities further deteriorate performance.

1.	Nominal Process Parameter Variations
2.	Statistical Process Parameter Spreads
3.	Large Temperature Coefficients
4.	Parasitic Resistors and Capacitors
5.	Passive Component Matching
6.	Active Component Matching

Table 1. Major Passive Factors Limiting Performance of Monolithic Analog Circuits

The magnitude of the problem associated with the limitations of Table 1 can be best appreciated by considering the typical magnitude of these factors and their combined effects on typical system performance. For comparative purposes, emphasis will be placed on silicon MOS processes although similar phenomenon are observed in other technologies.

Parameter variations from the design target associated with processing are quite large. ±50% variations in sheet resistances, $\pm 100mv$ variations in threshold voltages of MOSFETs and ±10% variations in oxide capacitor values are typical. Variations in the transconductance parameter $K'(K' = \mu Cox)$ of tens of percent are also common.

Chip level statistical parameter variations are somewhat smaller than the process parameter variations but are still significant. These variations are due to both local and global differences in the characteristics of silicon systems across the die. Variations (mean standard deviation) of threshold voltages are in the 1mv to 20mv range and variations in K' range from 0.5% to 5%[1].

Temperature coefficients of passive and process parameters are significant. For example, the TCR of the sheet resistance of polysilicon is typically in the 0.1%/°C range.

Parasitic capacitors from plate to substrate associated with poly-poly capacitors are in the 1% to 30% range of the capacitor itself. Inherent parasitic resistors associated with poly strings, contacts and drain and source diffusions range upward from tens of ohms. Layout parasitics associated with interconnections are often somewhat larger. The parasitic capacitances associated with resistor strings are typically both distributed and voltage dependent.

With considerable care in layout, ratio matching of capacitors to ±0.1% is possible[2]. Practical resistor ratio matching is in the ±2% range (5micron feature size)[3]. Accurate ratio matching of parasitic components is more difficult.

Active component matching is poorer than passive component matching. For example, for a FET resistor random variations in the .6% to 6% range are common.

The seriousness of the limitations of the factors in Table 1 can be appreciated only when one considers the specifications required in typical practical applications. Suffice it to say that many applications exist in all frequency ranges from low audio to many GHz if effective RC products or component ratios can be *practically controlled* to between 0.1% and 1% accuracy.

The DCASP approach that is presented here has inherent compensation for all of the factors listed in Table 1, is applicable over a very wide frequency range, and can be used in medium precision as well as in some high precision applications.

DCASP Approach

A block diagram of the architecture of a simplified version of the Digitally Controlled Analog Signal Processor (DCASP) is shown in Fig. 1. Although this simplified structure may not be optimal, it suffices to introduce the DCASP technique and demonstrate the performance potential of this approach. The block diagram contains four basic components, the Controlled Signal Processor (CSP), the Performance Detector, the Exciter, and the Digital Controller. The first three components enclosed in the dashed curves represent analog circuitry that will appear on a single substrate. The Digital Controller may also be on the same substrate or may be external. The switch, S_1, allows either the input signal or the output of the Exciter to be applied to the Controlled Signal Processor itself.

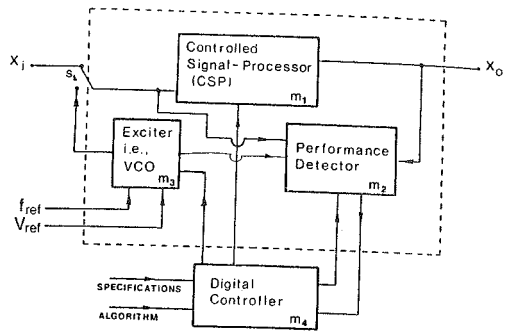


Fig. 1. DCASP Block Diagram

The basic operation of the system is very simple. S_1 is initially connected to the Exciter output. In this mode the Digital Controller "identifies" the Controlled Signal Processor by simultaneously identifying the three analog blocks: The Exciter, the Performance Detector, and the Controlled Signal Processor. Once the CSP is identified, the controllable components in the CSP are adjusted and latched to optimize performance of the CSP relative to the given specifications. Following optimization, S_1 changes states allowing the input signal to be applied to the CSP. All signal processing then takes place in the optimized analog CSP. Comments about the operation of each of the blocks and the overall system follow.

The Controlled Signal Processor should be designed to allow for adjustment of a large number of key parameters and functions. Large adjustment range and fine resolution for all components is important. For example, if the CSP is designed to act as a filter, a group of multiple input lossy integrators in which the loss and the unity gain frequency associated with each input are all independently adjustable over a wide range might serve as the basis for the CSP. By appropriately interconnecting these devices via the Digital Controller and adjusting the components to optimize performance, a universal precision filter structure is possible. For audio frequency applications, the adjustable components might be binarily weighted resistors and capacitors or switched capacitors or higher-level programmable structures such as Operational Transconductance Amplifiers (OTAs)[4]. Continuously adjustable rather than quantized components are also possible. A typical grid (in the s-plane) depicting by intersection of grid lines the possible pole locations of a filter constructed using this tech-

nique with quantized component values is shown in Fig. 2. Methods of selecting the adjustable quantized components to obtain maximal resolution for specific applications are discussed in the literature[5].

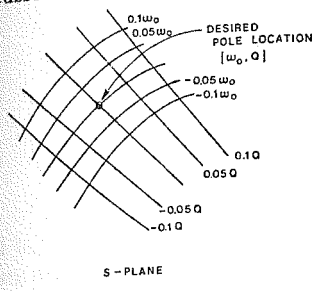


Fig. 2. Possible pole locations in a DCASP based active filter

The Exciter provides an excitation or sequentially, multiple excitations for the CSP during the identification state. Depending on the application, typically only f_{ref} or V_{ref} will be required. The exact value of these references is not critical but they must be known and stable. The identification and optimization problem simplifies if multiple inputs (but a fixed single reference) are sequentially applied by the Exciter. Considering again the filter example, the Exciter may consist only of a non-precision voltage-controlled oscillator (VCO). The Digital Controller is used to sequentially set the Exciter (i.e., VCO) operating frequency. The "exact" frequency of oscillation for each step in the VCO sequence is not critical but can be precisely determined with a modest amount of circuitry if f_{ref} is known.

The Performance Detector is used to measure the performance of the CSP itself. If one were to attempt to identify only the CSP, the required specifications for the design of the Performance Detector would typically be quite challenging. By also identifying the Performance Detector and Exciter, the specifications required for these devices will be modest. For algorithmic simplicity, the Performance Detector may also be made to be tunable by the Digital Controller. Considering again the filter example, the Performance Detector may be no more than a voltage comparator or a generic analog to digital converter. Nonideal characteristics of the Performance Detector, such as offset voltages (as a function of common mode input) may be identified and/or adjusted by the Digital Controller. Slew rate and hysteresis effects may also be identified or, in some applications, ignored.

The Digital Controller is used to monitor the performance of the system during the identification or pretune state. Based upon the output of the Performance Detector for each excitation supplied by the Exciter, the system is adjusted to optimally meet the specifications established for the CSP. The desired specifications must be stored in nonvolatile memory. For high-volume applications, tuning algorithms may be fixed in hardware. Once tuned, the Digital Controller may either power-down or enter a standby state in which it monitors portions of the system. Since the Digital Controller is not in the signal path, it is not needed for real-time operation. Since the pretune speed is typically not critical, the size and capabilities of the controller can be quite modest. Tradeoffs between algorithmic tuning complexity and capabilities of the Digital Controller can be made.

Referring back to the technological limitations of Table 1 which plague the continuous-time IC designer, it should be apparent that if an acceptable tuning strategy can be developed, and if the CSP has sufficient range and resolution so that the domain of realizable specifications (henceforth termed the tuning domain) intersects with the desired specifications (henceforth termed the specification domain), then the DCASP structure will be inherently unaffected by nominal process parameter variations, statistical process parameter spreads, parasitic resistors and capacitors as well as passive and active component matching.

If temperature changes after the initial trimming, several alternatives exist for temperature compensation. In those applications where the signal path can be periodically interrupted, the CSP structure can be re-calibrated. The Digital Controller can also monitor die temperature and make on-line corrections based upon nominal temperature characteristics of the devices. A dual signal path architecture in which the input signal is alternately applied to the two paths and in which the un-excited path is off-line calibrated is also possible.

High Frequency Applications

At high frequencies (10MHz to 200MHz) few techniques exist for signal processing on silicon. This can be attributed primarily to the relative significance of parasitic capacitances associated with both the passive and active devices as well as with the layout at these frequencies. As a consequence, at high frequencies drastic and non-controllable deterioration in the characteristics of amplifier structures is experienced rendering them impractical. This precludes the practical application of either SC or continuous-time active filters in this frequency range.

It has been demonstrated[6] that continuous-time circuits can "operate" at much higher frequencies than their digital counterparts. The main limitation of high frequency monolithic continuous-time circuits is the inability of designers to precisely control the characteristics of the analog circuits. To demonstrate the high frequency performance capabilities of continuous-time circuits, consider the high frequency bandpass filter of Fig. 3. This circuit is basically the cascade of three "digital" inverters configured in a feedback structure.

The frequency response of this circuit as obtained from a SPICE simulation for several different values of I and ν is shown in Fig. 4. In the simulation of this simplified circuit, the multiple-output current mirror and buffer amplifiers were assumed ideal, loading capacitors of 0.1pf

were connected to signal nodes, and the MOSFETs were characterized by parameters of a typical 5μ CMOS process. A dc level control was used to keep the quiescent output voltage constant. Potential for adjusting the characteristics of very high frequency circuits via dc control variables should be apparent from this example. If a good control structure to automatically adjust the characteristics of this circuit is developed, such as using the DCASP architecture of Fig. 1, precision high frequency performance is possible.

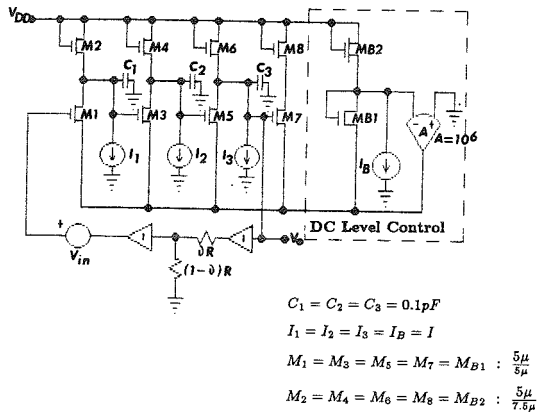
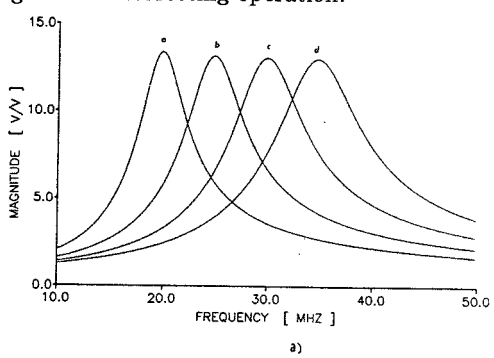


Fig. 3. Simplified High Frequency ω_o and Q Controllable Bandpass Filter

Conclusions

A new architecture for monolithic continuous-time precision signal processing has been introduced. The architecture employs a tunable non-precision signal processing path and a digital controller for precisely electronically tuning the signal path in the field. The DCASP structures are inherently insensitive to the major technological limitations plaguing other monolithic continuous-time approaches; namely, process variations, process parameter spreads, temperature variations, aging, parasitic resistor and capacitors as well as resistor and capacitor matching.

The DCASP architecture is amenable to a host of linear and non-linear signal processing applications over a wide range of frequencies. It is versatile in that it allows for post fabrication tayloring of circuit functions and specifications. It can be used in adaptive applications. It is microprocessor compatible and can be configured for self-testing and self-correcting operation.



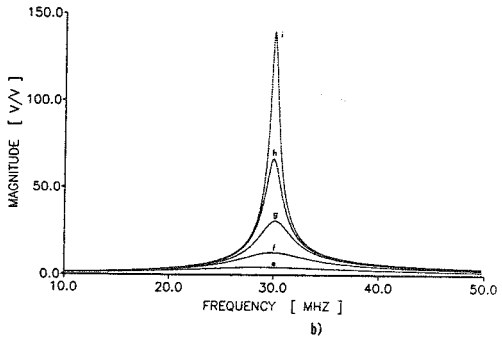


Fig. 4. Simulated Frequency Response for Circuit of Fig. 3 for various values of I and ν (Curve designations are in Table 3). a) Constant BW, Variable f_o, b) Constant f_o, variable BW

Plot	I	ν	Plot	I	ν
	μ A	V/V		μ A	V/V
a	43.93	0.0577	e	22.03	0.318
b	36.34	0.1375	g	31.75	0.2875
c & f	28.57	0.3050	h	33.67	0.2672
d	21.25	0.613	i	34.46	0.262

Table 2. Parameters for Plots of Fig. 4

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