DESIGN OF A CMOS DIFFERENTIAL AMPLIFIER USING A SOURCE-COUPLED BACKGATE PAIR

Soo-Won Kim and Randall L. Geiger

Department of Electrical Engineering
Texas A&M University
College Station, TX 77843

ABSTRACT:

A novel differential amplifier having a wide linear input range is described. This differential amplifier uses the back-gates of a conventional source-coupled pair as inputs. The nonlinear error is less than 1% over a $\pm 10 V_{p-p}$ input range. Both analytical solutions and experimental results are presented.

I. INTRODUCTION

The source coupled differential-input pair is widely used as the input stage in OP amps, OTAs and the other linear circuits. The usefulness of this stage stems from the fact that it is reasonably linear over a wide input voltage range, provides a high input impedance, a large common mode rejection ratio (CMRR), a good power supply rejection ratio (PSRR), and low dc offset voltage. Some applications, however, require more linearity than is offered by the source-coupled pair.

The large-signal analysis of the source-coupled pair illustrates the linearity limitations of the circuit. By assuming a simplified square law relationship of the MOSFET in the saturation region, $I_D = k(V_{GS} - V_{TH})^2$, and assuming M_1 and M_2 of Fig. 1 are matched, the drain currents, I_{D1} and I_{D2} can be found as

$$I_{D1} = \frac{k}{2}\left(\sqrt{\frac{I_{SS}}{k} - \frac{V_{id}^2}{2}} + \frac{V_{id}}{\sqrt{2}}\right)^2 \tag{1}$$

$$I_{D2} = \frac{k}{2}\left(\sqrt{\frac{I_{SS}}{k} - \frac{V_{id}^2}{2}} - \frac{V_{id}}{\sqrt{2}}\right)^2 \tag{2}$$

where

$$k = \frac{\mu C_{OX}}{2}\frac{W}{L}$$

From (1) and (2), the current difference, I_{od}, is expressed by

$$I_{od} = I_{D1} - I_{D2} = kV_{id}\sqrt{2\frac{I_{SS}}{k} - V_{id}^2} \tag{3}$$

This expression is valid when the input voltage does not exceed the range [1]

$$-\sqrt{\frac{I_{SS}}{k}} < V_{id} < \sqrt{\frac{I_{SS}}{k}} \tag{4}$$

Beyond this range, the output current becomes independent of the input voltage. It also can be seen that output current is linear only for the small range of V_{id} (*i.e.*, $V_{id} \ll \sqrt{2\frac{I_{SS}}{k}}$). To have less than 1 % nonlinearity, input voltage is limited by the expression

$$.99\sqrt{2\frac{I_{SS}}{k}} \leq \sqrt{2\frac{I_{SS}}{k} - V_{id}^2} \tag{5}$$

which simplifies to

$$-.28\sqrt{\frac{I_{SS}}{k}} \leq V_{id} \leq .28\sqrt{\frac{I_{SS}}{k}} \tag{6}$$

It is apparent that some improvement in the linear input range, for which both devices are active, can be obtained by 1) increasing the bias current, 2) increasing the device channel length , or 3) decreasing the channel width. Tradeoffs should be made between the bias current and the device sizes. When long input devices (equivalently, small width devices) are used to increase the input range, it will result in increased gate to source voltage drops for a fixed bias current. This will cause not only a large offset voltage but also a limited negative common mode input range [2]. It is well known that the offset voltage in the source-coupled differential pair is directly proportional to $(V_{GS} - V_{TH})$ [3]. The input transistors are practically sized to operate with values of $(V_{GS} - V_{TH})$ of several hundred millivolt to minimize the offset voltage due to the k mismatch. The same arguments can be applied when the bias current is increased with a fixed device size.

The circuit proposed here offers improvement in linear input range without requiring additional devices, high bias currents, or causing common mode input range reduction.

II. BACK GATE SOURCE-COUPLED INPUT PAIR

It is well known that the MOSFET is actually a four terminal device . The bulk (alternately "back gate") is generally considered to be a parasitic node of the device and designers usually attempt to use circuit structures which minimize any effects this node may have on circuit performance. The bulk is often connected to the source to minimize the bulk effects. If the device is fabricated in its

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own well as shown in Fig. 2, then the bulk can actually be used as an input terminal when a constant and sufficiently large voltage is applied to the gate to form a channel. If the input pair is biased in the ohmic region, a substantial improvement in transconductance linearity can be obtained if the back gates are used as inputs. Although the increased linearity is accompanied by a decrease in transconductance gain, this may be preferred in some applications. Additional current mirror gain can be used to recover the reduction in transconductance gain with minimal degradation in linearity if desired. An analysis of the back–gate differential amplifier shown in Fig. 1b follows.

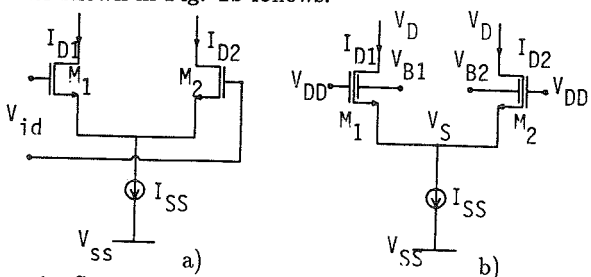

Figure 1. Source–coupled differential input stage a) conventional b) back–gate input

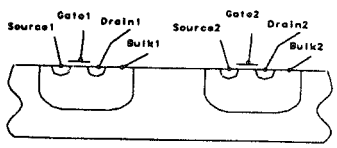

Figure 2. Cross–view of back–gate input transistors fabricated in the separated wells.

For simplicity, the drain voltages are assumed a constant voltage, V_x, where $V_x < V_{DD} - V_{To}$. To keep the input pair, M_1–M_2, in the ohmic region, the gates are connected to the highest potential, V_{DD}. The currents I_{D1} and I_{D2} are given by

$$I_{Dx} = k\left\{V_{GSx} - \left(V_{To} + \gamma\sqrt{|V_{BSx}| + \phi} - \gamma\sqrt{\phi}\right) - \frac{V_{DSx}}{2}\right\} V_{DSx} \tag{7}$$

where the quantity in parenthesis represents the threshold voltage of the x'th device

$$V_{Tx} = V_{To} + \gamma\left(\sqrt{\phi + V_S - V_B} - \sqrt{\phi}\right) \tag{8}$$

for $x = 1, 2$. If it is assumed that $|V_B| << V_S + \phi$, the quadratic term in (7) can be expanded in a Taylor's series and truncated after first–order terms to obtain

$$\sqrt{|V_{BSx}| + \phi} = \sqrt{V_S - V_{Bx} + \phi} \cong \sqrt{V_S + \phi}\left(1 - \frac{V_{Bx}}{2(V_S + \phi)}\right) \tag{9}$$

Substituting the quadratic term from (9) into (7) we obtain

$$I_{Dx} \simeq k\left\{V_{GS_x} - \left(V_{To} + \gamma\sqrt{\phi + V_S}\left(1 - \frac{V_{Bx}}{2(V_S + \phi)}\right) - \gamma\sqrt{\phi}\right) - \frac{V_{DS_x}}{2}\right\} V_{DS_x} \tag{10}$$

Defining the differential output current by the expression $I_{od} = I_{D1} - I_{D2}$ and assuming $V_{DS1} = V_{DS2} = V_{DS3} = V_D - V_S$, it follows from (10) that the differential output current is given by the expression

$$I_{od} = I_{D1} - I_{D2} \simeq k\left(-\gamma\frac{V_{DS}}{2\sqrt{V_S + \phi}}\right)(V_{B1} - V_{B2}) \tag{11}$$

The linearity of the source–coupled back gate pair is not apparent from (11) since the coefficient of $V_{B1} - V_{B2}$ is dependent upon V_S in both the numerator and denominator. If, however, V_S were independent of V_{B1} and V_{B2}, then the linearity of the transconductance (relationship between I_{od} and $V_{id} = V_{B1} - V_{B2}$) becomes apparent. In actuality, the voltage V_S is nearly independent of V_{B1} and V_{B2}. Although this is somewhat tedious to show mathematically, from a qualitative viewpoint it can be argued that the drain current is only weakly dependent upon the bulk voltage. If V_S were to change very much with V_{B1} or V_{B2}, this change in V_S would result in a corresponding large change in V_{GS} since the gate voltages are constant. This large change in V_{GS} would, in turn, cause a large change in the drain current thus contradicting our observation that the drain current is only weakly dependent upon the bulk voltage. It will thus be assumed that the source voltage is nearly constant over the entire input domain of V_{B1} and V_{B2} and conclude tht large changes in V_{B1} and V_{B2} will be required to generate significant changes in I_{od}. From this qualitative argument, and equation (11), both the linearity and wide input range of the back–gate source–coupled pair should be apparent. Since $I_{SS} = I_{D1} + I_{D2}$, the relationship between I_{SS} and V_S for a given V_{B1} and V_{B2} can be obtained from (7) to yield the expression

$$I_{SS} = 2k\left(V_{DD} + \gamma\sqrt{\phi} - V_{To} - \frac{V_S}{2} - \frac{V_D}{2} - \frac{\gamma}{2}\cdot\left(\sqrt{\phi + V_S - V_{B1}} + \sqrt{\phi + V_S - V_{B2}}\right)\right)(V_D - V_S) \tag{12}$$

The nominal relationship between I_{SS} and V_S, corresponding to $V_{B1} = V_{B2} = 0$, thus becomes

$$I_{SS} = 2k(V_{DD} + \gamma\sqrt{\phi} - V_{To} - \frac{V_S}{2} - \frac{V_D}{2} - \gamma\sqrt{\phi + V_S})(V_D - V_S) \tag{13}$$

Since V_S is only a weak function of V_{B1} and V_{B2}, the value of V_S obtained from (13) remains valid over a wide range of inputs. Since $I_{D1} + I_{D2} = I_{SS}$, it follows from (11) that I_{D1} and I_{D2} also vary linearly with $V_{B1} - V_{B2}$ and can be approximated by the expression

$$I_{Dx} = \frac{I_{SS}}{2} + \frac{kV_{DS}\gamma}{4\sqrt{V_S + \phi}}(V_{B1} - V_{B2})(-1_x) \tag{14}$$

for x=1, 2. Note that the input voltages, V_{B1} and V_{B2}, should be less than the source voltage to keep the bulk to source pn junction reverse biased.

The transconductance of this back–gate differential stage at the nominal operating point, $V_{B1} = V_{B2} = 0$, can be obtained from (11) to yield the expression

$$g_{m_B} = \frac{\partial(I_{D2} - I_{D1})}{\partial(V_{B1} - V_{B2})}\Big|_{V_{B1} = V_{B2} = 0} \cong \gamma \frac{kV_{DS}}{2\sqrt{\phi + V_S}} \quad (15)$$

It can be noticed that transconductance is a function of the drain bias and the source voltage.

To make the differential back–gate pair of Fig. 1b useful, it is necessary to generate a higher –level block which has a single–ended output current or voltage. The standard architecture for a back–gate coupled Operational Transconductance Amplifier (OTA) is shown in Fig. 3 where three current mirrors are used to mirror the drain currents in the output. The mirrors also improve the output impedance which is quite low due to the ohmic region operation of the source–coupled pair. A realization of this OTA structure is shown in Fig. 4.

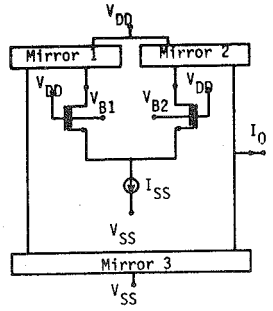

Figure 3. Basic OTA Architecture

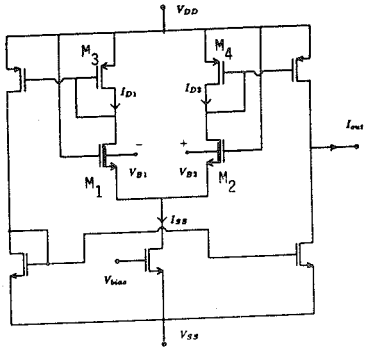

Figure 4. Circuit schematic of back–gate OTA structure

The analysis of the source–coupled pair of Fig. 1b was made under the assumptions that the drains were terminated into an ac short, specifically the equal valued voltage sources $V_{D1} = V_{D2} = V_D$. Since the output impedance of the back–gate source–coupled pair is low due to the ohmic region operation of these devices, the currents I_{D1} and I_{D2} in the circuit of Fig. 4 will differ from that predicted earlier and the transconductance characteristics will also change. Even though the currents I_{D1} and I_{D2} become quite dependent on the input characteristics of the current mirrors, the overall linearity of the Operational Transconductance Amplifier remains quite good.

III. COMPUTER SIMULATIONS AND EXPERIMENTAL RESULTS

The source–coupled back–gate pair of Fig. 1b was simulated on SPICE using a level2 MOSFET model and the process parameters for the 3μ MOSIS CMOS bulk process. V_{DD} was set at 10V, V_D at 7V and the current source I_{SS} was assumed ideal of value $100\mu A$. M_1 and M_2 were assumed matched and sized with W=20μ and L=10μ. The drain currents, I_{D1} and I_{D2}, as a function of the differential input $V_{B1} - V_{B2}$, centered around 0V, as obtained from this simulation are shown in Fig. 5. An error plot for I_{D1} relative to a full scale value of I_{SS} is shown in Fig. 6. Note that for differential input voltages up to $\pm 6V$, the nonlinear error remains below 1%.

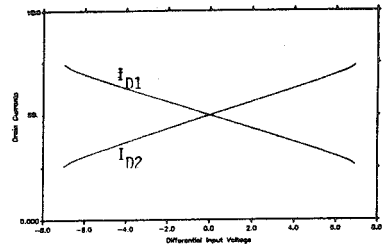

Figure 5. Simulated transconductance characteristics of back–gate differential pair of Fig. 1b.

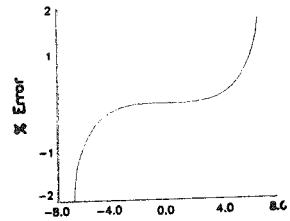

Figure 6. Nonlinear error simulation for circuit of Fig. 1b.

The transconductance amplifier of Fig. 4 was then simulated. In this simulation the mirrors, mirror 1 and mirror 2, had a current gain of 2; that of mirror 3 was unity. The voltage V_{DD} was 10V and V_{SS} was grounded. The tail current was held fixed at $I_{SS} = 30\mu A$. M_1 and M_2 were matched and sized with W=20μ and L=10μ. the devices M_3 and M_4 were matched with W=150μ. The excitations V_{B1} and V_{B2} were fully differential around 0V and the output current was into an ac short circuit load obtained by connecting the output to a dc reference of $\frac{V_{DD}}{2}$. The results of this simulation for varying size loads ($L_3 = L_4 = L$) are shown in Fig. 7. The linearity remains quite good over a wide range of inputs. The abrupt nonlinearity for short devices for inputs around $\pm 3V$ is primarily due to the fixed bias current which is essentially steered to one of the load devices for large excitations.

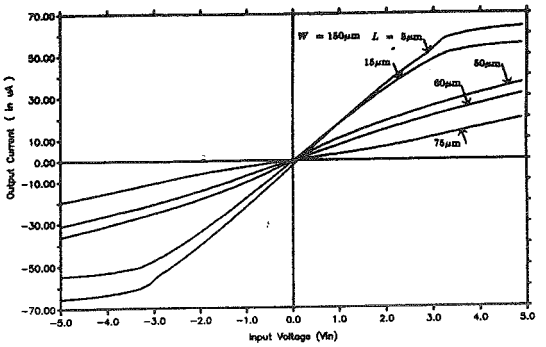

Figure 7. Simulated output characteristics of back–gate input OTA of Fig. 4

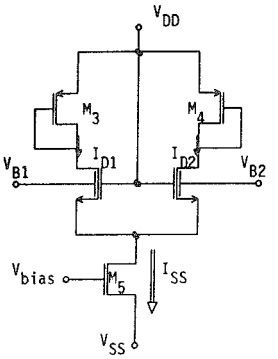

Figure 8. Loaded back–gate input differential amplifier

The circuit of Fig. 8 was experimentally evaluated to determine the combined nonlinear effects of both the back gate–input pair and the standard load device which forms the input stage to the simple current mirrors. It is thought that minimal additional nonlinearities will be introduced when the rest of the current mirror structures are added to complete the OTA circuit of Fig. 4. M_1 and M_2 were matched with $W = 20\mu$ and $L = 10\mu$. The load devices M_3 and M_4 were sized with $W = 10\mu$ and $L = 20\mu$. V_{DD} was held at 10V, V_{SS} was grounded and V_{BIAS} was used to establish the tail current at $I_{SS} = 100\mu A$ and $I_{SS} = 200\mu A$. The differential output current obtained by numerically subtracting the measured values of I_{D1} and I_{D2} is shown in Fig. 9. The nonlinear errors are plotted in Fig. 10. The large linear input range should be apparent from these measurements.

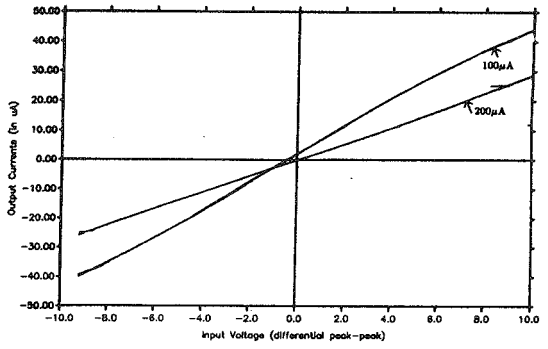

Figure 9. Experimental transconductance characteristics of loaded back–gate input stage of Fig. 8

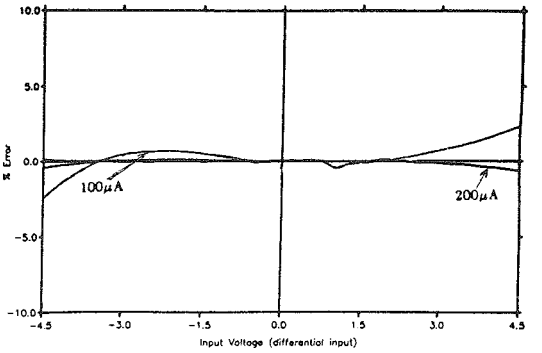

Figure 10. Measured nonlinear error of loaded back–gate input stage

IV. CONCLUSIONS

It has been shown that significant improvements in input signal swing and linearity are attainable if the back gates are used in place of the gates themselves as inputs in the basic source–coupled pair. Simulations showed the nonlinear error remains below 1% for differential inputs as large as $\pm 6V$. These results were substantiated by experimental measurements.

This input pair was then used as the input stage for a conventional operational transconductance amplifier. Simulations suggest a significant improvement in signal swing and linearity for the OTA. An OTA which uses $\pm 5V$ power supplies and back–gate inputs is under fabrication. Experimental results will be reported in the near future.

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