A Linear Monolithic Active Attenuator with Multiple Output Taps

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ABSTRACT

Design considerations for monolithic integrated attenuators are discussed. A multi-output active attenuator which has a very high input impedance and low distortion over a wide range of input voltages is introduced. Systematic attenuator design methodologies are given.

Experimental results based upon fabrication of test structures in a standard 3μ p-well CMOS process are presented. Experimental results show that the nonlinear error in an attenuator with attenuation factor η=0.1 is under 0.53% for inputs between 2V and 10V when biased with a single 10V power supply. When excited with a 4 V p-p sinusoid, the THD of the signal on all attenuator outputs was less than 0.15%.

I. Introduction

Attenuators find numerous applications in discrete electronic circuit design. Some of the most notable are in data converter and feedback amplifier design as well as in signal level shifting requirements in which the signal swing at the input of a circuit must be kept small to avoid saturating internal amplifier stages. In these applications, the attenuators are generally required to have exacting specifications either in terms of very good linearity and/or a high input impedance. These exacting specifications can be economically obtained in discrete applications with standard low-cost resistors.

Although resistors can conceptually also be used to build attenuators in monolithic applications, they have not proven practical for several reasons. First, the silicon area required to get the resistance sufficiently high to have an attractive input impedance and power dissipation is generally too large to be practical. Second, nonlinearities associated with diffused resistors are high and finally, distributed parasitics may cause an undesirable frequency dependence.

A multi-output active attenuator is presented here which has nearly infinite input impedence, good linearity and good high frequency performance.

II. Attenuator Design

An active voltage attenuator with n outputs is shown in Fig. 1. This structure is an extension of the single-output attenuator used as the input to a transconductance amplifier introduced by VanHorn [1, 2]. It can be shown that this circuit performs as a multi-output attenuator provided $M_1, ...M_n$ are operating in the ohmic region and M_{n+1} is operating in the saturation region.

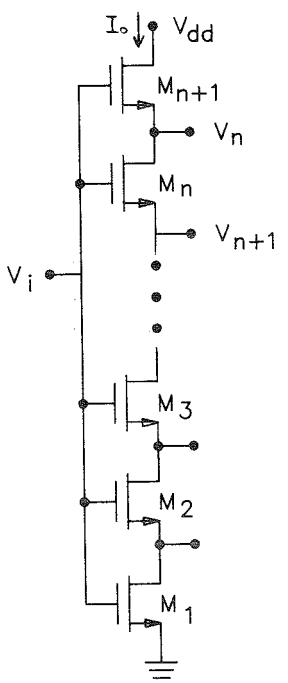

Fig. 1. Multiple-Output Active Attenuator

It can be shown that if $M_1, ...M_{n+1}$ are fabricated in the same process with the same zero-bias threshold voltage, V_{TO}, then the proper mode of operation of all transistors will be maintained provided V_i satisfies the inequality

$$V_{T_1} < V_i < V_{dd} + V_{T_{n+1}} \qquad (1)$$

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where V_{T_1} and $V_{T_{n+1}}$ are the threshold voltages of M_1 and M_{n+1}.

The relationship between the exicitation, V_i, and the multiple outputs of the attenuator will be derived under the assumption that channel length modulation effects are negligable ($\lambda = 0$) and the threshold voltages of M_1, ... M_{n+1} are all matched and equal to V_T.

Consider the cascade of k MOSFETS with a common gate as shown in Fig. 2. If all devices are asssumed operating in the ohmic and are modeled by the equation

$$I_{D_j} = K'\beta_j \left(2\left[V_{GS_j} - V_T\right] - V_{DS_j}\right) V_{DS_j} \qquad (2)$$

for $1 \leq j \leq k$, where $\beta_j = W_j/L_j$, then this cascade is equivalent to a single MOSFET modeled by the equation

$$I_D = K'\beta_{eq} \left(2\left[V_{GS} - V_T\right] - V_{DS}\right) V_{DS} \qquad (3)$$

where V_{GS} and V_{DS} are as labeled in Fig. 2 and

$$\beta_{eq} = \frac{1}{\sum_{j=1}^{k} \beta_j^{-1}} \qquad (4)$$

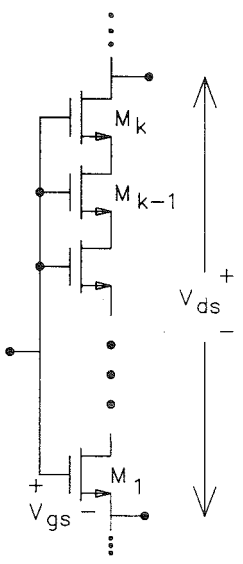

Fig. 2. Cascade of k MOSFETs

If transistors M_1 ... M_k in Fig. 1 are now grouped together as are M_{k+1} to M_n to form the equivalent MOSFETs T_k and Q_k respectively, then if only the attenuator output voltage V_k is considered, the circuit of Fig. 1 can be modeled by the three transistors of Fig. 3 where the effective length/width ratio of Q_k and T_k, β_{Qk} and β_{Tk}, are given by the expression

$$\beta_{Qk} = \frac{1}{\sum_{j=k+1}^{n} \beta_j^{-1}} \qquad (5)$$

$$\beta_{Tk} = \frac{1}{\sum_{j=1}^{k} \beta_j^{-1}} \qquad (6)$$

The three transistor equivalence of Fig. 4 is valid for $1 \leq j \leq n-1$. By extension of the work of Van Horn [1] it can be shown that the output voltage for the circuit of Fig. 4, V_n, relates to V_k, V_{in} and V_{DD}, by the expression

$$V_n = (V_{in} - V_T)\left(1 - \sqrt{\frac{1}{1 + \frac{\beta_{n+1}}{\beta_{Qk}}}}\right) + V_k \sqrt{\frac{1}{1 + \frac{\beta_{n+1}}{\beta_{Qk}}}} \qquad (7)$$

for $1 \leq k \leq n-1$. This equation can be solved for V_k to yield

$$V_k = (V_{in} - V_T)\left[1 - \sqrt{1 + \frac{\beta_{n+1}}{\beta_{Qk}}}\right] + V_n \sqrt{1 + \frac{\beta_{n+1}}{\beta_{Qk}}} \qquad (8)$$

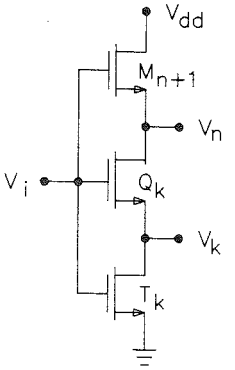

Fig. 3. Circuit Equivalent of Attenuator in Fig. 2 for Determining V_k , $1 \leq k \leq n$.

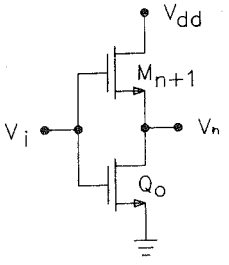

Fig. 4. Circuit Equivalent of Attenuator in Fig. 2 for Determining V_n.

It remains to obtain an expression for the voltage V_n. To obtain V_n, consider the two–MOSFET circuit equivalent to that of Fig. 1 shown in Fig. 4 where the width/length ratio of the equivalent transistor, Q_o, is given by

$$\beta_{Qo} = \frac{1}{\sum_{j=1}^{n} \beta_j^{-1}} \qquad (9)$$

This equivalence applies if V_n is the only output variable of interest. Note that (9) is just an extension of (5) to include the index variable k=0. It thus follows from (7) that

$$V_n = (V_{in} - V_T)\left(1 - \sqrt{\frac{1}{1+\frac{\beta_{n+1}}{\beta_{QO}}}}\right) \qquad (10)$$

which is an extension of (7) to include the index variable k=0 provided V_o is defined to be 0. Combining (8) and (10) we thus obtain for $1 \le k \le n-1$

$$V_k = (V_{in} - V_T)\left[1 - \sqrt{1+\frac{\beta_{n+1}}{\beta_{Qk}}}\sqrt{\frac{1}{1+\frac{\beta_{n+1}}{\beta_{Q0}}}}\right] \qquad (11)$$

From (10) and (11) it can be seen that the taps at all attenuator outputs relate linearly to V_{in} and that the input offset voltages are all identical and equal to V_T.

If we now define the attenuation factor from V_{in} to the output V_k by η_k, it follows from (10) and (11) that

$$\eta_n = 1 - \sqrt{\frac{1}{1+\frac{\beta_{n+1}}{\beta_{Q0}}}} \qquad (12)$$

$$\eta_k = 1 - \sqrt{\frac{1+\frac{\beta_{n+1}}{\beta_{Qk}}}{1+\frac{\beta_{n+1}}{\beta_{Q0}}}} \qquad 1 \le k \le n-1 \qquad (13)$$

Thus (11) can be rewritten for $1 \le k \le n$ as

$$V_k = (V_{in} - V_T)\,\eta_k \qquad (14)$$

Design equations for sizing the devices (i.e. determining $\beta_1, \ldots \beta_{n+1}$) in the active attenuator will now be derived. Assume $\eta_1, \ldots \eta_n$ are the desired attenuation factors where $\eta_1 < \eta_2 < \ldots < \eta_n$. From (12) and (13) we obtain

$$\frac{1}{\beta_{Qk}} = \frac{\left(\frac{1-\eta_k}{1-\eta_n}\right)^2 - 1}{\beta_{n+1}} \qquad 0 \le k \le n-1 \qquad (15)$$

where η_o is equal by definintion to zero. Substituting (5) into (15), one obtains a set of n simulataneous equations in the n+1 variables $\beta_1, \ldots \beta_{n+1}$. In this case these equations are sufficiently decoupled to obtain the simple solution

$$\beta_k = \frac{\beta_{n+1}(1-\eta_n)^2}{(1-\eta_{k-1})^2 - (1-\eta_k)^2} \qquad 1 \le k \le n \qquad (16)$$

The design strategy is thus to size M_{n+1} conveniently thus establishing β_{n+1}. The balance of the devices are sized according to (16).

III. Design Example

An attenuator circuit based upon the circuit of Fig. 1 was designed to give 6 outputs of 1V, 2V, 3V, 4V, 5V and 6V with an input of 10 V in a process with a design center of $V_T = 1V$. From (14) and (16) this corresponds to the attenuation factors given in Table 1. This circuit was fabricated in a standard 3μ p-well CMOS process.

The measured dc transfer characteristics for $V_{DD} = 10V$ are shown in Fig. 5. The linearity of the attenuator is quite good.

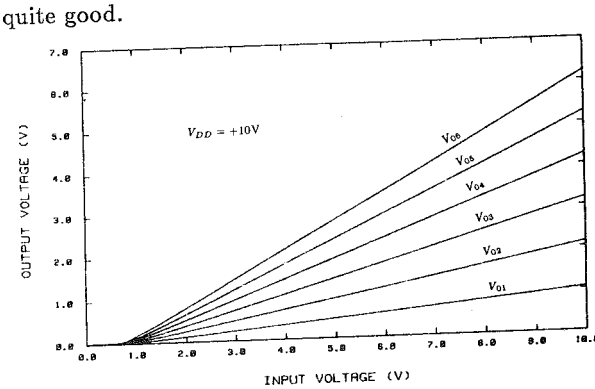

Fig. 5. Transfer Characteristics of Active Attenuator.

The actual nonlinearities of the attenuators cannot be determined from the plot in Fig. 5. The nonlinear errors and the THD are meaningful methods for characterizing the nonlinearities which may exist in the attenuator. The measured nonlinear errors of the attenuator are shown in Fig. 6 where the error is measured relative to a least–squares linear regression on the measured data and is expressed in % relative to a full–scale input range of 2V to 10V as defined by the equation

ACTUAL DEVICE SIZES	SIMULATION LEVEL 1	ATTENUATION LEVEL 2	MEASURED ATTENUATION
$W_1 = 60\mu$ $L_1 = 60\mu$			
$W_2 = 17\mu$ $L_2 = 15\mu$	$\eta_1 = 0.1179$	$\eta_1 = 0.1131$	$\eta_1 = 0.1031$
$W_3 = 17\mu$ $L_3 = 13\mu$	$\eta_2 = 0.2334$	$\eta_2 = 0.2221$	$\eta_2 = 0.2086$
$W_4 = 17\mu$ $L_4 = 11\mu$	$\eta_3 = 0.3490$	$\eta_3 = 0.3305$	$\eta_3 = 0.3239$
$W_5 = 30\mu$ $L_5 = 16\mu$	$\eta_4 = 0.4651$	$\eta_4 = 0.4378$	$\eta_4 = 0.4181$
$W_6 = 20\mu$ $L_6 = 8\mu$	$\eta_5 = 0.5867$	$\eta_5 = 0.5494$	$\eta_5 = 0.5270$
$W_7 = 19\mu$ $L_7 = 8\mu$	$\eta_6 = 0.7043$	$\eta_6 = 0.6512$	$\eta_6 = 0.6172$

TABLE 1 Attenuation Factors and Device Sizes Used in Design Example

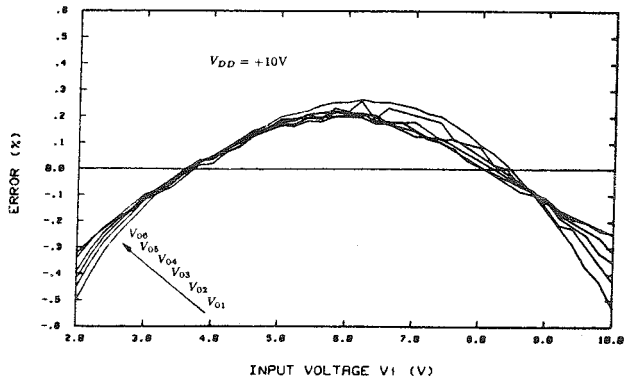

Fig. 6. Measured Nonlinear Errors of Active Attenuator.

$$\epsilon = \frac{V_{k_{meas}}|_{V_i} - V_{k_{mms}}|_{V_i}}{V_{k_{meas}}|_{V_i=10V} - V_{k_{meas}}|_{V_i=2V}} \times 100\% \qquad (17)$$

Although the curves correspond to errors on special outputs, they are not labeled since all have comparable nonlinear errors. The maximum full–scale errors over the input range $2V \leq V_i \leq 10V$ corresponding to the outputs $V_1, ...V_6$ are -0.53%, -0.45%, -0.42%, -0.39%, -0.34% and -0.32% respectively. If the input range were restricted from 2V to 8 V or from 3 V to 7 V as the full–scale input range, the maximum measured full–scale errors among the six outputs are 0.38% and 0.20% respectively.

The simulated frequency response of the active attenuator appears in Fig. 7. The performance is quite good up to 1 MHz. Instrumentation parasitics make it difficult to accurately measure the frequency response of the test structure experimentally. The results presented in Fig. 7 should, however, reflect what will be experienced when this attenuator is used internally in monolithic applications.

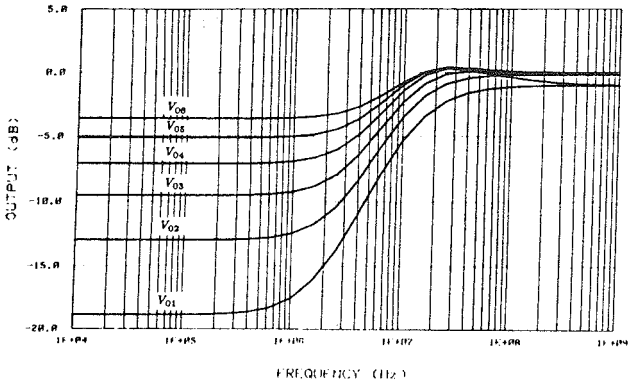

Fig. 7. Simulated Frequency Response of Active Attenuator.

The dynamic range of one of the outputs relative to a signal at 1% THD over the band (1KHz to 1MHz) was measured at 94.8 dB.

IV. Conclusions

A new multi–output active attenuator was introduced. The attenuator has nearly infinite input impedance. Design equations for designing attenuators with any number of outputs and an arbitrary set of attenuation factors were presented. The linearity of the attenuator is good over a wide range of inputs and the noise characteristics are attractive.

A test structure was fabricated in a 3μ p–well CMOS process. Experimental results were presented which verified the linearity of both the active attenuator and finite gain voltage amplifier. For an attenuation of $\eta = .1$, the nonlinear errors were well under 1% for an 8V input voltage range. The THD for a 4V p–p sinusoidal excitation was under .15% for all attenuator outputs.

REFERENCES

[1.] VanHorn, M., "A CMOS OTA for Voltage–Controlled Analog Signal Processing", MS Thesis, Texas A&M University, Dept. of Electr. Engr., 1985.

[2.] VanHorn, M., Qin, S. C. and Geiger, R. L., "A CMOS Transconductance Amplifier with Active Input Attenuation for Voltage–Controlled Analog Signal Processing", (under review).